Main

Background

Mode S Technology

Interviews

Reports

Bibliography

Glossary

Other Links

Error Correction Design

In order to allow error correction on Mode S messages, the signal format was designed to include a parity check. However, the transmission window is limited (due to the sidelobe suppression method). In order to conserve bits, Mode S parity and addressing bits are overlaid.

Reasons for parity

Having parity coding in Mode S messages represents a significant advantage; in the case that an error occurs, the sensor avoids the penalty of retransmission. In addition, the designers of Mode S needed to provide *some* form of redundancy in the message coding, to protect against possible interference.

Parity/address overlay

Because the LL researchers used sidelobe supression, they estimated that they could only send a maximum of 112 bits in the data block. One way they tried to conserve the number of bits used was to combine the address and parity fields. Instead of having a transponder check two separate message fields to determine if the received message should be displayed, a combined address-parity field allows the transponder to check only one field.

An error occurring would cause the decoded address to be modified; as a result, even the plane the message was originally intended for would ignore the interrogation.

The code selected for the Mode S uplink is a cyclic code generating 24 parity check bits, which can correct many error patterns, up to 24 bits. In designing Mode S, Lincoln Labs researchers assumed that ATCRBS pulses could cause error bursts up the 5 bits, and TACAN /DME pulses could cause error bursts up to a length of 19 bits. Therefore, this method of parity checking was well suited for the interference environment.

Polynomial generator

The particular cyclic code that is used is described by the following polynomial:

$g(x) = 1 + x^3 + x^{10} + x^{12} + x^{13} + x^{14} + x^{15} + x^{16} + x^{17} + x^{18} + x^{18} + x^{19} + x^{20} + x^{21} + x^{22} + x^{23} + x^{24}$

This code was first discovered by Kasami in 1964; it has been proven to be able to correct any single 12-bit error burst. This code also guarantees correction of any single 24-bit error burst over any length.

How it works

The parity check sequence of an encoded message is combined with the transponder address by modulo two summation. The transponder can remove the parity check bits by modulo summation. If the parity check bits calculated in the transponder equals the parity check bits combined in the address, the result of this summation produces the transponder address.

If there is an error, the incorrect transponder address is calculated. Since this address will not correspond to the transponder's address, the transponder will simply ignore the message.