Deep Submicron InP DHBT Technology with Electroplated Emitter and Base Contacts

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We report the development of a wide bandwidth InP double heterojunction bipolar transistor technology that utilizes novel *electroplating* processes to form the emitter and base contacts. The technology enables the fabrication of HBTs with deep submicron emitter-base junction dimensions and self-aligned base Ohmic contacts. Using this technology, HBTs have been fabricated with emitter junction widths scaled to 0.25μm. These devices demonstrated peak f_τ and f_{max} values of over 300 GHz. The transistors also support high current density operation (J_E > 7 mA/μm^2) and have a low collector-base capacitance to collector current ratio (C_{cb}/I_c ~ 0.55 ps/V), an important parameter for digital logic speed [1].

Submicron InP HBTs have application in mixed signal ICs for digital radar and communication systems [2]. Transistor counts in complex ADCs and DACs may approach ~10,000 devices. Improvements in the yield and manufacturability of submicron HBTs are necessary to realize the technology's full potential. A primary yield limitation in submicron III-V HBT processes is the formation of a self-aligned base-emitter junction. In this work, novel electroplating processes are used to form the emitter and base Ohmic contacts, and dielectric sidewall spacers are used to self-align the base contact to the base-emitter junction. Fig. 1 shows a SEM cross-section of a 0.25 μm emitter contact with dielectric sidewall spacers. The emitter contact is Au-based and is defined using electron-beam lithography. The electroplating process enables the formation of submicron features with large height-to-width ratios and straight sidewall profiles, characteristics that are difficult to achieve in evaporated liftoff processes. After the emitter mesa etch, dielectric sidewalls are formed by the conformal PECVD of dielectric films followed by an anisotropic reactive ion etch. The sidewalls provide electrical isolation between the emitter and base contacts and passivate the exposed base-emitter junction. The electroplating process used to define the base Ohmic contact *selectively* deposits the base metal on the base semiconductor and not on the emitter contact or sidewalls. This novel process offers an elegant method of forming self-aligned contacts in III-V devices. A critical element of the process is the proper selection of the materials in the base metal stack to ensure low contact resistance and thermal stability. The remaining process flow is similar to that of a standard triple-mesa HBT, with particular attention paid to reducing device parasitics. A cross-section of the HBT prior to dielectric planarization is shown in Fig. 2.

Gummel characteristics of 0.25x10.0 μm^2 HBT are shown in Fig. 3. These devices demonstrated a current gain β of approximately 60, and a common emitter breakdown voltage BV_{CEO} greater than 4.5 V. The transistor epitaxy has an abrupt InP/InGaAs emitter-base junction with a 30 nm carbon doped base. The collector thickness is 150 nm, and details of the base-collector grade design can be found in [3]. RF device measurements were made from 1-50 GHz using an Agilent 8510 VNA and calibration was performed using an off-wafer TRL calibration substrate. Fig. 4 shows the unilateral power gain (U) and short circuit current gain (h_{21}) for the HBT of Fig. 3. The device bias conditions are J_E=7 mA/μm^2 and V_{CB}= 0.4V. The extrapolated f_τ and f_{max} of the device are 325 GHz and 305 GHz, respectively. Fig. 4 shows the transistor f_τ and f_{max} plotted versus current density. The transistor is found to sustain high current-density operation at low collector-base operating voltages, an important characteristic for transistors in ECL and CML logic circuits. The extracted collector base capacitance of the device is a low 9.5 fF. In addition, to demonstrating impressive RF performance deep submicron devices have also been realized with high levels of integration. Fig. 6 shows the Gummel characteristics of a test structure with 1000 parallel submicron HBTs.

A wide bandwidth DHBT technology designed for mixed-signal and digital logic applications has been described. The process utilizes novel electroplating processes to form the emitter and base contacts. The technology enables scaling of the base-emitter junction to deep submicron dimensions in a high yield manufacturable process. Mixed-signal demonstrations circuits in the technology are currently being fabricated to confirm the transistor design approach.

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1. M. J.W. Rodwell et al, *International Journal of High Speed Electronics and Systems, Vol. 11, No. 1, pp. 159-215, 2001*
2. J. C. Zolper, *Proceedings 2003 IPRM Conference*, May, Santa Barbara, CA, pp. 8-11.
3. M. Dahlström et al, *IEEE Electron Device Letters*, vol. 24, no.7,July 2003 pp. 433-435.

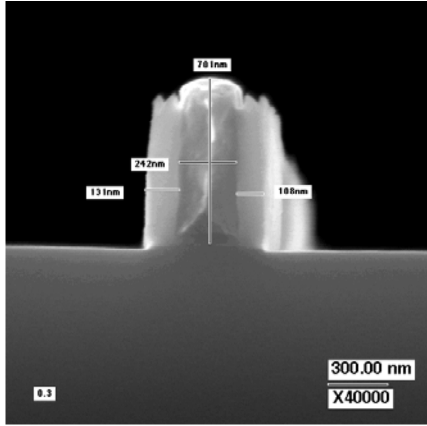

Fig. 1: Submicron electroplated emitter contact with dielectric sidewalls .

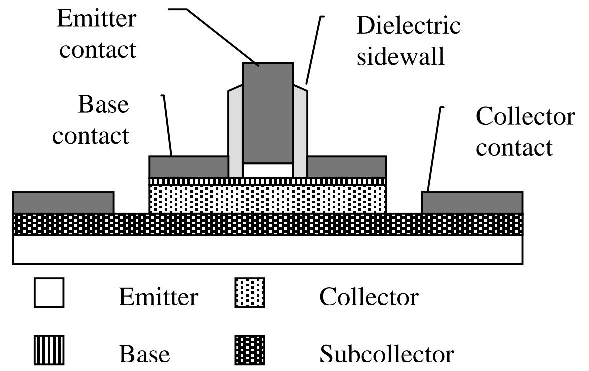

Fig.2: Schematic cross-section of submicron HBT

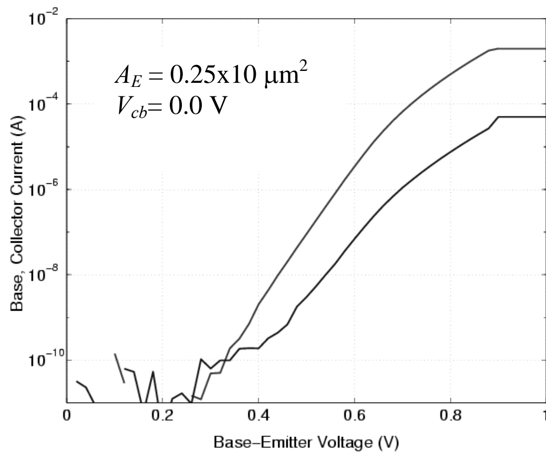

Fig. 3: Gummel characteristics of submicron HBT

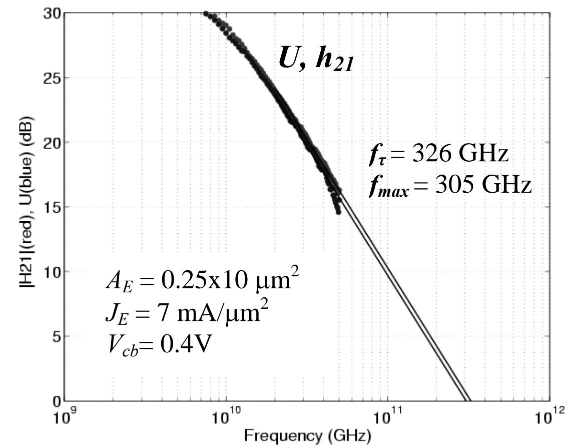

Fig.4: RF gains of submicron HBT

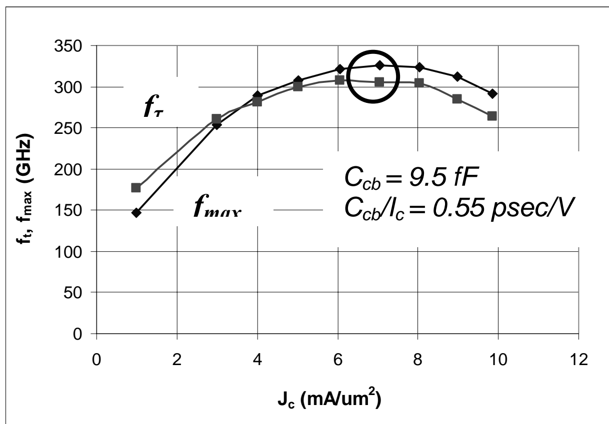

Fig. 5: f_τ and f_{max} versus J_E at $V_{cb} = 0.4\ V$.

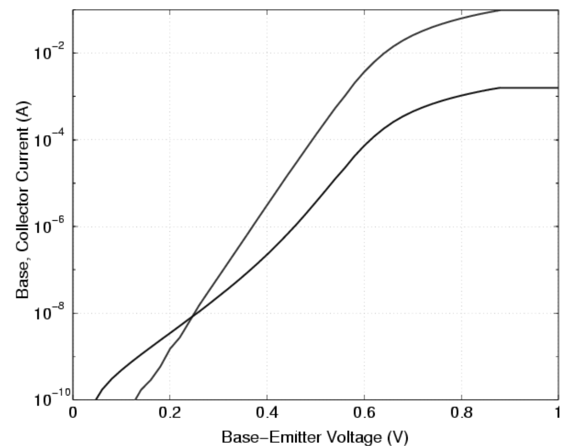

Fig. 5: *Gummel characteristics of 1000 parallel submicron HBTs.*