THz Monolithic Integrated Circuits Using InP High Electron Mobility Transistors

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(Invited Paper)

***Abstract*—In this paper, background describing THz monolithic integrated circuits using InP HEMT is presented. This three-terminal transistor technology has been used to realize amplifiers, mixers, and multipliers operating at 670 GHz. Transistor and processing technology, packaging technology, and circuit results at 670 GHz are described. The paper concludes with initial results from a 670-GHz InP HEMT receiver and trends for InP HEMT components.**

***Index Terms*—Active semiconductor circuit, solid-state sensor, solid-state source, three-terminal device.**

I. Introduction

In the last few years, the development of > 1 THz f_{MAX} transistor technologies [1] has pushed operating frequencies of amplifiers well into the sub-millimeter wave range. The first demonstrations of sub-millimeter amplification were undertaken at the 340-GHz atmospheric window using InP HEMT [2] and MHEMT [3] technologies. Amplification has now been demonstrated above the 300-GHz sub-millimeter wave threshold, with work in the 460–500 GHz range recently reported including a HEMT amplifier with 11.4-dB packaged gain [4], and noise figure of 11.7 dB [5], and a 16.1-dB gain amplifier measured on-wafer at 460 GHz [6]. Amplification has also been shown above 500 GHz with a cascode amplifier reported in [7], which reached a packaged gain of 10 dB at 550 GHz.

A variety of fundamental advancements are necessary to make this progress possible. First, transistors with extremely high f_{MAX} are essential for demonstrating gain at 670 GHz. Secondly, a tailored MMIC process for realizing the matching integrated and biasing networks. Third, specialized packaging techniques are required for getting the signals in and out of the circuit. The background for these is all described in this paper. These results include 670-GHz amplifier and mixer results. The paper concludes with initial results on an all InP HEMT receiver operating at 670 GHz and some circuit scaling predictions.

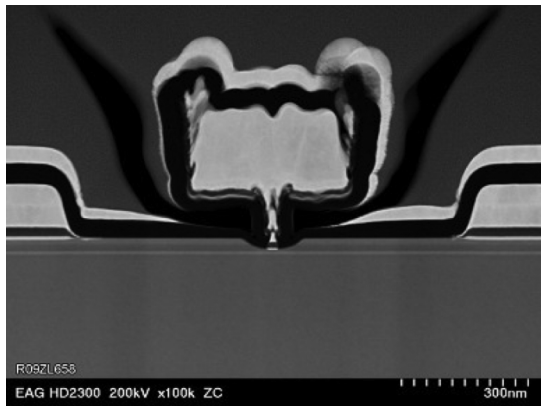

Fig. 1. Scanning Electron Tunneling (SEM) image of 30-nm InP HEMT gate.

In this paper, we provide background into the fundamental developments which now make amplifiers and other types of electronic circuits possible at 670 GHz using InP HEMT transistors. In addition to the 30-nm InP HEMT transistors (Fig. 1), the physical features of these integrated circuits are aggressively scaled with frequency. For this reason, we refer to these integrated circuits operating close to 1 THz as "Terahertz Monolithic Integrated Circuits", or "TMICs".

As a final comment, it should be noted that all of the 670 GHz results in this paper have been taken at room temperature and represent either first or second iteration results on a newly developed 30-nm InP process. For the presented application, the technology is therefore still relatively in its infancy for Terahertz applications. We therefore expect additional improvements to be made over time as the technology matures.

II. THz f_{MAX} InP HEMT Device

Critical for reaching Terahertz operational frequencies for integrated circuits are transistors with sufficiently high f_{MAX}. This paper describes development of amplifiers targeting 670 GHz. As a rule of thumb, transistor f_{MAX} should be 50–100% higher than the design frequency. Therefore, 1–1.3 THz f_{MAX} transistors are necessary. In this section, 30-nm InP HEMTs are described.

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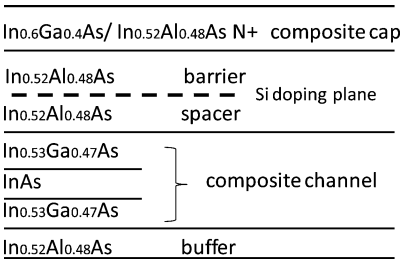

Fig. 2. Layer profile of the epi wafers.

An InP-based HEMT was developed as the key enabling technology. The epitaxial wafers were grown in molecular beam epitaxy (MBE) on 3-inch semi-insulating InP (100) substrates. As shown in Fig. 2, the layer structure consists of an n^+ InGaAs/InAlAs composite cap for enhanced ohmic contacts, an un-doped InAlAs as Schottky barrier and an InGaAs/InAs composite channel for superior electron transport properties. A Si doping plane was inserted in the Schottky layer to supply electrons for current conduction. A room temperature electron mobility over 15,000 $cm^2/V \bullet s$ has been achieved with a sheet charge of 3.3e12 cm^2.

The device ohmic contact was formed using a nonalloyed metal scheme, enabling an extremely consistent low contact resistance, Rc, typically 0.04 Ω mm, with the on-wafer standard deviation as low as 3%. The 30-nm gate process is another critical element in this technology (Fig. 1). Scaling the size of the gate allowed for a corresponding reduction in the gate capacitance, Cgs, which affects gain for circuits operating at high frequencies. The 30-nm gate pattern was defined using electron beam lithography. The self-aligned gate recess was then formed with wet chemical etching, and the T-gate was formed with a refractory Schottky metal stack. The devices were fully passivated with plasma-enhanced chemical vapor deposition SiN. The passivation thickness is 200 Angstroms.

The device dc and RF characteristics are summarized in Table I. The device S-parameters were measured on-wafer in an extended reference plane structure from 1 to 100 GHz. The current gain cutoff frequency, f_T, was calculated by extrapolating H21 to 0 dB with a -20 dB/decade slope. A small signal model was extracted from the S-parameters and the maximum available/stable gain (MAG/MSG) was simulated based on the model. The maximum oscillation frequency, f_{max}, was then obtained when MAG/MSG reaches 0 dB. The $>$ 600 GHz f_T and $>$ 1200 GHz f_{max} ensure sufficient device gain at TMIC frequencies. The combination of a high peak transconductance (Gmp), good BVgd, and a high I_{max} makes this device a good candidate for multiple high frequency applications, such as low noise and power amplifiers.

III. THz Monolithic Integrated Circuit Technology

The passive technologies used in the TMICs are essential for harnessing the speed of the transistor. We use a wavelength scaled processing technology capable of realizing miniaturized transmission lines and interconnects for operation at 670 GHz. In this section, several aspects are briefly described.

Some of the basics of our technology are shown in Fig. 3. Coplanar Waveguide (CPW) is useful because it provides low

TABLE I
DC and RF Performance of a 30 nm InGaAs/InAlAs/InP HEMT With 2 Fingers and 40ìM Total Gate Periphery

Device Parameters	Units	Typical Value
Gmp at Vd=1V	mS/mm	2400
BVgd (Two Terminal)	V	2.0
Vgp	V	0.3
I_{MAX} at Vd=1V	mA/mm	900
f_T	GHz	600
f_{MAX}	GHz	1200

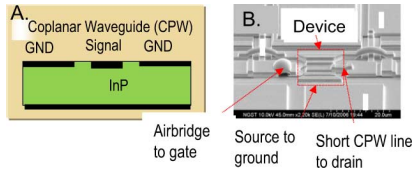

Fig. 3. Details of passive technology for Terahertz InP HEMT process.

TABLE II
Details of Passive Technology for Terahertz InP HEMT Process

Parameter	Unit	Value
Substrate Thickness	um	25
Backside via density (edge-to-edge)	um	15
MIM Capacitor	pF/mm^2	600
TFR	Ω/square Ω/square	20 100
Metal Interconnect Pitch	um	3

inductance access to ground. Our technology uses the 25 μm thick InP substrate as the dielectric for the CPW with ground and signal line formed from topside metallization. CPW is also natural for interconnecting 2-finger transistors typically used at sub-millimeter wave frequencies [Fig. 3(b)]. Some basic technology parameters are shown in Table II.

A key feature of our approach has been dimensional scaling of topside features. For instance, note that the line pitch is extremely narrow (3 μm). This kind of scaling is critical for realizing integrated circuits using planar transmission lines. The reasons for scaling become clear in Fig. 4 which shows loss per wavelength as a function of frequency for microstrip, coplanar waveguide and rectangular waveguide. Different segments indicate either different substrate thicknesses to avoid overmoding or waveguide bands. Note that the dimensions used in the plot were chosen using simple scaling and the message from the plot is not the absolute values for loss per wavelength, *but rather the observation that transmission line losses increase only gradually with frequency if all geometric features can be scaled with wavelength*. This highlights our approach for scaling topside features. This allows MMIC topologies and design techniques which have been successfully employed at millimeter wave frequencies to be used to as high as 670 GHz.

Some details of scaled features are shown in Fig. 5. Shown on the left is a SEM showing the interstage matching between two transistors at 670 GHz. Only 10 μm separate the gate and drain feeds. Four finger transistors are used, and a "Z" shaped airbridge *interconnects the ground planes of shunt biasing lines*. Shown on the right is a detail of an airbridge used to interconnect two coplanar waveguide ground planes and a coplanar waveguide passing beneath. Only 1.7 μm of height is present between

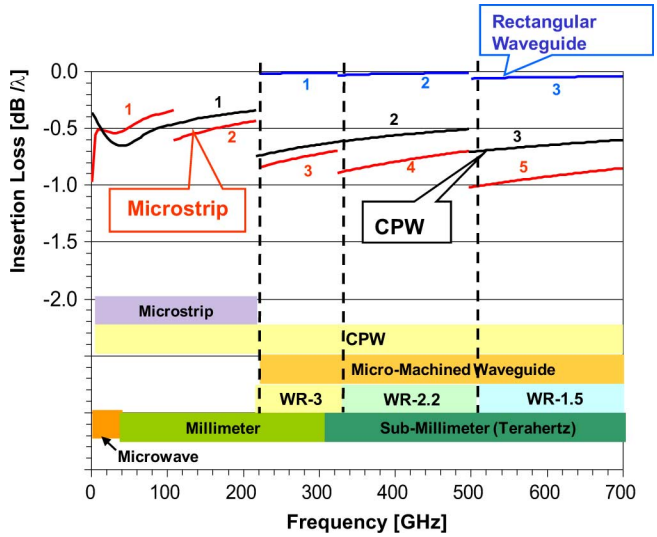

Fig. 4. Loss per wavelength for various kinds of transmission lines and waveguides as a function of frequency.

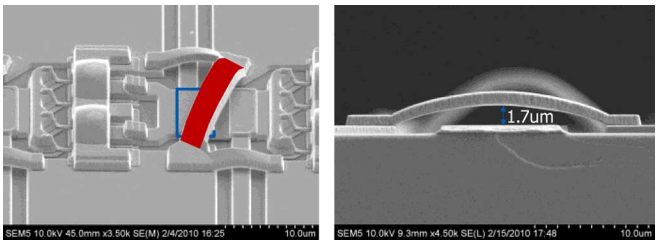

Fig. 5. SEMS of 670-GHz SSPA interstage matching network (left) and airbridge detail (right).

the signal line and airbridge, which is roughly comparable to the CPW gap between ground plane and signal line. This introduces parasitic capacitance.

Therefore, key features of our TMIC passive process are physically scaling dimensions with wavelength to keep electrical lengths short and losses manageably small. For our work, all circuits are implemented in CPW.

IV. THz Integrated Circuit Packaging

Packaging of the TMICs is a critical and challenging task for a variety of reasons. First, traditional wirebonds for passing RF signals become impractical as frequency increases due to the inductive reactance. Second, there is a practical limit to the electrical width of the chip set by the fact that DC must be brought in by wirebonds which touch down on DC bond pads. Third, as frequency increases and wavelength decreases, it becomes increasingly challenging to thin the semiconductor substrate enough to cut-off substrate modes. In this section, we will briefly touch on each of these issues and describe our solution to packaging TMICs

The first challenge to overcome in packaging the TMICs is to develop a low-loss method for getting the RF signal in and out of the chip. From our experience, RF wirebonds become challenging to work with due to the inductance associated with them. The approach that is used for THz mixers packaging is to use E-Plane probes monolithically integrated with the mixer

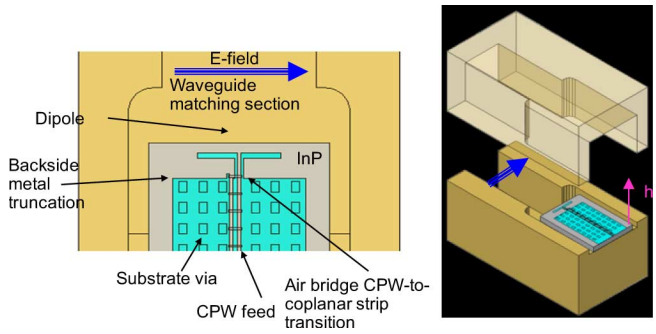

Fig. 6. Schematic of integrated coplanar waveguide to waveguide transition.

circuit. However, to avoid waveguide mode problems caused by cavity loading associated with the high permittivity semiconductor substrates, additional processing steps are taken including substrate removal leaving a thin substrate membrane [9] or transfer onto a lower permittivity quartz substrate [10]. Some work has been done in adapting this to amplifiers at high frequencies [11]–[13]. From a practical perspective, keeping the channel that the chip is placed in cut-off requires a narrow chip.

A method of remedying several of these shortcomings is to use the electromagnetic transition shown in Fig. 6. Since the highest frequency HEMT integrated circuits are typically realized in coplanar waveguide, this transition is advantageous because it directly transitions to CPW. As shown in Fig. 6, the TMIC chip sits on a pedestal fabricated on the split block housing. The pedestal acts as both a support and back-short for the integrated circuit. A dipole fabricated on the integrated circuit captures the electromagnetic signal from the waveguide. Note that the dipole is aligned in the same direction as the electric field of the waveguide. Use of this transition at sub-millimeter wave frequencies was reported in [14] which achieved transition loss less than 2 dB from 320–420 GHz for a circuit fabricated on a 50 μm thick substrate and has been used to $>$ 500 GHz in [4] when fabricated on a 25 μm InP substrate.

Reaching operating frequencies as high as 700 GHz has required several modifications to the approach described in the prior paragraph. First, the integrated circuit is fabricated on a 25 μm InP substrate. Therefore, to account for doubling the operating frequency, the substrate thickness has been cut in half. However, from a practical perspective, it is challenging to halve the chip width due to the need for allowing circuitry and DC bond pads at the north and south sides of the chip. Additionally, due to backside registration requirements and topside via pad size requirements, it has also been impractical to double the substrate via density. This has made it significantly more challenging in suppressing undesired modes. Our solution to this is shown in Fig. 7. Substrate is removed from the corners of the chip to create a region that is narrow enough to eliminate undesired resonances. Brighter gold patterns in the microphotograph indicate regions with substrate mode suppression vias. A dense row is present at the input and output. Electromagnetic simulation insures that the density of vias and narrowing of the chip is sufficient to insure transferring the majority of the signal from the rectangular waveguide to the CPW on-chip. Although not shown, the top and bottom regions are reserved in our active

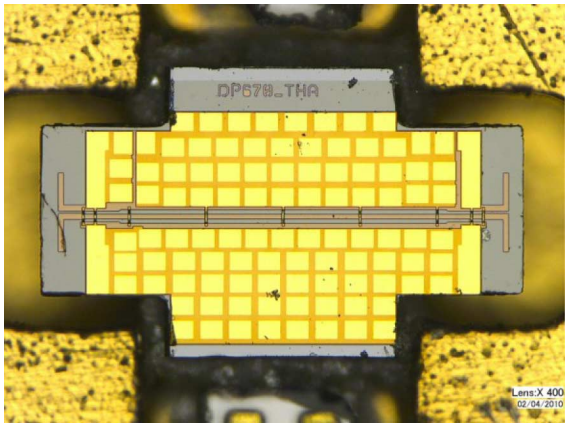

Fig. 7. Microphotograph of CPW through line with WR1.5 waveguide transitions at either end.

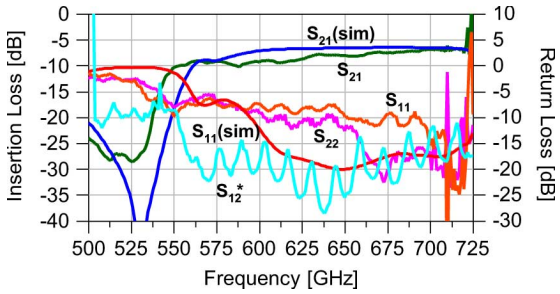

Fig. 8. Measured performance of WR1.5 package with CPW through line.

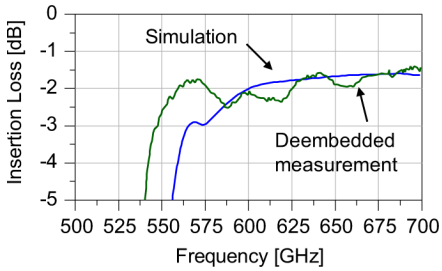

Fig. 9. De-embedded insertion loss of a single transition.

chips for DC bondpads. Channels for DC bias networks are visible at the top and bottom in the package.

Measured performance of the structure shown in Fig. 7 has been measured and is shown in Fig. 8. Note that the measured results include the CPW transmission line, two electromagnetic transitions and feed sections of rectangular waveguide. As a verification of isolation, a measurement of a similar structure terminated in open circuits instead of thru lines is shown as S_{21}^{*} in blue. Simulated performance of the total structure is also shown, and agrees well with the measurement. To determine the loss of the transition itself, we have subtracted the CPW line losses and divided the remaining losses in half assuming that the losses are symmetric. Note that we have verified the loss per millimeter by measuring long CPW lines on-wafer, so we believe the loss estimate is accurate. The resulting de-embedded loss for a single transition is shown in Fig. 9. The loss from 600–700 GHz ranges from 1.5–2 dB. Simulated transition loss is also shown, and agrees well with the de-embedded measurement.

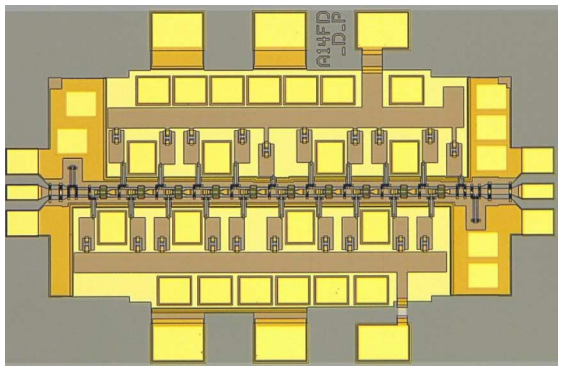

Fig. 10. Microphotograph of 10-Stage 670-GHz low noise amplifier.

V. THz Integrated Circuit Design and Performance

In this section, a variety of circuits are described which have been realized using the 30-nm InP HEMT process. Circuit functions which have been demonstrated using this process include low noise amplification, power amplification, mixing, and multiplication. These results are significant because they demonstrate that amplification is possible at frequencies approaching 1 THz, and that receiver and transmitters operating near 1 THz can be realized using a single semiconductor process.

A. Amplifiers

Amplification is a basic circuit function at lower frequencies and is used for small signal and power amplification. Until recently, these functions have been impossible at Terahertz frequencies and these systems have relied on diode based down-conversion and multiplier chains to process small signals and generate power. In this section, we describe several 670-GHz amplifier and their performance.

Shown in Fig. 10 is a microphotograph of a 10-stage amplifier. From the figure, note that ground-signal-ground patters are set up at the right and left instead of dipole integrated probes. This circuit is therefore set up to be measured on-wafer. The measurement setup consists of WR1.5 frequency extenders developed by Virginia Diodes, Inc., and on-wafer probes developed at the University of Virginia. The probes are scaled to the WR1.5 frequency band based on the designs presented in [15]. The measured S-parameters for the circuit are shown in Fig. 11. The circuit reaches a peak gain of about 30 dB at 670 GHz for a realized transistor gain of approximately 3 dB/stage.

The circuit itself is extremely compact. A typical spacing of only 25 μm is present between gate and drain feeds. All drain bias lines are fed to the top and tied together on a single pad and the gate bias lines are routed to the bottom. This means that the entire 10-stage amplifier must operate from a single bias. The amplifier uses 14 μm transistors biased at a V_{DS} of 1.2 V and a current density of 450 mA/mm, or $\sim$ 65 mA for the 10-stage design. To improve input and output match, a single open-circuited stub is used to improve matching. The bright gold rectangles are substrate mode suppression vias to eliminate the parallel plate waveguide mode.

Noise and power are critical metrics if amplifier technology is to become competitive against mature diode technologies which currently dominate the range from 300–2000 GHz. To date, we

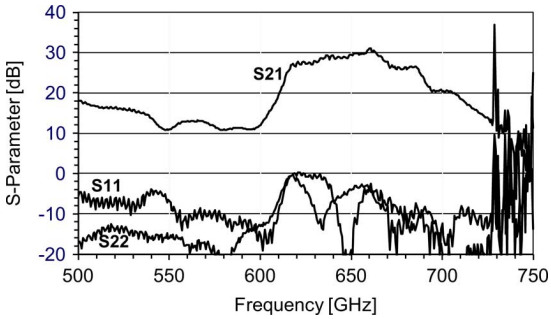

Fig. 11. Measured on-wafer S-Parameters of 10-stage LNA.

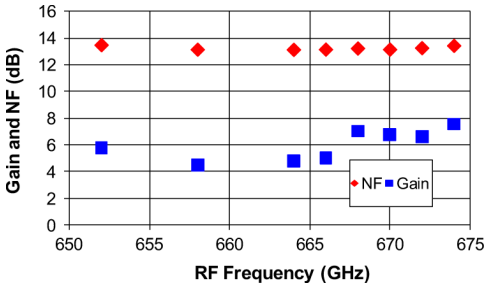

Fig. 12. Measured noise performance of packaged 5- stage low noise amplifier.

have not measured the noise figure of the amplifier shown in Fig. 10. However, we have measured the noise figure of an initial 5-stage prototype in package which was used as the basis of the 10-stage design. The results are shown in Fig. 12. Note that the 5-stage LNA chip contains sections of coplanar waveguide feed at the input and output with approximately 1.4-dB loss. Based on the results of Fig. 11, and the transition losses shown in Fig. 9, an expected packaged gain of 9–10 dB can be deduced. A peak packaged gain of $\sim$ 8 dB is obtained, about 1–2 dB lower. A packaged noise figure of 13 dB is obtained, which is competitive with GaAs Schottky receivers at these frequencies. With the layout changes to eliminate lossy CPW input lines, and additional gain stages of the 10-stage design shown in Fig. 10, it is estimated that the next generation of LNA can reach $<$ 12 dB noise figure with $>$ 20 dB packaged gain.

Power has also been measured from the packaged 5-stage amplifier, and the results are shown in Fig. 13. Note that the blue trace indicates the power measured at the waveguide flange output for the module, and a peak power of 0.6 mW is obtained at 655 GHz, which is considerably encouraging for the first measured result from an amplifier designed for low noise amplification at this frequency. We expect output powers to improve as device technology and modeling improve. Also shown in Fig. 13 is power referenced to the transistor (1.3 mW) which allows transistor Terahertz Frequency power density to be calculated. The 30-nm InP HEMT transistor obtains $\sim$ 100 mW/mm at this frequency.

B. Mixers

Three-terminal devices have long been useful in nonlinear circuits such as mixers and multipliers. Mixers [16] and multipliers [17] have been demonstrated to 220 GHz. With the high speed

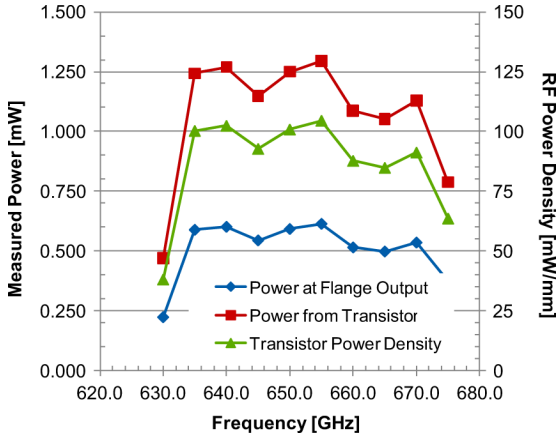

Fig. 13. Measured output power from 5-stage LNA.

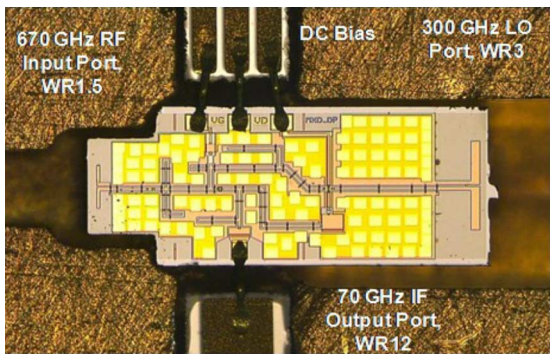

Fig. 14. Microphotograph of InP HEMT sub-harmonic down converting mixer in waveguide fixture.

transistors available in our 30-nm InP HEMT process, it is natural to pursue mixers and multipliers in this technology in addition to amplifiers. As component interconnect losses increase with frequency, it becomes increasingly useful to incorporate multiple functions on a single chip. In particular, direct integration of mixers and multiplier with amplifiers has the potential to improve system performance. In the next two sub-sections, initial results for InP HEMT mixers and multipliers are described.

The down-converter design uses a sub-harmonic single common-source mixer topology. The transistor was biased in the class-B range and designs were done using an Angelov nonlinear model. Open circuited stubs were used to suppress unwanted harmonics as well as for port impedance matching. A microphotograph of the fixture chip is shown in Fig. 14. The chip uses on-chip dipole transitions for RF interface with WR1.5 waveguide and for LO interface with WR3 waveguide. The IF signal is output from the TMIC using a wirebond connection to an off-chip waveguide transition to WR12 waveguide. A measurement of the down conversion loss is shown in Fig. 15. In this measurement, LO frequency was fixed at 304 GHz at a 7-dBm power level which was the maximum available source power at this frequency. The RF was swept from 660–680 GHz. Conversion loss ranges from 22–15 dB.

We expect future iterations to improve conversion loss by improving the model, and by incorporating the LO buffer amplifier directly on-chip. An LNA could also be placed on the same chip, and therefore eliminate $\sim$ 5 dB of interconnect losses.

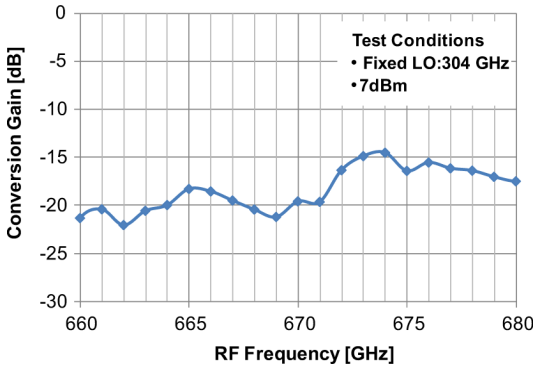

Fig. 15. Measured down conversion loss of sub-harmonic mixer.

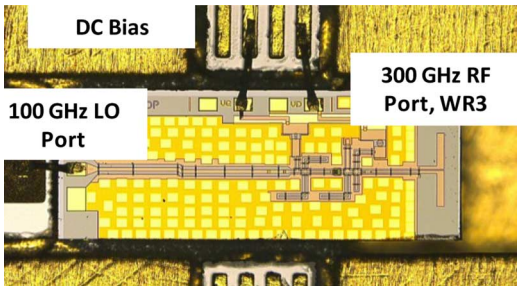

Fig. 16. Microphotograph of InP HEMT frequency tripler in waveguide fixture.

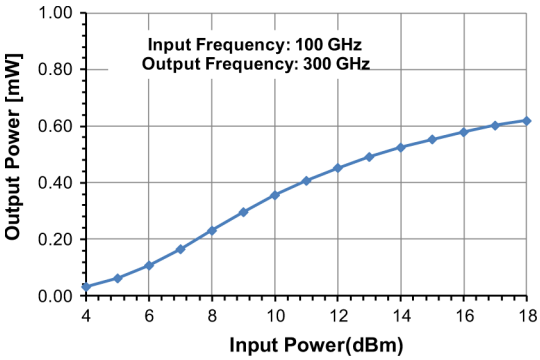

Fig. 17. Measured input power versus output power of the frequency tripler.

C. Multipliers

Frequency triplers have also been demonstrated in the 30-nm InP HEMT process. The tripler was designed using a single common-source device biased in class B mode. Open circuited stubs were used to suppress unwanted harmonics and to power match the RF output for optimum output power. A microphotograph of the fixture chip is shown in Fig. 16. The chip is fed using an off-chip waveguide transition designed for W-band (75–110 GHz). The x3 multiplied signal at 300 GHz is transitioned from the chip to the waveguide using an integrated dipole transition. A power measurement of the frequency multiplier conversion loss is shown in Fig. 17. A peak output power of 0.6 mW at 300 GHz is obtained under 18-dBm drive at 100 GHz. As with the mixer, future iterations would benefit by adding amplification stages to the chip.

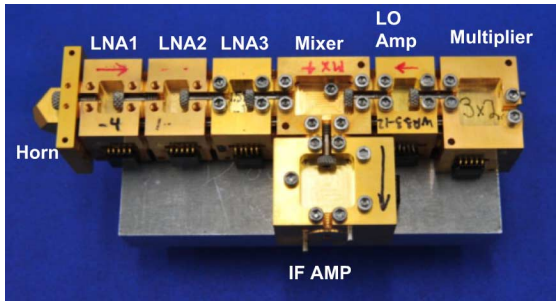

Fig. 18. A 670-GHz receiver with all functions realized in InP HEMT.

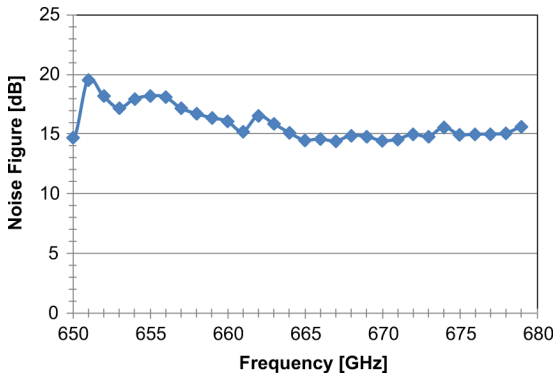

Fig. 19. Measured noise figure of receiver.

VI. InP HEMT Receiver

Based on the prior section, it is clear that all components necessary to build LNA front-end receivers and power-amplifier front-end transmitters at 670 GHz are currently viable in a single semiconductor technology. This provides advantages both in development costs, as well as by allowing a higher level of integration realizing multiple functions on a single-die. This reduces interconnect losses, which are considerable at these frequencies, and manufacturing costs by reducing the number of packages. To demonstrate the viability of an "all HEMT" Terahertz receiver, we have taken various piece-parts described in the prior section and assembled an entire receiver. The receiver is shown in Fig. 18. The receiver uses a 70-GHz IF frequency and a fixed 100-GHz LO frequency. Note that the IF amplifier is at 70 GHz to take advantage of the wide instantaneous RF bandwidth without tuning the LO frequency. Initial performance of the receiver is shown in Fig. 19. The minimum noise figure is below 15 dB. Note that no attempt has been made to de-embed backend noise contribution from the 70-GHz IF channel. Work is currently in progress to design a single-chip receiver incorporating all function on a single-die.

VII. THz Monolithic Integrated Circuit Performance Trends and Benchmarks

A significant amount of progress has been made in increasing the operating frequency of InP HEMT circuits. In this section, we summarize some of the key performance benchmarks across frequency for both low noise amplifiers and power amplifiers.

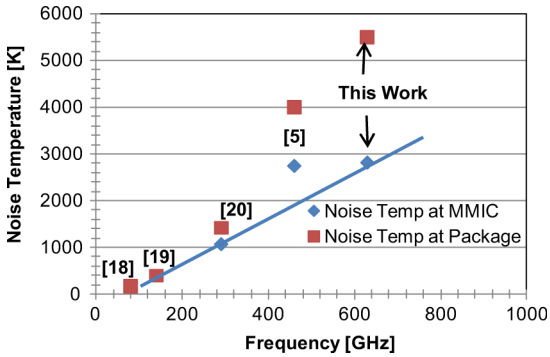

Fig. 20. Northrop Grumman InP HEMT noise temperature trend chart.

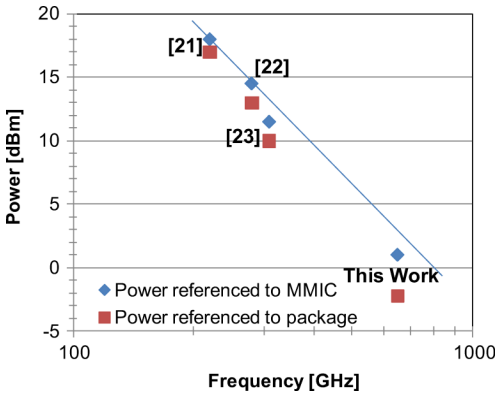

Fig. 21. Plot of measured output power versus frequency for 30- and 35-nm InP HEMT.

Note that some of the data presented here is previously unpublished due to the rapid advances in the field, but are included here to give a good snapshot of current technology capabilities for both low noise and power amplification. Although significant work has been made in other transistor technologies, we have restricted our data to include only the 30- and35-nm InP HEMT process at NGAS.

Low noise amplifier results are shown in Fig. 20, along with a citation for the measurement. Note that [18] and [20] are previously unreported results. From these results, referenced to the TMIC, noise temperature increases fairly linearly with frequency. The packaged results show more rapid increase with frequency due to the increased packaging loss with frequency.

Measured power output results are shown in Fig. 21 across frequency. Due to the greater challenge in developing power amplifiers at Terahertz frequencies, less data is available. In fact, the highest frequency data point is taken from data measured on a low noise amplifier. Note that we are currently developing higher power amplifiers, and project that considerably better power will soon be available at 670 GHz. All of these results are taken at room temperature and off-chip power combining is not used.

VIII. Conclusion

In this paper, the background describing development of amplifiers at 670 GHz using InP High Electron Mobility Transistors is described. This includes high f_{MAX} InP HEMT transistors, a MMIC process tailored to Terahertz integrated circuits, packaging techniques and various circuit types which have been realized in InP HEMT at 670 GHz. The paper concludes with an initial description of a 670-GHz InP HEMT receiver and a summary of 30- and 35-nm InP HEMT benchmarks accomplished over the last five years.

From the results of the paper, it is clear that three-terminal transistors are becoming a viable circuit technology at frequencies approaching 1 Terahertz for low noise amplification, power amplification, and frequency conversion. A significant benefit for using a HEMT process for all of these functions is integration of multiple functions on a single chip, which will eliminate interconnect losses between components, thus improving performance and simplifying packaging.

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