# A 285 GHz sub-harmonic injection locked oscillator in 65nm CMOS technology

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**Abstract — A 285 GHz Sub Harmonic Injection Locked Oscillator (SHILO) is presented using a standard 65nm CMOS process. The architecture of this oscillator is based on the differential LC tank with push-push but adapted to obtain a third harmonic oscillation. The output power is -19 dBm at 285 GHz for a dc power of 70 mW. This oscillator offers a measured phase noise of -96.3 dBc/Hz at 10 MHz and -80.5 dBc/Hz at 1 MHz, and a tuning range from 284.2 GHz to 289 GHz. The SHILO can be locked all along the tuning range with an injection signal corresponding to one sixth of the output frequency. The chip size is 921x451 µm$^2$.**

**Index Terms — Sub-harmonic injection-locked oscillator, THz, sub-THz, CMOS.**

## I. Introduction

Advancements in sub-micron standard CMOS technologies have enabled the opportunity of entirely based CMOS systems working near the sub-THz region and beyond. The maturity, low cost and high level of integration are one of the main advantages of CMOS technologies [1]; however the swapping from SiGe, III-V or other advanced process comes with many drawbacks. Low cut-off frequencies, low breakdown voltages and low quality factor of solid state passive components at those frequencies are some of those many shortcomings [2]. For instance the power lack must be compensated by advancements in the field of design. Much of the interest on THz/sub-THz CMOS circuits comes from the possible applications: THz imaging for quality control or security purposes, high data transfer and compact range radar [2, 3].

One of the most challenging building blocks at these frequencies is the oscillator because the frequency needed is far beyond the standard CMOS process cut off frequencies (fmax around 200GHz). The common technique is the harmonic generation, which means that a fundamental tone is synthesized below the cut off frequency and higher harmonics are boosted using various techniques. Second, third and fourth harmonic generation are the most common techniques [2, 4-7]. In this paper a modified version of the classic scheme of second harmonic generation is presented in order to exploit a third harmonic. It also has a fully functional sub-harmonic injection locking system. The main application of the presented circuit is its use as a local oscillator in a fully CMOS based heterodyne receiver as showed in the Figure 1. For that, the circuit is designed using an easy-lateral access to the output oscillating signal track.

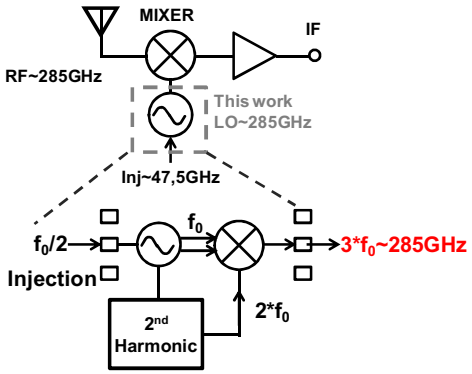


Figure 1: Basic diagram of sub-harmonic injection locked oscillator and its main application as a local oscillator for a heterodyne receiver.

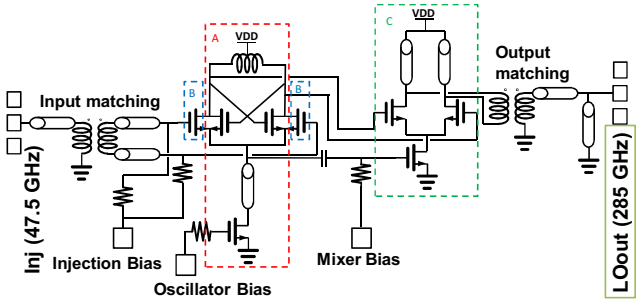


Figure 2: Schematic of the SHILO. *A* corresponds to the oscillator core, *B* shows the injection transistors and *C* is the mixer that allows the system to generate a third harmonic.

## II. Sub-Harmonic Injection-Locking Oscillator

### A. Architecture

The architecture of the SHILO is presented in Figure 1. A differential oscillator generates the fundamental signal; the second harmonic is obtained using a quarter wavelength transmission line. Both signals are injected into a mixer in order to obtain a third harmonic signal (push-push & mix). In Figure 2, the transistor level schematic is presented; for analysis purposes the system has been divided in three parts. Part *A* corresponds to the oscillator core: it consists of a cross coupled pair and an inductance that generate the fundamental signal. The cross coupled pair nMOS capacitances together with the inductance define the fundamental oscillation frequency. The second harmonic is obtained using push-push technique with the help of a short ended quarter wave-length micro-strip line at 190 GHz at the common mode node.

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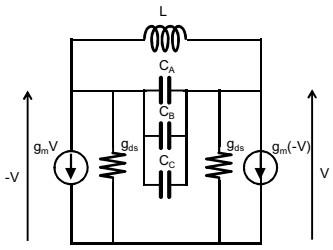
The injection transistors (part *B*) are used for locking the oscillator in order to stabilize the oscillation frequency and fix the phase noise on the injection source. The injection signal (around 47 GHz) is one sixth of the output oscillation frequency. In order to generate the third harmonic, a single balanced differential active mixer is used to mix the fundamental tone and the second harmonic (part *C*). Output 50 Ohm matching is adjusted to 285 GHz using micro-strip transmission lines and an output balun for single ended measurements. Thus, inferior mixing products are rejected.

The fundamental frequency also depends on the injection and the mixing circuitry transistors that add parallel capacitances to the resonator. In Figure 3, a simplified version of the small signal equivalent circuit is depicted.




$$C_A = \frac{C_{gs}}{2} + \frac{C_{ds}}{2} + 2C_{gd}$$

$$C_B = \frac{C_{gd\,injection}}{2} + \frac{C_{ds\,injection}}{2}$$

$$C_C = \frac{1}{2}\left(\frac{C_{gdmixer}\,C_{dsmixer}}{C_{gdmixer} + C_{dsmixer}} + C_{gsmixer}\right)$$

Figure 3: Simplified small signal equivalent circuit of the sub-harmonic injection locking oscillator

The fundamental oscillation frequency can be defined by the following expression:

$$F_{osc} = \frac{1}{2\pi\sqrt{L(C_A + C_B + C_C)}}. \qquad (1)$$

Since the frequency expression has many variables, the accuracy on the oscillation frequency depends extremely in the capacitance extraction of all the transistors (intrinsic part and accesses) as well as the inductance modelling. Inductive components used for the resonator and matching networks are thin film micro-strip lines modelled using full wave electromagnetic simulations with ANSYS HFSS. Injection and output baluns models as well as pads are generated using AGILENT MOMENTUM.

### *B. Tuning and Locking Range*

The oscillation frequency is tuned despite the lack of varactors; the intrinsic capacitances ($C_{gs}$, $C_{ds}$ and $C_{gd}$) of the cross coupled pair are inherently tuned as the oscillator bias is changed. As a result, the oscillator offers for the third harmonic a 4.8 GHz tuning range. However, as a counterpart the output power decreases as the bias is reduced in order to increase the frequency. The oscillator is locked all along the tuning range with a signal equivalent to one sixth of the output frequency (around 47 GHz). The main drawback of the implemented locking system is the additional parallel capacitance of the injection transistors which causes a significant decrease of the oscillation frequency tuning range.

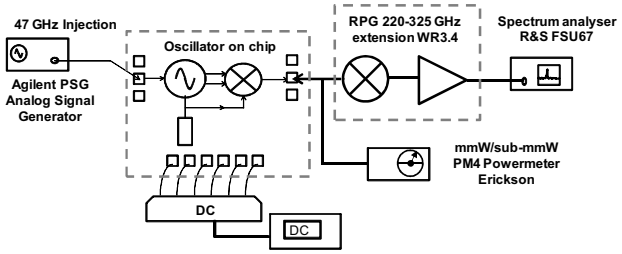



Figure 4: Test setups: spectrum analyzer and external mixer for frequency and phase noise measurements. Power meter for output power measurements.

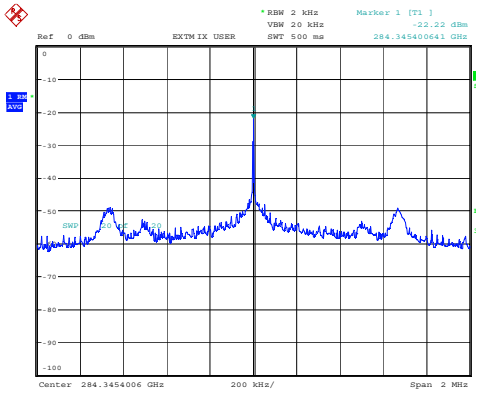



Figure 5: Measured output spectrum at 284.34 GHz.

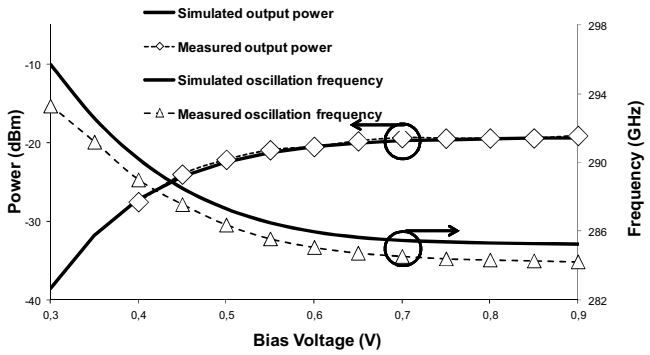



Figure 6: Output power and free running oscillation frequency vs. bias voltage. Symbols: measurements. Line: simulation.

## III. MEASUREMENTS

The test setup is presented in Figure 4. An AGILENT PSG analog signal generator was used as sub-harmonic injection source. The frequency and phase noise were measured with a R&S FSU67 spectrum analyzer with 220-325 GHz extension, and the output power with an Erickson PM4 mmW/sub-mmW powermeter. Figure 5 depicts a snapshot of the output spectrum when a 47.39 GHz injection signal is applied.

Figure 6 depicts the measured and simulated results of the output power and the free running oscillation frequency for different bias configurations. Oscillation frequency spans from 284.2 GHz to 289 GHz while the output power varies from -19 dBm to -27 dBm. We observe that simulations fit measurements with good accuracy which validates the chosen modelling approach.

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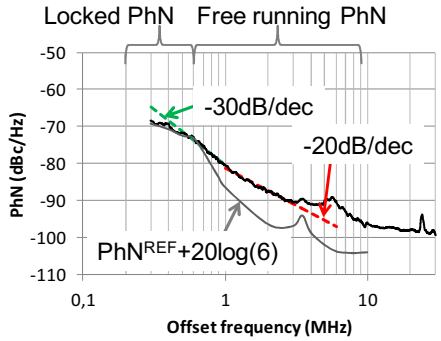


Figure 7: Injection source and locked oscillator phase noise.

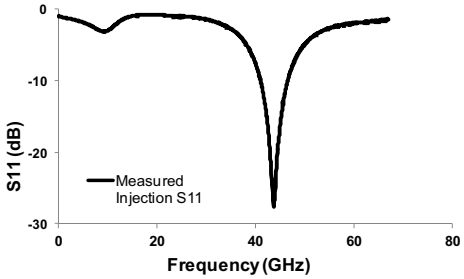


Figure 8: Reflection coefficient of the injection port

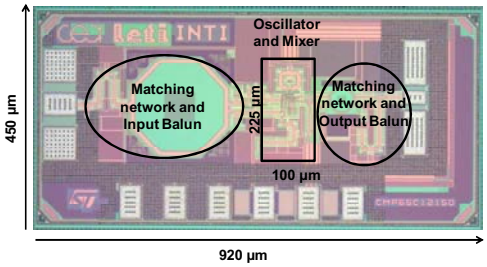


Figure 9: Chip micrograph of the CMOS 65nm sub-harmonic injection locked 285 GHz oscillator.

Figure 7 represents the locked oscillator as well as the injection source +20log (6) phase noise. Up to 700 KHz offset, the oscillator phase noise fits to the reference phase noise + 20log(6). Above 700 KHz offset, the measured phase noise corresponds to the free running oscillator phase noise. It is equal to -80.5 dBc/Hz and -96.3 dBc/Hz at 1 MHz and 10 MHz offset, respectively.

The injection input S11 is presented in Figure 8. A micrograph of the circuit is shown in Figure 9; the core area of the oscillator is 100x225 µm². The signal output track is located at the right side of the chip which enables the use of this circuit in any heterodyne receiver or transmitter without topological modifications on the layout. However, the lateral direct access to the signal implies an asymmetrical layout that decreases matching and output power compared to a fully balanced structure with middle point access.

## IV. Conclusion

A 285 GHz SHILO has been designed and fabricated in a standard 65nm CMOS process. It offers a third harmonic output of 285 GHz with an output power of -19 dBm and a tuning range of 4.8 GHz. The injection signal corresponds to one sixth of the output frequency and locks the oscillator all along the tuning range. The DC consumption of the circuit is 70 mW. An easy access to the output signal track is designed that enables its co-integration in real case receiver or transmitter circuits. The chip size is 921µm x 451µm including matching networks and pads. To the authors' knowledge, this is the first CMOS injection locked oscillator around 300 GHz (see Table I).

TABLE I
COMPARISON OF REPORTED OSCILLATORS

| References | [2] | [2] | [5] | [7] | [7] | **This Work** |
|---|---|---|---|---|---|---|
| CMOS Tech. | 130nm | 65nm | 65nm | 65nm | 65nm | **65nm** |
| Harmonic # | 3 | 3 | 3 | 4 | 4 | **3** |
| Fosc (GHz) | 256 | 482 | 288 | 290 | 320 | **285** |
| Pout (dBm) | -17 | -7.9 | -1.5 | -1.2 | -3.3 | **-19** |
| $P_{DC}$ (mW) | 71 | 61 | 275 | 325 | 339 | **70** |
| Injection Locking | No | No | No | No | No | **Yes** |
| Accesibility | Center | Side | Side | Center | Center | **Side** |
| Free Osc. Phase noise at 1MHz (dBc/Hz) | -88 | -76 | -87 | -78 | -77 | **-80.5** |


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