A 310–340-GHz Coupled-Line Voltage-Controlled Oscillator Based on 0.25-μm InP HBT Technology

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***Abstract*—A THz voltage-controlled oscillator (VCO) has been developed in this work based on a 0.25-μm InP heterojunction bipolar transistor (HBT) technology. The cross-coupled push-push oscillator adopted a novel coupled-line topology, in which the DC blocking capacitors and the load inductance are replaced by a pair of coupled-lines to improve the oscillation frequency and reduce the circuit area. Also, a base bias tuning was employed for effective oscillation frequency tuning. The circuit exhibited the voltage tuning from 309.5 GHz to 339.5 GHz, leading to a tuning range of 30 GHz. The maximum output power was −6.5 dBm at 334 GHz, achieved with a dc power consumption of 13.5 mW. Measured phase noise was −86.55 at 10-MHz offset. The circuit occupies only 0.014 mm^2 excluding the probing pads.**

***Index Terms*—Frequency control, heterjunction bipolar transistor (HBT), voltage-controlled oscillators (VCOs).**

I. Introduction

THERE is a growing interest in the frequency band around 300 GHz for various applications such as THz broadband communication and THz imaging. With the recent advances in semiconductor device technologies, integrated circuits operating in this band became readily available. The oscillator is one of the key components in THz systems, mainly adopted as a signal source for transmitters or a local oscillator (LOs) for receivers. Hence, there have been growing recent efforts to implement oscillators operating in the THz band [1]–[5]. The primary requirement for the high-frequency oscillators is the high output power, and III-V technologies have been favored for this aspect. The recent THz oscillators based on III-V technologies are either based on Colpitts [6] or common-base cross-coupling topology [7]. In this work, we propose a new coupled-line structure based on the common-emitter cross-coupled topology, in which the dc blocking capacitors in the coupling path and the load inductance are replaced by a pair of coupled lines. With a 0.25-μm InP HBT technology, we experimentally show that the adoption of the coupled-line structure enhances the operation frequency while significantly reducing the area for compact layout. Additionally, it is demonstrated that base bias control can be conveniently employed for oscillation frequency tuning, which is particularly useful when varactors are not readily available as in the case of the InP HBT technology used for this work.

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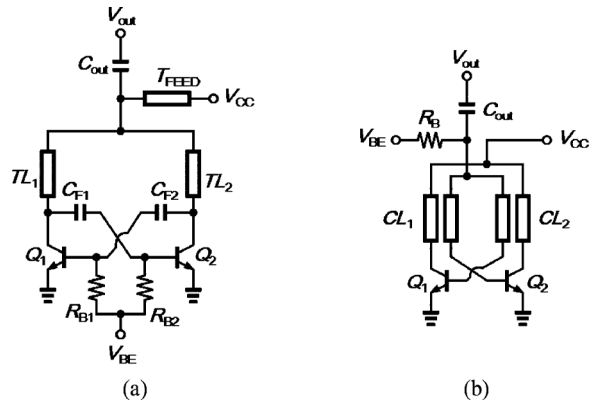

Fig. 1. Schematic of (a) conventional cross-coupled oscillator and (b) proposed cross-coupled oscillator.

II. Circuit Design

Fig. 1(a) shows the schematic of a conventional common-emitter cross-coupled push-push oscillator. One distinctive feature of the bipolar-based cross-coupled oscillator core, which is not typically found in the FET-based core, is the inclusion of dc blocking capacitors on the feedback path ($\mathrm{CF}_1, \mathrm{CF}_2$). They are needed to separate the potentials at the base of $\mathrm{Q}_1(\mathrm{Q}_2)$ and the collector of $\mathrm{Q}_2(\mathrm{Q}_1)$ for independently optimized bias conditions at the base and the collector. For this purpose, metal–oxide–metal (MIM) capacitors are usually employed, but they necessarily accompany additional parasitic series inductance. For example, for the technology used in this work, a MIM capacitor of 100 fF involves a series inductance of 6 pH, which is comparable to or even larger than the line inductance from the feedback path. This parasitic inductance degrades the oscillation frequency of the cross-coupled oscillator, as indicated by the relation [7]

$$\omega_{\mathrm{OSC}} = \sqrt{\frac{1}{(L_F + L_C)}\left(\frac{1}{C_F} + \frac{1}{C_{\mathrm{BE}}}\right)} \tag{1}$$

where L_{F} is the total inductance of the feedback path, which includes the parasitic inductance of the dc blocking capacitor, L_{C} is the load inductance, C_{F} is the capacitance of the dc blocking capacitor, and C_{BE} is the base-emitter capacitance of the HBT. L_{F} can be reduced to increase the oscillation frequency by shortening the feedback path, but the parasitic inductance of the dc blocking capacitor remains unaffected and cannot be removed. This issue is resolved in the proposed oscillator shown in Fig. 1(b). In this topology, the dc blocking capacitors and the load inductance are replaced by a pair of coupled lines. The coupled lines serve to separate the biases of

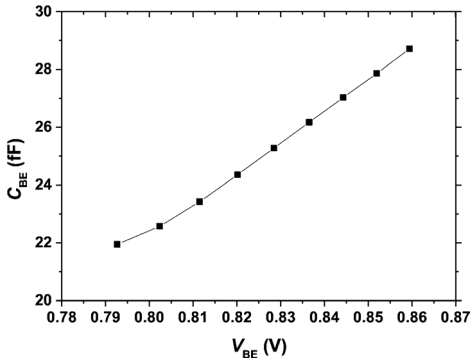

Fig. 2. $C_{\rm BE}$ plotted as a function of $V_{\rm BE}$ variation obtained from the device model.

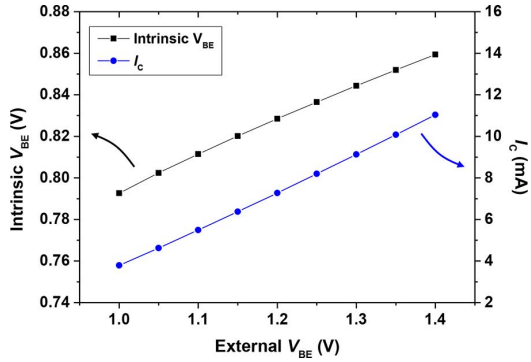

Fig. 3. Intrinsic $V_{\rm BE}$ and collector current plotted as a function of the external $V_{\rm BE}$.

the base and the collector while providing the load inductance, thus obviating the need for the dc blocking capacitors. Hence, parasitic inductance from the MIM capacitor is absent and oscillation frequency is increased.

Additionally, the proposed oscillator benefits from another advantage of chip area reduction, which comes from three factors. First, the area for the capacitor is saved, which ranges around 20 μm $\times$ 20 μm. Second, the coupled lines occupy smaller area than the original load inductance. They employ a stacked structure composed of M3 (t = 1 μm) and M4 (t = 3 μm), avoiding lateral spread. Moreover, the required physical length of the coupled lines to provide the same reactive effect as the original load inductance is only a half of the load inductance based on the single transmission line [8]. Third, $T_{\rm FEED}$, which was originally included for the isolation of the $V_{\rm CC}$ node from the output port, can be removed because the output is now taken from the common node of the base, not of the collector, which naturally isolates the output from the $V_{\rm CC}$ node. As will be revisited later, the proposed oscillator occupies only 95 μm $\times$ 100 μm when implemented. It can be commented that the output extraction at the base common node instead of the collector common node does not affect the output power level since they are ac-coupled to each other.

Another distinctive feature of the proposed circuit is that the oscillation frequency tuning is achieved by the base bias variation instead of the varactor tuning. As indicated by (1), $C_{\rm BE}$ affects the oscillation frequency of the cross-coupled oscillator. $C_{\rm BE}$ tends to increase with increasing base bias, because both the junction and the diffusion capacitances at the B-E junction increase as $V_{\rm BE}$ increases. This is well depicted in Fig. 2, which shows $C_{\rm BE}$ extracted from the device model [9] as a function of $V_{\rm BE}$ for the device size used in this work. One problem that may be associated with this tuning method is the high tuning sensitivity over the base bias voltage. To relax the sensitivity, a resistor $R_{\rm B}$ is inserted at the base common node of the proposed oscillator. Due to the low current gain of III-V HBTs, there is substantial base current flowing that leads to a considerable voltage drop across $R_{\rm B}$, which is more significant with a large $V_{\rm BE}$. As a result, the change in the intrinsic $V_{\rm BE}$ due to the increase in the external $V_{\rm BE}$ tuning is only moderate. Also, because the change in $V_{\rm BE}$ is small, the variation in the collector current $I_{\rm C}$ due to tuning is not excessive, either. Fig. 3 shows the simulated intrinsic $V_{\rm BE}$ and $I_{\rm C}$ plotted against the external $V_{\rm BE}$.

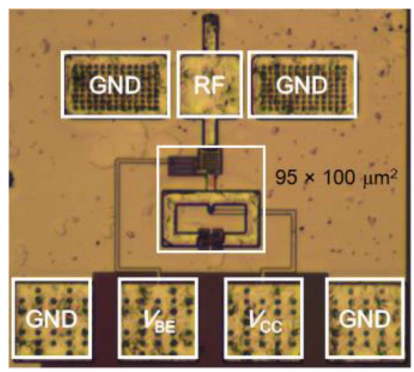

Fig. 4. Chip photograph of the fabricated oscillator.

III. Measurement Results

The proposed oscillator was fabricated with Teledyne 0.25-μm HBT technology which shows $f_{\rm T}/f_{\rm max}$ = 359 GHz/859 GHz [10]. Fig. 4 shows the chip photo of the fabricated circuit. The chip size exclusive of the probing pads is 95 μm $\times$ 100 μm.

The oscillator was characterized with two measurement setups [7]. First, the oscillation frequency and the phase noise were measured with a spectrum analyzer for the output signal down-converted with an H-band subharmonic mixer. Fig. 5 shows the measured oscillation frequency of the circuit with external $V_{\rm BE}$ variation. Shown as an inset is the output spectrum measured at oscillation frequency of 317.5 GHz. With $V_{\rm BE}$ varied from 1.0 to 1.4 V, the oscillation frequency is tuned from 339.5 to 309.5 GHz, leading to a tuning range of 30 GHz. Also shown is the simulated tuning behavior, which shows a slightly steeper slope. It appears to be related to the observed weaker sensitivity of I_C over the external $V_{\rm BE}$ variation in the measurement. The phase noise of the oscillator measured at a bias condition of $V_{\rm BE}$ = 1.3 V is shown in Fig. 6. At the corresponding oscillation frequency of 317.5 GHz, the measured phase noise at 10 MHz offset was -86.55 dBc/Hz. Note that the collector bias $V_{\rm CC}$ was fixed at 1.5 V for the entire measurement.

Second, the output power was measured with a setup where the output signal of the circuit was directly injected into a VDI PM4 power meter without frequency down-conversion. Fig. 7 shows the measured and the simulated output power of the oscillator plotted as a function of the external $V_{\rm BE}$ tuning voltage. The measured output power was varied with $V_{\rm BE}$

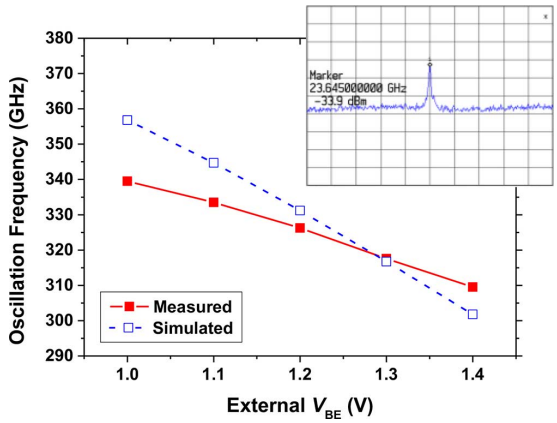

Fig. 5. Tuning characteristics of the oscillator. Inset is the measured output spectrum of the oscillator at $V_{\mathrm{BE}} = 1.3$ V.

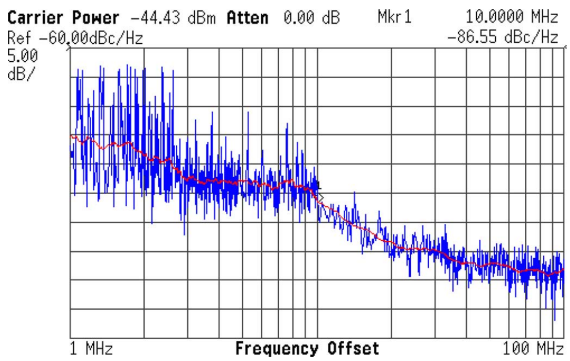

Fig. 6. Measured phase noise of the oscillator. V_{BE} (external) $= 1.3$ V and $V_{\mathrm{CC}} = 1.5$ V.

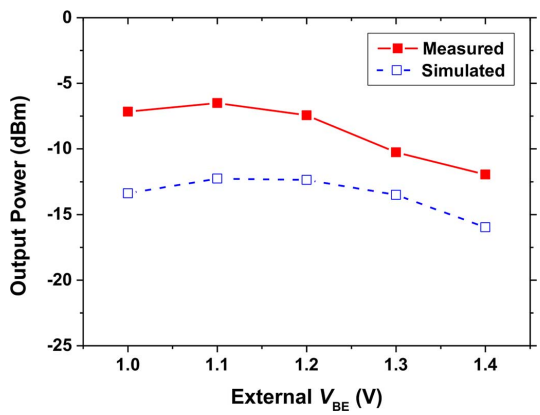

Fig. 7. Measured output power of the oscillator.

tuned from 1.0 to 1.4 V, the maximum value being measured as -6.5 dBm at 334 GHz with V_{BE} of 1.1 V. The corresponding dc power dissipation was 13.5 mW. The measured output power is larger than simulation, partly due to the larger measured I_C than simulation. It is noted that the measurement loss from the H-band probe and the waveguide were compensated for in the values reported here.

Table I compares the result obtained in this work with the prior arts reported near H-band. The proposed oscillator shows the largest tuning range, while occupying a significantly smaller area.

TABLE I
COMPARISON OF H-BAND OSCILLATORS

Technology	Frequency (GHz)	Peak P_{out} (dBm)	Tuning Range (GHz)	Chip Area (mm^2)
65 nm CMOS [1]	293	-2.74	-	0.25 ‡
120 nm SiGe HBT [2]	309-330	-13.3	21	-
35 nm InP HEMT [3]	330	-5.7	-	0.35†
250 nm InP HBT [4]	325	-5	-	0.23*
250 nm InP HBT [5]	248-262	2.9	14	0.27†
250 nm InP HBT (This Work)	309.5-339.5	-6.5	30	0.14† 0.015*

† including pads ‡ including antenna * oscillator core only

IV. CONCLUSION

A common-emitter cross-coupled push-push VCO has been developed based on an InP HBT technology, which adopted the coupled-line topology for improved oscillation frequency and size reduction. It exhibited an oscillation frequency tuning of 309.5–339.5 GHz with V_{BE} variation, with measured maximum output of -6.5 dBm at 334 GHz and chip size of only 0.015 mm^2 excluding the pads. This compact oscillator is expected to be well suited for various THz applications that needs a wide frequency tuning near H-band.

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