A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs

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(Invited Paper)

***Abstract*—Gallium–nitride power transistor (GaN HEMT) and integrated circuit technologies have matured dramatically over the last few years, and many hundreds of thousands of devices have been manufactured and fielded in applications ranging from pulsed radars and counter-IED jammers to CATV modules and fourth-generation infrastructure base-stations. GaN HEMT devices, exhibiting high power densities coupled with high breakdown voltages, have opened up the possibilities for highly efficient power amplifiers (PAs) exploiting the principles of waveform engineered designs. This paper summarizes the unique advantages of GaN HEMTs compared to other power transistor technologies, with examples of where such features have been exploited. Since RF power densities of GaN HEMTs are many times higher than other technologies, much attention has also been given to thermal management—examples of both commercial "off-the-shelf" packaging as well as custom heat-sinks are described. The very desirable feature of having accurate large-signal models for both discrete transistors and monolithic microwave integrated circuit foundry are emphasized with a number of circuit design examples. GaN HEMT technology has been a major enabler for both very broadband high-PAs and very high-efficiency designs. This paper describes examples of broadband amplifiers, as well as several of the main areas of high-efficiency amplifier design—notably Class-D, Class-E, Class-F, and Class-J approaches, Doherty PAs, envelope-tracking techniques, and Chireix outphasing.**

***Index Terms*—Broadband, gallium nitride (GaN), high efficiency, monolithic microwave integrated circuit (MMIC), power amplifier (PAs), power transistor, silicon carbide.**

TABLE I
MATERIAL PROPERTIES OF MICROWAVE SEMICONDUCTORS [1]

Material	Mobility, μ, $cm^2/V.s$	Dielectric Constant, ε	Bandgap, Eg, eV	Break down field, Eb 10^6V/cm	BFOM Ratio	Tmax, ^oC
Si	1300	11.9	1.12	0.3	1.0	300
GaAs	5000	12.5	1.42	0.4	9.6	300
4H-SiC	260	10	3.2	3.5	3.1	600
GaN	1500	9.5	3.4	2	24.6	700

BFOM is Baliga's figure of merit for power transistor performance ($\mu*\varepsilon*Eg^3$)

TABLE II
IMPACT OF GaN ON PA CONCEPTS

Concept	Silicon	GaN on SiC
Class E/F/J	Low f_T, moderate breakdown voltage	High f_T, high breakdown voltage
Doherty	Low off-state impedance, high output capacitance	High off-state impedance, low output capacitance
LINC	Large non-linear output capacitance	Small non-linear output capacitance
EER/ET	Poor amplitude to phase modulation conversion, moderate bandwidth	Good amplitude to phase modulation conversion, large bandwidth
Digital Pre-Distortion	High thermal time constant, moderate bandwidth	Low thermal time constant, large bandwidth

I. INTRODUCTION

WIDE-BANDGAP semiconductor technology for high-power microwave devices has matured rapidly over the last several years as evidenced by the fact that AlGaN/GaN HEMTs have been available as commercial-off-the-shelf (COTS) devices since 2005. The material properties of GaN compared to competing materials are presented in Table I. AlGaN/GaN HEMTs possess high breakdown voltage, which allows large drain voltages to be used, leading to high output impedance per watt of RF power, resulting in easier matching and lower loss matching circuits. The high sheet charge leads to large current densities and transistor area can be reduced resulting in high watts per millimeter of gate periphery. The high saturated drift velocity leads to high saturation current densities and watts per unit gate periphery. In turn, this leads to lower capacitances per watt of output power. Low output capacitance and drain-to-source resistance per watt also make GaN HEMTs suitable for switch-mode amplifiers.

Research and development of GaN HEMTs gained considerable momentum in the late 1990s and early 2000s when it became possible to reproducibly grow high-quality 4H-SiC substrates [2], [3]. In particular, GaN HEMT technologies have had a significant impact on various power amplifier (PA) concepts, as outlined in Table II [4] where a comparison is made between silicon LDMOSFETs (the "incumbent" technology for many applications) and GaN on SiC HEMTs.

High total RF powers from GaN HEMT transistors over a wide frequency range have been reported for single die up to several hundred watts [5], [6]. However, these high power densities, in terms of watts per millimeter, also present extreme power dissipation demands on both the transistor layouts, as

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well as the semiconductor substrates. Fortunately, the high thermal conductivity of SiC substrates (>330 W/m · K) allows these high power densities to be efficiently dissipated for realistic drain efficiencies, preventing the extreme channel temperatures that would result due to self-heating with other substrate technologies. For example, a commercially available 120-W discrete transistor (Cree CGH40120F) operating at 28 V will generate 120 W of continuous wave (CW) RF power, and at its saturated output power, has a drain efficiency of 65%. With a rated CW thermal resistance of 1.5 °C/W, the dissipated power is 64 W with a channel temperature rise of 96 °C allowing the device to comfortably operate at baseplate temperatures in excess of 100 °C. The effective pulsed thermal resistances of such devices are also lower (dependent on pulsewidth and duty factor)—this aspect will be covered in Section IX.

In summary, GaN offers a rugged and reliable technology capable of high-voltage and high-temperature operation. This opens up many industrial, defense, medical, and commercial applications that can be targeted by GaN.

II. Overview of Technology

Early progress on GaN/AlGaN HEMT technology in the 1990s was concentrated on three main areas, including improving epitaxial layer material quality, selecting the best substrate materials, and developing unit processes (e.g., [7]). Many of the advances in hetero-epitaxy of GaN and AlGaN were based on early metal–organic chemical vapor deposition (MOCVD) work in the field of opto-electronics [8]. However, both molecular beam epitaxy (MBE) and MOCVD growth methods were perceived as viable for GaN-based electronics devices [9], [10]. Most of the advancements in epitaxial growth were first achieved on sapphire due to its availability, but commercial ventures for GaN HEMT devices have all adopted either Si as a "low-cost" substrate or semi-insulating 6H- or 4H-SiC for superior high-power performance and thermal management. State-of-the-art power levels have been demonstrated on SiC substrates with total output powers of 800 W at 2.9 GHz [6] and over 500 W at 3.5 GHz [11].

The performance benefits for these devices are remarkable due to their ability to make heterostructures in a material system that also supports high breakdown fields. This has provided the key components necessary for high breakdown voltage and high transconductance device results as the technology advanced in the mid 1990s [10]. Clear understanding of the phenomenon of 2DEG carrier densities greater than $1 \times 10^{13}/\text{cm}^2$ was achieved after strain- and polarization-induced charges were clearly explained [11]. Subsequent device structure and processing enhancements led to the first results of passivated GaN HEMTs with results showing the clear thermal advantage of using SiC as a substrate instead of sapphire for high total RF power [14] and [15].

The epilayers for Cree commercial HEMTs are grown by MOCVD in a high-volume reactor on 100-mm semi-insulating 4H silicon carbide (SI 4H-SiC) substrates that are cut on-axis. The epitaxial growth process is highly reproducible and in production for several years, in part due to the funding on the Defense Advanced Research Projects Agnecy (DARPA) Wide Bandgap Semiconductor (WBGS) Program that was initiated

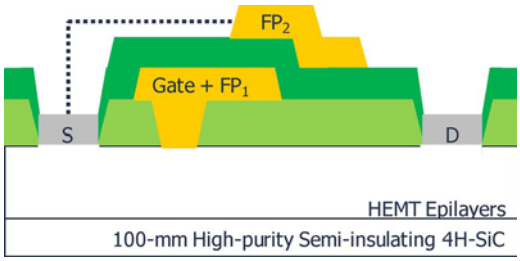

Fig. 1. Schematic cross section of the AlGaN/AlN/GaN HEMT RF structure showing integrated first field plate and source-connected second field plate.

in 2002 [16]. Typical structures comprise an AlN nucleation layer, 1.4 μm of Fe-doped insulating GaN, approximately 0.6 nm of an AlN barrier layer, and a 25-nm cap layer of undoped $Al_{0.22}Ga_{0.78}N$. This nominal layer thickness and mole fraction yield sheet electron concentrations in the range of 8 to $10 \times 10^{12}/\text{cm}^2$, but due to the AlN interlayer has the strong advantage of electron mobilities near 2000 $\text{cm}^2/\text{V} \cdot \text{s}$ at room temperature [17]. The channel sheet resistance is about 335 Ω per square.

As shown in the schematic cross section of Fig. 1, the device is fabricated with ohmic contacts that are formed directly on the top AlGaN layer. Device isolation is achieved using nitrogen implants to achieve a planar structure [18]. Gate electrodes are formed by recessing through a first SiN dielectric to the AlGaN and then depositing Ni/Pt/Au metallization. Very strong peak electric fields occur at the drain-side edge of the metal semiconductor junction in this lateral device. The optimized device includes a lateral extension of the gate electrode on the drain side to provide an elegant integration of field shaping with the gate metallization. The gate footprint is offset to reduce source resistance and increase gate-to-drain breakdown voltage. The gate length of the device is nominally 0.4 μm, and the gate-to-drain spacing is about 3 μm. After a second passivation, a source connected second field plate is fabricated to provide further electric field shaping at the highest drain voltages and to reduce gate to drain feedback capacitance of the device [19], [20]. The 1-mA/mm (gate current) breakdown voltage of this structure exceeds 150 V. Unit cell devices exhibit CW on-wafer output power levels of 4–5 W/mm when measured on a load–pull bench at 28 V and 3.5 GHz. The gate connected second field plate together with integrated first field plate has become the most widespread device structure in the industry for RF applications below 20 GHz.

Microwave monolithic circuit demonstrations were an early goal of those developing the technology. Besides Cree Inc., a number of other GaN MMIC foundries provide similar technologies such as Triquint, Raytheon, and Hughes Research Laboratories. After the basic transistor device is completed, standard passive components such as metal–insulator–metal (MIM) capacitors, thin-film resistors, and through-wafer slot vias are utilized in the Cree Inc. process to achieve high-performance versatile monolithic microwave integrated circuit (MMIC) products (Fig. 2). The MIM capacitors have been developed to support peak voltages greater than 100 V. SiC substrate vias has allowed the straightforward implementation of the amplifier circuits without the need of cumbersome

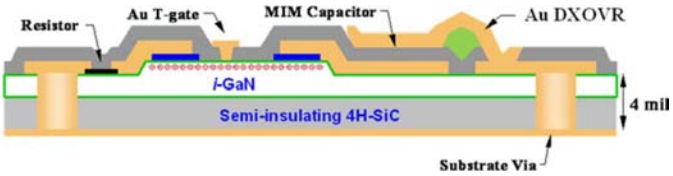

Fig. 2. Schematic cross section of typical GaN HEMT MMIC process.

coplanar waveguide grounding schemes. Specifically, slot vias are implemented in the 100-μm-thick SiC substrates to simplify layout and increase gain. Three types of resistors are available: nichrome thin film with 12-Ω/square resistance and two "bulk" GaN resistors with 70- and 400-Ω/square resistance. Bulk GaN resistor layers are covered by thick dielectric insulators, enabling metal crossovers. A 0.4-μm gate-length 28-V process provides 4.5 W/mm of gate periphery for circuits between dc to 8 GHz, while a 0.25-μm gate-length 40-V process provides 7 W/mm of gate periphery between dc and 18 GHz.

III. GaN HEMT Large-Signal Modeling

Field-effect transistor (FET) models have a long history. In Shockley's original FET work, a physical representation was derived to predict operation of the junction field-effect transistor (JFET). Models have evolved from this point to describe and design new field-effect devices and to facilitate their various uses. There have been many new device structures and circuits produced over the 60 years that have passed since Shockley's work, as well as an equally impressive list of modeling approaches. This branching of FET lineage has been driven by both military and civilian radar and communication system needs. In addition, various types of device models have been developed depending on application. An area of intense focus for both device and model development has been that of high-efficiency PAs. System cost is driven by prime power and cooling requirements and improved efficiency is the key to reducing these costs. Improved power devices, along with proper measurements and models, have driven an increase in performance; hence, the focus of the presently described review.

Recently, most effort in PA design has been focused on GaAs pseudomorphic HEMTs (pHEMTs), Si LDMOSFETs, and GaN HEMTs. Models have been developed and adapted to these devices and share many common features because they are all field-effect structures. The focus of this study is to provide an example of this adaptation to the development of GaN HEMT models for MMIC and RF integrated circuit (RFIC) design. There have been excellent overviews of the state of modeling over the years. One recent example is by Dunleavy *et al.* [21]. The intent of this section of this paper is to present one possible solution to the modeling/design problem as applied to the GaN HEMT while acknowledging that there are many other viable solutions.

There are two general approaches to HEMT (or other active device) modeling. One is table based, the best known of which has been developed by Root. The table data can either be measured or simulated using 2-D physical simulators. An extension of this work appears in [22]. A more recent version of this approach is the new X-parameter model formulation, which is based on significant small- and large-signal measurements [23]. This approach can be very accurate, but requires intensive measurement resources. To improve accuracy, the entire simulation space must be mapped using both large- and small-signal measurements including load–pull and linearity. It is certainly desirable to have the largest possible measurement database from which to extract and verify any model, but these measurements can be time consuming and expensive. A properly formulated model based on physical equations allows a reduction in required measurements without a significant loss in accuracy.

The second approach involves the description of the active device by closed-form physical equations, the parameters of which can be extracted from measured data. This is the approach chosen to support Cree Inc. device models and reported here. There has been much work over the past 60 years on this topic, ramping significantly with the advent of the GaAs MESFET in the late 1970s. The model described here uses various formulations, from published work, combined in such a way as to allow parameter extraction using a minimal set of measurements. An added aspect to the model development is verification using an extensive library of MMIC amplifier designs up to 20 GHz, as well as a large number of hybrid circuits using packaged devices. The model was originally developed specifically for MMIC design, thus allowing continuous improvements as MMICs were developed, measured, and simulations verified.

The starting point for the HEMT model is the drain current formulation. The basis for the $I_D(V_G, V_D)$ function is very similar to the formulation given by Statz *et al.* [24]. A common feature in the drain formulation of this model and other notable versions [25], [26] is the drain voltage saturation parameter

$$I_D \sim \tanh(\alpha * V_D).$$

A variant of this function is included in the present model together with a gate voltage parameter similar to that in [25]. Another feature, using work from [26], has proven useful in modeling drain current variations near pinch-off as

$$I_D \sim \beta(V_D - V_{\mathrm{DSO}}).$$

A feature common to these drain current formulations, which caused an issue early in the work, was the lack of a gate voltage saturation mechanism. The original intent would be to limit channel current with forward gate conduction. This proved somewhat problematic in practice, particularly when high compression is used in high-efficiency PAs. The hyperbolic tangent function, ubiquitous in modeling, proved helpful in saturating $I_D(V_G)$. A well-known application is found in the Angelov (or Chalmers) model [27]. A deficiency in this approach became apparent in fitting GaN HEMT devices for both linearity and efficiency predictions. As shown in [24], the GaAs MESFET (and in the GaN HEMT as well) drain current obeys a square-law dependence on gate voltage near pinch-off. This can be approximated with a high-order polynomial argument within the tanh function, but this is difficult to fit and has shown convergence problems. Furthermore, compression both at pinch-off and open channel necessarily share characteristics

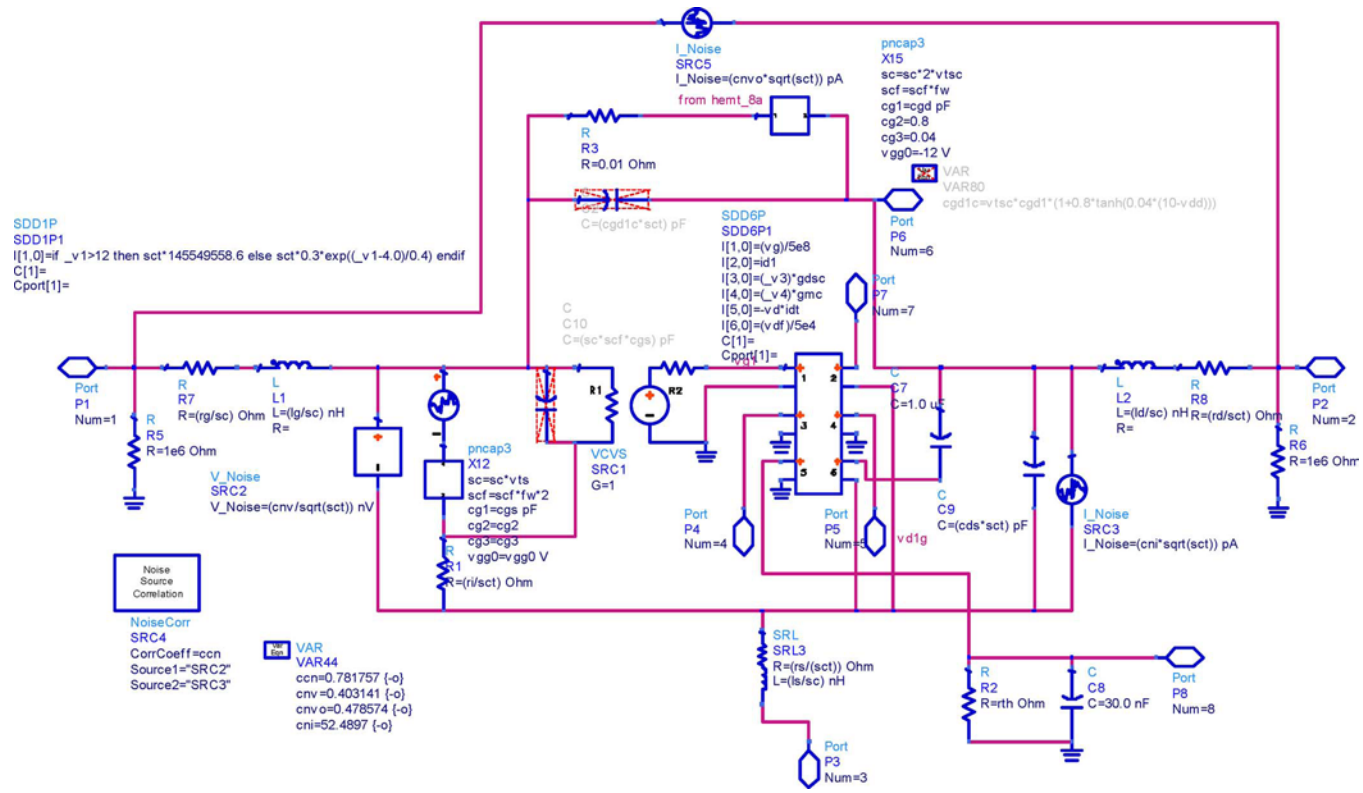

Fig. 3. HEMT SDD model schematic.

in the Angelov formulation. Experience did not show good fits either in linearity or high levels of compression. A reasonable solution for this problem has been proposed by Fager *et al.* [28] and the gate voltage compression expression allows the $G_M(V_G)$ function to be tailored separately from the square-law pinch-off allowing compression in a controlled and continuous manner.

The $I_D(V_G, V_D)$ characteristic also involves trapping and dispersive effects. Many device models are formulated to fit both transconductance and output conductance dispersion, as well as knee collapse, which is common in high-breakdown high-voltage devices. The Cree Inc. model uses the dc knee voltage as controlled by the α parameter to fit the observed RF knee without explicit fitting of the dc knee. This has not proven to be an issue in drain current prediction, nor has transconductance dispersion been shown to be a particular problem with GaN HEMT devices. Observations have shown output conductance dispersion to be an issue for self-consistent fits from small to large-signal operation. The solution for this problem has been found in the work of Jeon *et al.* [29]. Adding a small-signal perturbation to the $I_D(V_G, V_D)$ function separates the small-signal output conductance from the drain current slope providing a good fit over the range of input power.

The HEMT model schematic is shown in Fig. 3. This shows the drain current implemented in Agilent's Advanced Design System as a symbolically defined device (SDD). The overall structure is based on the standard 13-element small-signal FET model. Although there have been many corrections and additions to this model since development of the GaAs MESFET, the standard 13-element model is straightforward to fit and lends itself well to simple voltage-dependent capacitance models. Inspection of the schematic shows that both $C_{\rm GS}$ and $C_{\rm GD}$ are functions of the terminal voltages and implemented as gate charge formulations. There is also a gate forward conduction diode based on the standard exponential characteristic. Proper modeling of forward conduction is essential to the prediction of over-compressed operation, particularly in the case of broadband amplifiers. Improvement of convergence dictates that the exponential function must be limited. In this case, some arbitrarily large hard limit can be chosen with detriment to convergence properties. The $C_{\rm GS}$ and $C_{\rm GD}$ voltage functions use the tanh function similar to Fager *et al.* [28]. Extensive modeling and load–pull fits show that $C_{\rm DS}$ does not need to dynamically vary with drain voltage, but should scale as drain voltage is changed for the wide-bandgap HEMT device.

The model as shown in Fig. 3 also includes noise calculation, is dependent on a dynamic thermal model based on channel dissipated power [30], and can be scaled for various unit cell configurations, as well as for parallel operation. The four noise sources represent the drain current noise and thermal noise from the FET internal resistances. Input and output noise is found to be correlated for the GaN HEMT. The model is partially based on the work of Lazaro *et al.* [31], as well as an empirical study of noise data [32]. The implementation as correlated noise sources simplifies the transition to a Verilog-A [33] translation used to develop models for both Agilent's ADS and AWR's Microwave Office simulators. The thermal model is based on a single-pole configuration, which provides for scaling as a function of dc dissipated power. Additional detailed thermal modeling can be performed using finite-element simulators and an

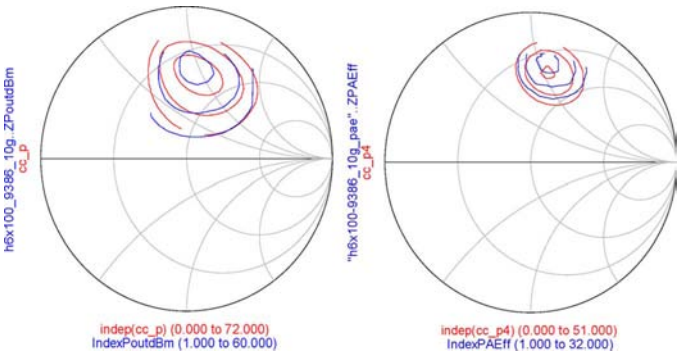

Fig. 4. Measured versus modeled load–pull contours (output power: left; PAE: right).

equivalent thermal resistance is defined for the electro-thermal model. Thermal resistance calculations can also be calculated analytically as demonstrated by Darwish *et al.* [34]. Thermal calculations are essential for GaN HEMT amplifier design due to the high dissipated power associated with high drain bias.

The model parameters are extracted from measured S-parameters over a range of bias values, as well as measured load–pull data. The thermal degradation has been characterized using pulsed on-wafer measurements and equates to 0.01 dBm per °C in output power. As previously discussed, the model is self-consistent over power and fits measurements over a large dynamic range. All model development was based on a two-fingered 720-μm device and has been scaled successfully to a total gate periphery of 48 mm. The model fits S-parameters up to 20 GHz and a typical load–pull fit at 10 GHz is shown in Fig. 4.

The power contours are in 0.5-dB steps from 33.5 to 34.5 dBm and power-added efficiency (PAE) contours are in 10% steps from 30% to 50%. Extracting model parameters over the full range of S-parameters up to 20 GHz and at least two load–pull frequencies, typically 3.5 and 10 GHz, provide accurate results for both narrowband and broadband designs up to 20 GHz with narrowband power levels in excess of 100 W. Packaged model parameters have also been developed to support discrete transistors using the same intrinsic model used for MMIC PA design.

IV. Brief Description of Amplifier Classes

GaN HEMT technology has not only opened up a resurgence in the investigation of various PA classes such as D, E, and F, but has also led to investigations into new modes of operation such as Class J [35], [36]. In general, there has been a lot of attention given to "waveform engineering" in the last few years [37], [38]—this has undoubtedly been due to the fact that GaN HEMT devices allow voltage and current swings on the drains of the devices that can far exceed other RF power semiconductor technologies. Table III gives a basic summary of the theoretical maximum efficiencies that can be provided by various amplifier classes. In practice, the maximum efficiencies will be lower because of a number of reasons [39]: conductance losses, V_{KNEE} losses, passive component losses, and discharge losses.

TABLE III
Theoretical Maximum Efficiencies of Various Class PAs

Class	A	B	C	D	E	F	J
Efficiency, %	50	78.5	100	100	100	100	78.5

V. Broadband Amplifier Examples

Since GaN HEMTs have high-power densities and low input and output capacitances per watt of RF output power, compared to most other microwave semiconductors, they have become useful devices to achieve high powers over broad bandwidths. A variety of circuit approaches have been demonstrated over a range of power levels, frequencies and terminating impedances—these include distributed (traveling wave), lossy match, and gate-to-drain feedback. Three of the most popular applications have been in software-defined radios, broadband jammers, and instrumentation amplifiers. In the latter case, relatively large power levels are required for such applications as automotive electromagnetic compatibility (EMC) testing—multiple baluns for power combining are often used to achieve wide bandwidths at high power levels.

Cree Inc. has been developing GaN products for the past six years. All of these devices are based on a 0.4-μm gate-length process and range in complexity from discrete unmatched transistors for wideband applications to multichip hybrid assemblies and packaged MMICs. An example of a discrete GaN HEMT for a very broadband amplifier application is the CGH40006S. This device is an unmatched transistor suitable for use in broadband applications, either as an output stage in military communication handheld radios or as a driver in counter IED jamming amplifiers. The challenge at this power level was to design an amplifier that would cover from 2 through 6 GHz. The transistor is housed in a plastic surface mount quad-flat no-leads (QFN) package. This package approach presents two key challenges: thermal management and electrical design to 6 GHz. The thermal design challenge was solved by placing the QFN packaged part on top of an array of filled vias. The vias were filled with conductive epoxy. The thermal conductivity of such epoxy-filled vias, although not as high as copper-plated vias, is sufficient. Simulations of the thermal stack were made using finite-element analysis (FEA) software (Fig. 5). Initial thermal simulations were performed at 4 W/mm (of gate periphery) of power dissipation to ensure that the channel temperature remained under 225 °C when operating at a case temperature of 85 °C.

Consideration was also given to the surface temperature of the die as the plastic of the QFN package is in direct contact with the transistor. From simulation it was determined that the surface of the die would be 30 °C lower than the peak channel temperature. The target power dissipation was then used as a design goal in the electrical simulations. Using the thermal engine of the large-signal model, it was possible to optimize the circuit's electrical performance for best thermal performance. The electrical design challenge of the amplifier was caused by the source inductance of the via array and its impact on the performance of the final circuit. It was determined, during the design process that the launch of the RF signal from the printed circuit board to the package was critical. The use of a ground–signal–ground

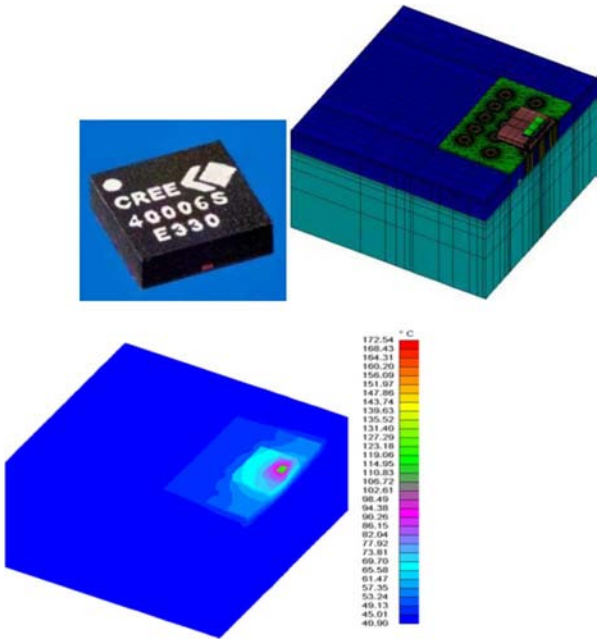

Fig. 5. Use of FEA tools to design a via array for best thermal management (top left: QFN package; top right: half of QFN package on via array; bottom left: temperature profile of QFN packaged transistor).

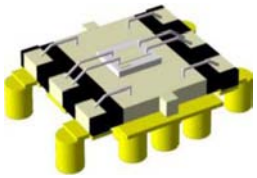

Fig. 6. Layout view of CGH40006S with associated via array and GSG feed structure.

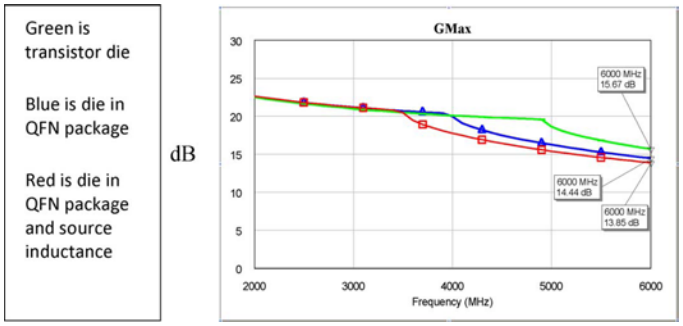

Fig. 7. Effects of source inductance and GSG feed on G_{MAX}.

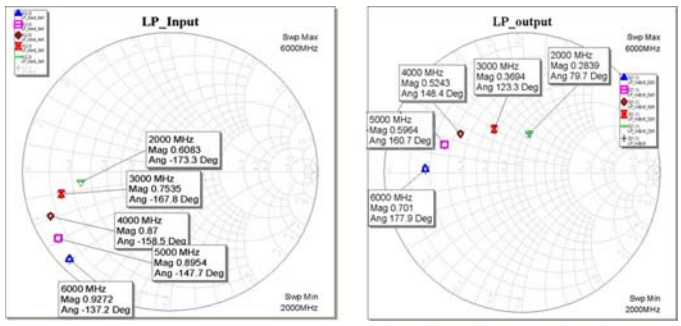

Fig. 8. Simulated optimum source and load impedances for CGH40006S.

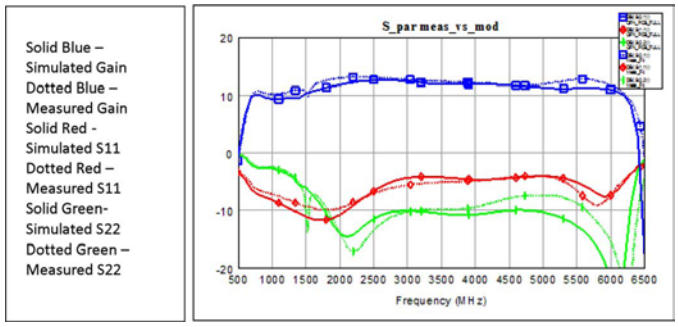

Fig. 9. Measured versus simulated small-signal performance of the CGH40006S in a broadband reference design.

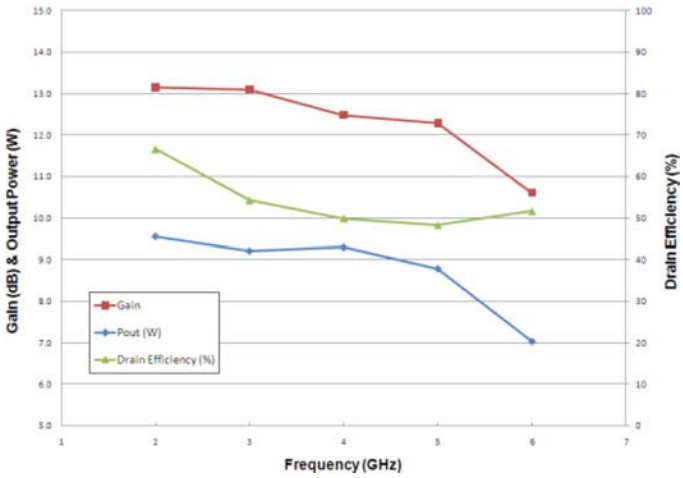

Fig. 10. Large-signal performance of the CGH40006S in a broadband reference design.

(GSG) launch reduced the effect of source inductance on the maximum available gain of the device above 4 GHz.

The breakpoint in G_{MAX} is extended from 3.5 to 5 GHz, resulting in an increase in gain of 2 dB at 6 GHz (Figs. 6 and 7). The via array was modeled using a layout-driven simulation approach in Microwave Office. The circuit design approach was to synthesize matching circuits to match simulated source and load–pull impedances derived from the large-signal model. Fig. 8 indicates that matching to the input of this device was more complex than matching to the output. This is often the case with broadband circuit designs using GaN HEMTs.

Excellent correlation was shown between measured and simulated circuit performances (Fig. 9) demonstrating the accuracy of the large-signal model. Furthermore, with careful layout driven techniques, a more complex and time-consuming 3-D analysis of the via array was not necessary.

Fig. 10 shows the measured large-signal performance of the complete amplifier (Fig. 11) over 2–6 GHz. Power gain is maintained at greater than 11 dB with 7-W minimum output power and drain efficiencies of greater than 50%.

Lin *et al.* [40] have used both the distributed and feedback approaches to design a range of commercial amplifiers covering saturated power levels up to 40 dBm over frequency ranges covering from 30 to 4000 MHz. Fig. 12 shows a comparison be-

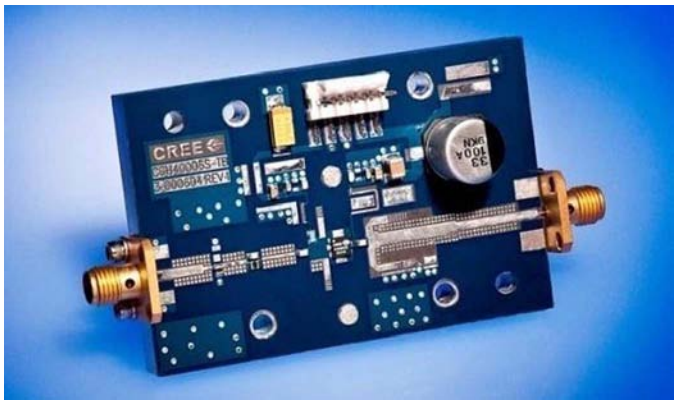

Fig. 11. Photograph of CGH40006S in a 2–6-GHz broadband reference design.

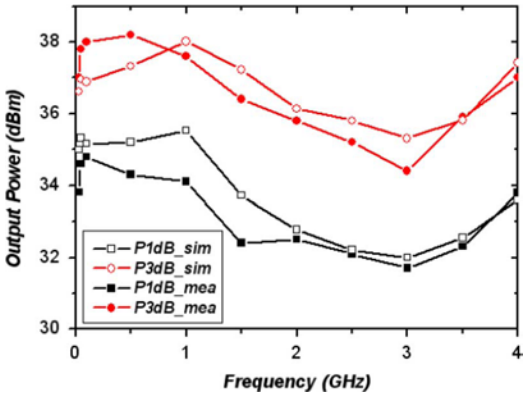

Fig. 12. Measured and simulated output power for broadband feedback amplifier [40].

tween measured and large-signal modeled results for one of the feedback amplifiers.

Carrubba *et al.* [41] recently demonstrated a novel, highly efficient, and broadband RF PA operating in "continuous class-F" mode. The introduction and experimental verification of this new PA mode demonstrated that it is possible to maintain expected output performance, both in terms of efficiency and power, over a very wide bandwidth. Using recently established continuous Class-F theory, an output matching network was designed to terminate the first three harmonic impedances. This resulted in a PA delivering an average drain efficiency of 74% and average output power of 10.5 W for an octave bandwidth between 0.55–1.1 GHz. Fig. 13 shows the practical implementation of the PA, while Fig. 14 shows the comparison between measurements and simulations.

VI. High Efficiency PA Examples

Much recent work has been achieved in the area of high-efficiency PA design using GaN HEMTs for a variety of classes of operation. This paper provides a number of circuit examples, but is, by no means, an exhaustive source of recent multiple designs.

Class D: Lin and Fathy [42] have demonstrated a Class-D amplifier using Cree CGH40010F transistors. A 50–550-MHz wideband GaN HEMT PA with over 20-W output power and

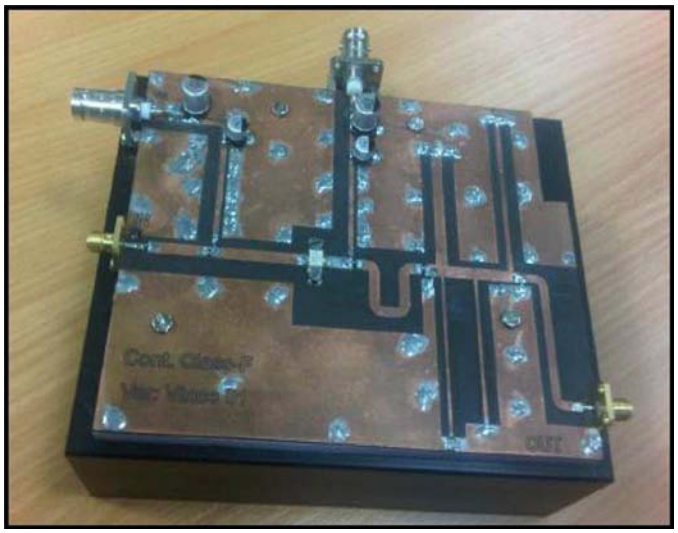

Fig. 13. Continuous Class-F mode PA [41].

63% drain efficiency was successfully developed. The wideband PA utilized two GaN HEMTs and operated in a push–pull voltage mode—Class D. The design was based on a large-signal simulation to optimize the PA's output power and efficiency. To assure wideband operation, a coaxial line impedance transformer was used as part of the input matching network; a wideband 1:1 ferrite loaded balun and low-pass filters were utilized on the amplifier's output instead of the conventional serial harmonic termination. Peak voltage swing on the drains of the transistors is 55 V (well within the breakdown voltage of the process). The practical implementation of the amplifier is shown in Fig. 15 and measured results are shown in Fig. 16.

Class E: Shi *et al.* [43] have developed a very compact highly efficient 65-W wideband GaN Class-E PA. Optimum Class-E loading conditions were achieved over a broad frequency range using a wideband design and implementation approach using bond-wire inductors and MOS/MIM capacitors. The amplifier output network schematic is shown in Fig. 17. A photograph of the implementation is presented in Fig. 18, showing the employment of Cree 14.4-mm GaN die. The PA operates from 1.7 to 2.3 GHz with a power gain of 12.3 $\pm$ 0.9 dB, while providing an output power of 42–65 W with a PAE ranging from 63% to 72%. The total area of the amplifier including bias networks is only 20 mm $\times$ 20 mm.

Class-E Doherty: Combining the advantages of Class-E and Doherty PA (DPA) operations has resulted in some of the highest PAEs at backed-off power levels reported to date. For example, Choi *et al.* [44] have described work on a two-way Doherty amplifier employing Class-E single-ended circuits for both the carrier and peaking amplifiers. The individual amplifiers, utilizing Cree CGH40010F transistors, were optimally matched at fundamental, second, and third harmonics using transmission lines on Taconic substrates (with dielectric constant of 2.6) to provide PAEs from 58% to 76% with output powers from 39.6 to 41.2 dBm and gains from 8.3 to 14.3 dB across 2.7–3.1 GHz. The switching Doherty amplifier consists of a carrier amplifier, peaking amplifier, broadband Wilkinson divider, offset lines, and output combiner. Fig. 19 shows the

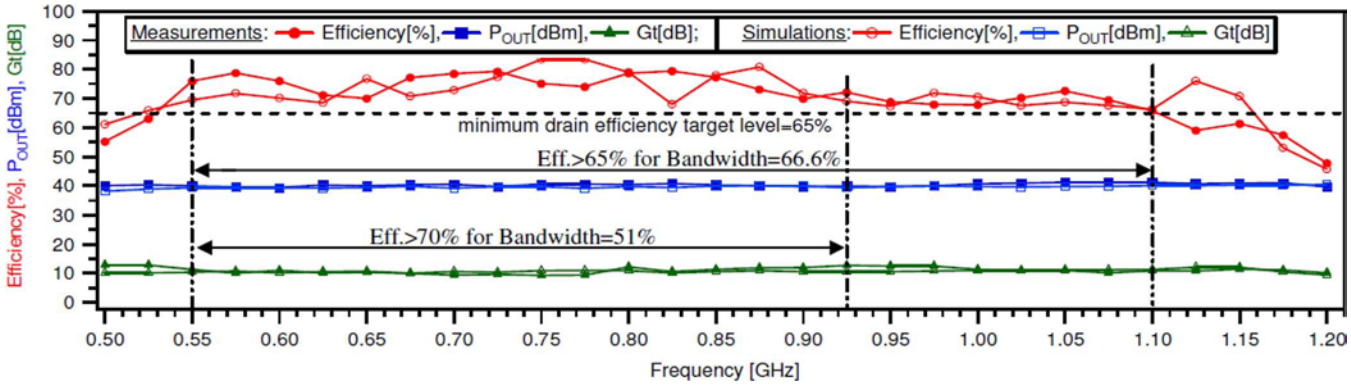

Fig. 14. Measured and simulated performance of continuous Class-F PA [41].

fabricated PA where the input divider uses multiple sections to minimize the effect of Class-E load conditions. Linearity of the amplifier was not a major concern since the application was for multifunction radar. PAE and drain efficiency at 6-dB back-off were 63% and 73%, respectively (Fig. 20).

Class-E Chireix Outphasing: A Chireix outphasing PA is a promising candidate to work around classical linearity-efficiency tradeoffs and is based on linear amplification using nonlinear components (LINC). In an out-phasing transmitter, a complex modulated input signal is split into two signals with constant amplitude and a relative phase difference, corresponding to the time-varying envelope of the original input signal. The two branch signals are amplified by switch-mode power amplifiers (SMPAs). After combining both branch signals at the outputs of these SMPAs, an amplified replica of the original input signal results. Unfortunately, due to the nonisolating properties of the combiner, a time-varying reactive load modulation exists at the output of both SMPAs. To mitigate this unwanted load modulation, Chireix compensation elements are placed at the input ports of the power combiner. This creates an efficiency peak at a specified power back-off level, resulting in an improved average PA efficiency. The Chireix outphasing combiner is usually based on quarter-wave transmission lines and can be found in many publications on outphasing PAs. The Chireix compensation elements are either lumped or can be incorporated in the combiner. There are, however, some drawbacks to the classical Chireix combiner. The efficiency not only depends on the outphasing angle, but also on frequency since both the Chireix compensation elements and the quarter-wave lines are frequency dependent. Class-B, Class-D, and Class-F implementations have traditionally been used in the branch PAs, but recently Class-E has been identified as an even better candidate, demonstrating higher efficiency over a wider dynamic range [45].

Transformers can convert a single-ended load into a floating load. However, a lumped-element transformer is difficult to implement for high powers at RF frequencies. Coupled lines can be used to combine the outputs as in a Marchand balun. Van der Heijden *et al.* [46] have fabricated an outphasing SMPA with a Class-E Chireix coupled-line combiner. Fig. 21 shows the schematic of the amplifier. The Class-E PA switches were realized with commercially available Cree GaN HEMT transistor die. Since the GaN stages need to be driven with pulse-wave

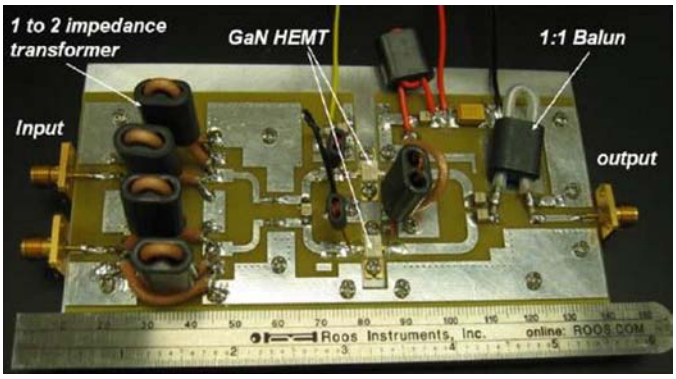

Fig. 15. Practical implementation of Class-D UHF PA [42].

signals (to obtain the highest efficiency), a high-voltage CMOS driver topology was used in a 65-nm process. Fig. 22 shows a close-up of the CMOS-GaN SMPA lineup. Fig. 23 shows drain efficiency, total lineup efficiency, and power gain as a function of output power. At 10-dB back-off, the drain efficiency is 65% and the total lineup efficiency is 44%. At 8-dB back-off, the drain efficiency is 70% and the total lineup efficiency is 53%. The drain efficiency at 10-dB back-off is comparable to what has been published for a three-way GaN DPA, but with wider bandwidth capability.

Class-F: A wide range of both Class-F and inverse Class-F PAs have been described in the literature. Typical of these is the PA design produced by Schelmzer and Long [47]. In a Class-F amplifier, the output matching network must absorb the $C_{\rm DS}$ of the HEMT and the interconnect inductance while providing the correct fundamental and harmonic resistances at the intrinsic drain of the transistor. It is beneficial if the matching network can be tuned to different values of R_L so the amplifier can be designed for different supply voltages, especially for GaN transistors, which can be matched to a range of impedances due to their high breakdown voltage.

Fig. 24 illustrates a matching network that can accomplish this. Two separate bond-wires are used at the drain pad. This allows the bond-wire inductance to be incorporated into the quarter-wavelength drain bias transmission line giving the lowest even harmonic impedances at the drain. $Z2, \theta 2$, and $Z3$ can be tuned to absorb $C_{\rm DS}$ and $L_{\rm BW}$ and simultaneously present a real impedance at the fundamental, R_L, and a very

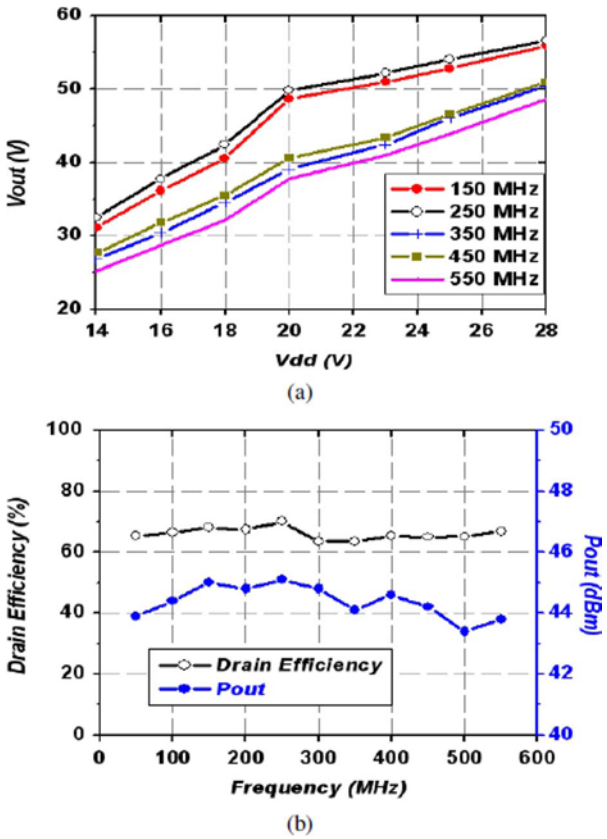

Fig. 16. Measured performance of Class-D PA [42].

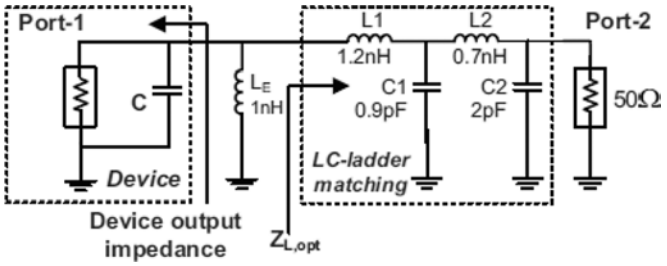

Fig. 17. Class-E output matching network for compact PA [43].

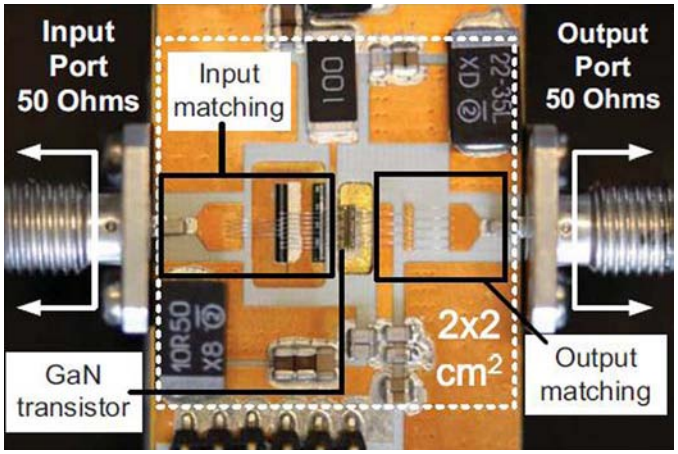

Fig. 18. Practical implementation of compact Class-E PA [43].

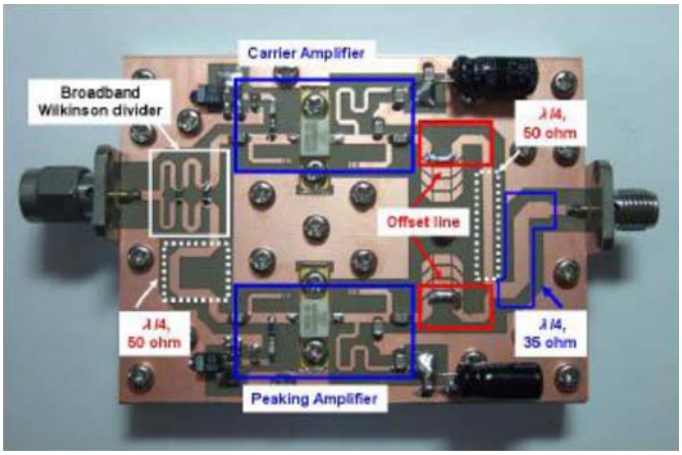

Fig. 19. Practical implementation of Class-E DPA [44].

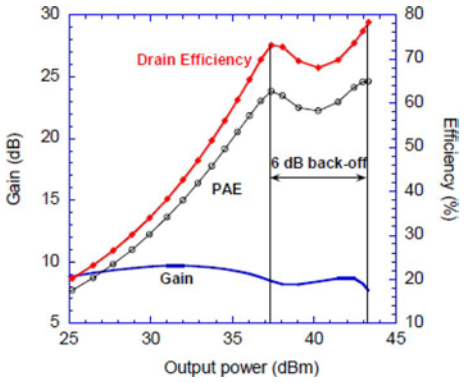

Fig. 20. Gain and efficiency of Class-E DPA [44].

high real impedance at the third harmonic. Effectively, both matching networks terminate the second, third, and fourth harmonics and some of the higher order even harmonics as well.

The output matching network topology is a particularly good fit for the GaN transistor used (Cree CGH60015D, 3.6-mm gatewidth transistor) having a $C_{\rm DS}$ of about 0.9 pF. The output matching network was capable of tuning R_L from 25 to 120 Ω while maintaining a high third harmonic impedance and realizable transmission-line impedance.

The amplifier was constructed on a low-loss printed-circuit-board substrate with gold-plated traces mounted to a copper carrier. The GaN HEMT was directly mounted to the copper carrier and used wire-bond interconnects. Fig. 25 shows a photograph of the amplifier. The amplifier was tested at 2 GHz where only the fundamental frequency component was measured for the results. The amplifier had a peak PAE of 85.5% with an output power of 16.5 W with a drain bias voltage of 42.5 V. The peak gain was 15.8 dB, and it had a compressed gain at peak PAE of 13.0 dB. The peak drain efficiency was 91%.

Class-J: Moon *et al.* [36] have presented the theory of operation of Class-J PAs with linear and nonlinear output capacitors ($C_{\rm OUT}$). The efficiency of a Class-J amplifier is enhanced by the nonlinear capacitance because of harmonic generation from the nonlinear $C_{\rm OUT}$, especially the second-harmonic voltage component. This harmonic voltage allows the reduction of the phase difference between the fundamental voltage and current components from 45° to less than 45° while maintaining a

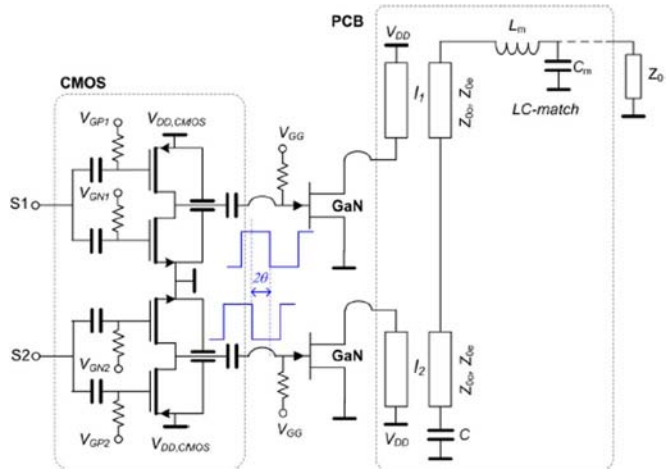

Fig. 21. Schematic of Class-E Chireix coupled line outphasing PA [46].

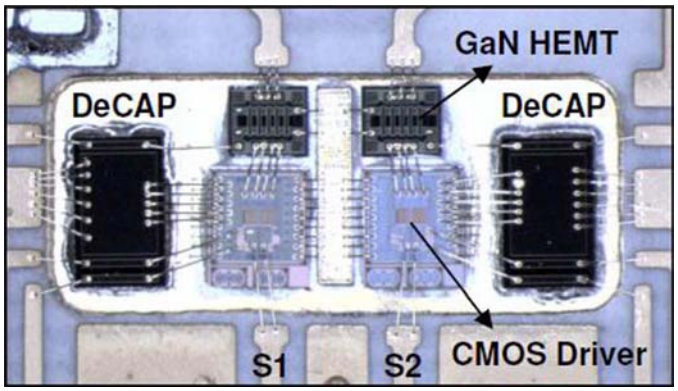

Fig. 22. Close-up photograph of CMOS driven Class-E GaN HEMTs [46].

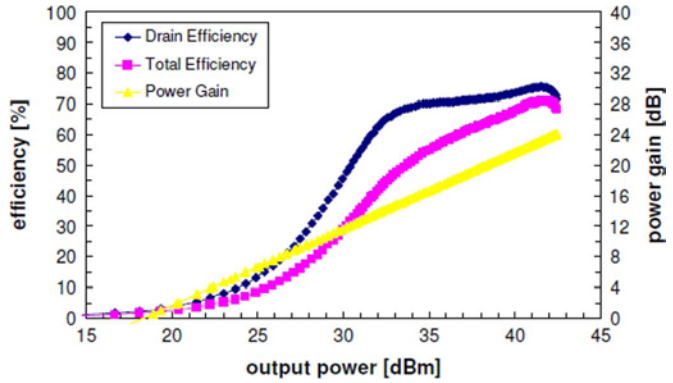

Fig. 23. Power gain, drain, and total lineup efficiencies of Class-E Chireix outphasing PA [46].

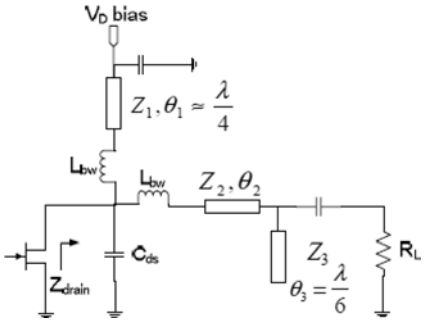

Fig. 24. Output matching network for Class-F PA [47].

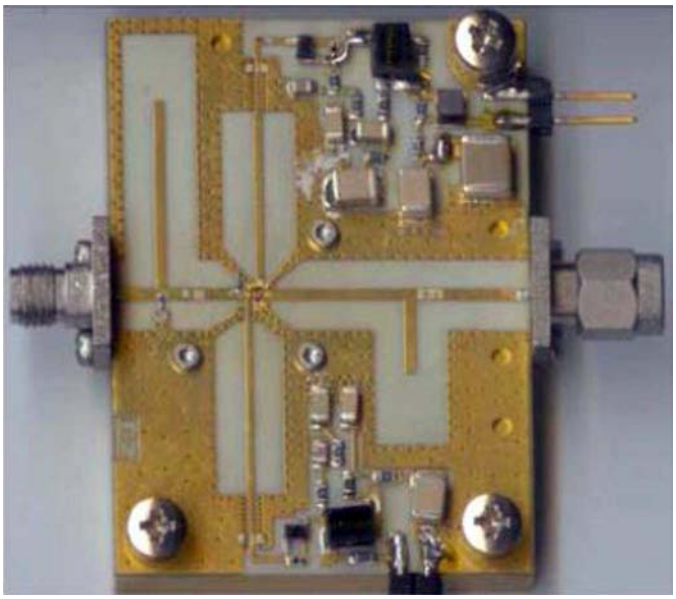

Fig. 25. Practical implementation of bare die GaN HEMT Class-F PA [47].

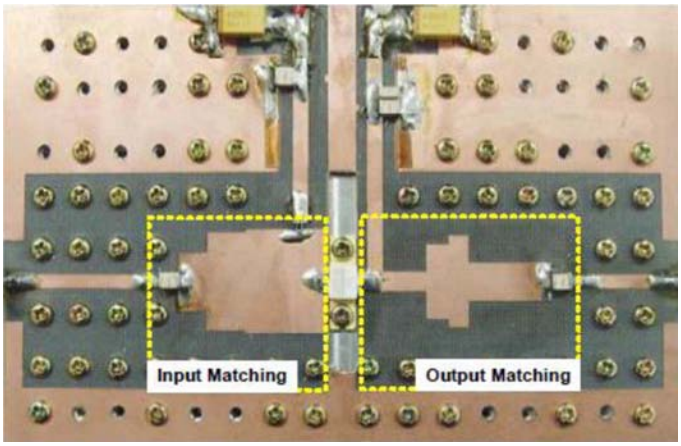

Fig. 26. Practical implementation of Class-J PA [36].

half-sinusoidal shape. Therefore, a Class-J amplifier with the nonlinear C_{OUT} can deliver larger output power and higher efficiency compared with a linear C_{OUT}. The Class-J amplifier can be further optimized by employing a so-called saturated PA, a recently reported amplifier type presented by the same authors. The phase difference of that proposed PA is zero. Like the Class-J amplifier, the PA uses a nonlinear C_{OUT} to shape the voltage waveform with a purely resistive fundamental load impedance at the current source, which enhances the output power and efficiency. A highly efficient amplifier based on the saturated PA was designed using a Cree CGH40010F GaN HEMT at 2.14 GHz (Fig. 26). It provided a PAE of 77.3% at a saturated power of 40.6 dBm (11.5 W).

DPAs: There has been a very large body of work completed on high-efficiency DPAs over the last few years. This paper will only describe a few examples, but there are various approaches

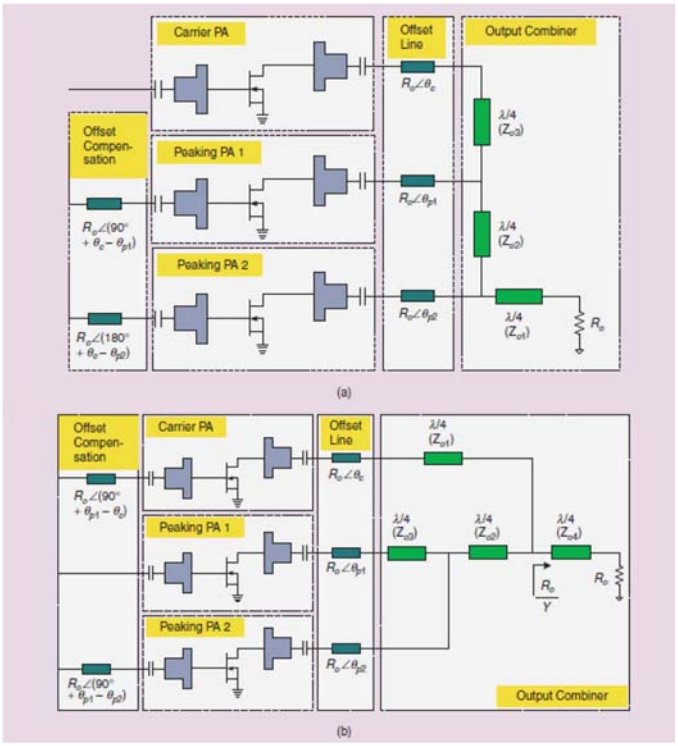

Fig. 27. Two different types of three-stage DPAs [48].

TABLE IV
VARIOUS TYPES OF DPA CONFIGURATIONS

802.16 WiMAX with 8.5 dB PAPR		
N-Way	**Back-off, dB**	**Average Drain Efficiency, %**
2 way	-6	59
3 way	-9.54	61.2
Three-Stage Type 1		
1:2:2	-4.44/-9.54	69.8
1:2:3	-6/-9.54	69.4
1:3:3	-4.87/-12	70.5
1:3:4	-6/-12	71
Three-Stage Type 2		
1:1:1	-6/-9.54	69.4
1:2:2	-6/-13.98	70.1
2:3:3	-6/-12	71

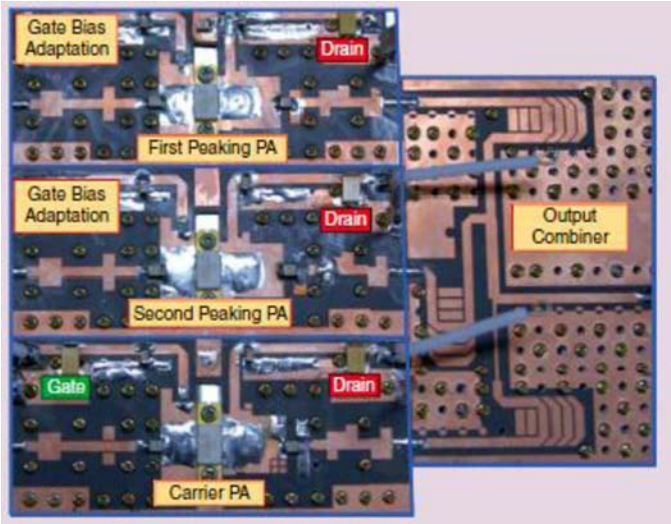

Fig. 28. Practical implementation of three-stage DPA [48].

covering "conventional" two-way, N-way, and N-stage, asymmetrical (both unequal power division and unequal transistor peripheries), as well as different classes of operation for carrier and peaking amplifiers.

Kim *et al.* have provided an extensive overview of DPA design specifically employing GaN HEMTs [48]. Of particular interest is the description of various three-way approaches shown schematically in Fig. 27. There are two kinds of three-stage DPA architectures, as shown in Fig. 27(a) and (b). Fig. 27(a) is a widely known structure. The topology is a parallel combination of one DPA used as a carrier PA with an additional peaking PA. The first peaking PA modulates the load of the carrier PA initially and the second peaking PA modulates the load of the previous Doherty stage at a higher power. The topology in Fig. 27(b) is a parallel combination of one carrier PA and one DPA used as a peaking PA. Both the three-stage and the three-way architectures use three PA units, but the two peaking PAs are turned on sequentially in the three-stage DPA instead of simultaneously like a multistage amplifier. Thus, three peak efficiency points are formed: at the two turn-on points and at the peak power. In the three-way structure, the peaking PAs are turned on simultaneously, similar to N-way power combining. To achieve proper load modulation, the three-way DPA requires two quarter-wavelength transmission lines, but the three-stage DPAs require three and four quarter-wavelength transmission lines, respectively. A comparison of the achievable efficiencies of various types of DPAs is shown in Table IV.

To implement the three-stage DPA, a Class-AB mode PA was designed at 2.655 GHz using Cree's CGH40045F GaN HEMT devices. A simple method to overcome the problem of incomplete load modulation due to unequal currents in the carrier and peaking amplifiers was to control the gate bias of the peaking PAs. Gate bias control of the DPA is also often employed for accurate intermodulation cancellation. Gate bias control of the peaking PA was also used for performance optimization, that is, to simultaneously achieve high efficiency at the backed-off input power, as well as at high peak powers. In this example, the quiescent bias current of the carrier PA was 55 mA, and the PA delivered 64.6% drain efficiency at an output power of 46.4 dBm. The implemented PA with 1:1:1 ratio is shown in Fig. 28. The measured efficiency is illustrated in Fig. 29(a). This amplifier was employed for amplification of an 802.16e Mobile WiMAX signal with 7.8-dB peak-to-average power ratio (PAPR). Fig. 29(b) shows the measured efficiency of the envelope-tracking three-stage DPA with and without gate bias adaptation.

Grebennikov [49] described a novel high-efficiency four-stage DPA architecture convenient for practical implementation in base-station applications for modern communication standards. Each PA was based on a 25-W Cree GaN HEMT device with the transmission-line load network corresponding to an inverse Class-F mode approximation. In a CW operation

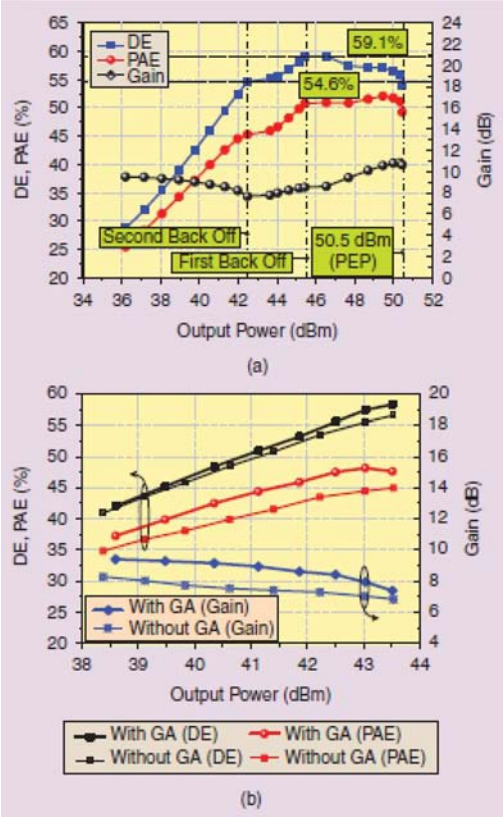

Fig. 29. (a) Gain and efficiency of DPA versus output power. (b) Gain, output power, and efficiencies of DPA with and without gate bias adaptation [48].

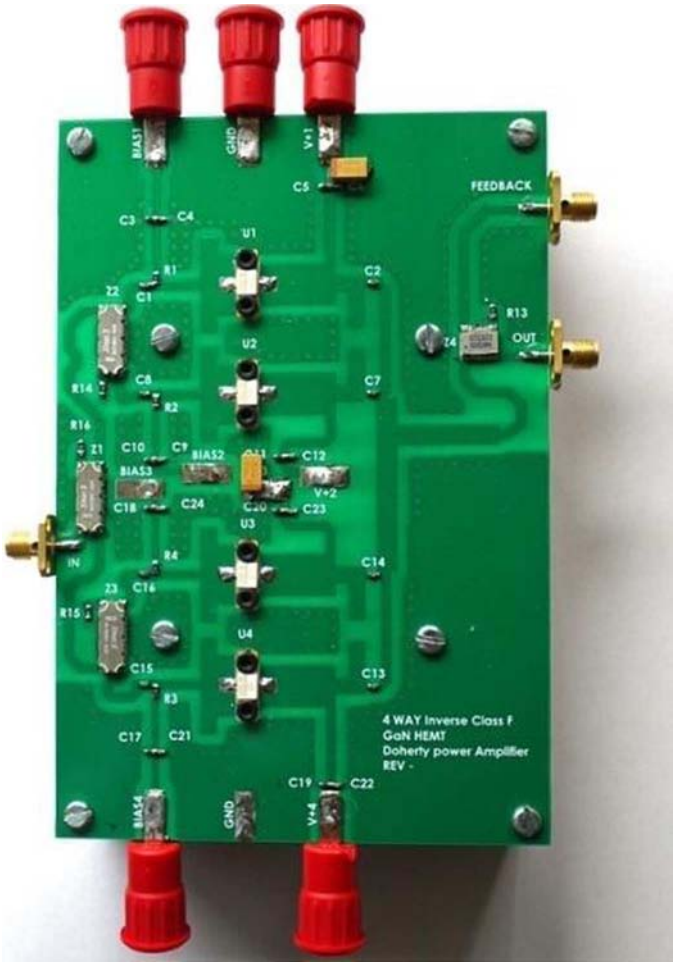

Fig. 30. Four-way DPA implementation [49].

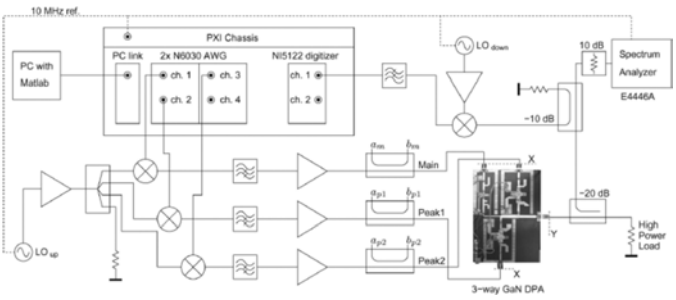

Fig. 31. Schematic diagram of three-way mixed-signal DPA [50].

mode with the same bias voltage for each transistor, an output power of 50 dBm with a drain efficiency of 77% was achieved at a supply voltage of 34 V. In a single-carrier W-CDMA operation mode with a PAPR of 6.5 dB, a high drain efficiency of 61% was achieved at an average output power of 43 dBm, with ACLR1 measured at a −31-dBc level. The Doherty configuration is shown in Fig. 30 and affords high efficiency to be maintained over a wide region of back-off conditions.

In theory, three-way DPA implementations can offer even better efficiencies in power back-off operation, which is highly desirable when dealing with single or multiple (unclipped) W-CDMA channels or modern fourth-generation (4G) signals with high crest factors. Unfortunately, practical three-way DPA implementations rarely meet their expectations due their complicated implementation. To overcome these implementation issues and enable reproducible, as well as very efficient N-way Doherty amplifiers, the use of mixed-signal techniques was recently proposed to establish digital input control of the individual amplifier cells [50]. This approach facilitates the independent optimization of the amplifier-cell drive conditions for maximum efficiency. Neo *et al.* [51] had previously employed Si LDMOS transistors in the PAs, but have extended this concept to demonstrate the capabilities with GaN HEMT transistors. The system setup for the three-way DPA is shown in Fig. 31.

The system is calibrated to maximize the backed-off power efficiency by adjusting the relative input phases of the three signals, as well as optimizing performance as a function of the relative sizes of the transistors used in the carrier and peaking amplifiers. Fig. 32 also shows the normalized measured PAE of a 45-W Class-B GaN amplifier, which utilized an identical device as applied in the peak 1 amplifier. It is interesting to see that at maximum output powers, both the DPA, as well as the Class-B amplifier using the same device technology reach a maximum PAE of almost 70%, confirming the close to ideal operation of the DPA design at full power. Note that the PAE of the Class-B GaN amplifier decreases proportionally to the square of the back-off power, whereas the GaN three-way DPA demonstrates very high efficiency throughout the entire back-off range of 12 dB. At the 12-dB back-off point, the GaN three-way DPA provides three times higher PAE than the Class-B amplifier

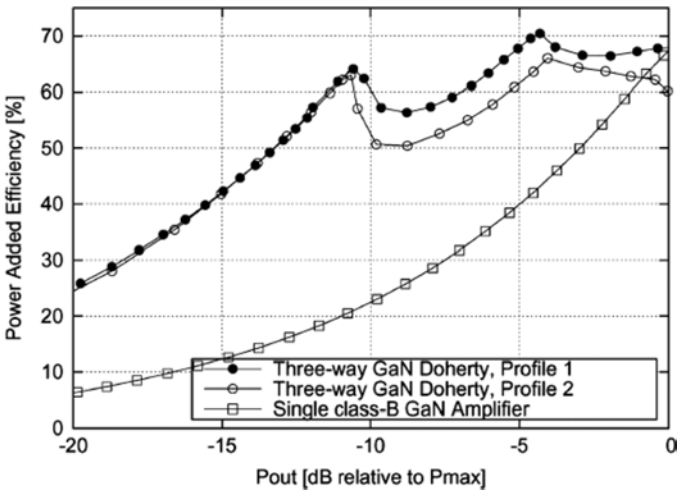

Fig. 32. Measured PAE of three-way DPA versus output power under two different mixed-signal conditions when compared to a single-ended Class-B amplifier [50].

for CW signals, indicating the very high efficiency potential of the three-way DPA for complex modulated signals with a high PAPR. The CW performance of the three-way GaN DPA was characterized and optimized using software control, yielding a measured performance of: 68% PAE at 50 dBm (full power), 70.4% at 45 dBm (first back-off point), and 64% at 38 dBm (second back-off point), while the measured transducer power gain was greater than 10 dB at all times. To demonstrate that this exceptional high-efficiency performance could be effectively utilized for practical base-station operation, the GaN three-way DPA was driven by a W-CDMA signal with a crest factor of 11.5 dB. Using a dedicated memory-effect compensating predistortion algorithm, the resulting measured PAE for this signal was 53% at an average power of 38.5 dBm, while meeting all linearity specifications. This was the highest PAE performance ever reported for any PA operating with a W-CDMA signal without using crest factor reduction techniques (at the time of the publication in 2008).

Envelope Tracking (ET) PAs: The high-voltage operation of GaN HEMTs is particularly attractive for ET techniques that are used to maintain high efficiencies over a wide range of operating drain voltages under saturated power conditions. Over the last few years there have been a variety of reported results on ET-based amplifiers using a variety of RF semiconductor technologies such as Si LDMOSFET, GaAs HVHBT, and GaN HEMT [52], [53], [54].

Yamaki *et al.* [5] have described an optimized GaN device consisting of a single-die HEMT with 43 mm of gate periphery together with internal matching circuits in a package. The package size is 13.2 mm × 21.0 mm. In order to realize high efficiencies, the authors implemented an inverse Class-F PA with harmonic terminations with output-matching networks inside the package. A single GaN HEMT die has advantages in terms of simplicity and cost effectiveness. The authors processed two types of GaN HEMT (A and B). The gate periphery and length were 43 mm and 0.6 μm for 200-W output power, respectively. The gate electrode consisted of Ni/Au, and SiN

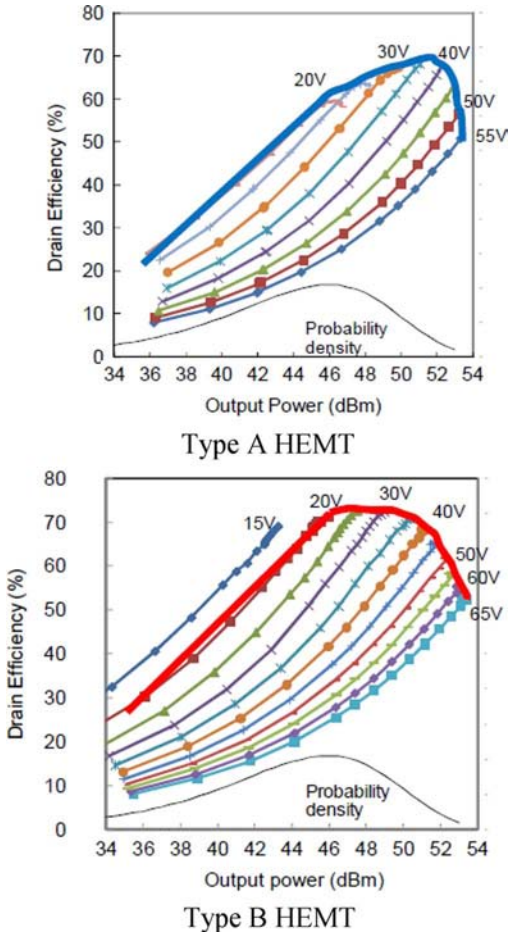

Fig. 33. Drain efficiency versus output power for GaN HEMTs A and B [5].

passivation was deposited on the GaN cap layer using plasma CVD. The structure of GaN HEMT (A) was "conventional," which had already been manufactured as the commercially available EGN21C210I2D. The electrode structure and AlGaN electron supply layer of GaN HEMT (B) was changed to improve breakdown voltage to greater than 300 V allowing safe drain voltage operation under ET up to 65 V.

Fig. 33 shows the drain efficiency measured at various drain voltages as a function of output power at 2.14 GHz together with a probability density function (PDF) of the W-CDMA signal. The bold line on the efficiency curves represents the operating point of the ET system. As shown in Fig. 33(a), the drain efficiency of the GaN HEMT (A) device was more than 65% over a 30 V ($P_{\rm out} = 49.2$ dBm) to 40 V (52.7 dBm) drain bias range with a maximum drain efficiency of 68%. When a W-CDMA signal with 7-dB PAPR is used in this case, the drain efficiency of the GaN HEMT (A) device decreased significantly below the average power. As shown in Fig. 33(b), the drain efficiency of the GaN HEMT (B) device was more than 65% over a 15-V ($P_{\rm out} = 42.5$ dBm) to 45-V (51.5 dBm) drain bias range with maximum drain efficiency of 72.5%. This result indicated that the GaN HEMT (B) device provided 65% efficiency over a wide range of powers (9 dB) as a result of the high-voltage operation and the improved $C_{\rm DS}$ characteristics.

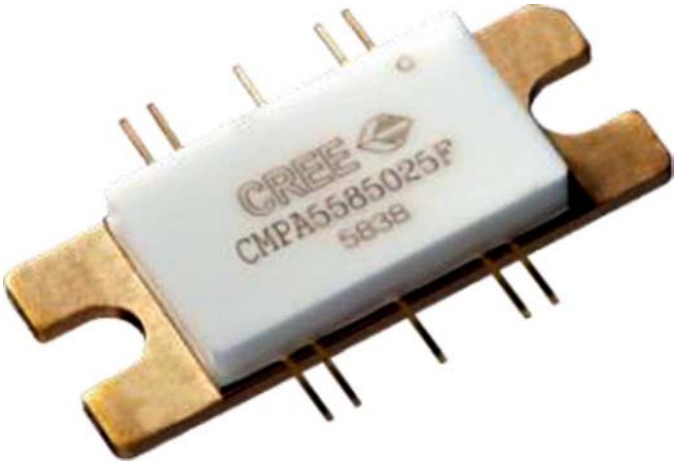

Fig. 34. CMPA5585025F shown in custom developed ten-lead 50-Ω package with dedicated bias leads.

TABLE V
COMMONLY USED MATERIALS FOR THERMAL MANAGEMENT OF GaN HEMT TRANSISTORS AND MMICS

	CuW-10 10%Cu 90%W	CuMoCu 30%Cu 70%Mo	CMC Cu/Mo/Cu 1:1:1	CPC Cu/CuMo/Cu 1:4:1	Alumina
Thermal Conductivity, W/mK	197	190	260	220	35
Coefficient of Thermal Expansion, ppm/K	8	7.65	7.1	7.5 to 8.5	5.4
		Super CMC Cu/Mo multilayers		Aluminum Diamond/Silver Diamond	
Thermal Conductivity, W/mK		370		>500/800	
Coefficient of Thermal Expansion, ppm/K		6 to 10		7.5/<10	

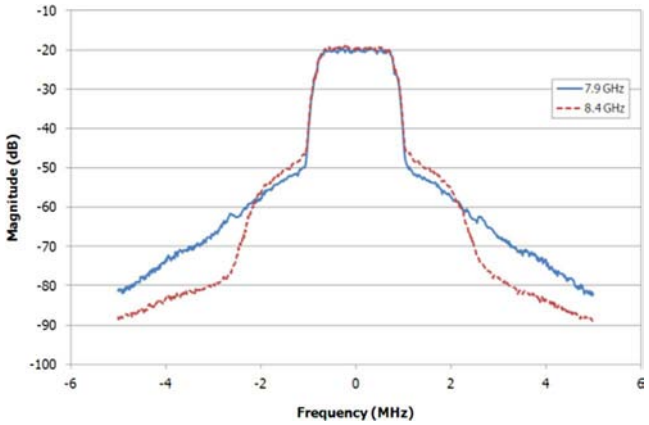

Fig. 35. CMPA5585025F spectral mask under 1.6-Ms/s OQPSK at 15-W average output power.

VII. MONOLITHIC PA EXAMPLES

SiC is an excellent semi-insulating material, which allows it to be used for low-loss transmission lines and lumped elements (see Table I for properties of SiC) in addition to active devices such as HEMTs. Thus, GaN on SiC monolithic integrated circuits have become a popular platform for a range of circuits including wideband PAs. The first example is of a commercially available GaN HEMT MMIC, the CMPA5585025F, from Cree Inc. This MMIC is a packaged two-stage amplifier for satellite communications applications. The MMIC covers both the commercial, 5.8–7.2 GHz, and military, 7.9–8.4 GHz, frequency allocations. The availability of this packaged GaN HEMT MMIC has increased significantly state-of-the-art performance in terms of efficiency, gain, and power. In comparison, an internally matched GaAs FET only covers one band of interest. Target RF output power at 85 °C case temperature, assuming a copper–tungsten composite package flange, was 25 W (CW). The efficiency and power gain targets were 40% PAE and 15–20 dB, respectively, across the frequency bands. A new multilead package was also developed for the MMIC, which can be used for a complete range of MMICs. The availability of commercially available packages for high-power large-area MMICs is somewhat limited. Most high power packages have relatively poor thermal conductivities and only have a single input and output RF lead. To take full advantage of a high-performance MMIC, it is very desirable to have multiple dedicated bias leads on either side of the RF leads to optimally distribute bias voltages to the MMIC (Fig. 34). This is an important design consideration since dc-bias networks often affect the overall stability of the amplifier—especially when working with high-power high-gain MMICs enclosed within small form factors. Each lead is also provides RF impedance of 50 Ω operating to 15 GHz or so. This package also has the advantage of superior thermal conductivity as the flange material is 1:3:1 CPC (see Table V) enabling the packaged MMIC to be used to full case temperature without any de-rating of its linear output power.

The MMIC was characterized for its linear performance under offset quadrature phase shift keyed (OQPSK) modulation. The linearity specification requires spectral purity measurements at a spectral offset of one symbol from the center frequency, i.e., for a 1.6-Ms/s signal rate, the spectral mask is measured at 1.6-MHz offset from the center of the carrier. At this frequency, the spectral emissions are required to be less than −25 dBc. The multiple bias leads of the package allow for large video bandwidths to be supported. This allows compliance with the inevitable increase in data that satellite communications systems will have to handle in the near future.

Fig. 35 shows the spectral mask of the CMPA5585025F at both 7.9 and 8.4 GHz. At these frequencies, the PAE is 25%—over twice that of an internally matched discrete GaAs FET. GaN HEMTs have adequate linearity when biased in Class A/B, whereas GaAs FETs are biased in Class A and are operated typically at 10 dB below their 1-dB compression point. Consequently the PAEs for the latter devices are usually less than 10%. Also, due to their low power densities, GaAs FETs also have large gate peripheries to achieve the required output power, which lead to devices with very high output capacitance with power gains of only 6 dB or so. The GaN MMIC described here typically provides 20-dB gain at its rated linear output power across both C- and X-bands. A summary of performance is shown in Fig. 36.

Distributed MMIC Amplifier Design Example: A dc–6-GHz distributed MMIC amplifier (Cree CMPA0060025F) was designed using the nonlinear model-based design process described earlier [55]. The distributed (traveling wave) amplifier

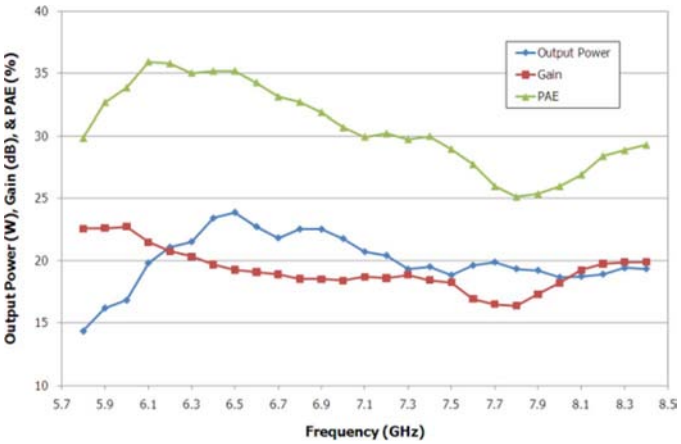

Fig. 36. CMPA5585025F output power, gain, and PAE at rated linear output power under 1.6-Ms/s OQPSK modulation.

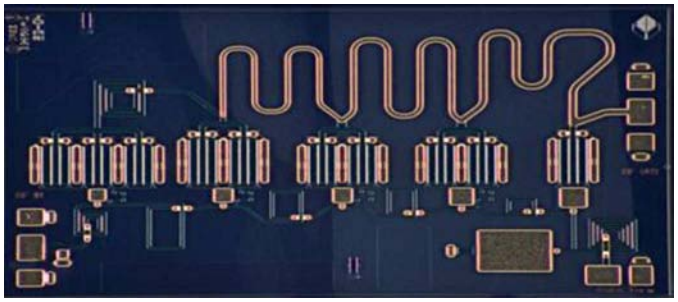

Fig. 37. Cascode NDPA MMIC.

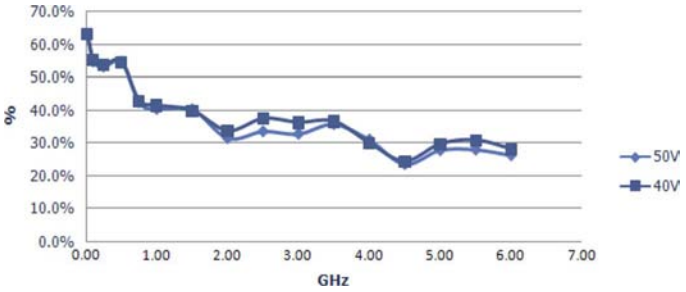

Fig. 38. Drain efficiency versus frequency at $P_{\mathrm{IN}} = 32$ dBm for NDPA MMIC.

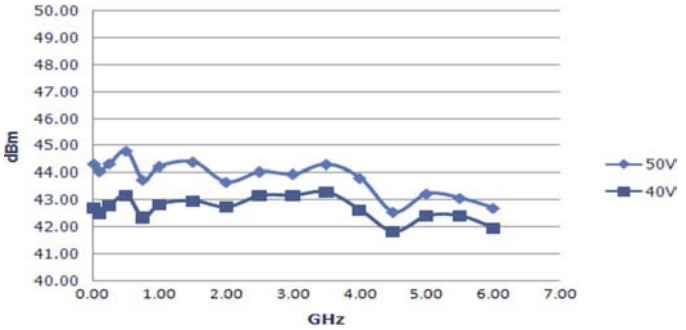

Fig. 39. Output power at $P_{\mathrm{IN}} = 32$ dBm for NDPA MMIC.

is particularly useful in low-pass multioctave applications. The power and efficiency limitations for a reactively match amplifier are governed by the Bode–Fano power-bandwidth limit and by passive circuit losses. For very high-power levels, these limits dictate a maximum drain voltage based on a load-line match over the required bandwidth. In principle, the reactive elements of the active devices can be absorbed into the gate and drain synthetic transmission lines of a distributed topology with the limitations being gate line cutoff frequency and loss along the drain line [56]. A further complication in the design of power distributed amplifiers is that of device load-line match over the required band. Using standard distributed design techniques, some active devices may actually sink power in parts of the band.

To achieve high efficiency from the distributed amplifier, a nonuniform approach is used in the design of the output transmission line where the characteristic impedance changes cell by cell and the output reverse termination is eliminated [57]. Proper design of the gate and drain lines and resizing of the individual cells will establish a reasonable load-line impedance for each cell.

Other issues affecting nonuniform distributed power amplifier (NDPA) performance include output line loss, drain–gate feedback, and drain voltage level required to provide power to a 50-Ω load. Each of these design problems can be reduced by using a balanced cascode configuration for individual cells [58]. The cascode configuration exhibits significantly reduced feedback and output conductance compared to a single common-source stage. With the common-source and common-gate stages balanced as shown in [58], the drain voltage can be increased as much as twofold without incurring breakdown issues.

Although device breakdown would support operation of the cascode cell up to a drain voltage of 80 V, the design becomes thermally limited. For CW operation, experience shows that 4–5 W/mm is the limit of dissipated power to maintain channel temperatures $<200\,^{\circ}$C. The dynamic self-heating feature of the nonlinear model is crucial for predicting this operation. For the five-stage design example shown in Fig. 37, this limit is a drain voltage of 50 V. This should give an output power into 50 Ω of

$$P_{\mathrm{OUT}} = V_D^2/(1.414 * 50) = 25 \text{ W}.$$

The measured performance of this amplifier is shown in Figs. 38 and 39. The amplifier produces 25 W of RF power up to 6 GHz with approximately 30% PAE. This shows that the cascode cell NDPA can be designed with a high-efficiency load line over a decade bandwidth.

VIII. Very High PAs

The majority of existing radar systems utilize technologies such as klystrons, magnetrons, or traveling-wave tube amplifiers (TWTAs) for their PAs. As end users demand more capability and operability for radar systems, they have been in search of more reliable cost-effective highly efficient, yet small-sized radar PAs. There have been two major independent approaches to overcome these challenges and to meet the needs—the first approach is to provide a miniaturized traveling-wave tube (TWT) to help make radar system smaller; the other approach is based on solid-state PAs using GaAs MESFETs or Si bipolar transistors. More recently, GaN HEMTs have become a very promising technology for small-size

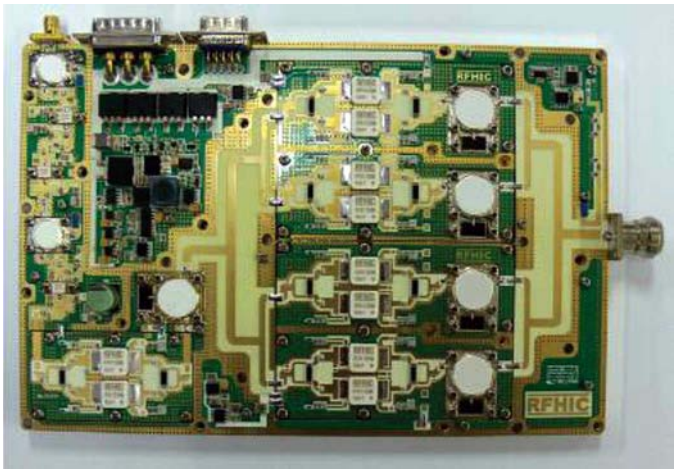

Fig. 40. Practical implementation of 1-kW S-band GaN HEMT PA [59].

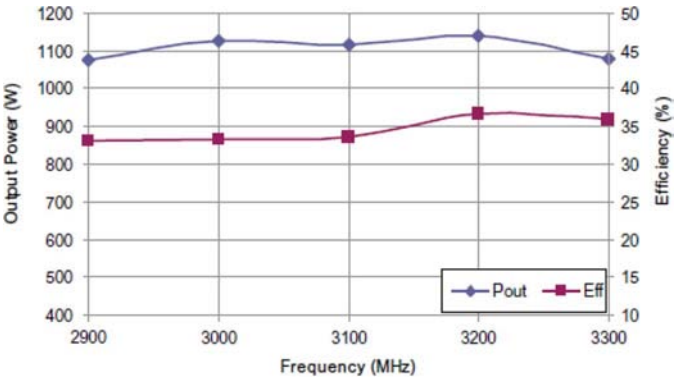

Fig. 41. Measured output power and total line-up efficiency of 1-kW S-band PA [59].

high-efficiency PAs in the kilowatt range. Kwack *et al.* [59], for example, have described the design and manufacture of multistage S-band 1-kW pallets consisting of a pre-driver stage, driver stage, and four combined 300-W units. Fig. 40 shows detail of the complete 1-kW pallet.

As shown in Fig. 41, the SSPA successfully achieved output powers above 1 kW from 2900 to 3300 MHz. The efficiency of the whole PA, including the bias circuits, was about 34%. The output power was measured at the midpoint of the pulsewidth (100 ms with a 10% duty factor), and the efficiency was calculated using the peak current value during the pulse. During the pulse, the output power overshoots at the beginning of the pulse, and then gradually comes down with time, which is defined as power droop (the main cause of power droop being the thermal degradation of performance in the particular semiconductor technology, which for GaN is considerably better than either GaAs or Si due to the superior thermal conductivity of SiC).

IX. Thermal Management and Packaging

A systematic and consistent approach to the thermal modeling and measurement of GaN on SiC HEMT power transistors has been described [60]. Since the power density of such multilayered wide bandgap structures and assemblies can be very high compared with other transistor technologies, the application of such an approach to the prediction of operating channel temperatures (and hence, product lifetime) is important. Both CW and transient (i.e., pulsed and digitally modulated) thermal resistances were calculated for a range of transistor structures and sizes as a function of power density, pulse length, and duty factor and compared with measured channel temperatures and RF parameters. The resulting thermal resistance values have then been imported into new "self-heating" large-signal models so that transistor channel temperatures and the resulting effects on RF performance such as gain, output power, and efficiency can be determined during the amplifier design phase.

GaN HEMT devices place considerable onus on the type of packaging used to house them because of the relatively high RF power density and resulting dissipated heat density from the die. Table V shows some of the commonly available materials used for commercial transistor packages that are suitable for many GaN HEMT devices. The most popular materials used today are copper–tungsten copper–molybdenum–copper, and copper–copper–molybdenum–copper. These materials not only have good thermal expansion coefficient matches to SiC, but also to the alumina ceramic materials most often employed for lead frames. All flange materials also need to have stable properties with regard to temperature, e.g., bowing and flatness, as well as suitable low surface roughness after plating allowing efficient, and void free die attach usually employing AuSn eutectic solder pre-forms.

PAEs for relatively narrowband CW PAs employing GaN can be high (typically greater than 60%), but in certain cases (such as high-frequency ultra-broadband MMICs), efficiencies can be in the low 20% region. In these cases, more exotic materials are required for die mounting such as aluminum diamond or silver diamond composites [61], [62], which have thermal conductivities two to three times that of copper-based materials. Such increases in thermal conductivity have a marked effect on the operating channel temperature of the transistors—typically lowering the temperature by 25% or so (thus, if with Cu–Mo–Cu the T_{CHANNEL} was 200 °C it will be reduced to 150 °C (using silver diamond).

For pulsed applications, the situation is quite different. With almost an infinite number of pulsewidth and duty cycle combinations, an effective way of communicating the thermal resistance θ_{jc} versus time is essential. The best approach is plotting θ_{jc} versus time in a semi-log scale for several duty cycles. In order to perform transient thermal analysis, density and specific heat material properties must be used in addition to thermal conductivity for time constant calculations of each material. The density and specific heat values used are listed in Table VI.

Fig. 42 shows the transient thermal response of a 28.8-mm gatewidth GaN HEMT device in a 60-mil-thick CMC package dissipating 8 W/mm of power at 10%, 20%, 50% duty cycles. The transient response shows two distinct slopes of resistance versus time prior to full thermal saturation at approximately 400 ms. These two slopes can be attributed to the different transient thermal properties of the die and package. Fig. 43 shows how performing a transient thermal analysis with the same die, but mounted into a 40-mil-thick CuW package has the same thermal response during the first 100 ms, but is significantly

TABLE VI
MATERIAL PROPERTIES FOR TRANSIENT THERMAL ANALYSIS

Material	Density (gm/cm^3)	Specific Heat (J/KgC)
GaN	6.1	490
SiC	3.1	681
Au	19.32	126
AuSn	14.5	150
Cu	8.3	385
Mo	10.3	250

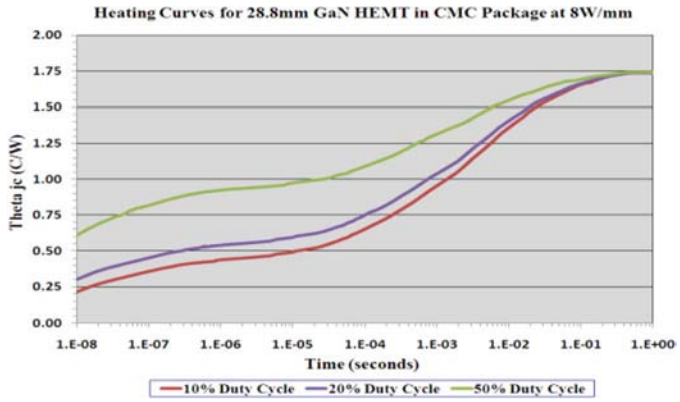

Fig. 42. Thermal resistance versus time for a 28.8-mm gatewidth GaN HEMT.

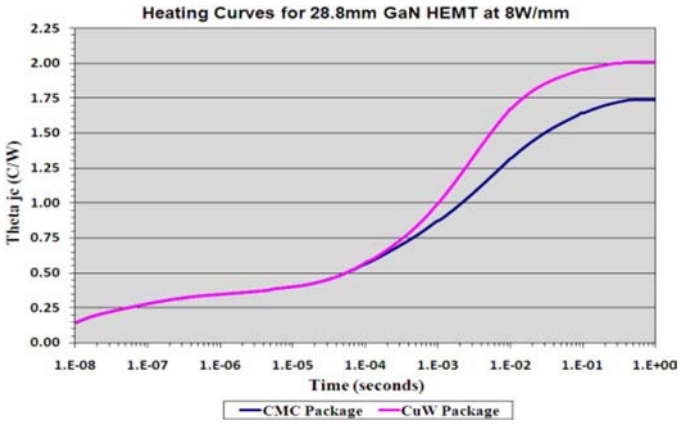

Fig. 43. Transient response of 28.8-mm gatewidth GaN HEMT in two different packages.

different after this point. The thermal resistance increase of the device with the CuW package can be explained by the slower thermal response of the material.

X. ROBUSTNESS

GaN HEMTs have been shown to survive output voltage standing-wave ratio (VSWR) mismatches well compared to Si LDMOSFETs and GaAs FETs. This can result in eliminating or simplifying protection circuitry and reducing field failure rates. The robustness is directly linked to the ability of the devices to handle large voltage and current swings for both transmitted and reflected RF power, as well as to deal with increased heat dissipation. Most GaN transistors are specified to withstand a 10:1 output mismatch VSWR at fully rated output power. For example, Quay *et al.* [63] have described a series of mismatch

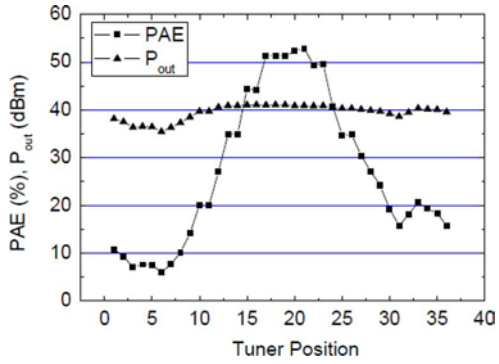

Fig. 44. Output power and PAE of nominal 30-W PA versus 10:1 VSWR mismatch [63].

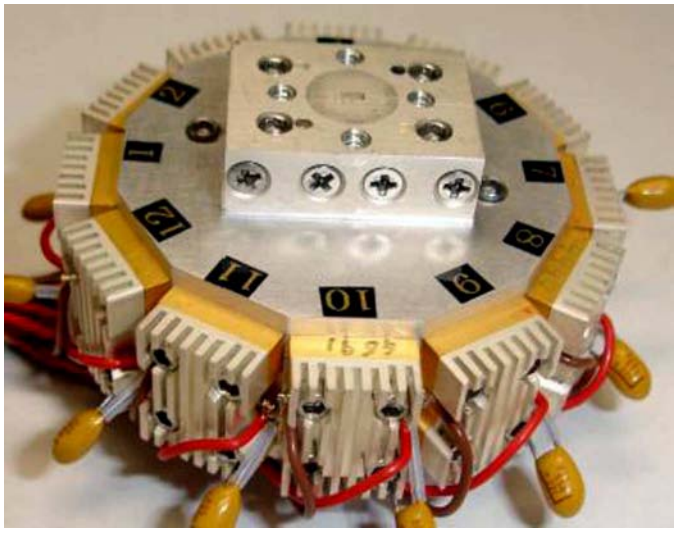

Fig. 45. Twelve 95-GHz GaN HEMT MMIC modules in a low-loss radial line combiner arrangement.

stress testing on a nominal 30-W device operating at 50 V under 10:1 VSWR. Fig. 44 shows the resultant degradation in output power and PAE as a function of output tuner position. The PAE, under certain tuner positions, can be as low as 7% with a corresponding drop in RF power to 4 W with a maximum channel temperature of 278 °C—even so the device did not fail.

XI. OTHER DEVELOPMENTS

Although commercially available GaN HEMT transistors and MMICs today are concentrated at frequencies below 18 GHz, a considerable amount of work has been achieved at much higher frequencies, indicating the potential for short gate-length devices. For example, Micovic *et al.* [64] have reported promising results for MMIC PAs at 88 GHz. The authors used 4×37.5 μm wide devices having a gate length of 0.15 μm as the basic unit cell building blocks. The devices had extrinsic peak transconductances exceeding 360 mS/mm at $V_{\rm DS} = 10$ V, I_{DSS} of 0.8 A/mm, $I_{\rm MAX}$ of 1.2 A/mm, f_T exceeding 90 GHz, and $f_{\rm MAX}$ exceeding 200 GHz. Three-stage MMIC PAs had small-signal gains of 19.6 dB at 84 GHz. The peak power of a MMIC-based module was 842 mW at a drain bias of 14 V and a frequency of 88 GHz. Associated PAE of the

module at peak output power was 14.8% with associated gain of 9.3 dB. The output power of the module exceeded 560 mW over 84–95 GHz. Schellenberg *et al.* [65] have produced a solid-state PA with an output power of 5.2 W at 95 GHz and greater than 3 W over the 94–98.5-GHz band employing such MMICs. The results were achieved by combining 12 of the MMICs in a low-loss radial line combiner network, as shown in Fig. 45.

XII. Conclusion

This paper has attempted to give a broad review of GaN HEMTs in terms of their wide-bandgap advantages over other semiconductor technologies. An overview of a typical AlGaN/GaN on SiC manufacturing technology was followed with a review of small- and large-signal models allowing the accurate design of both hybrid and monolithic circuits. An extensive description of various examples of broadband and high-efficiency PAs was given and followed by comments on thermal management and robustness. GaN HEMT technologies and applications have been and continue to be some of the most challenging and exciting in the RF and microwave industry [66].

Acknowledgment

The authors would like to thank numerous colleagues and coworkers for their successful work on wide-bandgap transistors, hybrid, and MMIC PAs. Acknowledgements are made particularly to those referenced authors that have provided examples of PAs covering a wide range of frequencies and power levels.

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