

Ukazi ARM

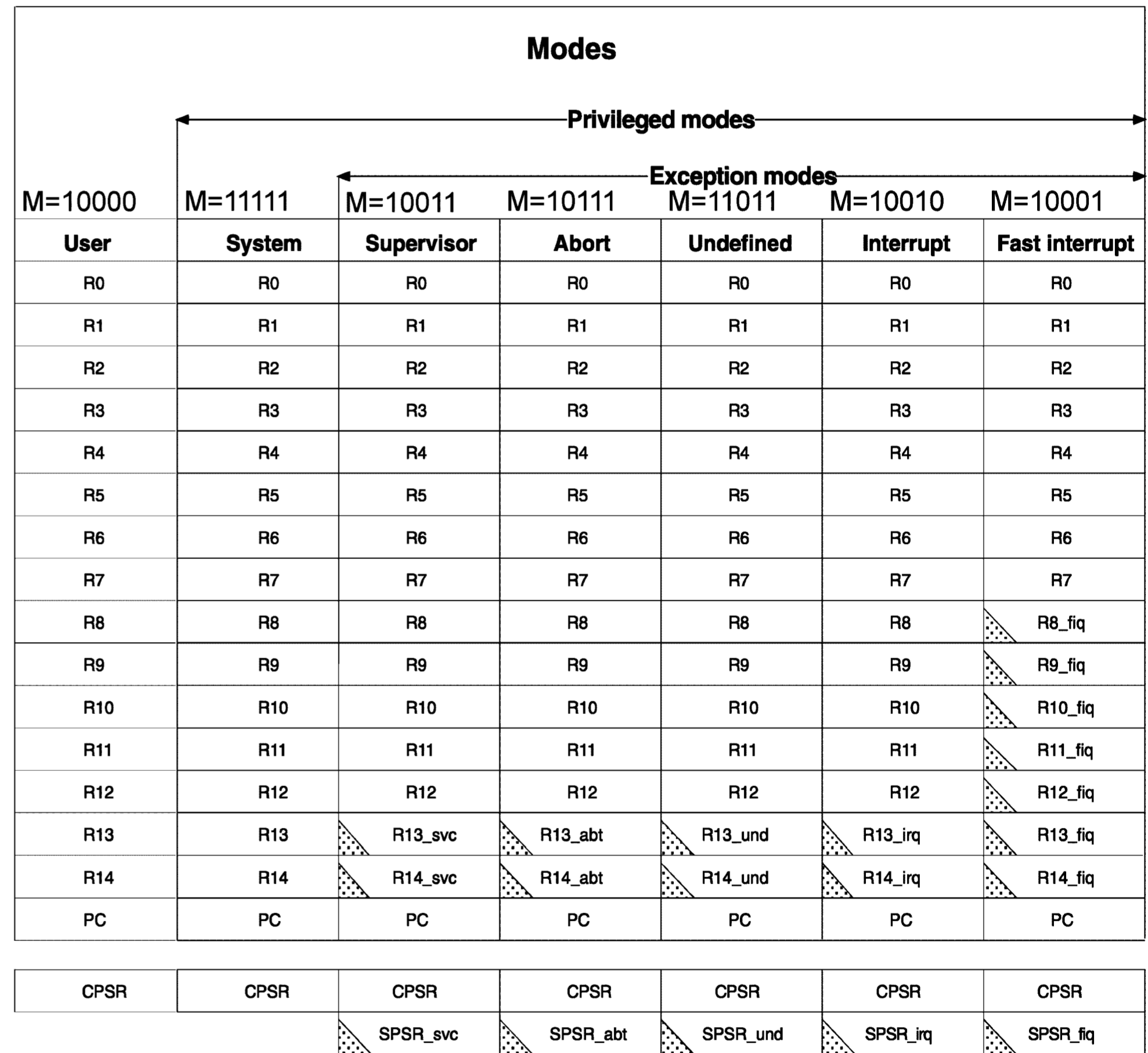
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Data processing immediate shift	cond [1]	0	0	0	opcode	S	Rn	Rd	shift amount	shift	0	Rm																					
Miscellaneous instructions: See Figure A3-4	cond [1]	0	0	0	1 0 x x	0	x x x x x x x x x x x x x x x x x x	0	x x x x x x x x x x x x x x x x x x	0	x x x x																						
Data processing register shift [2]	cond [1]	0	0	0	opcode	S	Rn	Rd	Rs	0	shift	1	Rm																				
Miscellaneous instructions: See Figure A3-4	cond [1]	0	0	0	1 0 x x	0	x x x x x x x x x x x x x x x x x x	0	x x x x	0	x x	1	x x x x																				
Multiplies: See Figure A3-3 Extra load/stores: See Figure A3-5	cond [1]	0	0	0	x x x x x x	x x x x x x x x x x x x x x x x x x	1	x x	1	x x x x																							
Data processing immediate [2]	cond [1]	0	0	1	opcode	S	Rn	Rd	rotate	immediate																							
Undefined instruction	cond [1]	0	0	1	1 0 x 0 0	x x x x x x x x x x x x x x x x x x x x																											
Move immediate to status register	cond [1]	0	0	1	1 0 R 1 0	Mask	SBO	rotate	immediate																								
Load/store immediate offset	cond [1]	0	1	0	P U B W L	Rn	Rd	immediate																									
Load/store register offset	cond [1]	0	1	1	P U B W L	Rn	Rd	shift amount	shift	0	Rm																						
Media instructions [4]: See Figure A3-2	cond [1]	0	1	1	x x x x x x x x x x x x x x x x x x x x	1	x x x x																										
Architecturally undefined	cond [1]	0	1	1	1 1 1 1 1	x x x x x x x x x x x x x x x x x x	1 1 1 1	x x x x																									
Load/store multiple	cond [1]	1	0	0	P U S W L	Rn	register list																										
Branch and branch with link	cond [1]	1	0	1	L	24-bit offset																											
Coprocessor load/store and double register transfers	cond [3]	1	1	0	P U N W L	Rn	CRd	cp_num	8-bit offset																								
Coprocessor data processing	cond [3]	1	1	1	0	opcode1	CRn	CRd	cp_num	opcode2	0	CRm																					
Coprocessor register transfers	cond [3]	1	1	1	0	opcode1	L	CRn	Rd	cp_num	opcode2	1	CRm																				
Software interrupt	cond [1]	1	1	1	1	swi number																											
Unconditional instructions: See Figure A3-6	1 1 1 1	x x																															

Opcode [31:28]	Mnemonic extension	Meaning	Condition flag state
0000	EQ	Equal	Z set
0001	NE	Not equal	Z clear
0010	CS/HS	Carry set/unsigned higher or same	C set
0011	CC/LO	Carry clear/unsigned lower	C clear
0100	MI	Minus/negative	N set
0101	PL	Plus/positive or zero	N clear
0110	VS	Overflow	V set
0111	VC	No overflow	V clear
1000	HI	Unsigned higher	C set and Z clear
1001	LS	Unsigned lower or same	C clear or Z set
1010	GE	Signed greater than or equal	N set and V set, or N clear and V clear (N == V)
1011	LT	Signed less than	N set and V clear, or N clear and V set (N != V)
1100	GT	Signed greater than	Z clear, and either N set and V set, or N clear and V clear (Z == 0, N == V)
1101	LE	Signed less than or equal	Z set, or N set and V clear, or N clear and V set (Z == 1 or N != V)
1110	AL	Always (unconditional)	-
1111	-	See Condition code 0b1111	-

Pogoji ARM

Izjeme ARM

Address	Exception	Mode on entry	I state on entry	F state on entry
0x00000000	Reset	Supervisor	Disabled	Disabled
0x00000004	Undefined instruction	Undefined	I	F
0x00000008	Software interrupt	Supervisor	Disabled	F
0x0000000C	Abort (Prefetch)	Abort	I	F
0x00000010	Abort (Data)	Abort	I	F
0x00000014	Reserved	Reserved	-	-
0x00000018	IRQ	IRQ	Disabled	F
0x0000001C	FIQ	FIQ	Disabled	Disabled



indicates that the normal register used by User or System mode has been replaced by an alternative register specific to the exception mode

Registri jedra ARM

