AN1226
APPLICATION NOTE

UNDERSTANDING LDMOS DEVICE FUNDAMENTALS

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1. ABSTRACT

This paper focuses on the structural aspects of two basic types of RF power MOSFETS: the DMOS and the LDMOS. The comparison of the DMOS and LDMOS structures reveals the basic fundamentals of the RF MOSFET device technology and the challenges that exist to improve their RF performance and reliability.

To date, MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) research has predominately focused on VLSI technology, which has been driven by computer IC market pressures. VLSI devices employ physical structures similar to RF power MOSFETs, but VLSI devices utilize much smaller physical dimensions. The salient differences between RF MOSFETs and VLSI devices are larger channel lengths, greater junction depths and thicker gate oxides, employed by the former, as required to obtain the high power needed for most RF applications. Todays power RF applications need higher gain and more power without complicated peripheral circuitry. The RF market is being driven by the need for higher reliability, gain, linearity and output power requirements that will be constrained by the application's DC power supply limitations. Most high power RF applications are using DC supply voltages ranging from 20 to 50 volts.

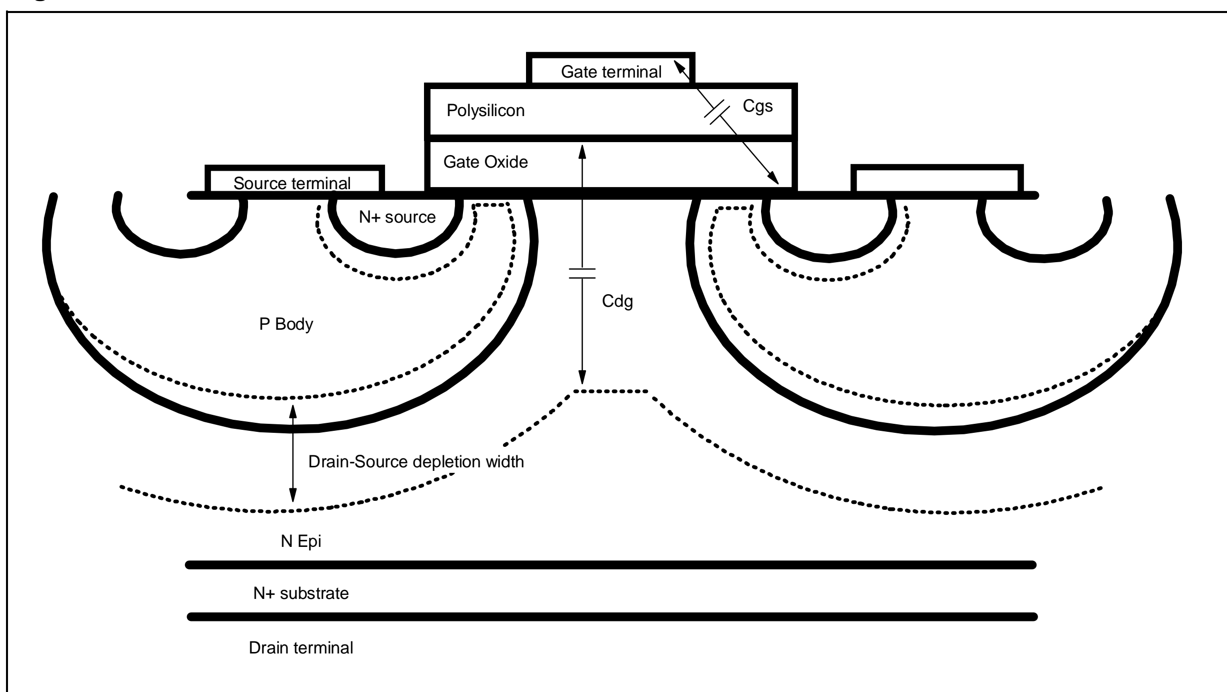
2. MOSFETs.

There are two major structural categories of RF MOSFETs in use today. These structures, DMOS (double-diffused Metal-Oxide-Semiconductor) and LDMOS (laterally diffused Metal-Oxide-Semiconductor), have unique behaviors: semiconductor process and geometry dependent. These acronyms can be confusing, especially since the acronym LDMOS is a concatenation of acronyms that have been used to designate various aspects of the lateral device and often stands for lateral current (L) double-diffused MOS (DMOS). These devices can be created in two common types, the PMOS (p-type MOSFET) and NMOS (n-type MOSFET), but this paper will focus on NMOS only. Figures 1 and 2 depict the physical structures of DMOS and LDMOS, respectively. From these figures, it is apparent LDMOS is predominately a lateral, surface-effect device, while the DMOS geometry incorporates large vertical and lateral structures forcing the time and current density of the spatial dependent vector to contain significant vertical and lateral component.

Both of these MOSFETs are composed of three terminal devices (assuming substrate shorted to source), commonly identified as the source, gate and drain, where the voltage on the gate controls the current flowing from the drain to the source. The most common circuit configuration for these devices is the common source (CS) configuration, which is comparable (in some respects) to the common emitter configuration of the bipolar transistor. Considering this, any frequency-dependent source to ground connection will introduce negative feedback. Other configurations are used but under the CS configuration the drain is connected to the high DC voltage while the source is grounded. The gate is used to induce a field-enhanced depletion region between the source and drain, and thereby creating a "channel". The acronym NMOS was derived from the fact that the p-type channel has been inverted,

creating an effective n-type material due to the depletion of the holes in the p-type channel. A high concentration of electrons is left with energy near the conduction band due to the barrier lowering caused by the gate field, and the electrons can then accelerate due to the field produced by the drain to source biasing. The details of the above mentioned gate-induced channel are critical to MOS operation. The LDMOS channel is predominately defined by the physical size of the gate structure (ignoring secondary effects due to diffusion vagaries) that overlies the graded p-type threshold adjust, implantation and diffusion area. The source and drain regions are on the laterally opposing sides of the gate area, and the diffusion process may produce an undercut region below the gate due to the single-step lateral diffusion process that defines the source and drain regions. The source and drain regions under bias create depletion regions that are connected by the gate induced depletion region in the p-body, and this connection defines the “effective channel length” which is a measure of the distance between the source and drain depletion edges. For NMOS, the depletion region is a region where the high electric field lowers the energy barrier to the electron conduction band. Once the barrier is lowered sufficiently, current easily flows between source and drain. LDMOS channel current is controlled by the vertical electric field induced by the gate and the lateral field that exists between the source and drain.

Figure 1: Basic DMOS Structure



The depletion region between the source and drain is dependent on the junction doping profiles. In general, the depletion region will reach farther into a lower doped region than a higher doped region. The depletion region will extend into the channel region reducing the actual channel length formed by diffusion to the effective channel length. This creates the possibility of undesired behavior in the form of hot carrier injection due to the high electric fields, drain induced barrier lowering (DIBL) and short channel effects (SCE). A carefully designed, lightly doped drain, and threshold adjust p-body (that is graded appropriately) will mitigate the undesired behavior.

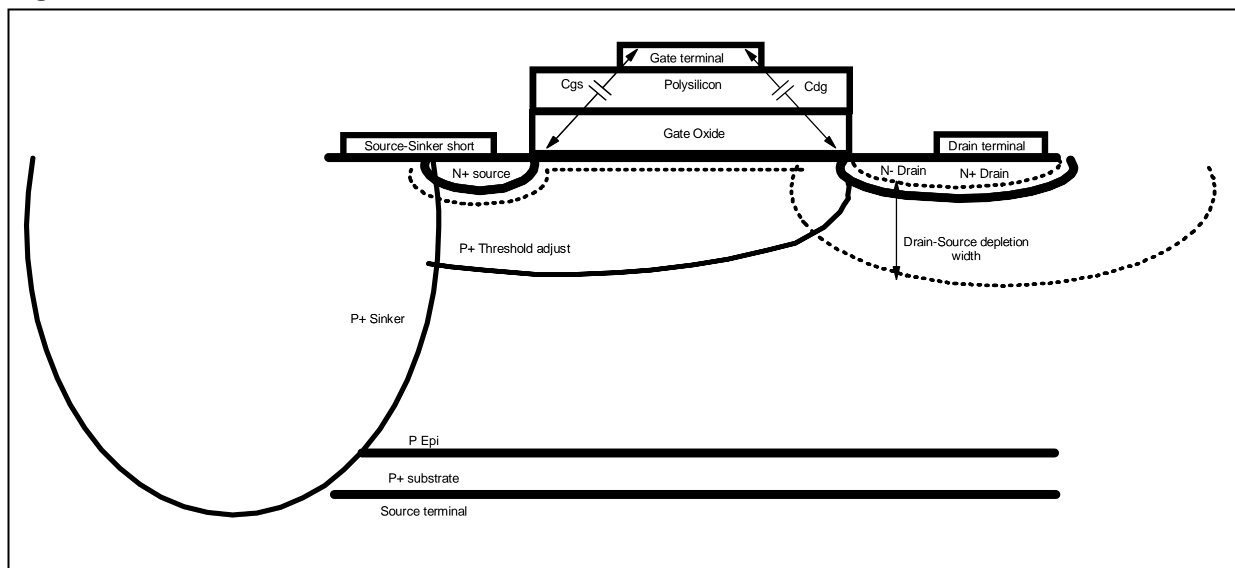
In contrast to the LDMOS, the DMOS structure consists of an n-type substrate on which is grown an n-epitaxial layer that forms the large drain region. The gate region is formed on the surface that overlies the graded p-type body implantation and diffusion area. The source regions are implanted and diffused on either side of the gate to form two separate transistors with a common drain region. The depletion regions

will form around the source and p-body and these depletion regions can be connected by the field induced depletion region formed by the gate. The depletion region connecting the drain and source defines the channel and its dimensions are determined by the source and body doping.

Another fundamental difference between the DMOS and LDMOS is the characteristic of the source connection to the outside world. The source of a DMOS is located at the surface of the die, while the drain is formed by the substrate region and therefore wire bonds must be used to connect the source to the external circuitry. These wire bonds form a dependant frequency element reducing gain at high frequencies due to negative feedback. In addition, the common surface connection dictates that insulating material (BeO) can be used to isolate the drain. This insulating material is a thermal impedance that must be considered for power dissipation. The source of the LDMOS is also on the surface, however its common connection is formed by diffusing a highly doped p-type region, which acts like an ohmic connection from the source at the surface of the substrate, eliminating the need for parasitic wire bonds. This method also eliminates the ceramic interface (that exists in DMOS) and improves the junction to case thermal resistance, and therefore, relieves some of the associated power dissipation issues.

In summary, the LDMOS channel is determined by the gate length, source diffusion and drain diffusion.

Figure 2: Basic LDMOS Structure



The DMOS channel is determined by the lateral source diffusion edge and p-body diffusion edge. The differences in the electrical field distributions influence each of the MOSFET's behaviors due to the fact that the DMOS has significant lateral and vertical components, whereas the LDMOS is predominately a lateral field device. The differences in the source connections are significant in terms of the high frequency behavior, in that the DMOS will have greater negative feedback. These inherent differences establish the appropriate domain of applications for each of these MOSFET structures.

The salient parameters that distinguish the differences in the circuit-level performance (as used in SPICE) for DMOS and LDMOS are $V_{DS(on)}$, C_{ISS}, and C_{RSS} (see Figures 1 and 2). $V_{DS(on)}$ is the inverse of $R_{DS(on)}$. In contrast to DMOS, the LDMOS contains an additional p-type sinker element which has a graded doping concentration subsequent to diffusion. This is a portion of $R_{DS(on)}$ and optimization of this element is critical to reducing $R_{DS(on)}$. The shallow junctions of the LDMOS and subsequent reduction of gate overlap, reduce the input capacitance (C_{ISS}). One of the most significant differences between LDMOS and DMOS in terms of circuit performance pertains to the feedback capacitance (C_{RSS}). C_{RSS} in

the LDMOS structure is primarily composed of the gate drain overlap which is minimal compared to the DMOS. The DMOS C_{RSS} is larger because the entire Drain contributes to the $C_{RSS.}$ The other significant parameters that are important for circuit behavior are not critically dependent on the DMOS and LDMOS specific structures. For example, the transconductance is directly proportional to the channel width/length ratio, and the voltage threshold is always determined by the doping of the channel, gate oxide thickness..., etc.

3. CONCLUSION

This brief description of the fundamental structure of the LDMOS and DMOS invites a comparison of the critical parameters which determine the unique behavior of these two different MOSFET devices. From this comparison one can speculate on the qualitative aspect of LDMOS and DMOS. For example, if contemplating which structure is most susceptible to drain to source punch-through, one would consider the depletion regions. The LDMOS channel length and doping must prevent the drain and source depletion edges from meeting. The geometry and doping profiles are the keys to understanding many other issues as well.

The following paper in this series (AN1228 - Related LDMOS Device Parameters to RF Performance) investigates the root causes of the various failure mechanisms that are endemic to DMOS and LDMOS. This investigation will require the understanding of the microscopic aspects of semiconductor physics and processing and will therefore enlighten the reader on some of the esoteric phenomena that exist with MOSFETs.

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