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REV 6

TMOS

Power MOSFET Transistor Device Data

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TMOS Power MOSFET Transistor Device Data

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To enter combinations of letters and numbers (such as a part number, your first initial, your last name or company name), you must use sequences of two-digit codes to represent all of the letters and numbers. The telephone keypad groups three letters on each key. Numbers are prefixed with a “0”. The number “7” would be entered as 07.

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Two-digit codes:	61	23	06	05	03	00

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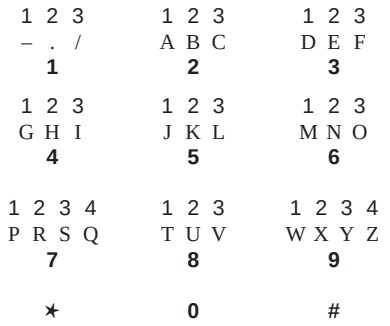

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Section One
Alphanumeric Index of Part Numbers

Alphanumeric Index of Part Numbers

The following index provides you with a quick page number reference for complete data sheets. Contact your local Motorola Sales Office for data sheets not referenced in this index.

Motorola Part Number	Data Sheet Page Number
MTP3055VL	4–926
MTSF1P02HD	4–932
MTSF2P02HD	4–940
MTSF3N02HD	4–943
MTSF3N03HD	4–951
MTV6N100E	4–959
MTV10N100E	4–965
MTV16N50E	4–971
MTV20N50E	4–977
MTV25N50E	4–983
MTV32N20E	4–989

Motorola Part Number	Data Sheet Page Number
MTV32N25E	4–995
MTW6N100E	4–1001
MTW7N80E	4–1007
MTW8N60E	4–1013
MTW10N100E	4–1019
MTW14N50E	4–1025
MTW16N40E	4–1031
MTW20N50E	4–1037
MTW24N40E	4–1043
MTW32N20E	4–1049

Motorola Part Number	Data Sheet Page Number
MTW32N25E	4–1055
MTW35N15E	4–1061
MTW45N10E	4–1067
MTY14N100E	4–1073
MTY16N80E	4–1079
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MTY25N60E	4–1091
MTY30N50E	4–1097
MTY55N20E	4–1103
MTY100N10E	4–1109

Obsolete Part Numbers Cross Reference

Old Part Number	New Part Number
BUZ11	MTP36N06V
BUZ71	MTP15N06V
BUZ71A	MTP15N06V
IRF510	MTP10N10E
IRF520	MTP10N10E
IRF530	MTP12N10E
IRF540	MTP27N10E
IRF610	MTP7N20E
IRF620	MTP7N20E
IRF630	MTP20N20E
IRF640	MTP20N20E
IRF720	MTP4N40E
IRF730	MTP5N40E
IRF740	MTP10N40E
IRF820	MTP3N50E
IRF840	MTP8N50E

Old Part Number	New Part Number
IRFZ20	MTP15N06V
MMFT3055E	MMFT3055V
MMFT3055EL	MMFT3055VL
MTB15N06E	MTB15N06V
MTB23P06E	MTB23P06V
MTB30N06EL	MTB30N06VL
MTB36N06E	MTB36N06V
MTB50N06E	MTB50N06V
MTB50N06EL	MTB50N06VL
MTD5P06E	MTD5P06V
MTD8N06E	MTD15N06V
MTD10N05E	MTD15N06V
MTD2955E	MTD2955V
MTD3055E	MTD3055V
MTD3055EL	MTD3055VL
MTP3N25E	MTP9N25E

Old Part Number	New Part Number
MTP8N06E	MTP15N06V
MTP15N05E	MTP15N06V
MTP15N05EL	MTP15N06VL
MTP15N06E	MTP15N06V
MTP23P06	MTP23P06V
MTP30N06EL	MTP30N06VL
MTP36N06E	MTP36N06V
MTP50N05E	MTP50N06V
MTP50N05EL	MTP50N06VL
MTP50N06E	MTP50N06V
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MTP3055EL	MTP3055VL
MTW20P10	MTP12P10
MTW23N25E	MTW32N25E
MTW26N15E	MTW35N15E
MTW54N05E	MTP50N06V

Section Two

TMOS Power MOSFETs Products Selector Guide

In Brief . . .

Motorola continues to build a world class portfolio of TMOS Power MOSFETs with new advances in silicon and packaging technology. The following new advances have been made in the area of silicon technology.

- Additional high voltage devices with voltages up to 1200 volts.
- The new High Cell Density (HDTMOS) Family of standard and Logic Level devices in both N and P-channel are available in SO–8, DPAK and D^2PAK surface mount packages and in the industry standard TO-220 package.

The following new advances have been made in the area of packaging technology.

- Motorola has added Micro8, SO-8 (MiniMOS) and SOT-223 packages to the surface mount portfolio.
- New High Power packages capable of housing very large die and higher power dissipation are now available in the TO-264 (TO-3PBL) and SOT-227B (ISOTOP) packages.

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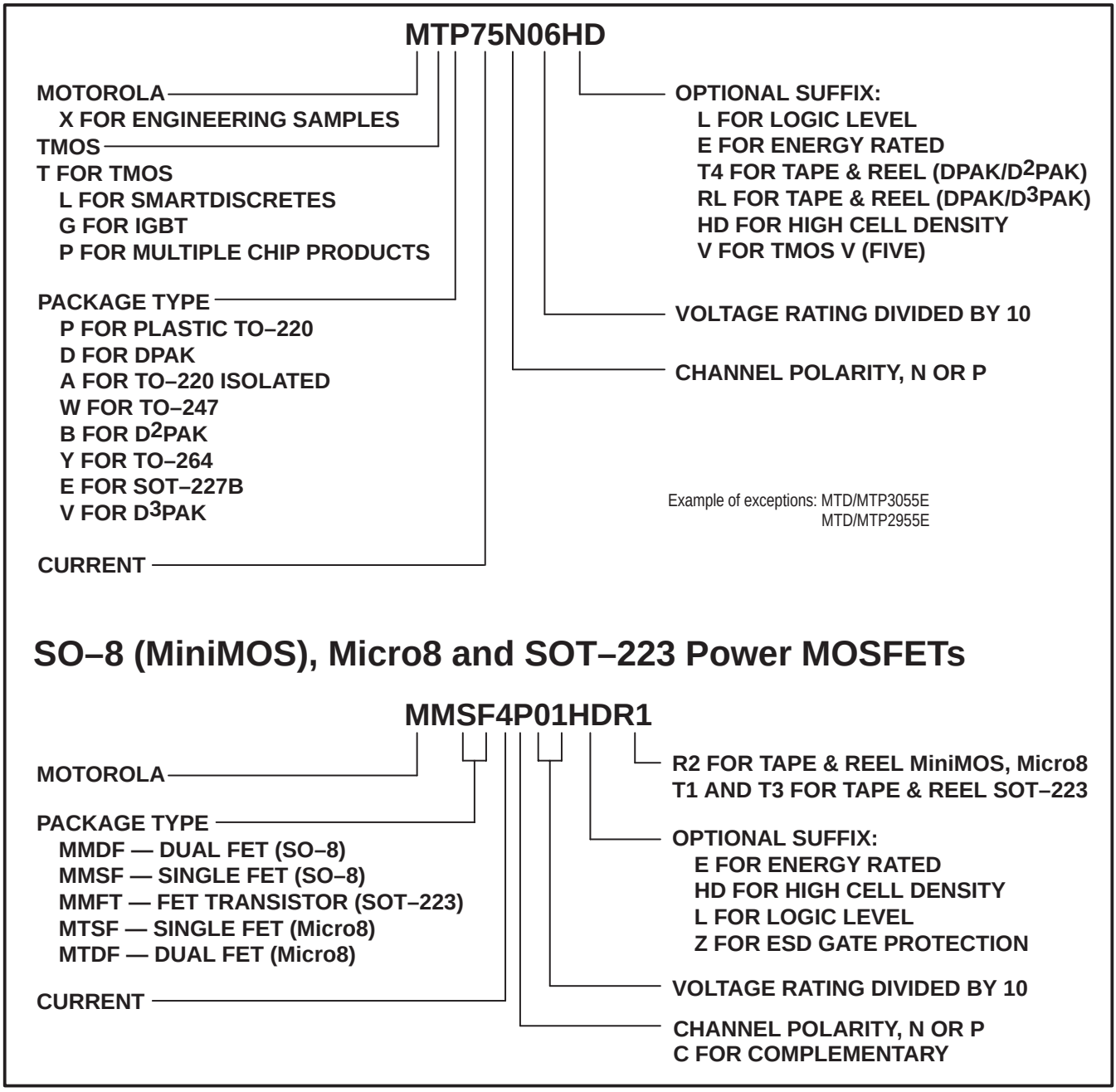
TMOS
Power MOSFETs

TMOS Power MOSFETs Numbering System

Wherever possible, Motorola has used the following numbering systems for TMOS power MOSFET products.



SO–8 (MiniMOS), Micro8 and SOT–223 Power MOSFETs

SO–8 (MiniMOS™)

$V_{(BR)DSS}$	$R_{DS(on)}$ @ V_{GS}			I_D			P_D (3)
(V)	10 V (mΩ)	4.5 V (mΩ)	2.7 V (mΩ)	(A)	Device (5)	Package Type	(Watts) Max
Table 1. SO–8 — N–Channel							
50	300	500	—	1.5	***MMDF1N05E***	SO–8	2.0
40	80	100	—	3.4	***MMDF3N04HD***	SO–8	2.0
30	28	40	—	8	***MMSF7N03HD***	SO–8	2.5
	40	50	—	5	***MMSF5N03HD***	SO–8	2.5
	70	75	—	2.8	***MMDF3N03HD***	SO–8	2.0
	70/200 (11)	75/300	—	2	***MMDF2C03HD***	SO–8	2.0
20	25	40	—	5	***MMSF5N02HD***	SO–8	2.5
	90	100	—	3	***MMDF3N02HD***	SO–8	2.0
	100	200	—	2	***MMDF2N02E***	SO–8	2.0
	90/160 (11)	100/180 (11)	—	2	***MMDF2C02HD***	SO–8	2.0
	100/250 (11)	200/400 (11)	—	2	***MMDF2C02E***	SO–8	2.0
12	—	45	55	4	***MMDF4N01HD***	SO–8	2.0
	—	45/180	55/220 (11)	2	***MMDF2C01HD***	SO–8	2.0
Table 2. SO–8 — P–Channel							
30	100	110	—	3	***MMSF3P03HD***	SO–8	2.5
	200	300	—	2	***MMDF2P03HD***	SO–8	2.0
20	75	95	—	3	***MMSF3P02HD***	SO–8	2.5
	160	180	—	2	***MMDF2P02HD***	SO–8	2.0
	250	400	—	2	***MMDF2P02E***	SO–8	2.0
	250	400	—	2	***MMSF2P02E***	SO–8	2.0
12	—	100	110	4	***MMSF4P01HD***	SO–8	2.5
	—	180	220	2	***MMDF2P01HD***	SO–8	2.0

(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(5) Available in tape and reel only — R1 suffix = 500/reel, R2 suffix = 2500/reel.
(11) N–Channel/P–Channel $R_{DS(on)}$

Micro8™ HDTMOS Products

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (mΩ) Max	@	V_{GS} (Volts)	I_D (cont) Amps	Device	Product Description
Table 3. N–Channel and P–Channel						
20	190		2.7	2	***MTSF1P02HD***	Single P–Channel
	200			1.5	***MTDF1N02HD***	Dual N–Channel
30	75		4.5	3	***MTSF3N03HD***	Single N–Channel
	225			1.5	***MTDF1N03HD***	Dual N–Channel

Devices listed in ***bold, italic*** are Motorola preferred devices.

EZFET™ — Power MOSFETs with Zener Gate Protection

$V_{(BR)DSS}$ (Volts) Min	Description	$R_{DS(on)}$ (mΩ) Max @ V_{GS} (Volts) 10 V	4.5 V	2.7 V	I_D (cont) Amps	Device	V_{GS} (Volts) Max	Package	P_D(3) (Watts) Max
Table 4. SO–8 — N–Channel									
20	Single N–Channel	—	22	27	6	***MMSF6N02Z***	±10	SO–8	1.6
30	Single N–Channel	35	30	—	5	***MMSF5N03Z***	±15		
50	Dual N–Channel	300	500	—	2	***MMDF2N05Z***			
60	N–Channel	18	—	—	55	***MTP55N06Z***	±20	TO–220	136
						MTB55N06Z		D^2PAK	3
		26	28	—	35	***MTP35N06ZL***	±15	TO–220	94
						MTB35N06ZL		D^2PAK	3

SOT–223

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device(12)	I_D (cont) Amps	P_D(1) (Watts) Max
Table 5. SOT–223 — N–Channel					
100	0.30	0.5	***MMFT1N10E***	1	0.8(3)
60	0.14	0.75	***MMFT3055VL***(2)	1.5	
	0.13	0.85	***MMFT3055V***	1.7	
20	0.15	1	***MMFT2N02EL***(2)	2	
Table 6. SOT–223 — P–Channel					
60	0.30	0.6	***MMFT2955E***	1.2	0.8(3)

(1) T_C = 25°C
(2) Indicates logic level
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(12) Available in tape and reel only — T1 suffix = 1000/reel, T3 suffix = 4000/reel.

DPAK

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max @	I_D (Amps)	Device(4)	I_D (cont) Amps	P_D(1) (Watts) Max
Table 7. DPAK — N–Channel					
800	12	0.5	***MTD1N80E***	1	1.75(3)
600	8	0.5	***MTD1N60E***	1	
500	5	0.5	***MTD1N50E***	1	
	3.60	1	***MTD2N50E***	2	
400	3.50	1	***MTD2N40E***	2	
250	1.40	1.5	***MTD3N25E***	3	
	1	2.5	***MTD5N25E***	5	
200	1.5	1.5	***MTD3N20E***	3	
	1.20	2	***MTD4N20E***	4	
	0.70	3	***MTD6N20E***	6	
150	0.30	3	MTD6N15	6	

(1) T_C = 25°C
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.

(continued)

Devices listed in ***bold, italic*** are Motorola preferred devices.

DPAK (continued)

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@	I_D (Amps)	Device[4]	I_D (cont) Amps	P_D[1] (Watts) Max
Table 7. DPAK — N–Channel (continued)						
100	0.40		3	***MTD6N10E***	6	1.75[3]
	0.25		4.5	***MTD9N10E***	9	
	0.22		5	***MTD10N10EL***	10	
			7	***MTD14N10E***	14	
60	0.15		4	***MTD3055V***	8	
	0.18		6	***MTD3055VL***[2]	12	
	0.18		6	***MTD12N06EZL***[2][13]	12	
	0.12		7.5	***MTD15N06V***	15	
	0.085		7.5	***MTD15N06VL***[2]	15	
	0.045		10	***MTD20N06HD***	20	
	0.045		10	***MTD20N06HDL***[2]	20	
	0.080		10	***MTD20N06V***	20	
30	0.035		10	***MTD20N03HDL***[2]	20	
Table 8. DPAK — P–Channel						
500	15.0		0.5	***MTD1P50E***	1	1.75[3]
100	0.66		3	***MTD6P10E***	6	
60	0.45		2.5	***MTD5P06V***	5	
	0.30		6	***MTD2955V***	12	
	0.15		10	***MTD20P06HDL***[2]	20	
30	0.099		10	***MTD20P03HDL***[2]	19	

(1) T_C = 25°C
(2) Indicates logic level
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.
(13) ESD protected to 4 kV.

D^2PAK

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@	I_D (Amps)	Device[4]	I_D (cont) Amps	P_D[1] (Watts) Max
Table 9. D^2PAK — N–Channel						
1200	5.0		1.5	***MTB3N120E***	3	2.5[3]
1000	9		0.5	***MTB1N100E***	1	
	4		1.5	***MTB3N100E***	3	
800	3		2	***MTB4N80E***	4	
600	1.20		3	***MTB6N60E***	6	
	4.16		1	***MTB2N60E***	2	
500	0.80		4	***MTB8N50E***	8	
400	3.50		1	***MTB2N40E***	2	
	0.55		5	***MTB10N40E***	10	
250	0.50		4.5	***MTB9N25E***	9	
	0.25		8	***MTB16N25E***	16	

(1) T_C = 25°C
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.

(continued)

Devices listed in ***bold, italic*** are Motorola preferred devices.

D²PAK (continued)

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@	I_D (Amps)	Device (4)	I_D (cont) Amps	P_D (1) (Watts) Max
Table 9. D²PAK — N–Channel (continued)						
200	0.16		10	***MTB20N20E***	20	2.5 (3)
100	0.060		16.5	***MTB33N10E***	33	
60	0.12		7.5	***MTB15N06V***	15	
	0.05		15	***MTB30N06VL*** (2)	30	
	0.026		17.5	***MTB35N06ZL***	35	
	0.04		18	***MTB36N06V***	32	
	0.032		21	MTB50N06VL (2)	42	
	0.028		21	MTB50N06V	42	
	0.024		26	***MTB52N06VL*** (2)	52	
	0.018		27.5	***MTB55N06Z*** (13)	55	
	0.022		26	***MTB56N06V***	52	
	0.014		30	***MTB60N06HD***	60	
	0.01		37.5	***MTB75N06HD***	75	
50	0.0095		37.5	***MTB75N05HD***	75	
25	0.009		37.5	***MTB75N03HDL*** (2)	75	
Table 10. D²PAK — P–Channel						
500	6		1	***MTB2P50E***	2	2.5 (3)
60	0.12		11.5	***MTB23P06V***	23	
	0.080		15	***MTB30P06V***	30	
30	0.025		25	***MTB50P03HDL*** (2)	50	

(1) T_C = 25°C
(2) Indicates logic level
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.
(13) ESD protected to 4 kV.

D³PAK

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@	I_D (Amps)	Device (4)	I_D (cont) Amps	P_D (1) (Watts) Max
Table 11. D³PAK — N–Channel						
1000	1.50		3	***MTV6N100E***	6	178
	1.30		5	***MTV10N100E***	10	250
500	0.400		8	***MTV16N50E***	16	250
	0.240		10	***MTV20N50E***	20	250
	0.200		12.5	***MTV25N50E***	25	250
250	0.080		16	***MTV32N25E***	32	250
200	0.075		16	***MTV32N20E***	32	180

(1) T_C = 25°C
(4) Available in tape and reel — add T4 suffix to part number.

Devices listed in ***bold, italic*** are Motorola preferred devices.

TO–220AB

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@	I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
Table 12. TO–220AB — N–Channel						
1200	5.0		1.5	***MTP3N120E***	3	125
1000	9		0.5	***MTP1N100E***	1	75
	4.0		1.5	***MTP3N100E***	3	125
800	12		1	***MTP1N80E***	1	48
	3		2	***MTP4N80E***	4	125
600	8		0.5	***MTP1N60E***	1	50
	3.80		1	***MTP2N60E***	2	
	2.20		1.5	***MTP3N60E***	3	75
	1.20		3	***MTP6N60E***	6	125
500	5		0.5	***MTP1N50E***	1	50
	3.60		1	***MTP2N50E***	2	75
	3		1.5	***MTP3N50E***	3	50
	1.50		2	***MTP4N50E***	4	75
	0.80		4	***MTP8N50E***	8	125
400	3.50		1	***MTP2N40E***	2	50
	1.80		2	***MTP4N40E***	4	
	1		2.5	***MTP5N40E***	5	75
	0.55		5	***MTP10N40E***	10	125
250	0.5		4.5	***MTP9N25E***	9	75
	0.25		8	***MTP16N25E***	16	125
200	0.70		3.5	***MTP7N20E***	7	75
	0.16		10	***MTP20N20E***	20	125
100	0.25		5	***MTP10N10E***	10	75
	0.22		5	***MTP10N10EL***	10	40
	0.16		6	***MTP12N10E***	12	75
	0.070		13.5	***MTP27N10E***	27	125
	0.060		16.5	***MTP33N10E***	33	150
60	0.18		6	***MTP3055VL***(2)	12	48
	0.15		6	***MTP3055V***	12	
	0.12		7.5	***MTP15N06V***	15	60
	0.085		7.5	***MTP15N06VL***	15	
	0.080		10	***MTP20N06V***	20	90
	0.05		15	***MTP30N06VL***(2)	30	
	0.026		17.5	***MTP35N06ZL***	35	94
	0.04		18	***MTP36N06V***	32	90
	0.032		21	MTP50N06VL(2)	42	150
	0.028		21	MTP50N06V	42	
	0.022		26	***MTP52N06V***	52	
	0.024		26	***MTP52N06VL***	52	
	0.018		22.5	***MTP55N06Z***	55	
	0.014		30	***MTP60N06HD***	60	
	0.01		37.5	***MTP75N06HD***	75	
50	0.0095		37.5	***MTP75N05HD***	75	
25	0.009		37.5	***MTP75N03HDL***(2)	75	

(1) T_C = 25°C
(2) Indicates logic level

(continued)

Devices listed in ***bold, italic*** are Motorola preferred devices.

TO–220AB (continued)

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
Table 13. TO–220AB — P–Channel					
500	6	1	***MTP2P50E***	2	75
200	1	3	***MTP6P20E***	6	
100	0.30	6	***MTP12P10***	12	88
60	0.45	2.5	***MTP5P06V***	5	40
	0.30	6	***MTP2955V***	12	60
	0.12	11.5	***MTP23P06V***	23	125
	0.08	15	***MTP30P06V***	30	125
30	0.025	25	***MTP50P03HDL***(2)	50	150

(1) T_C = 25°C
(2) Indicates logic level

TO–247 (Isolated Mounting Hole)

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
Table 14. TO–247 — N–Channel					
1000	1.50	3	***MTW6N100E***	6	180
	1.30	5	***MTW10N100E***	10	250
800	1	3.5	***MTW7N80E***	7	180
600	0.55	4	***MTW8N60E***	8	180
500	0.40	7	***MTW14N50E***	14	180
	0.24	10	***MTW20N50E***	20	250
400	0.24	8	***MTW16N40E***	16	180
	0.16	12	***MTW24N40E***	24	250
250	0.08	16	***MTW32N25E***	32	250
200	0.075	16	***MTW32N20E***	32	180
150	0.05	17.5	***MTW35N15E***	35	180
100	0.035	22.5	***MTW45N10E***	45	180

(1) T_C = 25°C

TO–264

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@ I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
Table 15. TO–264 — N–Channel					
1000	0.80	7	***MTY14N100E***	14	568
800	0.50	8	***MTY16N80E***	16	568
600	0.21	12.5	***MTY25N60E***	25	568
500	0.26	10	***MTY20N50E***	20	300
	0.15	15	***MTY30N50E***	30	568
200	0.028	27.5	***MTY55N20E***	55	568
100	0.011	50	***MTY100N10E***	100	568

(1) T_C = 25°C

Devices listed in ***bold, italic*** are Motorola preferred devices.

SOT–227B (ISOTOP™) Ⓤ

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	@	I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max

Table 16. SOT–227B (ISOTOP)

500	0.15	15	***MTE30N50E***	30	250
	0.08	26.5	***MTE53N50E***	53	460
200	0.015	62.5	***MTE125N20E***	125	460
100	0.0055	107	***MTE215N10E***	215	460

(1) T_C = 25°C

Ⓤ Indicates UL Recognition — File #E69369

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Table 17. Ignition IGBTs

BV_{CES} (Volts) Clamped	$V_{CE(on)}$ @ 10 A	Device	P_D(1) (Watts) Max	Package
140 V	1.8	***MGP20N14CL***	150	TO–220AB
350 V	1.8	***MGP20N35CL***	150	TO–220AB
		MGB20N35CL	2.5(3)(4)	D^2PAK
400 V	1.8	***MGP20N40CL***	150	TO–220AB
		MGB20N40CL	2.5(3)(4)	D^2PAK

Table 18. TO–220AB

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
60 Clamped Voltage	0.75	1	***MLP1N06CL***	Current Limited	40
62 Clamped Voltage	0.4	2	MLP2N06CL	Current Limited	40

Table 19. DPAK

$V_{(BR)DSS}$ (Volts) Min	$R_{DS(on)}$ (Ohms) Max	I_D (Amps)	Device	I_D (cont) Amps	P_D(1) (Watts) Max
60 Clamped Voltage	0.75	1	***MLD1N06CL***	Current Limited	1.75
62 Clamped Voltage	0.4	2	***MLD2N06CL***	Current Limited	1.75

(1) T_C = 25°C
(3) Power rating when mounted on an FR–4 glass epoxy printed circuit board with the minimum recommended footprint.
(4) Available in tape and reel — add T4 suffix to part number.

Devices listed in ***bold, italic*** are Motorola preferred devices.

IGBT — Insulated Gate Bipolar Transistor

Device	BVCES (V)	IC90 (A)	IC @ 25°C (A)	$V_{CE(on)}$ @ IC90 (V) typ	E_{off} @ IC90 (mJ) typ @ 125°C	Package
Table 20. IGBT — N–Channel						
MGP20N60	600	20	32	2.90	1.20	TO–220
MGW20N60D						TO–247
MGW30N60		30	50	2.60	1.80	TO–247
MGY30N60D						TO–264
MGY40N60		40	66	2.60	2.40	TO–264
MGY40N60D						
MGW10N120	1200	12	20	3.10	1.43	TO–247
MGW10N120D						
MGY25N120		25	38	2.90	4.29	TO–264
MGY25N120D						

IC90 = Collector current rating at 90°C case temperature

Power MOS Gate Drivers

Device	Description	Package
Table 21.		
MC33153D	V_{CC}–V_{EE} = 23 V, 1 A Source, 2 A Sink Low Side Driver (Can be used as High Side Driver with Opto–coupler)	8 Pin SOIC
MC33153P		8 Pin PDIP
MPIC2111D	600 V, 420 mA, Half Bridge Driver	8 Pin SOIC
MPIC2111P		8 Pin PDIP
MPIC2112DW	600 V, 420 mA, Half Bridge Driver	16 Pin SOIC–Wide
MPIC2112P		14 Pin PDIP
MPIC2113DW	600 V, 2 A, Half Bridge Driver	16 Pin SOIC–Wide
MPIC2113P		14 Pin PDIP
MPIC2117D	600 V, 420 mA, High Side Driver	8 Pin SOIC
MPIC2117P		8 Pin PDIP
MPIC2130P	600 V, 420 mA, Three Phase Driver	28 Pin PDIP
MPIC2130FN		44 Pin PLCC (modified)
MPIC2131P	600 V, 420 mA, Three Phase Driver	28 Pin PDIP
MPIC2131FN		44 Pin PLCC (modified)
MPIC2151D	600 V, 210 mA, Self Oscillating, Half Bridge Driver	8 Pin SOIC
MPIC2151P		8 Pin PDIP

Devices listed in ***bold, italic*** are Motorola preferred devices.

Section Three
Introduction to Power MOSFETs
Basic Characteristics of Power MOSFETs

Table of Contents

Chapter 1: Introduction to Power MOSFETs

Symbols, Terms and Definitions

The following are the most commonly used letter symbols, terms and definitions associated with Power MOSFETs.

Symbol	Term	Definition
C_{ds}	drain–source capacitance	The capacitance between the drain and source terminals with the gate terminal connected to the guard terminal of a three–terminal bridge.
C_{dg}	drain–gate capacitance	The same as C_{rss} – See C_{rss}.
C_{gs}	gate–source capacitance	The capacitance between the gate and source terminals with the drain terminal connected to the guard terminal of a three–terminal bridge.
C_{iss}	short–circuit input capacitance, common–source	The capacitance between the input terminals (gate and source) with the drain short–circuited to the source for alternating current. (Ref. IEEE No. 255)
C_{oss}	short–circuit output capacitance, common–source	The capacitance between the output terminals (drain and source) with the gate short–circuited to the source for alternating current. (Ref. IEEE No. 255)
C_{rss}	short–circuit reverse transfer capacitance, common–source	The capacitance between the drain and gate terminals with the source connected to the guard terminal of a three–terminal bridge.
g_{FS}	common–source large–signal transconductance	The ratio of the change in drain current due to a change in gate–to–source voltage.
I_D	drain current, dc	The direct current into the drain terminal.
$I_{D(on)}$	on–state drain current	The direct current into the drain terminal with a specified forward gate–source voltage applied to bias the device to the on–state.
I_{DSS}	zero–gate–voltage drain current	The direct current into the drain terminal when the gate–source voltage is zero. This is an on–state current in a depletion–type device, an off–state in an enhancement–type device.
I_G	gate current, dc	The direct current into the gate terminal.
I_{GSS}	reverse gate current, drain short–circuited to source	The direct current into the gate terminal of a junction–gate field–effect transistor when the gate terminal is reverse biased with respect to the source terminal and the drain terminal is short–circuited to the source terminal.
I_{GSSF}	forward gate current, drain short–circuited to source	The direct current into the gate terminal of an insulated–gate field–effect transistor with a forward gate–source voltage applied and the drain terminal short–circuited to the source terminal.
I_{GSSR}	reverse gate current, drain short–circuited to source	The direct current into the gate terminal of an insulated–gate field–effect transistor with a reverse gate–source voltage applied and the drain terminal short–circuited to the source terminal.

Symbol	Term	Definition
I_S	source current, dc	The direct current into the source terminal.
P_T, P_D	total nonreactive power input to all terminals	The sum of the products of the dc input currents and voltages.
Q_g	total gate charge	The total gate charge required to charge the MOSFETs input capacitance to $V_{GS(on)}$.
$R_{DS(on)}$	static drain–source on–state resistance	The dc resistance between the drain and source terminals with a specified gate–source voltage applied to bias the device to the on state.
$R_{\theta CA}$	thermal resistance, case–to–ambient	The thermal resistance (steady–state) from the device case to the ambient.
$R_{\theta JA}$	thermal resistance, junction–to–ambient	The thermal resistance (steady–state) from the semiconductor junction(s) to the ambient.
$R_{\theta JC}$	thermal resistance, junction–to–case	The thermal resistance (steady–state) from the semiconductor junction(s) to a stated location on the case.
$R_{\theta JM}$	thermal resistance, junction–to–mounting surface	The thermal resistance (steady–state) from the semiconductor junction(s) to a stated location on the mounting surface.
T_A	ambient temperature or free–air temperature	The air temperature measured below a device, in an environment of substantially uniform temperature, cooled only by natural air convection and not materially affected by reflective and radiant surfaces.
T_C	case temperature	The temperature measured at a specified location on the case of a device.
t_c	turn–off crossover time	The time interval during which drain voltage rises from 10% of its peak off–state value and drain current falls to 10% of its peak on–state value, in both cases ignoring spikes that are not charge–carrier induced.
T_J	channel temperature	The temperature of the channel of a field–effect transistor.
T_{stg}	storage temperature	The temperature at which the device, without any power applied, may be stored.
$t_{d(off)}$	turn–off delay time	Synonym for current turn–off delay time (see Note 1)*.
$t_{d(off)i}$	current turn–off delay time	The interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain current waveform falls to 90% of its on–state amplitude, ignoring spikes that are not charge–carrier induced.
$t_{d(off)v}$	voltage turn–off delay time	The time interval during which an input pulse that is switching the transistor from a conducting to a nonconducting state falls from 90% of its peak amplitude and the drain voltage waveform rises to 10% of its off–state amplitude, ignoring spikes that are not charge–carrier induced.
$t_{d(on)}$	turn–on delay time	Synonym for current turn–on delay time (see Note 1)*.
$t_{d(on)i}$	current turn–on delay time	The time interval during which can input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the drain current waveform rises to 10% of its on–state amplitude, ignoring spikes that are not charge–carrier induced.

Symbol	Term	Definition
$t_{d(on)v}$	voltage turn–on delay time	The time interval during which an input pulse that is switching the transistor from a nonconducting to a conducting state rises from 10% of its peak amplitude and the drain voltage waveform falls to 90% of its off–state amplitude, ignoring spikes that are not charge–carrier induced.
t_f	fall time	Synonym for current fall time (see Note 1)*.
t_{fi}	current fall time	The time interval during which the drain current changes from 90% to 10% of its peak off–state value, ignoring spikes that are not charge–carrier induced.
t_{fv}	voltage fall time	The time interval during which the drain voltage changes from 90% to 10% of its peak off–state value, ignoring spikes that are not charge–carrier induced.
t_{off}	turn–off time	Synonym for current turn–off time (see Note 1)*.
$t_{off(i)}$	current turn–off time	The sum of current turn–off delay time and current fall time, i.e., $t_{d(off)i} + t_{fi}$.
$t_{off(v)}$	voltage turn–off time	The sum of voltage turn–off delay time and voltage rise time, i.e., $t_{d(off)v} + t_{rv}$.
t_{on}	turn–on time	Synonym for current turn–on time (see Note 1)*.
$t_{on(i)}$	current turn–on time	The sum of current turn–on delay time and current rise time, i.e., $t_{d(on)i} + t_{ri}$.
$t_{on(v)}$	voltage turn–on time	The sum of voltage turn–on delay time and voltage fall time, i.e., $t_{d(on)v} + t_{fv}$.
t_p	pulse duration	The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform. **Note:** The two reference points are usually 90% of the steady–state amplitude of the waveform existing after the leading edge, measured with respect to the steady–state amplitude existing before the leading edge. If the reference points are 50% points, the symbol t_w and term average pulse duration should be used.
t_r	rise time	Synonym for current rise time (see Note 1)*.
t_{ri}	current rise time	The time interval during which the drain current changes from 10% to 90% of its peak on–state value, ignoring spikes that are not charge–carrier induced.
t_{rv}	voltage rise time	The time interval during which the drain voltage changes from 10% to 90% of its peak off–state value, ignoring spikes that are not charge–carrier induced.
t_{ti}	current fall time	The time interval following current fall time during which the drain current changes from 10% to 2% of its peak on–state value, ignoring spikes that are not charge–carrier induced.
t_w	average pulse duration	The time interval between a reference point on the leading edge of a pulse waveform and a reference point on the trailing edge of the same waveform, with both reference points being 50% of the steady–state amplitude of the waveform existing after the leading edge, measured with respect to the steady–state amplitude existing before the leading edge. **Note:** If the reference points are not 50% points, the symbol t_p and term pulse duration should be used.

Symbol	Term	Definition
$V_{(BR)DSR}$	drain–source breakdown voltage with (resistance between gate and source)	The breakdown voltage between the drain terminal and the source terminal when the gate terminal is (as indicated by the last subscript letter) as follows: R = returned to the source terminal through a specified resistance.
$V_{(BR)DSS}$	gate short–circuited to source	S = short–circuited to the source terminal.
$V_{(BR)DSV}$	voltage between gate and source	V = returned to the source terminal through a specified voltage.
$V_{(BR)DSX}$	circuit between gate and source	X = returned to the source terminal through a specified circuit.
$V_{(BR)GSSF}$	forward gate–source breakdown voltage	The breakdown voltage between the gate and source terminals with a forward gate–source voltage applied and the drain terminal short–circuited to the source terminal.
$V_{(BR)GSSR}$	reverse gate–source breakdown voltage	The breakdown voltage between the gate and source terminals with a reverse gate–source voltage applied and the drain terminal short–circuited to the source terminal.
V_{DD}, V_{GG} V_{SS}	supply voltage, dc (drain, gate, source) voltage	The dc supply voltage applied to a circuit or connected to the reference terminal.
V_{DG} V_{DS} V_{GD} V_{GS} V_{SD} V_{SG}	drain–to–gate drain–to–source gate–to–drain gate–to–source source–to–drain source–to–gate	The dc voltage between the terminal indicated by the first subscript and the reference terminal indicated by the second subscript (stated in terms of the polarity at the terminal indicated by the first subscript).
$V_{DS(on)}$	drain–source on–state voltage	The voltage between the drain and source terminals with a specified forward gate–source voltage applied to bias the device to the on state.
$V_{GS(th)}$	gate–source threshold voltage	The forward gate–source voltage at which the magnitude of the drain current of an enhancement–type field–effect transistor has been increased to a specified low value.
$Z_{\theta JA(t)}$	transient thermal impedance, junction–to–ambient	The transient thermal impedance from the semiconductor junction(s) to the ambient.
$Z_{\theta JC(t)}$	transient thermal impedance, junction–to–case	The transient thermal impedance from the semiconductor junction(s) to a stated location on the case.

Note 1: As names of time intervals for characterizing switching transistors, the terms “fall time” and “rise time” always refer to the change that is taking place in the magnitude of the output current even though measurements may be made using voltage waveforms. In a purely resistive circuit, the (current) rise time may be considered equal and coincident to the voltage fall time and the (current) fall time may be considered equal and coincident to the voltage rise time. The delay times for current and voltage will be equal and coincident. When significant amounts of inductance are present in a circuit, these equalities and coincidences no longer exist, and use of the unmodified terms delay time, fall time, and rise time must be avoided.

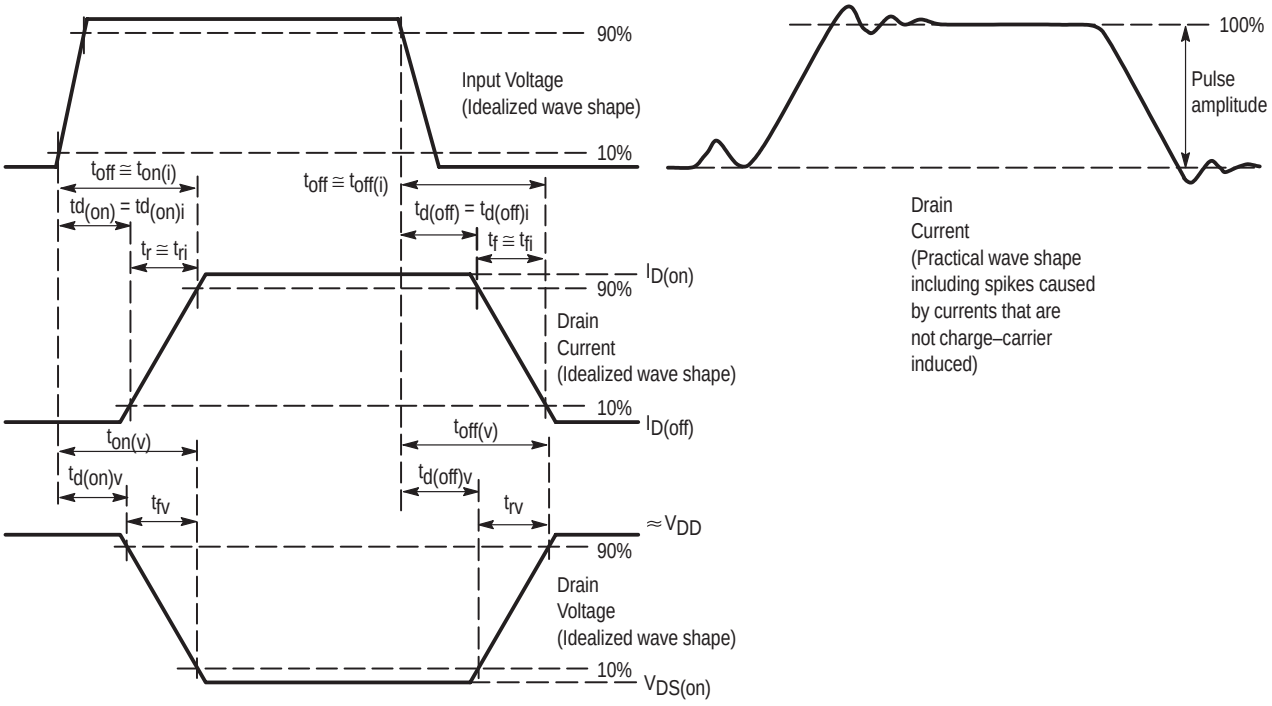
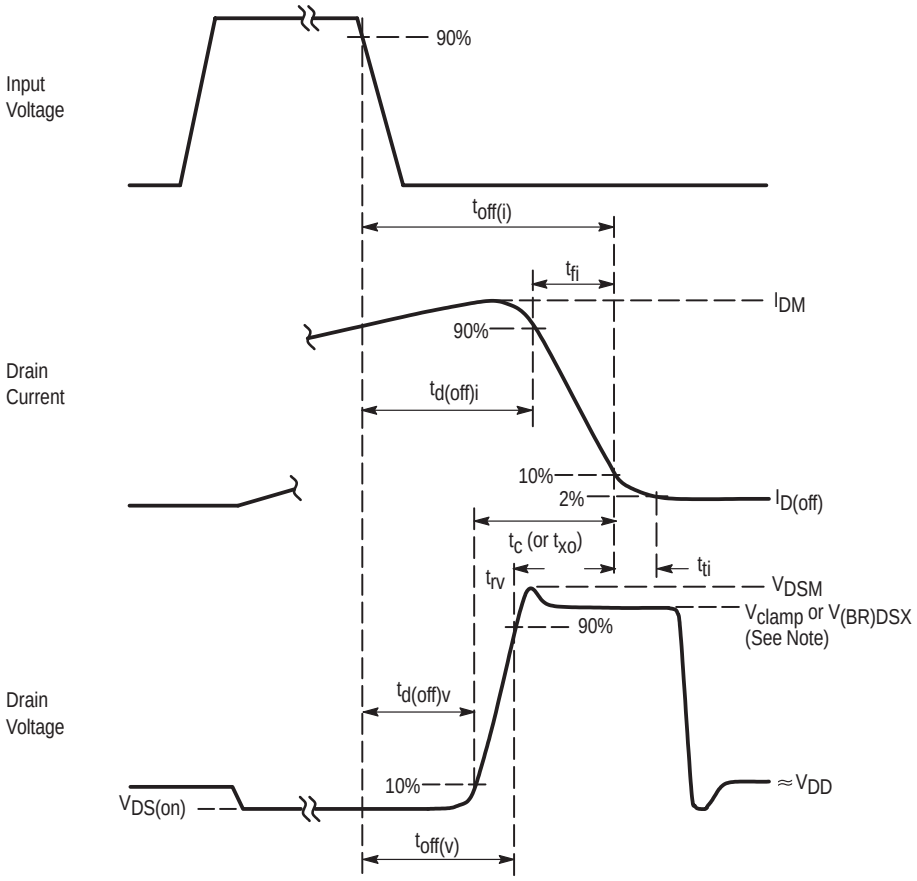


Figure 1–1. Waveforms for Resistive–Load Switching



NOTE: V_{clamp} (in a clamped inductive–load switching circuit) or $V_{(BR)DSX}$ (in an unclamped circuit) is the peak off–state voltage excluding spikes.

Figure 1–2. Waveforms for Inductive Load Switching, Turn–Off

Structures:

Motorola's TMOS Power MOSFET family is a matrix of diffused channel, vertical, metal–oxide–semiconductor power field–effect transistors which offer an exceptionally wide range of voltages and currents with low $R_{DS(on)}$. The inherent advantages of Motorola's power MOSFETs include:

- Nearly infinite static input impedance featuring:
  — Voltage driven input
  — Low input power
  — Few driver circuit components
- Very fast switching times
  — No minority carriers
  — Minimal turn–off delay time
  — Large reversed biased safe operating area
  — High gain bandwidth product
- Positive temperature coefficient of on–resistance
  — Large forward biased safe operating area
  — Ease in paralleling
- Almost constant transconductance
- High dv/dt immunity

Motorola's TMOS power MOSFET line is the latest step in an evolutionary progression that began with the conventional small–signal MOSFET and superseded the intermediate lateral double diffused MOSFET (LDMOSFET) and the vertical V–groove MOSFET (VMOSFET).

The conventional small–signal lateral N–channel MOSFET consists of a lightly doped P–type substrate into which two highly doped N^+ regions are diffused, as shown in Figure 1–3. The N^+ regions act as source and drain which are separated by a channel whose length is determined by photolithographic constraints. This configuration resulted in long channel lengths, low current capability, low reverse blocking voltage and high $R_{DS(on)}$.

Two major changes in the small–signal MOSFET structure were responsible for the evolution of the power MOSFET. One was the use of self aligned, double diffusion techniques to achieve very short channel lengths, which allowed higher channel packing densities, resulting in higher current capability and lower $R_{DS(on)}$. The other was the incorporation of a lightly doped N^+ region between the channel and the N^+ drain allowing high reverse blocking voltages.

These changes resulted in the lateral double diffused MOSFET power transistor (LDMOS) structure shown in Figure 1–4, in which all the device terminals are still on the top surface of the die. The major disadvantage of this configuration is its inefficient use of silicon area due to the area needed for the top drain contact.

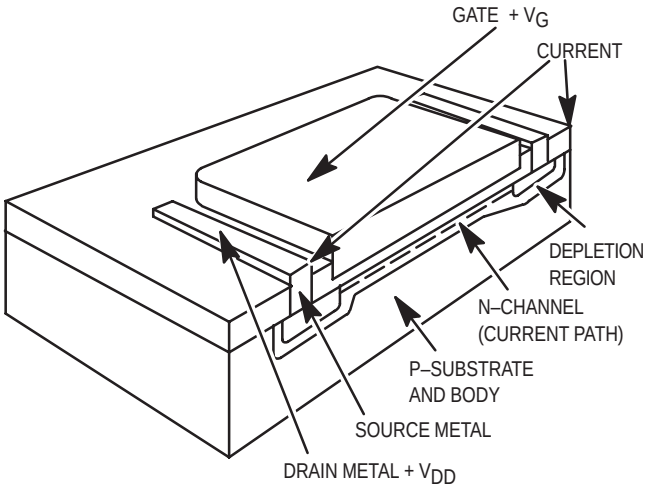


Figure 1–3. Conventional Small–Signal MOSFET has Long Lateral Channel Resulting in Relatively High Drain–to–Source Resistance

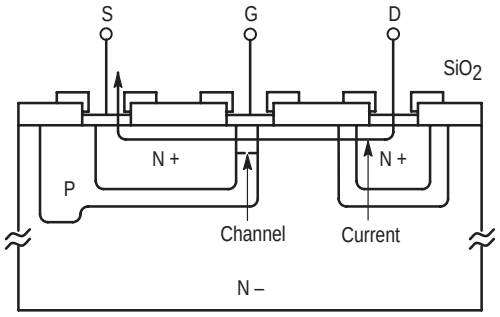


Figure 1–4. Lateral Double Diffused MOSFET Structure Featuring Short Channel Lengths and High Packing Densities for Lower On Resistance

The next step in the evolutionary process was a vertical structure in which the drain contact was on the back of the die, further increasing the channel packing density. The initial concept used a V–groove MOSFET power transistor as shown in Figure 1–5. The channels in this device are defined by preferentially etching V–grooves through double diffused N^+ and P^- regions. The requirements of adequate packing density, efficient silicon usage and adequate reverse blocking voltage are all met by this configuration. However, due to its non–planar structure, process consistency and cleanliness requirements resulted in higher die costs.

The cell structure chosen for Motorola's TMOS power MOSFET's is shown in Figure 1–6. This structure is similar to that of Figure 1–4 except that the drain contact is dropped through the N^- substrate to the back of the die. The gate structure is now made with polysilicon sandwiched between two oxide layers and the source metal applied continuously over the entire active area. This two layer electrical contact gives the optimum in packing density and maintains the processing advantages of planar LDMOS. This results in a highly manufacturable process which yields low $R_{DS(on)}$ and high voltage product.

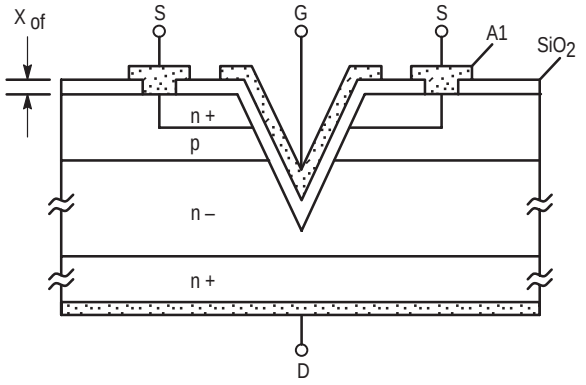


Figure 1–5. V–Groove MOSFET Structure Has Short Vertical Channels with Low Drain–to–Source Resistance

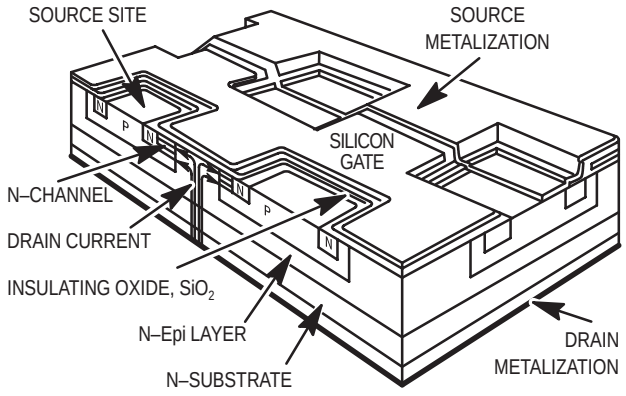


Figure 1–6. TMOS Power MOSFET Structure Offers Vertical Current Flow, Low Resistance Paths and Permits Compact Metalization on Top and Bottom Surfaces to Reduce Chip Size

Operation:

Transistor action and the primary electrical parameters of Motorola's TMOS power MOSFET can be defined as follows:

Drain Current, I_D:

When a gate voltage of appropriate polarity and magnitude is applied to the gate terminal, the polysilicon gate induces an inversion layer at the surface of the diffused channel region represented by r_{CH} in Figure 1–7 (page A–8). This inversion layer or channel connects the source to the lightly doped region of the drain and current begins to flow. For small values of applied drain–to–source voltage, V_{DS}, drain current increases linearly and can be represented by Equation (1).

$$(1)\quad I_D \approx \frac{Z}{L}\ \mu Co\ [V_{GS}–V_{GS(th)}]\ V_{DS}$$

As the drain voltage is increased, the drain current saturates and becomes proportional to the square of the applied gate–to–source voltage, V_{GS}, as indicated in Equation (2).

$$(2)\quad I_D \approx \frac{Z}{2L}\ \mu Co\ [V_{GS}–V_{GS(th)}]^2$$

Where μ = Carrier Mobility
Co = Gate Oxide Capacitance per unit area
Z = Channel Width
L = Channel Length

These values are selected by the device design engineer to meet design requirements and may be used in modeling and circuit simulations. They explain the shape of the output characteristics discussed in Chapter 2.

Transconductance, g_{FS}:

The transconductance or gain of the TMOS power MOSFET is defined as the ratio of the change in drain current and an accompanying small change in applied gate–to–source voltage and is represented by Equation (3).

$$(3)\quad g_{FS} = \frac{\Delta I_{D(sat)}}{\Delta V_{GS}} = \frac{Z}{L}\ \mu Co\ [V_{GS}–V_{GS(th)}]$$

The parameters are the same as above and demonstrate that drain current and transconductance are directly related and are a function of the die design. Note that transconductance is a linear function of the gate voltage, an important feature in amplifier design.

Threshold Voltage, $V_{GS(th)}$

Threshold voltage is the gate–to–source voltage required to achieve surface inversion of the diffused channel region, (r_{CH} in Figure 1–7) and as a result, conduction in the channel.

As the gate voltage increases the more the channel is "enhanced," or the lower its resistance (r_{CH}) is made, the more current will flow. Threshold voltage is measured at a specified value of current to maintain measurement correlations. A value of 1.0 mA is common throughout the industry. This value is primarily a function of the gate oxide thickness and channel doping level which are chosen during the die design to give a high enough value to keep the device off with no bias on the gate at high temperatures. A minimum value of 1.5 volts at room temperature will guarantee the transistor remains an enhancement mode device at junction temperatures up to 150°C.

On–Resistance, $R_{DS(on)}$:

On–resistance is defined as the total resistance encountered by the drain current as it flows from the drain terminal to the source terminal. Referring to Figure 1–7, $R_{DS(on)}$ is composed primarily of four resistive components associated with:

The Inversion channel, r_{CH}; the Gate–Drain Accumulation Region, r_{ACC}; the junction FET Pinch region, r_{JFET}; and the lightly doped Drain Region, r_D, as indicated in Equation (4).

$$(4)\quad R_{DS(on)} = r_{CH} + r_{ACC} + r_{JFET} + r_D$$

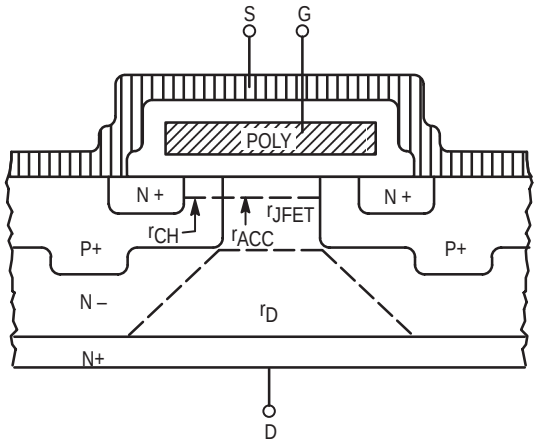


Figure 1–7. TMOS Device On–Resistance

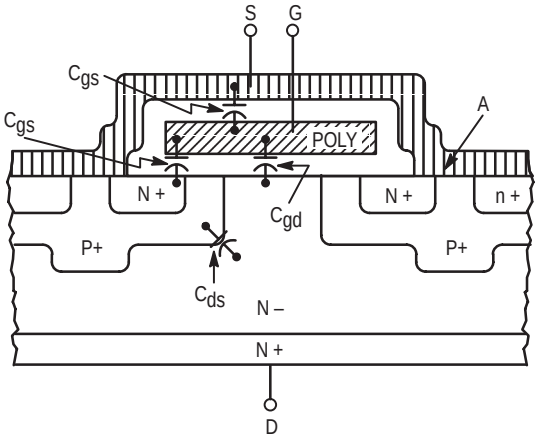


Figure 1–8. TMOS Device Parasitic Capacitances

Whereas the channel resistance increases with channel length, the accumulation resistance increases with poly width and the JFET pinch resistance increases with epi resistivity and all three are inversely proportional to the channel width and gate–to–source voltage. The drain resistance is proportional to the epi resistivity, poly width and inversely proportional to channel width. This says that the on–resistance of TMOS power FETs with the thick and high resistivity epi required for high voltage parts will be dominated by r_D.

Low voltage devices have thin, low resistivity epi and r_{CH} will be a large portion of the total on–resistance. This is why high voltage devices are “full on” with moderate voltages on the gate, whereas with low voltage devices the on–resistance continues to decrease as V_{GS} is increased toward the maximum rating of the device.

Note: $R_{DS(on)}$ is inversely proportional to the carrier mobility. This means that the $R_{DS(on)}$ of the P–Channel MOSFET is approximately 2.5 to 3.0 times that of a similar N–Channel MOSFET. Therefore, in order to have matched complementary on characteristics, the Z/L ratio of the P–Channel device must be 2.5–3.0 times that of the N–Channel device. This means larger die are required for P–Channel MOSFET’s with the same $R_{DS(on)}$ and same breakdown voltage as an N–Channel device and thus device capacitances and costs will be correspondingly higher.

Breakdown Voltage, $V_{(BR)DSS}$:

Breakdown voltage or reverse blocking voltage of the TMOS power MOSFET is defined in the same manner as $V_{(BR)CES}$ in the bipolar transistor and occurs as an avalanche breakdown. This voltage limit is reached when the carriers within the depletion region of the reverse biased P–N junction acquire sufficient kinetic energy to cause ionization or when the critical electric field is reached. The magnitude of this voltage is determined mainly by the characteristics of the lightly doped drain region and the type of termination of the die’s surface electric field.

Figure 1–9 shows a schematic representation of the cross–section in Figure 1–8 and depicts the bipolar transistor built in the epi layer. Point A shows where the emitter and base of the bipolar is shorted together. This is why $V_{(BR)DSS}$ of the power FET is equal to $V_{(BR)CES}$ of the bipolar. Also note the short brings the base in contact with the source metal allowing the use of the base–collector junction. This is the diode across the TMOS power MOSFET.

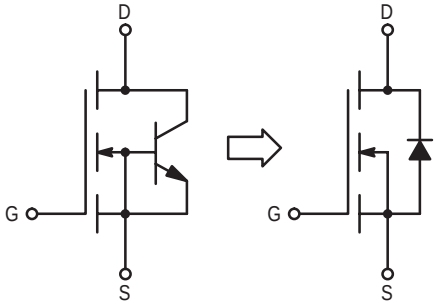


Figure 1–9. Schematic Diagram of all the Components of the Cross Section of Figure 1–7

TMOS Power MOSFET Capacitances:

Two types of intrinsic capacitances occur in the TMOS power MOSFET – those associated with the MOS structure and those associated with the P–N junction.

The two MOS capacitances associated with the MOSFET cell are:

Gate–Source Capacitance, C_{gs}
Gate–Drain Capacitance, C_{gd}

The magnitude of each is determined by the die geometry and the oxides associated with the silicon gate.

The P–N junction formed during fabrication of the power MOSFET results in the drain–to–source capacitance, C_{ds}. This capacitance is defined the same as any other planar junction capacitance and is a direct function of the channel drain area and the width of the reverse biased junction depletion region.

The dielectric insulator of C_{gs} and C_{gd} is basically a glass. Thus these are very stable capacitors and will not vary with voltage or temperature. If excessive voltage is placed on the gate, breakdown will occur through the glass, creating a resistive path and destroying MOSFET operation.

Optimizing TMOS Geometry:

The geometry and packing density of Motorola's MOSFETs vary according to the magnitude of the reverse blocking voltage.

The geometry of the source site, as well as the spacing between source sites, represents important factors in efficient power MOSFET design. Both parameters determine the channel packing density, i.e.: ratio of channel width per cell to cell area.

For low voltage devices, channel width is crucial for minimizing $R_{DS(on)}$, since the major contributing component of $R_{DS(on)}$ is r_{CH}. However, at high voltages, the major contributing component of resistance is r_D and thus minimizing $R_{DS(on)}$ is dependent on maximizing the ratio of active drain area per cell to cell area. These two conditions for minimizing $R_{DS(on)}$ cannot be met by a single geometry pattern for both low and high voltage devices.

Distinct Advantages of Power MOSFETs

Power MOSFETs offer unique characteristics and capabilities that are not available with bipolar power transistors. By taking advantage of these differences, overall systems cost savings can result without sacrificing reliability.

Speed

Power MOSFETs are majority carrier devices, therefore their switching speeds are inherently faster. Without the minority carrier stored base charge common in bipolar transistors, storage time is eliminated. The high switching speeds allow efficient switching at higher frequencies which reduces the cost, size and weight of reactive components.

MOSFET switching speeds are primarily dependent on charging and discharging the device capacitances and are essentially independent of operating temperature.

Input Characteristics

The gate of a power MOSFET is electrically isolated from the source by an oxide layer that represents a dc resistance greater than 40 megohms. The devices are fully biased–on with a gate voltage of 10 volts. This significantly simplifies the drive circuits and in many instances the gate may be driven directly from logic integrated circuits such as CMOS and TTL to control high power circuits directly.

Since the gate is isolated from the source, the drive requirements are nearly independent of the load current. This reduces the complexity of the drive circuit and results in overall system cost reduction.

Safe Operating Area

Power MOSFETs, unlike bipolars, do not require derating of power handling capability as a function of applied voltage. The phenomena of second breakdown does not occur within the ratings of the device. Depending on the application, snubber circuits may be eliminated or a smaller capacitance value may be used in the snubber circuit. The safe operating boundaries are limited by the peak current ratings, breakdown voltages and the power capabilities of the devices.

On–Voltage

The minimum on–voltage of a power MOSFET is determined by the device on–resistance $R_{DS(on)}$. For low voltage devices the value of $R_{DS(on)}$ is extremely low, but with high voltage devices the value increases. $R_{DS(on)}$ has a positive temperature coefficient which aids in paralleling devices.

Examples of Advantages Offered by MOSFETs

High Voltage Flyback Converter

An obvious way of showing the advantages of power MOSFETs over bipolars is to compare the two devices in the same system. Since the drive requirements are not the same, it is not a question of simply replacing the bipolar with the FET, but one of designing the respective drive circuits to produce an equivalent output, as described in Figures 1–10 and 1–11.

For this application, a peak output voltage of about 700 V driving a 30 kΩ load ($P_{O(pk)} \approx 16$ W) was required. With the component values and timing shown, the inductor/device current required to generate this flyback voltage would have to ramp up to about 3.0 A.

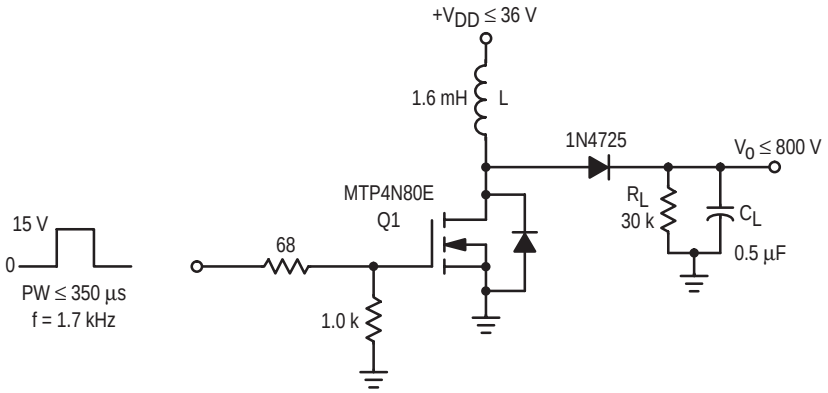


Figure 1–10. TMOS Output Stage

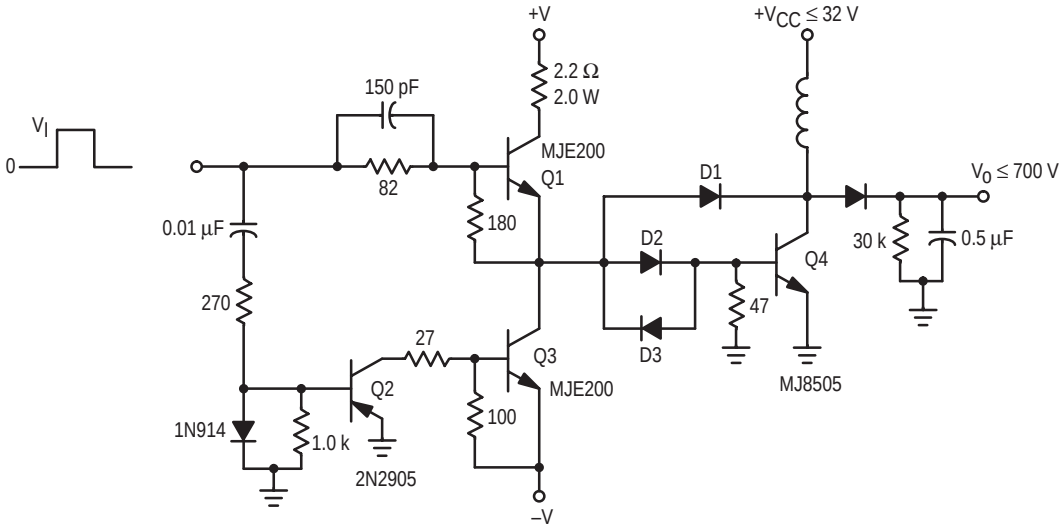


Figure 1–11. Bipolar Driver and Output Stage

Figures 1–10 and 1–11. Circuit Configurations for a TMOS and Bipolar Output Stage of a High Voltage Flyback Converter

Figure 1–10 shows the TMOS version. Because of its high input impedance, the FET, an MTP4N80E, can be directly driven from the pulse width modulator. However, the PWM output should be about 15 volts in amplitude and for relatively fast FET switching be capable of sourcing and sinking 100 mA. Thus, all that is required to drive the FET is a resistor or two. The peak drain current of 3.2 A is within the MTP4N80E pulsed current rating of 18.0 A (4.0 A continuous), and the turn–off load line of 3.2 A, 700 V is well within the Switching SOA (18.0 A/800 V) of the device. Thus, the circuit demonstrates the advantages of TMOS:

- High input impedance
- Fast Switching
- No Second breakdown

Compare this circuit with the bipolar version of Figure 1–11.

To achieve the output voltage, using a high voltage Switchmode MJ8505 power transistor, requires a rather complex drive circuit for generating the proper I_{B1} and I_{B2}. This circuit uses three additional transistors (two of which are power transistors), three Baker clamp diodes, eleven passive components and a negative power supply for generating an off–bias voltage. Also, the RBSOA capability of this device is only 3.0 A at 900 V and 4.7 A at 800 V, values below the 18.0 A/800 V rating of the MOSFET. A detailed description of these circuits is shown in Chapter 8, Switching Power Supplies.

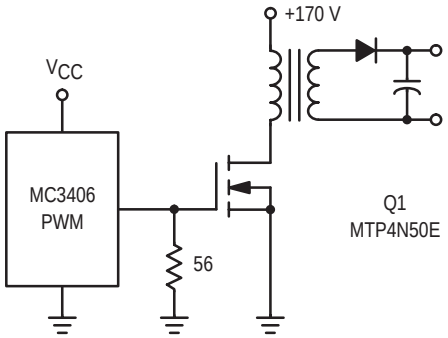


Figure 1–12. TMOS Version

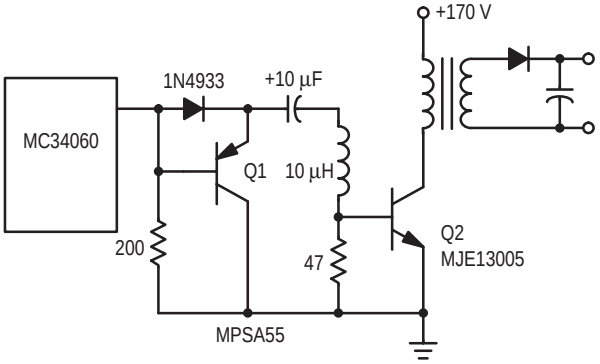


Figure 1–13. Bipolar Version

Figures 1–12 and 1–13. Comparison of Power MOSFET and Bipolar in the Power Output Stage of a 20 kHz Switcher

20 kHz Switcher

An example of MOSFET advantage over bipolar that illustrates its superior switching speed is shown in the power output section of Figures 1–12 and 1–13. In addition to the drive simplicity and reduced component count, the faster switching speed offers better circuit efficiency. For this 35 W switching regulator, using the same small heatsink for either device, a case temperature rise of only 18°C was measured for the MTP4N50E power MOSFET compared to a 46°C rise for the MJE13005 bipolar transistor. Although the saturation losses were greater for the TMOS, its lower switching losses predominated, resulting in a more efficient switching device.

In general, at low switching frequencies, where static losses predominate, bipolars are more efficient. At higher frequencies, above 50 kHz, the power MOSFETs are more efficient.

Chapter 2: Basic Characteristics of Power MOSFETs

Output Characteristics

Perhaps the most direct way to become familiar with the basic operation of a device is to study its output characteristics. In this case, a comparison of the MOSFET characteristics with those of a bipolar transistor with similar ratings is in order, since the curves of a bipolar device are almost universally familiar to power circuit design engineers.

As indicated in Figures 2–1 and 2–2, the output characteristics of the power MOSFET and the bipolar transistor can be divided similarly into two basic regions. The figures also show the numerous and often confusing terms assigned to those regions. To avoid possible confusion, this section will refer to the MOSFET regions as the “on” (or “ohmic”) and “active” regions and bipolar regions as the “saturation” and “active” regions.

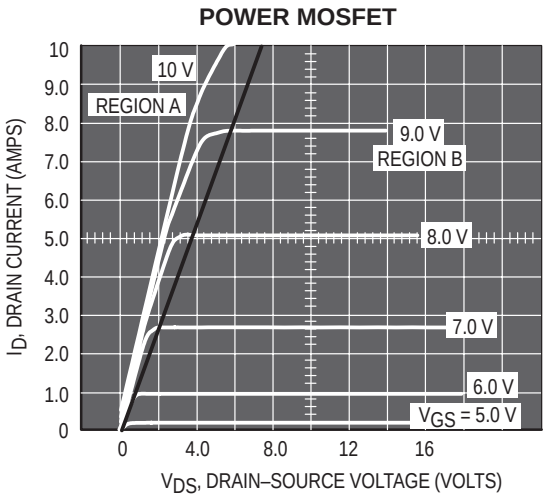


Figure 2–1. I_D–V_{DS} Output Characteristics of a Power MOSFET. Region A is Called the Ohmic, On, Constant Resistance or Linear Region. Region B is Called the Active, Constant Current, or Saturation Region.

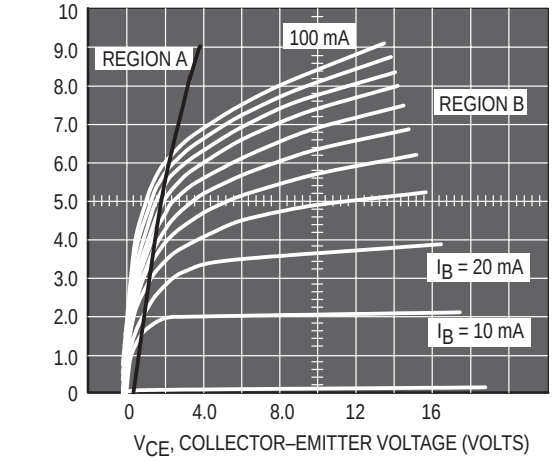


Figure 2–2. I_C–V_{CE} Output Characteristics of a Bipolar Power Transistor. Region A is the Saturation Region. Region B is the Linear or Active Region.

One of the three obvious differences between Figures 2–1 and 2–2 is the family of curves for the power MOSFET is generated by changes in gate voltage and not by base current variations. A second difference is the slope of the curve in the bipolar saturation region is steeper than the slope in the ohmic region of the power MOSFET indicating that the on–resistance of the MOSFET is higher than the effective on–resistance of the bipolar.

The third major difference between the output characteristics is that in the active regions the slope of the bipolar curve is steeper than the slope of the TMOS curve, making the MOSFET a better constant current source. The limiting of I_D is due to pinch–off occurring in the MOSFET channel.

Basic MOSFET Parameters

On–Resistance

The on–resistance, or $R_{DS(on)}$, of a power MOSFET is an important figure of merit because it determines the amount of current the device can handle without excessive power dissipation. When switching the MOSFET from off to on, the drain–source resistance falls from a very high value to $R_{DS(on)}$, which is a relatively low value. To minimize $R_{DS(on)}$ the gate voltage should be large enough for a given drain current to maintain operation in the ohmic region. Data sheets usually include a graph, such as Figure 2–3, which relates this information. As Figure 2–4 indicates, increasing the gate voltage above 12 volts has a diminishing effect on lowering on–resistance (especially in high voltage devices) and increases the possibility of spurious gate–source voltage spikes exceeding the maximum gate voltage rating of 20 volts. Somewhat like driving a bipolar transistor deep into saturation, unnecessarily high gate voltages will increase turn–off time because of the excess charge stored in the input capacitance. All Motorola TMOS FETs will conduct the rated continuous drain current with a gate voltage of 10 volts.

As the drain current rises, especially above the continuous rating, the on–resistance also increases. Another important relationship, which is addressed later with the other temperature dependent parameters, is the effect that temperature has on the on–resistance. Increasing T_J and I_D both effect an increase in $R_{DS(on)}$ as shown in Figure 2–5.

Transconductance

Since the transconductance, or g_{FS}, denotes the gain of the MOSFET, much like beta represents the gain of the bipolar transistor, it is an important parameter when the device is operated in the active, or constant current, region. Defined as the ratio of the change in drain current corresponding to a change in gate voltage ($g_{FS} = dI_D/dV_{GS}$), the transconductance varies with operating conditions as seen in Figure 2–6. The value of g_{FS} is determined from the active portion of the V_{DS}–I_D transfer characteristics where a change in V_{DS} no longer significantly influences g_{FS}. Typically the transconductance rating is specified at half the rated continuous drain current and at a V_{DS} of 15 V.

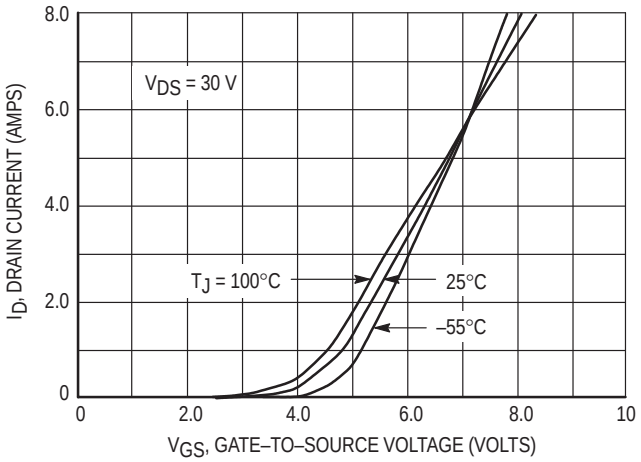


Figure 2–3. Transfer Characteristics

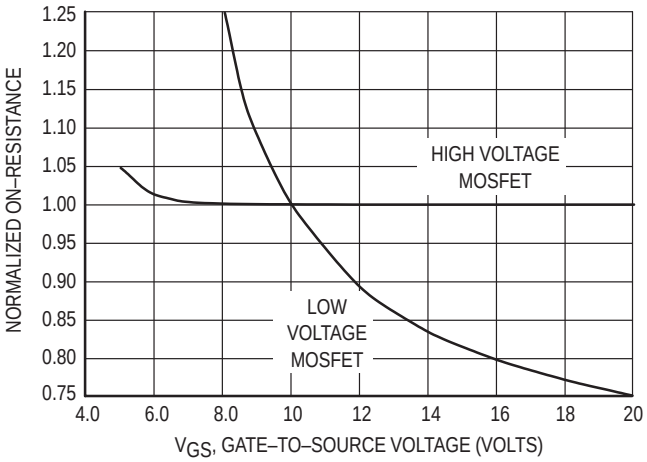


Figure 2–4. The Effect of Gate–to–Source Voltage on On–Resistance Varies with a Device's Voltage Rating

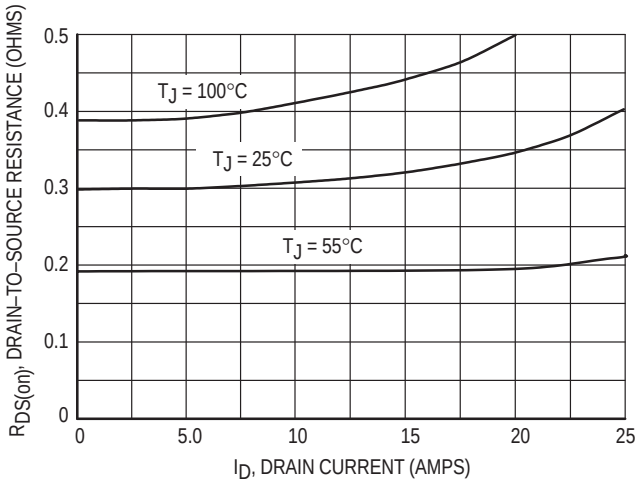


Figure 2–5. Variation of $R_{DS(on)}$ with Drain Current and Temperature

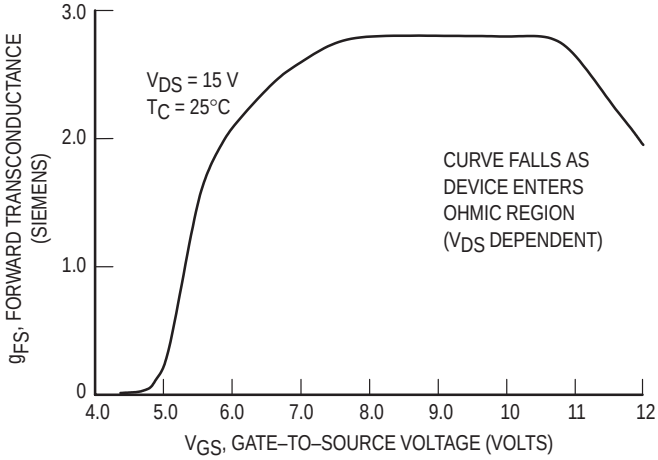


Figure 2–6. Small–Signal Transconductance versus V_{GS}

For designers interested only in switching the power MOSFET between the on and off states, the transconductance is often an unused parameter. Obviously when the device is switched fully on, the transistor will be operating in its ohmic region where the gate voltage will be high. In that region, a change in an already high gate voltage will do little to increase the drain current; therefore, g_{FS} is almost zero.

Threshold Voltage

Threshold Voltage, $V_{GS(th)}$, is the lowest gate voltage at which a specified small amount of drain current begins to flow. Motorola normally specifies $V_{GS(th)}$ at an I_D of one milliampere. Device designers can control the value of the threshold voltage and target $V_{GS(th)}$ to optimize device performance and practicality. A low threshold voltage is desired so the TMOS FET can be controlled by low voltage chips such as CMOS and TTL. A low value also speeds switching because less current needs to be transferred to charge the parasitic input capacitances. But the threshold voltage can be too low if noise can trigger the device. Also, a positive–going voltage transient on the drain can be coupled to the gate by the gate–to–drain parasitic capacitances and can cause spurious turn–on of a device with a low $V_{GS(th)}$.

Temperature Dependent Characteristics $R_{DS(on)}$

Junction temperature variations and their effect on the on–resistance, $R_{DS(on)}$, should be considered when designing with power MOSFETs. Since $R_{DS(on)}$ varies approximately linearly with temperature, power MOSFETs can be assigned temperature coefficients that describe this relationship.

Figure 2–7 shows that the temperature coefficient of $R_{DS(on)}$ is greater for high voltage devices than for low voltage MOSFETs. A graph showing the variation of $R_{DS(on)}$ with junction temperature is shown on most data sheets, Figure 2–5.

Switching Speeds are Constant with Temperature

High junction temperatures emphasize one of the most desirable characteristics of the MOSFET, that of low dynamic or switching losses. In the bipolar transistor, temperature increases will increase switching times, causing greater dynamic losses. On the other hand, thermal variations have little effect on the switching speeds of the power MOSFET. These speeds depend on how rapidly the parasitic input capacitances can be charged and discharged. Since the magnitudes of these capacitances are essentially temperature

invariant, so are the switching speeds. Therefore, as temperature increases, the dynamic losses in a MOSFET are low and remain constant, while in the bipolar transistors the switching losses are higher and increase with junction temperature.

Drain–To–Source Breakdown Voltage

The drain–to–source breakdown voltage is a function of the thickness and resistivity of a device's N–epitaxial region. Since that resistivity varies with temperature, so does $V_{(BR)DSS}$. As Figure 2–8 indicates, a 100°C rise in junction temperature causes a $V_{(BR)DSS}$ to increase by about 10%. However, it should also be remembered that the actual $V_{(BR)DSS}$ falls at the same rate as T_J decreases.

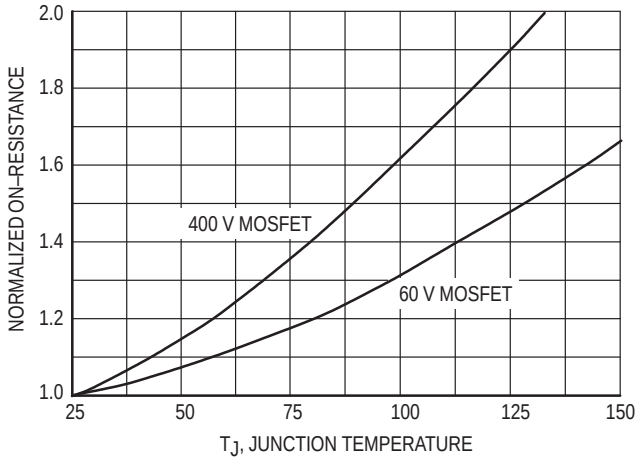


Figure 2–7. The Influence of Junction Temperature on On–Resistance Varies with Breakdown Voltage

Threshold Voltage

The gate voltage at which the MOSFET begins to conduct, the gate–threshold voltage, is temperature dependent. The variation with T_J is linear as shown on most data sheets. Having a negative temperature coefficient, the threshold voltage falls about 10% for each 45°C rise in the junction temperature.

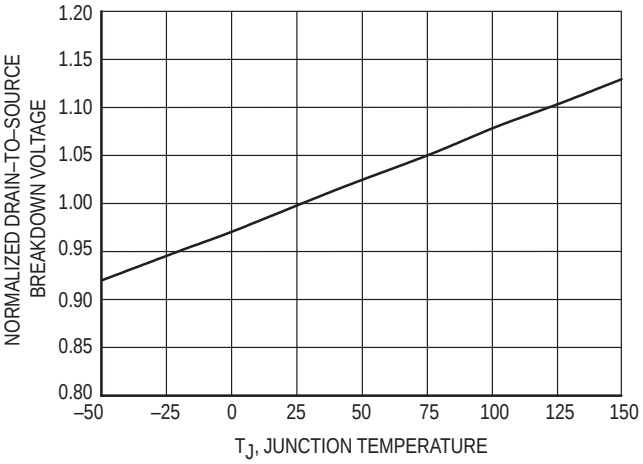


Figure 2–8. Typical Variation of Drain–to–Source Breakdown Voltage with Junction Temperature

Importance of $T_{J(max)}$ and Heat Sinking

Two of the packages that commonly house the TMOS die are the TO–220AB and the TO–204. The power ratings of these packages range from 40 to 250 watts depending on the die size and the type of materials used in construction. These ratings are nearly meaningless, however, unless some heat sinking is provided. Without heat sinking the TO–204 and the TO–220 can dissipate only about 4.0 and 2.0 watts respectively, regardless of the die size.

Because long term reliability decreases with increasing junction temperature, T_J should not exceed the maximum rating of 150°C. Steady–state operation above 150°C also invites abrupt and catastrophic failure if the transistor experiences additional transient thermal stresses. Excluding the possibility of thermal transients, operating below the rated junction temperature can enhance reliability. A $T_{J(max)}$ of 150°C is normally chosen as a safe compromise between long term reliability and maximum power dissipation.

In addition to increasing the reliability, proper heat sinking can reduce static losses in the power MOSFET by decreasing the on–resistance. $R_{DS(on)}$, with its positive temperature coefficient, can vary significantly with the quality of the heat sink. Good heat sinking will decrease the junction temperature, which further decreases $R_{DS(on)}$ and the static losses.

Drain–Source Diode

Inherent in most power MOSFETs, and all TMOS transistors, is a "parasitic" drain–source diode. Figure 2–9, the illustration of cross section of the TMOS die, shows the P–N junction formed by the P–well and the N–Epi layer. Because of its extensive junction area, the current ratings of the diode are the same as the MOSFET's continuous and pulsed current ratings. For the N–Channel TMOS FET shown in Figure 2–10, this diode is forward biased when the source is at a positive potential with respect to the drain. Since the diode may be an important circuit element, Motorola Designer's Data Sheets specify typical values of the forward on–voltage, forward turn–on and reverse recovery time. The forward characteristic of the drain–source diode of a TMOS power MOSFET is shown in Figure 2–11.

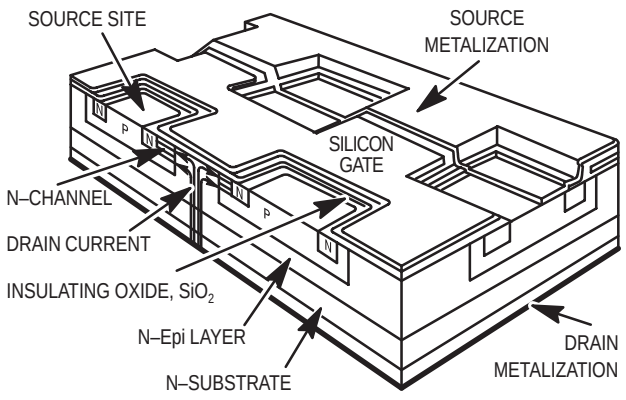


Figure 2–9. Cross Section of TMOS Cell

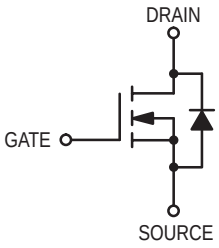


Figure 2–10. N–Channel Power MOSFET Symbol Including Drain–Source Diode

Most rectifiers, a notable exception being the Schottky diode, exhibit a “reverse recovery” characteristic as depicted in Figure 2–12. When forward current flows in a standard diode, a carrier gradient is formed in the high resistivity side of the junction resulting in an apparent storage of charge. Upon sudden application of a reverse bias, the stored charge temporarily produces a negative current flow during the reverse recovery time, or t_{rr}, until the charge is depleted. The circuit conditions that influence t_{rr} and the stored charge are the forward current magnitude and the rate of change of current from the forward current magnitude to the reverse current peak. When tested under the same circuit conditions, the parasitic drain–source diode of a TMOS transistor has a t_{rr} similar to that of a fast recovery rectifier.

In many applications, the drain–source diode is never forward biased and does not influence circuit operation. However, in multi–transistor configurations, such as the totem pole network of Figure 2–13, the parasitic diodes play an important and useful role. Each transistor is protected from excessive flyback voltages, not by its own drain–source diode, but by the diode of the opposite transistor. As an illustration, assume that Q2 of Figure 2–13 is turned on, Q1 is off and current is flowing up from ground, through the load and into Q2. When Q2 turns off, current is diverted into the drain–source diode of Q1 which clamps the load’s inductive kick to V^+. By similar reasoning, one can see that D2 protects Q1 during its turn–off.

As a note of caution, it should be realized that diode recovery problems may arise when using MOSFETs in multiple transistor configurations. A treatment of the subject in Chapter 5 gives greater details.

TMOS power MOSFET intrinsic diodes also have forward recovery times, meaning that they do not instantaneously conduct when they are forward biased. However, since those times are so brief, typically less than 10 ns, their effect on circuit operation can almost always be ignored. Package, lead and wiring inductance are often at least as great a factor in limiting current rise time.

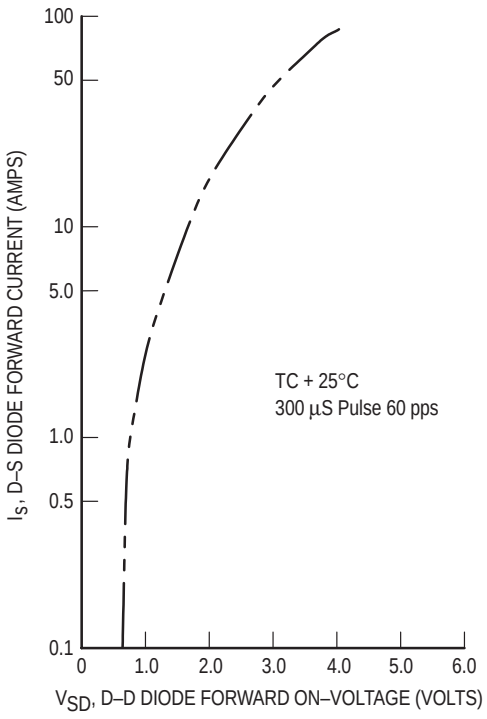


Figure 2–11. Forward Characteristics of Power MOSFETs D–S Diodes

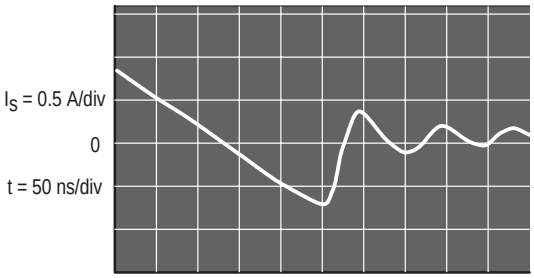


Figure 2–12. Typical Reverse Recovery Characteristics of a Drain–Source Diode

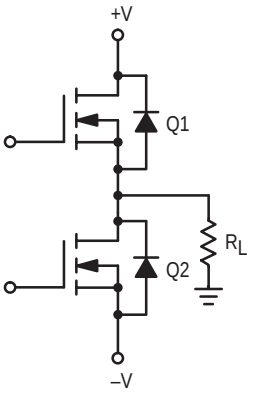


Figure 2–13. TMOS Totem Pole Network with Integral Drain–Source Diodes

Chapter 3: The Data Sheet

Introduction

Motorola prides itself in having one of the most complete and accurate Power MOSFET data sheets in the industry. For consistency, data sheet templates have been established for each technology and or application grouping. This insures that the best approach is used in describing the performance characteristics of each device for the applications they are used in. Additionally, this allows for the automation of the data sheet generation process which has lead to a reduction in new product introduction cycle time as well as providing more accurate and repeatable data.

Headline Information

Motorola's TMOS™ Power MOSFET numbering system contains coded information describing technology, package, current and voltage information. A complete explanation of the nomenclature used is contained in Figure 3–1.

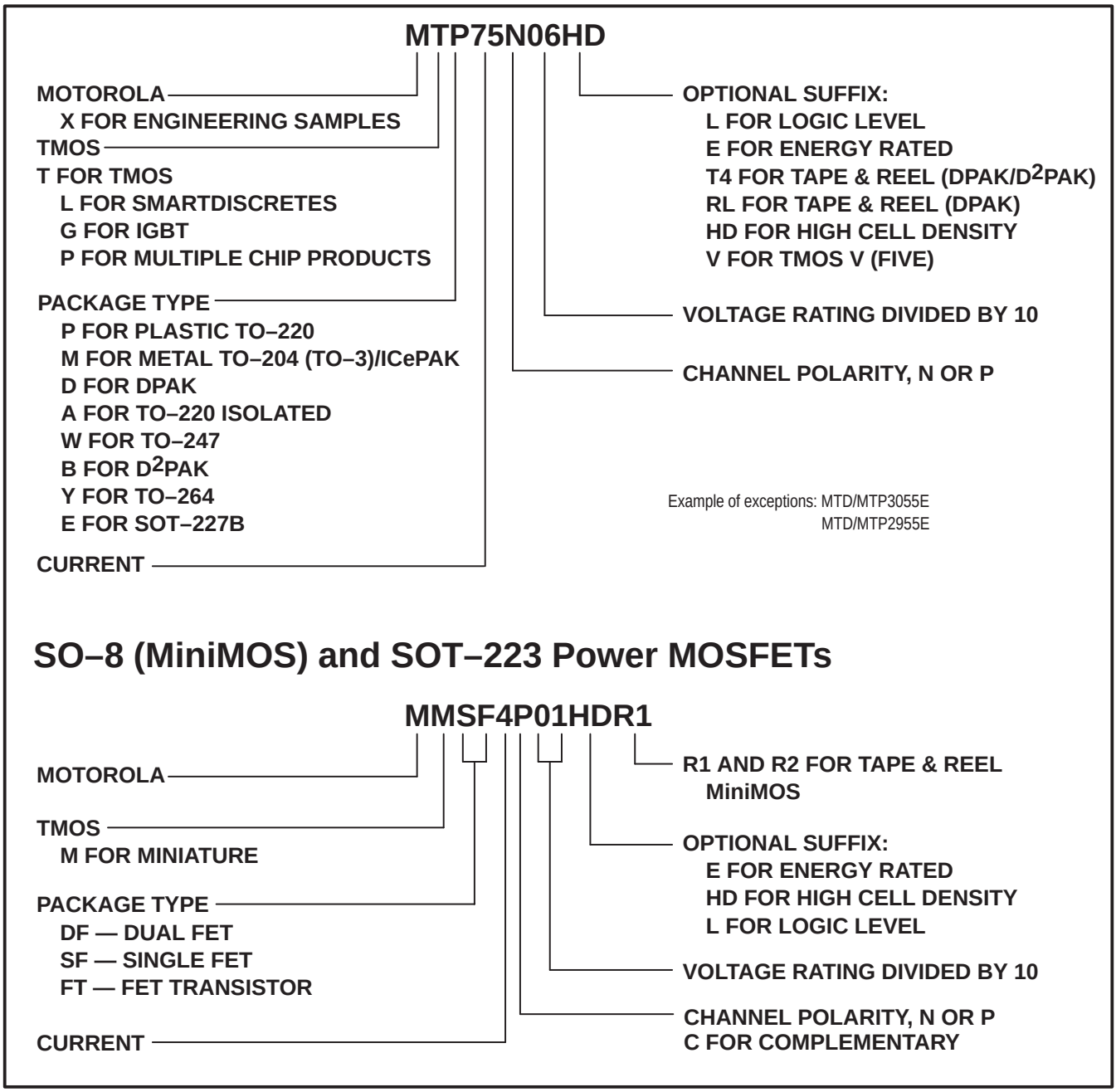


Figure 3–1. TMOS Power MOSFET Numbering System

Absolute Maximum Ratings

Absolute maximum ratings represent the extreme capabilities of the device. They can best be described as device characterization boundaries and are given to facilitate "worst case" design.

Drain–to–Source Voltage (V_{DSS}, V_{DGR}) – This represents the lower limit of the devices blocking voltage capability from drain–to–source when either the gate is shorted to the source (V_{DSS}), or when a 1 MΩ gate–to–source resistor is present (V_{DGR}). It is measured at a specific leakage current and has a positive temperature coefficient. The voltage across the Power MOSFET should never exceed this rating in order to prevent breakdown of the drain–to–source junction.

Maximum Gate–to–Source Voltage (V_{GS}, V_{GSM}) – The maximum allowable gate–to–source voltage as either a continuous condition (V_{GS}), or as a single pulse non–repetitive condition (V_{GSM}). Exceeding this limit may result in permanent device degradation.

Continuous Drain Current (I_D) – The dc current level that will raise the devices junction temperature to it's rated maximum while it's reference temperature is held at 25°C. This can be calculated by the equation:

$$I_D = \text{SQRT}\ (P_D/R_{DS(on)}\ @\ \text{MAX}\ T_J)$$

where,

SQRT = Square root
P_D = Device's maximum power dissipation
$R_{DS(on)}$ = Device's "on" resistance
MAX T_J = Device's maximum rated junction temperature

Pulsed Drain Current (I_{DM}) – The maximum allowable peak drain current the device can safely handle under a 10 μs pulsed condition. This rating takes into consideration the devices thermal limitation as well as $R_{DS(on)}$, wire bond and source metal limitations.

Drain–to–Source Avalanche Energy (EAS) – This specification defines the maximum allowable energy that the device can safely handle in avalanche due to an inductive current spike. It is tested at the I_D of the device as a single pulse non–repetitive condition. This value has a negative temperature coefficient as shown by the "Maximum Avalanche Energy versus Starting Junction Temperature" figure shown in the data sheet. For repetitive avalanche conditions, this value should be derated using the "Thermal Response" figure shown in the data sheet for calculating the junction temperature and the "Maximum Avalanche Energy versus Starting Junction Temperature" figure also shown in the data sheet.

Maximum Power Dissipation (P_D) – Specifies the power dissipation limit which takes the junction temperature to it's maximum rating while the reference temperature is being held at 25°C. It is calculated by the following equation:

$$P_D = (T_J - T_r)/R_{thjr}$$

where,

P_D = Maximum power dissipation
T_J = Maximum allowable junction temperature
T_r = Reference (case and or ambient) temperature
R_{thjr} = Thermal resistance junction–to–reference (case or ambient)

Junction Temperature (T_J) – This value represents the maximum allowable junction temperature of the device. It is derived and based off of long term Reliability data. Exceeding this value will only serve to shorten the device's long term operating life.

Thermal Resistance (R_{thjc}, R_{thja}) – The quantity that resists or impedes the flow of heat energy in a device is called thermal resistance. Thermal resistance values are needed for proper thermal design. These values are measured as detailed in Motorola Application Note AN1083.

Electrical Characteristics

The intent of this section in the data sheet is to provide detailed device characterization so that the designer can predict with a high degree of accuracy the behavior of the device in a specific application.

Drain–to–Source Breakdown Voltage ($V_{(BR)DSS}$) – As described earlier, this represents the lower limit of the devices blocking voltage capability from drain–to–source with the gate shorted to the source. It is measured at a specific leakage current and has a positive temperature coefficient.

Zero Gate Voltage Drain Current (I_{DSS}) – The direct current into the drain terminal of the device when the gate–to–source voltage is zero and the drain terminal is reversed biased with respect to the source terminal. This parameter generally increases with temperature as shown in the "Drain–to–Source Leakage Current versus Voltage" figure found in the device's data sheet.

Gate–Body Leakage Current (I_{GSS}) – The direct current into the gate terminal of the device when the gate terminal is biased with either a positive or negative voltage with respect to the source terminal and the drain terminal is short–circuited to the source terminal.

Gate Threshold Voltage ($V_{GS(th)}$) – The forward gate–to–source voltage at which the magnitude of drain current has been increased to some low threshold value, usually specified as 250 μA or 1 mA. This parameter has a negative temperature coefficient.

Drain–to–Source On–Resistance ($R_{DS(on)}$) – The dc resistance between the drain–to–source terminals with a specified gate–to–source voltage applied to bias the device into the on–state. This parameter has a positive temperature coefficient.

Drain–to–Source On–Voltage ($V_{DS(on)}$) – The dc voltage between the drain–to–source terminals with a specified gate–to–source voltage applied to bias the device into the on–state. This parameter has a positive temperature coefficient.

Forward Transconductance (g_{FS}) – The ratio of the change in drain current due to a change in gate–to–source voltage (i.e., $\Delta I_D/\Delta V_{GS}$).

Device Capacitance (C_{iss}, C_{oss}, C_{rss}) – Power MOSFET devices have internal parasitic capacitance from terminal–to–terminal. This capacitance is voltage dependent as shown by the "Capacitance Variation" figure on the device's data sheet. C_{iss} is the capacitance between the gate–to–source terminals with the drain terminal short–circuited to the source terminal for alternating current. C_{oss} is the capacitance between the drain–to–source terminals with the gate

short–circuited to the source terminal for alternating current. C_{rss} is the capacitance between the drain–to–gate terminals with the source terminal connected to the guard terminal of a three–terminal bridge (Ref. IEEE No. 255). Figures 3–2, 3–3 and 3–4 show test circuits used for Power MOSFET capacitance measurements.

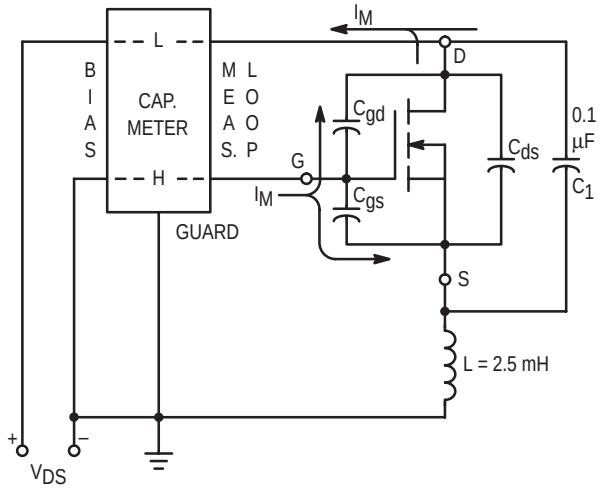


Figure 3–2. C_{iss} Test Configuration

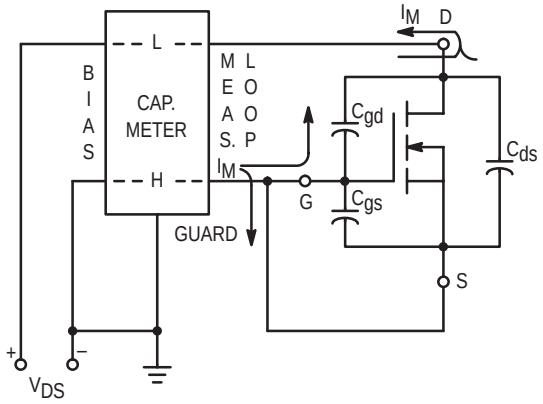


Figure 3–3. C_{oss} Test Configuration

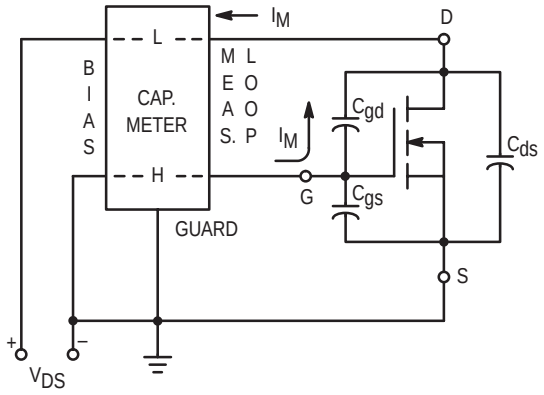


Figure 3–4. C_{rss} Test Configuration

Resistive Switching ($t_{d(on)}$, t_r, $t_{d(off)}$, t_f) – MOSFET switching speeds are very fast, relative to comparably sized bipolar transistors. They are tested and measured using a resistive switching test circuit as shown in Figure 3–5. A typical switching waveform showing parameter measurement points is shown in Figure 3–6.

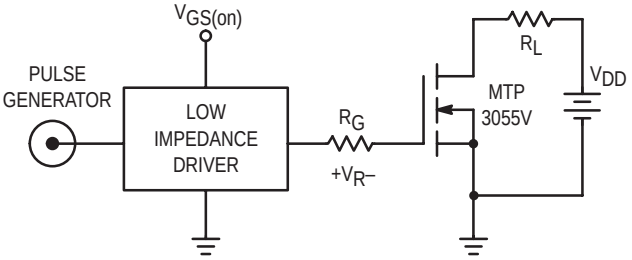


Figure 3–5. Switching Test Circuit

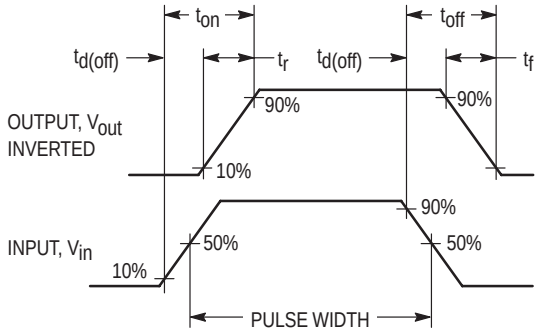


Figure 3–6. Switching Waveforms

Gate Charge (Q_T, Q_1, Q_2) – Gate charge values are used to size the gate drive circuit and to estimate switching speeds and switching losses. Q_T is defined as the total gate charge required to charge the device's input capacitance to the applied gate voltage. Q1 is defined as the charge required to charge the devices input capacitance to the $V_{GS(on)}$ required to maintain the test current I_D. The time required to deliver this charge is called turn–on delay time. Q2 is defined as the charge time required for the drain–to–source voltage to drop to $V_{DS(on)}$.

Forward On–Voltage (V_{SD}) – The dc voltage between the source–to–drain terminals when the power MOSFET's intrinsic body diode is forward biased.

Reverse Recovery Time (t_{rr}, t_a, t_b, Q_{RR}) – The intrinsic body diode of a power MOSFET is a minority carrier device and thus has a finite reverse recovery time. T_a is defined as the time between the dropping I_S current's zero crossing point to the peak I_{RM}. T_b is defined as the time between the peak I_{RM} to a projected I_{RM} zero current crossing point through a 25% I_{RM} projection as shown in Figure 3–7. Total reverse recovery time, t_{rr}, is defined as the sum of t_a and t_b. Q_{RR} is defined as the integral of the area made up by the I_{RM} waveform and V_R, the reapplied blocking voltage which forces reverse recovery.

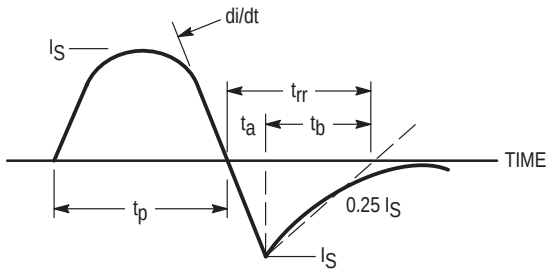


Figure 3–7. Diode Reverse Recovery Waveform

Section Four
Data Sheets

MOTOROLA

MC33153

Advance Information

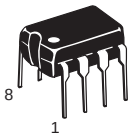
Single IGBT Gate Driver

The MC33153 is specifcally designed as an IGBT driver for high power applications that include ac induction motor control, brushless dc motor control and uninterruptable power supplies. Although designed for driving discrete and module IGBTs, this device offers a cost effective solution for driving power MOSFETs and Bipolar Transistors. Device protection features include the choice of desaturation or overcurrent sensing and undervoltage detection. These devices are available in dual–in–line and surface mount packages and include the following features:

- High Current Output Stage: 1.0 A Source/2.0 A Sink
- Protection Circuits for Both Conventional and Sense IGBT's
- Programmable Fault Blanking Time
- Protection against Overcurrent and Short Circuit
- Undervoltage Lockout Optimzed for IGBT's
- Negative Gate Drive Capability
- Cost Effectively Drives Power MOSFETs and Bipolar Transistors

SINGLE IGBT GATE DRIVER

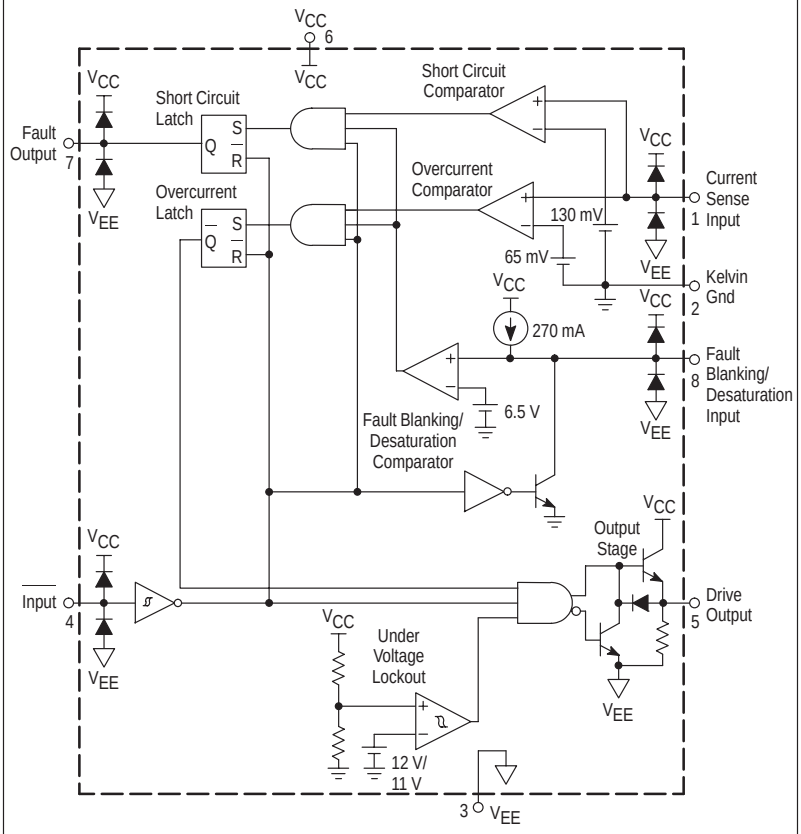
SEMICONDUCTOR TECHNICAL DATA



P SUFFIX
PLASTIC PACKAGE
CASE 626

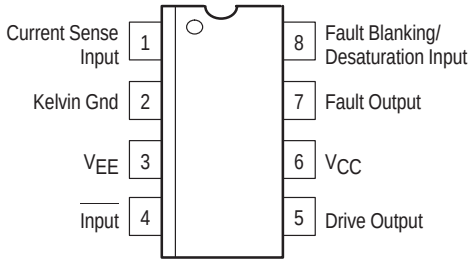
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

Representative Block Diagram



This device contains 133 active transistors.

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC33153D	T_A = –40° to +105°C	SO–8
MC33153P		DIP–8

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage V_{CC} to V_{EE} Kelvin Ground to V_{EE}	 $V_{CC} - V_{EE}$ $KGnd - V_{EE}$	 23 23	V
Logic Input	V_{in}	V_{EE} –0.3 to V_{CC}	V
Current Sense Input	V_S	–0.3 to V_{CC}	V
Blanking/Desaturation Input	V_{BD}	–0.3 to V_{CC}	V
Gate Drive Output Source Current Sink Current Diode Clamp Current	I_O	 1.0 2.0 1.0	A
Fault Output Source Current Sink Curent	I_{FO}	 25 10	mA
Power Dissipation and Thermal Characteristics D Suffix SO–8 Package, Case 751 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air P Suffix DIP–8 Package, Case 626 Maximum Power Dissipation @ T_A = 50°C Thermal Resistance, Junction–to–Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 0.56 180 1.0 100	 W °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature	T_A	–40 to +105	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, V_{EE} = 0 V, Kelvin Gnd connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
LOGIC INPUT					
Input Threshold Voltage High State (Logic 1) Low State (Logic 0)	 V_{IH} V_{IL}	 – 1.2	 2.70 2.30	 3.2 –	V
Input Current High State (V_{IH} = 3.0 V) Low State (V_{IL} = 1.2 V)	 I_{IH} I_{IL}	 – –	 130 50	 500 100	µA
DRIVE OUTPUT					
Output Voltage Low State (I_{Sink} = 1.0 A) High State (I_{Source} = 500 mA)	 V_{OL} V_{OH}	 – 12	 2.0 13.9	 2.5 –	V
Output Pull–Down Resistor	R_{PD}	–	–	200	kΩ
FAULT OUTPUT					
Output voltage Low State (I_{Sink} = 5.0 mA) High State (I_{Source} = 20 mA)	 V_{FL} V_{FH}	 – 12	 0.2 13.3	 1.0 –	V
SWITCHING CHARACTERISTICS					
Propagation Delay (50% Input to 50% Output C_L = 1.0 nF) Logic Input to Drive Output Rise Logic Input to Drive Output Fall	 $t_{PLH(in/out)}$ $t_{PHL (in/out)}$	 – –	 80 120	 300 300	ns
Drive Output Rise Time (10% to 90%) C_L = 1.0 nF	t_r	–	17	55	ns
Drive Output Fall Time (90% to 10%) C_L = 1.0 nF	t_f	–	17	55	ns
Propagation Delay Current Sense Input to Drive Output	 $t_{P(OC)}$	 –	 0.3	 1.0	µs

NOTE: 1. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
T_{low} = –40°C for MC33153 T_{high} = +105°C for MC33153

ELECTRICAL CHARACTERISTICS (continued) (V_{CC} = 15 V, V_{EE} = 0 V, Kelvin Gnd connected to V_{EE}. For typical values T_A = 25°C, for min/max values T_A is the operating ambient temperature range that applies (Note 1), unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (continued)					
Fault Blanking/Desaturation Input to Drive Output	$t_{P(FLT)}$	–	0.3	1.0	
UVLO					
Startup Voltage	$V_{CC\ start}$	–	12	12.6	V
Disable Voltage	$V_{CC\ dis}$	10.4	11	–	V
COMPARATORS					
Overcurrent Threshold Voltage (V_{Pin8} > 7.0 V)	V_{SOC}	50	65	80	mV
Short Circuit Threshold Voltage (V_{Pin8} > 7.0 V)	V_{SSC}	100	130	160	mV
Fault Blanking/Desaturation Threshold (V_{Pin1} > 100 mV)	$V_{th(FLT)}$	6.0	6.5	7.0	V
Current Sense Input Current (V_{SI} = 0 V)	I_{SI}	–	–1.4	–10	µA
FAULT BLANKING/DESATURATION INPUT					
Current Source (V_{Pin8} = 0 V, V_{Pin4} = 0 V)	I_{chg}	–200	–270	–300	µA
Discharge Current (V_{Pin8} = 15 V, V_{Pin4} = 5.0 V)	I_{dschg}	1.0	2.5	–	mA
TOTAL DEVICE					
Power Supply Current	I_{CC}				mA
Standby ($V_{Pin\ 4}$ = V_{CC}, Output Open)		–	7.2	14	
Operating (C_L = 1.0 nF, f = 20 kHz)		–	7.9	20	

NOTE: 1. Low duty cycle pulse techniques are used during test to maintain the junction temperature as close to ambient as possible.
T_{low} = –40°C for MC33153 T_{high} = +105°C for MC33153

Figure 1. Input Current versus Input Voltage

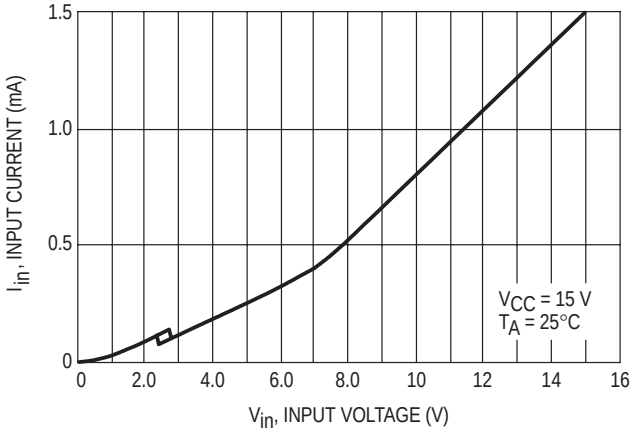


Figure 2. Output Voltage versus Input Voltage

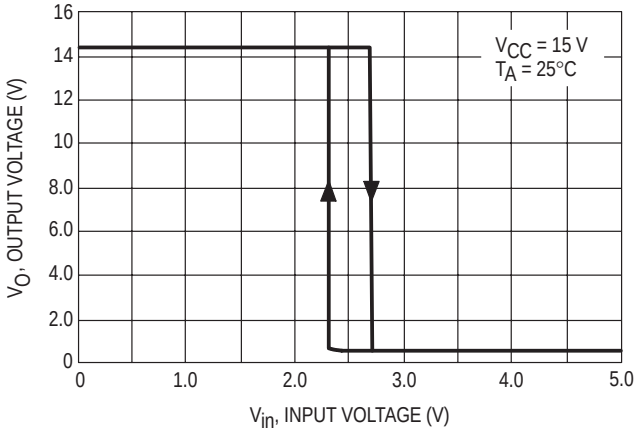


Figure 3. Input Threshold Voltage versus Temperature

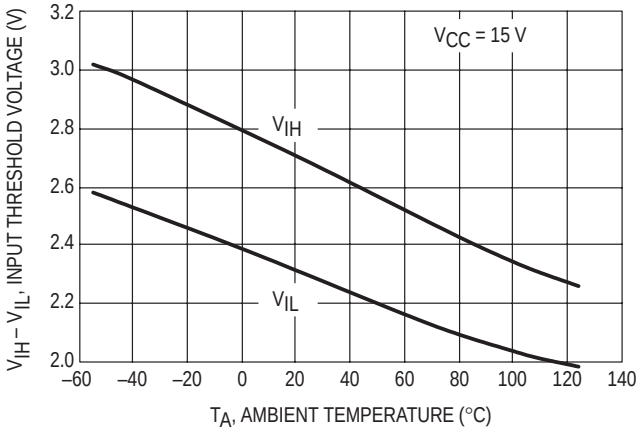


Figure 4. Input Threshold Voltage versus Supply Voltage

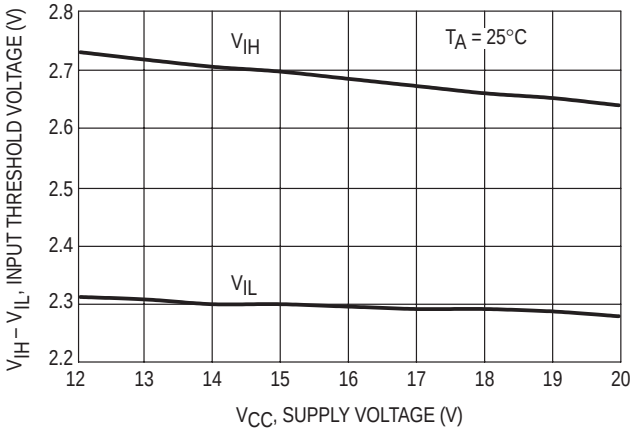


Figure 5. Drive Output Low State Voltage versus Temperature

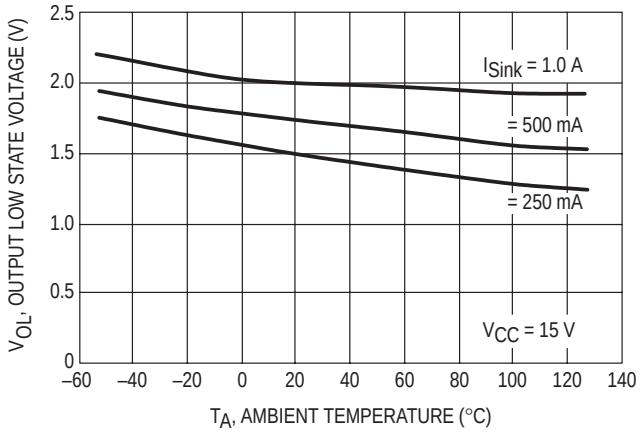


Figure 6. Drive Output Low State Voltage versus Sink Current

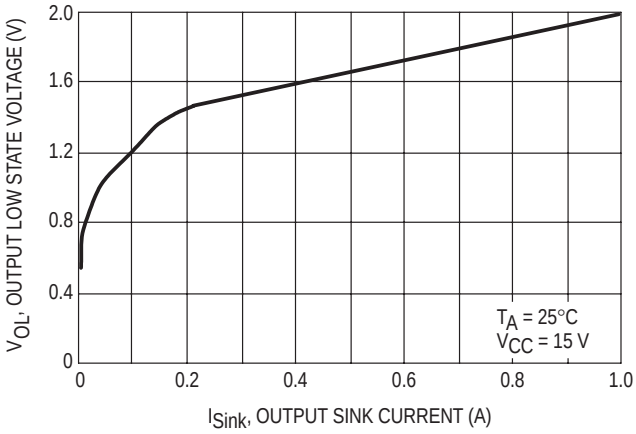


Figure 7. Drive Output High State Voltage versus Temperature

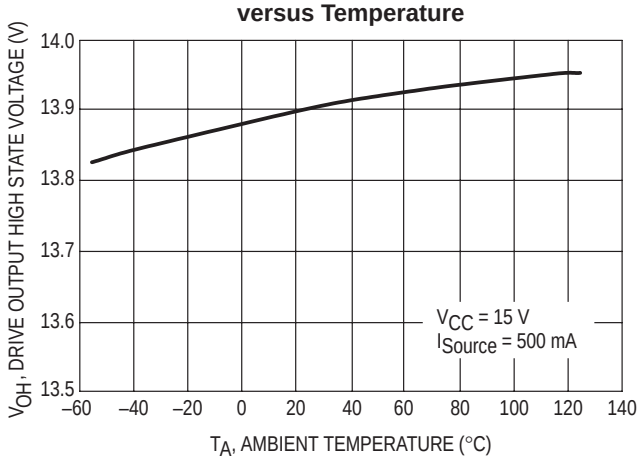


Figure 8. Drive Output High State Voltage versus Source Current

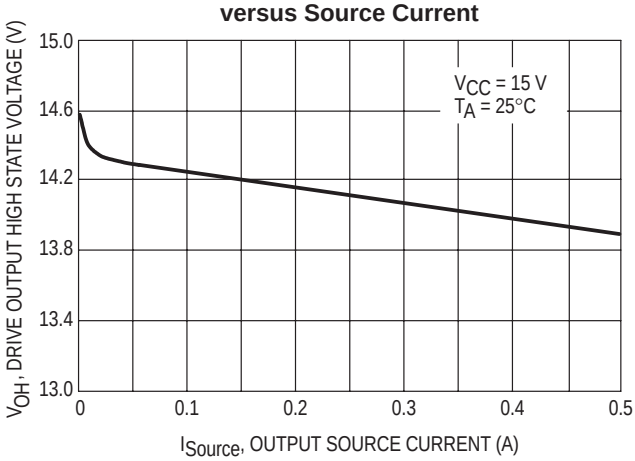


Figure 9. Drive Output Voltage versus Current Sense Input Voltage

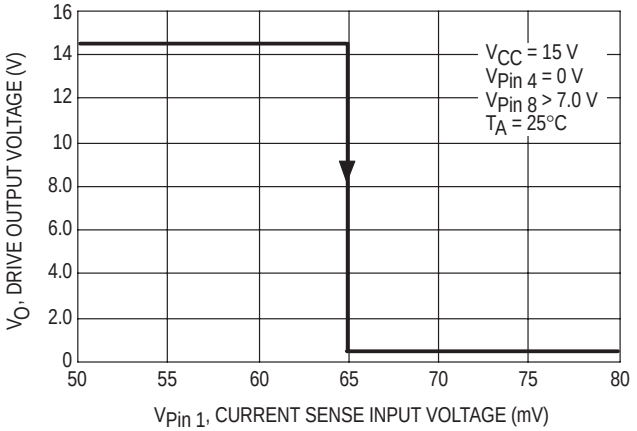


Figure 10. Fault Output Voltage versus Current Sense Input Voltage

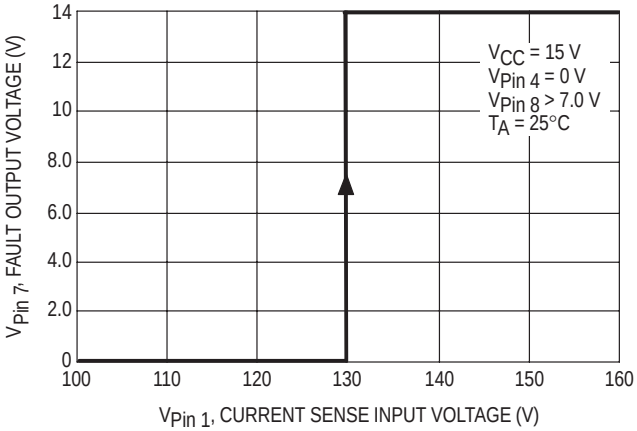


Figure 11. Overcurrent Protection Threshold Voltage versus Temperature

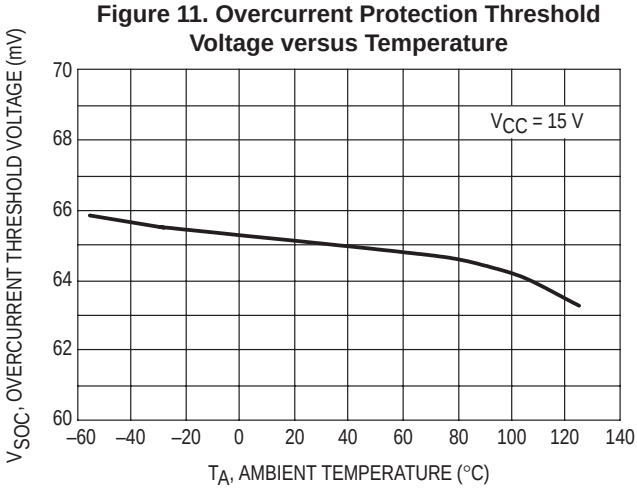


Figure 12. Overcurrent Protection Threshold Voltage versus Supply Voltage

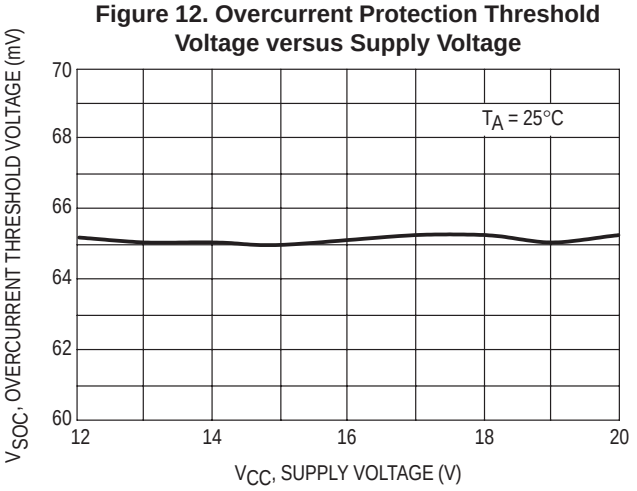


Figure 13. Short Circuit Comparator Threshold Voltage versus Temperature

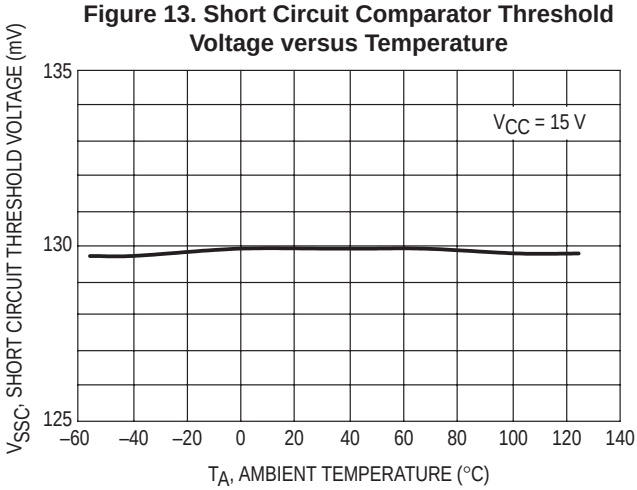


Figure 14. Short Circuit Comparator Threshold Voltage versus Supply Voltage

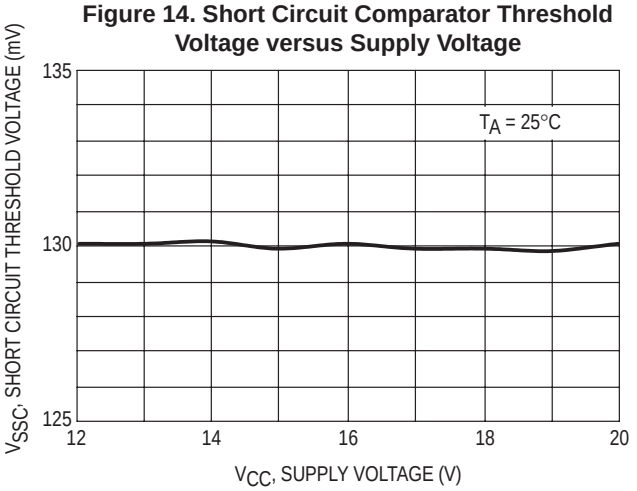


Figure 15. Current Sense Input Current versus Voltage

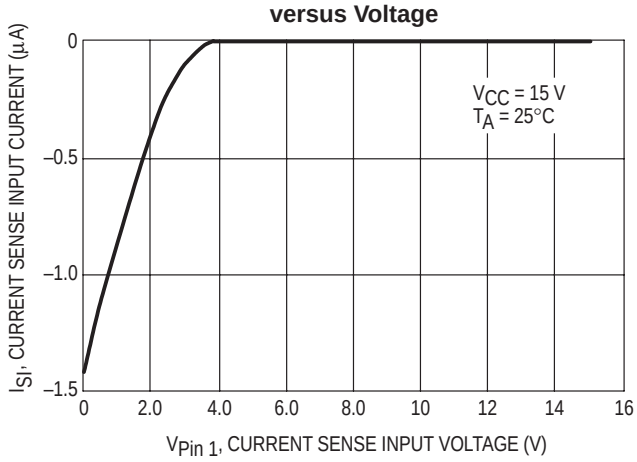


Figure 16. Drive Output Voltage versus Fault Blanking/Desaturation Input Voltage

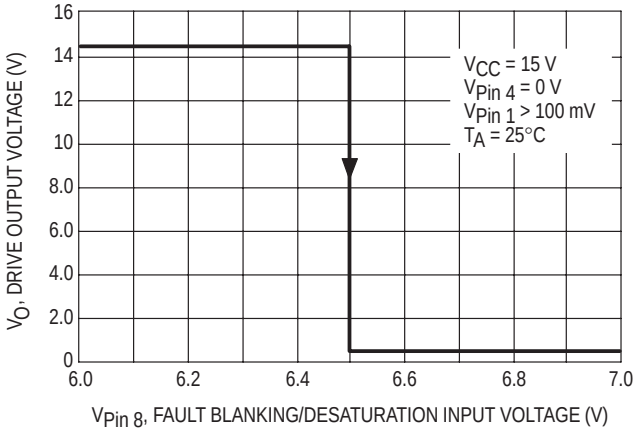


Figure 17. Fault Blanking/Desaturation Comparator Threshold Voltage versus Temperature

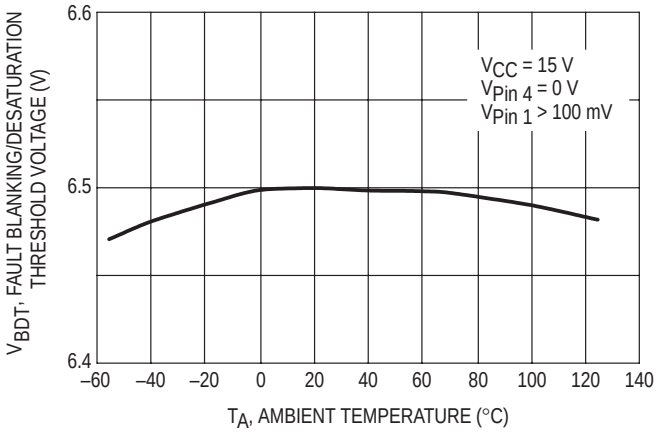


Figure 18. Fault Blanking/Desaturation Comparator Threshold Voltage versus Supply Voltage

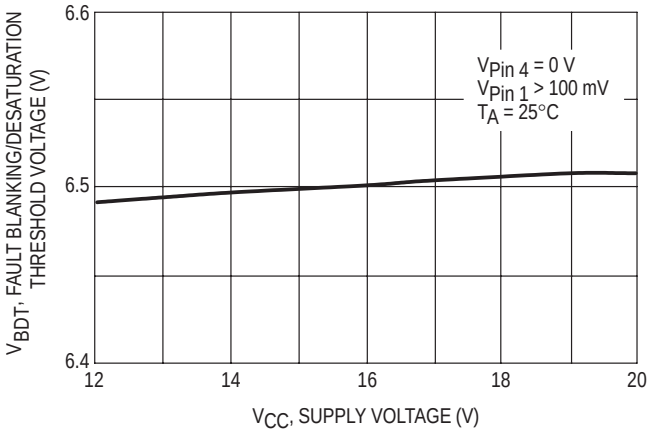


Figure 19. Fault Blanking/Desaturation Current Source versus Temperature

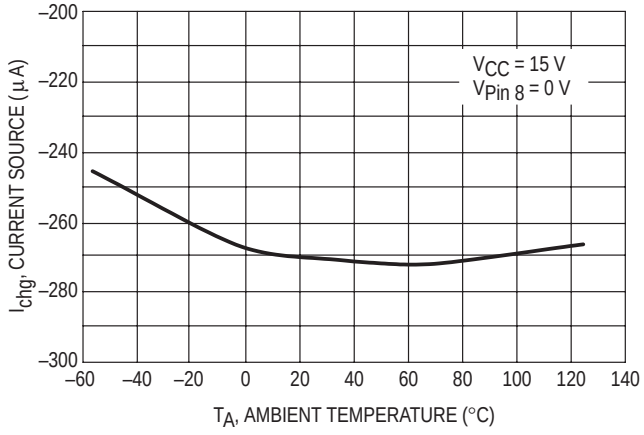


Figure 20. Fault Blanking/Desaturation Current Source versus Supply Voltage

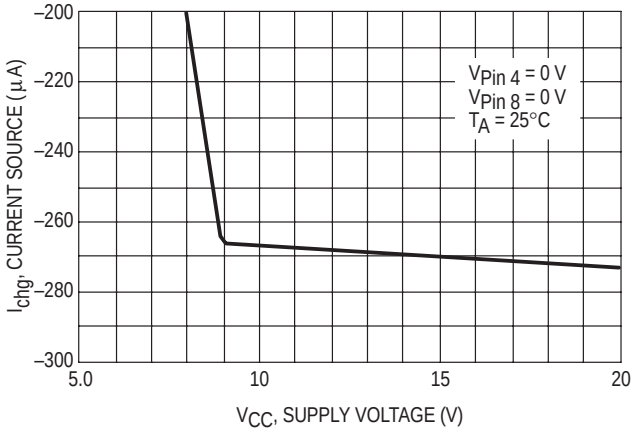


Figure 21. Fault Blanking/Desaturation Current Source versus Input Voltage

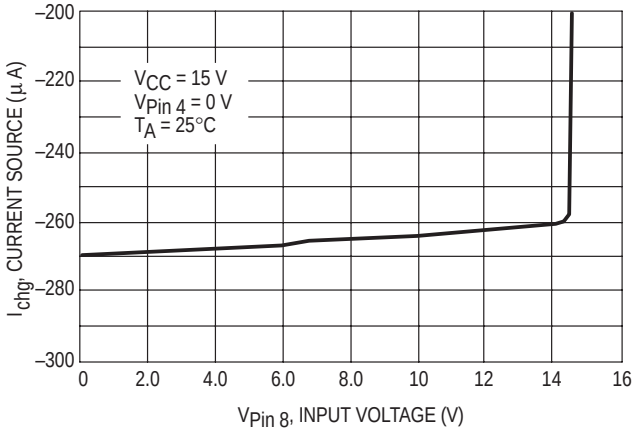


Figure 22. Fault Blanking/Desaturation Discharge Current versus Input Voltage

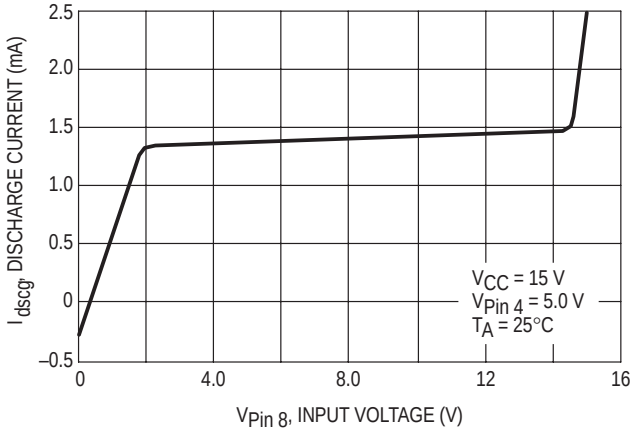


Figure 23. Fault Output Low State Voltage versus Sink Current

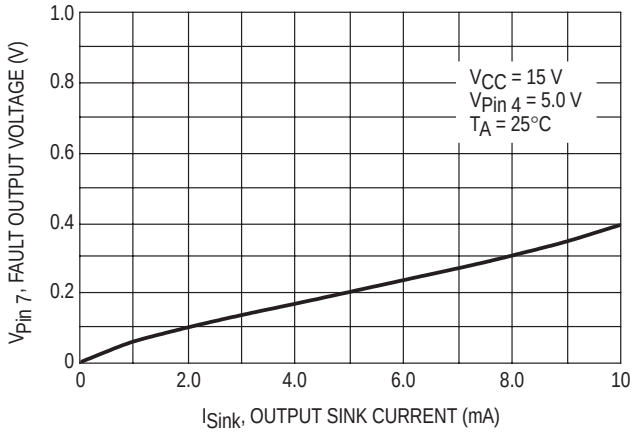


Figure 24. Fault Output High State Voltage versus Source Current

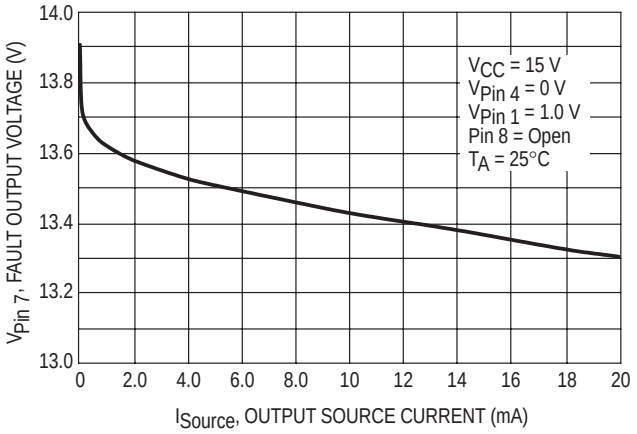


Figure 25. Drive Output Voltage versus Supply Voltage

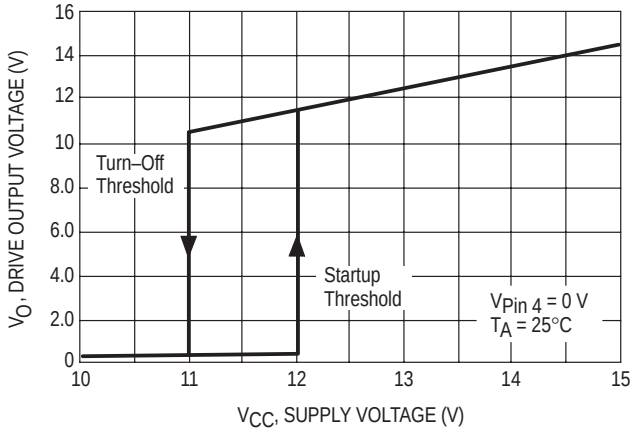


Figure 26. UVLO Thresholds versus Temperature

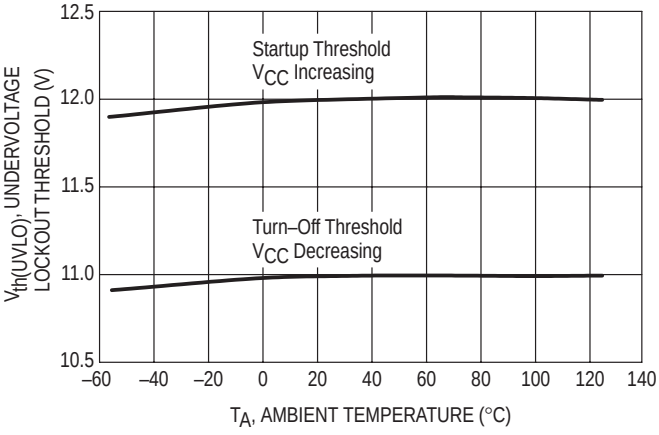


Figure 27. Supply Current versus Supply Voltage

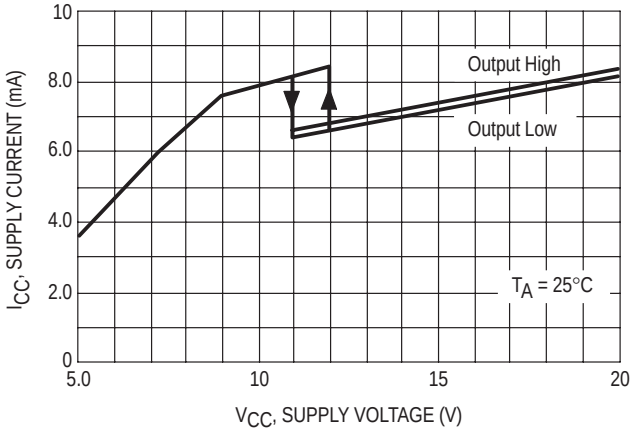


Figure 28. Supply Current versus Temperature

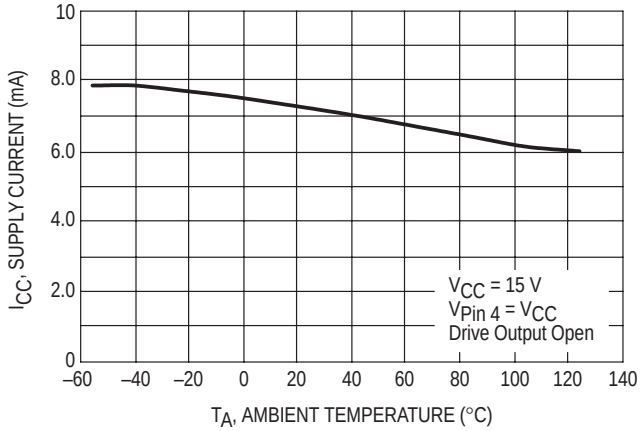
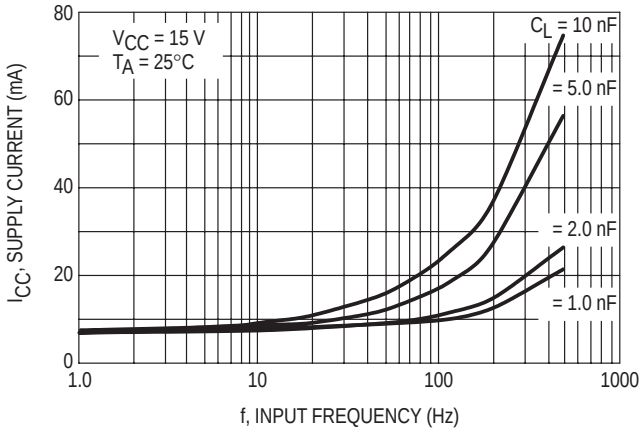


Figure 29. Supply Current versus Input Frequency



OPERATING DESCRIPTION

GATE DRIVE

Controlling Switching Times

The most important design aspect of an IGBT gate drive is optimization of the switching characteristics. The switching characteristics are especially important in motor control applications in which PWM transistors are used in a bridge configuration. In these applications, the gate drive circuit components should be selected to optimize turn–on, turn–off and off–state impedance. A single resistor may be used to control both turn–on and turn–off as shown in Figure 30. However, the resistor value selected must be a compromise in turn–on abruptness and turn–off losses. Using a single resistor is normally suitable only for very low frequency PWM. An optimized gate drive output stage is shown in Figure 31. This circuit allows turn–on and turn–off to be optimized separately. The turn–on resistor, R_{on}, provides control over the IGBT turn–on speed. In motor control circuits, the resistor sets the turn–on di/dt that controls how fast the free–wheel diode is cleared. The interaction of the IGBT and free–wheeling diode determines the turn–on dv/dt. Excessive turn–on dv/dt is a common problem in half–bridge circuits. The turn–off resistor, R_{off}, controls the turn–off speed and ensures that the IGBT remains off under commutation stresses. Turn–off is critical to obtain low switching losses. While IGBTs exhibit a fixed minimum loss due to minority carrier recombination, a slow gate drive will dominate the turn–off losses. This is particularly true for fast IGBTs. It is also possible to turn–off an IGBT too fast. Excessive turn–off speed will result in large overshoot voltages. Normally, the turn–off resistor is a small fraction of the turn–on resistor.

The MC33153 contains a bipolar totem pole output stage that is capable of sourcing 1.0 amp and sinking 2.0 amps peak. This output also contains a pull down resistor to ensure that the IGBT is off whenever there is insufficient V_{CC} to the MC33153.

In a PWM inverter, IGBTs are used in a half–bridge configuration. Thus, at least one device is always off. While the IGBT is in the off–state, it will be subjected to changes in voltage caused by the other devices. This is particularly a problem when the opposite transistor turns on.

When the lower device is turned on, clearing the upper diode, the turn–on dv/dt of the lower device appears across the collector emitter of the upper device. To eliminate shoot–through currents, it is necessary to provide a low sink impedance to the device that is in the off–state. In most applications the turn–off resistor can be made small enough to hold off the device that is under commutation without causing excessively fast turn–off speeds.

Figure 30. Using a Single Gate Resistor

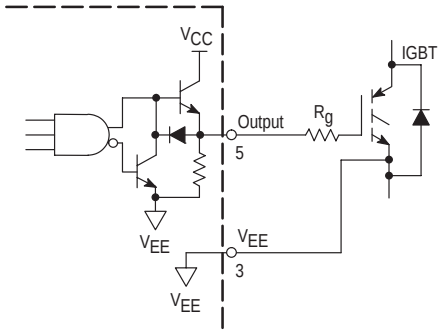
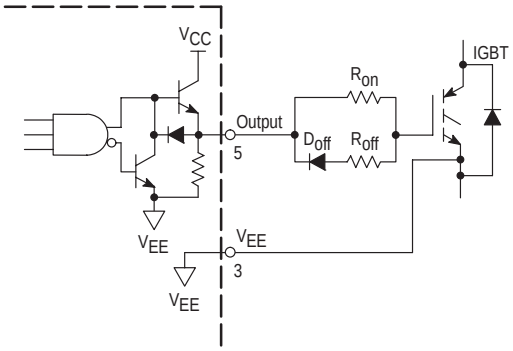


Figure 31. Using Separate Resistors for Turn–On and Turn–Off



A negative bias voltage can be used to drive the IGBT into the off–state. This is a practice carried over from bipolar Darlington drives and is generally not required for IGBTs. However, a negative bias will reduce the possibility of shoot–through. The MC33153 has separate pins for V_{EE} and Kelvin Ground. This permits operation using a +15/–5.0 V supply.

INTERFACING WITH OPTOISOLATORS

Isolated Input

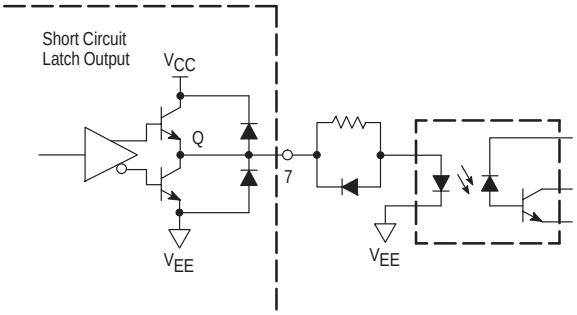
The MC33153 may be used with an optically isolated input. The optoisolator can be used to provide level shifting, and if desired, isolation from ac line voltages. An optoisolator with a very high dv/dt capability should be used, such as the Hewlett Packard HCPL4053. The IGBT gate turn–on resistor should be set large enough to ensure that the opto's dv/dt capability is not exceeded. Like most optoisolators, the HCPL4053 has an active low open–collector output. Thus, when the LED is on, the output will be low. The MC33153 has an inverting input pin to interface directly with an optoisolator using a pull up resistor. The input may also be interfaced directly to 5.0 V CMOS logic or a microcontroller.

Optoisolator Output Fault

The MC33153 has an active high fault output. The fault output may be easily interfaced to an optoisolator. While it is important that all faults are properly reported, it is equally important that no false signals are propagated. Again, a high dv/dt optoisolator should be used.

The LED drive provides a resistor programmable current of 10 to 20 mA when on, and provides a low impedance path when off. An active high output, resistor, and small signal diode provide an excellent LED driver. This circuit is shown in Figure 32.

Figure 32. Output Fault Optoisolator



UNDERVOLTAGE LOCKOUT

It is desirable to protect an IGBT from insufficient gate voltage. IGBTs require 15 V on the gate to achieve the rated on–voltage. At gate voltages below 13 V, the on–voltage increases dramatically, especially at higher currents. At very low gate voltages, below 10 V, the IGBT may operate in the linear region and quickly overheat. Many PWM motor drives use a bootstrap supply for the upper gate drive. The UVLO provides protection for the IGBT in case the bootstrap capacitor discharges.

The MC33153 will typically start up at about 12 V. The UVLO circuit has about 1.0 V of hysteresis and will disable the output if the supply voltage falls below about 11V.

PROTECTION CIRCUITRY

Desaturation Protection

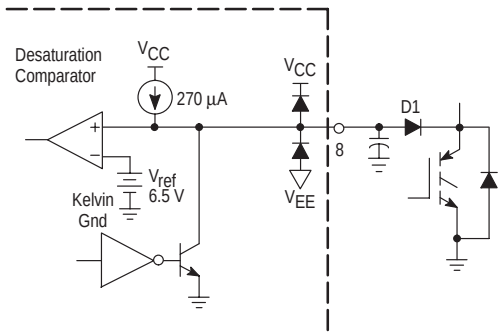
Bipolar Power circuits have commonly used what is known as “Desaturation Detection”. This involves monitoring the collector voltage and turning off the device if this voltage rises above a certain limit. A bipolar transistor will only conduct a certain amount of current for a given base drive. When the base is overdriven, the device is in saturation. When the collector current rises above the knee, the device pulls out of saturation. The maximum current the device will conduct in the linear region is a function of the base current and the dc current gain (h_{FE}) of the transistor.

The output characteristics of an IGBT are similar to a Bipolar device. However, the output current is a function of gate voltage instead of current. The maximum current depends on the gate voltage and the device type. IGBTs tend to have a very high transconductance and a much higher current density under a short circuit than a bipolar device. Motor control IGBTs are designed for a lower current density under shorted conditions and a longer short circuit survival time.

The best method for detecting desaturation is the use of a high voltage clamp diode and a comparator. The MC33153 has a Fault Blanking/Desaturation Comparator which senses the collector voltage and provides an output indicating when the device is not fully saturated. Diode D1 is an external high voltage diode with a rated voltage comparable to the power device. When the IGBT is “on” and saturated, D1 will pull down the voltage on the Fault Blanking/Desaturation Input. When the IGBT pulls out of saturation or is “off”, the current source will pull up the input and trip the comparator. The comparator threshold is 6.5 V, allowing a maximum on–voltage of about 5.8 V.

A fault exists when the gate input is high and V_{CE} is greater than the maximum allowable $V_{CE(sat)}$. The output of the Desaturation Comparator is ANDed with the gate input signal and fed into the Short Circuit and Overcurrent Latches. The Overcurrent Latch will turn–off the IGBT for the remainder of the cycle when a fault is detected. When input goes high, both latches are reset. The reference voltage is tied to the Kelvin Ground instead of the V_{EE} to make the threshold independent of negative gate bias. Note that for proper operation of the Desaturation Comparator and the Fault Output, the Current Sense Input must be biased above the Overcurrent and Short Circuit Comparator thresholds. This can be accomplished by connecting Pin 1 to V_{CC}.

Figure 33. Desaturation Detection



The MC33153 also features a programmable fault blanking time. During turn–on, the IGBT must clear the opposing free–wheeling diode. The collector voltage will remain high until the diode is cleared. Once the diode has been cleared, the voltage will come down quickly to the $V_{CE(sat)}$ of the device. Following turn–on, there is normally considerable ringing on the collector due to the C_{OSS} capacitance of the IGBTs and the parasitic wiring inductance. The fault signal from the Desaturation Comparator must be blanked sufficiently to allow the diode to be cleared and the ringing to settle out.

The blanking function uses an NPN transistor to clamp the comparator input when the gate input is low. When the input is switched high, the clamp transistor will turn “off”, allowing the internal current source to charge the blanking capacitor. The time required for the blanking capacitor to charge up from the on–voltage of the internal NPN transistor to the trip voltage of the comparator is the blanking time.

If a short circuit occurs after the IGBT is turned on and saturated, the delay time will be the time required for the current source to charge up the blanking capacitor from the $V_{CE(sat)}$ level of the IGBT to the trip voltage of the comparator. Fault blanking can be disabled by leaving Pin 8 unconnected.

Sense IGBT Protection

Another approach to protecting the IGBTs is to sense the emitter current using a current shunt or Sense IGBTs. This method has the advantage of being able to use high gain IGBTs which do not have any inherent short circuit capability. Current sense IGBTs work as well as current sense MOSFETs in most circumstances. However, the basic problem of working with very low sense voltages still exists. Sense IGBTs sense current through the channel and are therefore linear with respect to the collector current. Because IGBTs have a very low incremental on–resistance, sense IGBTs behave much like low–on resistance current sense MOSFETs. The output voltage of a properly terminated sense IGBT is very low, normally less than 100 mV.

The sense IGBT approach requires fault blanking to prevent false tripping during turn–on. The sense IGBT also requires that the sense signal is ignored while the gate is low. This is because the mirror output normally produces large transient voltages during both turn–on and turn–off due to the collector to mirror capacitance. With non–sensing types of IGBTs, a low resistance current shunt (5.0 to 50 mΩ) can be used to sense the emitter current. When the output is an actual short circuit, the inductance will be very low. Since the blanking circuit provides a fixed minimum on–time, the peak current under a short circuit can be very high. A short circuit discern function is implemented by the second comparator which has a higher trip voltage. The short circuit signal is latched and appears at the Fault Output. When a short circuit is detected, the IGBT should be turned–off for several milliseconds allowing it to cool down before it is turned back on. The sense circuit is very similar to the desaturation circuit. It is possible to build a combination circuit that provides protection for both Short Circuit capable IGBTs and Sense IGBTs.

APPLICATION INFORMATION

Figure 34 shows a basic IGBT driver application. When driven from an optoisolator, an input pull up resistor is required. This resistor value should be set to bias the output transistor at the desired current. A decoupling capacitor should be placed close to the IC to minimize switching noise.

A bootstrap diode may be used for a floating supply. If the protection features are not required, then both the Fault Blanking/Desaturation and Current Sense Inputs should both be connected to the Kelvin Ground (Pin 2). When used with a single supply, the Kelvin Ground and V_{EE} pins should be connected together. Separate gate resistors are recommended to optimize the turn–on and turn–off drive.

Figure 34. Basic Application

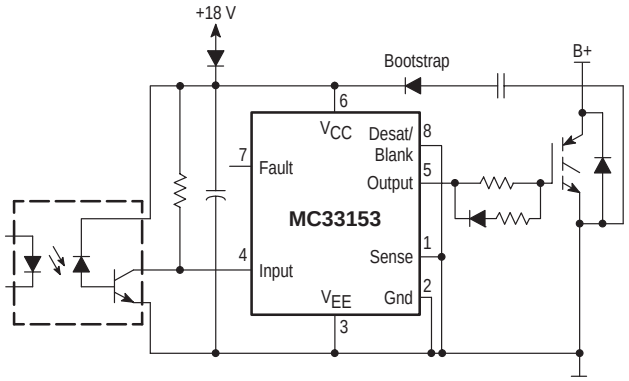
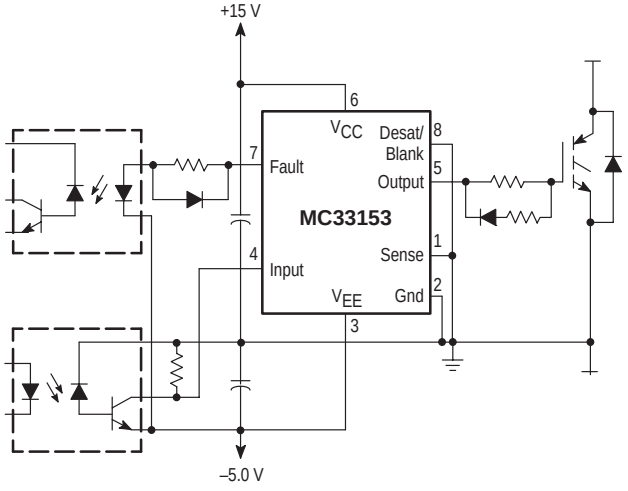


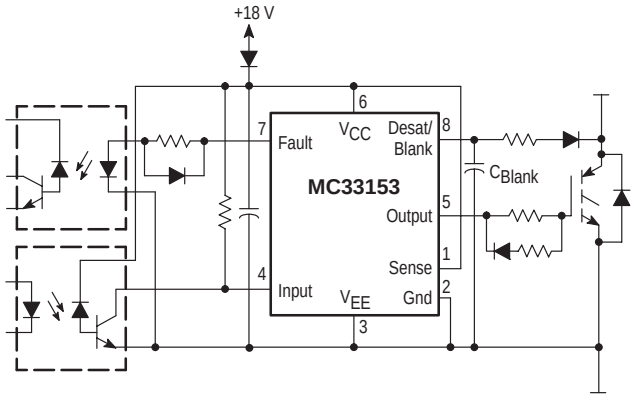
Figure 35. Dual Supply Application



When used in a dual supply application as in Figure 35, the Kelvin Ground should be connected to the emitter of the IGBT. If the protection features are not used, then both the Fault Blanking/Desaturation and the Current Sense Inputs should be connected to Ground. The input optoisolator should always be referenced to V_{EE}.

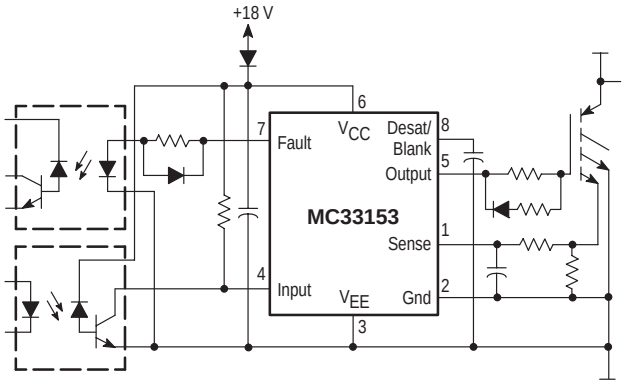
If desaturation protection is desired, a high voltage diode is connected to the Fault Blanking/Desaturation pin. The blanking capacitor should be connected from the Desaturation pin to the V_{EE} pin. If a dual supply is used, the blanking capacitor should be connected to the Kelvin Ground. The Current Sense Input should be tied high because the two comparator outputs are ANDed together. Although the reverse voltage on collector of the IGBT is clamped to the emitter by the free–wheeling diode, there is normally considerable inductance within the package itself. A small resistor in series with the diode can be used to protect the IC from reverse voltage transients.

Figure 36. Desaturation Application



When using sense IGBTs or a sense resistor, the sense voltage is applied to the Current Sense Input. The sense trip voltages are referenced to the Kelvin Ground pin. The sense voltage is very small, typically about 65 mV, and sensitive to noise. Therefore, the sense and ground return conductors should be routed as a differential pair. An RC filter is useful in filtering any high frequency noise. A blanking capacitor is connected from the blanking pin to V_{EE}. The stray capacitance on the blanking pin provides a very small level of blanking if left open. The blanking pin should not be grounded when using current sensing, that would disable the sense. The blanking pin should never be tied high, that would short out the clamp transistor.

Figure 37. Sense IGBT Application



Product Preview

SMARTDISCRETES™ Internally Clamped, N-Channel IGBT

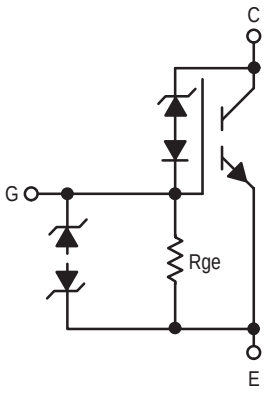
MGP20N14CL

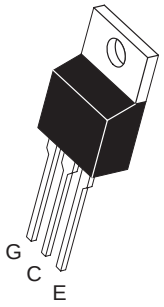
20 AMPERES
VOLTAGE CLAMPED
N–CHANNEL IGBT
$V_{ce(on)}$ = 1.9 VOLTS
135 VOLTS (CLAMPED)

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

- Temperature Compensated Gate–Drain Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- High Pulsed Current Capability

TMOS®





CASE 221A–06, Style 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CGR}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous @ T_C = 25°C — Single Pulsed (t_p = ±10 μs)	I_C I_{CM}	20 60	Adc Apk
Total Power Dissipation @ T_C = 25°C (TO–220) Derate Above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Collector–Emitter Avalanche Energy @ Starting T_J = 25°C (V_{CC} = 80 V, V_{GE} = 5 V, Peak I_L = 10 A, L = 10 mH)	E_{AS}	500	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO–220) — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Clamp Voltage (I_{Clamp} = 10 mA, T_J = –40 to 150°C)		B_{VCES}	135			Vdc
Zero Gate Voltage Collector Current (V_{CE} = 100 V, V_{GE} = 0 V) (V_{CE} = 100 V, V_{GE} = 0 V, T_J = 150°C)		I_{CES}	— —	— —	10 100	μA
Gate–Emitter Clamp Voltage (I_G = 1 mA)		B_{VGES}	10			Vdc
Gate–Emitter Leakage Current (V_{GE} = ±5 V, V_{CE} = 0 V)		I_{GES}	—	—	1.0	μA
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mA) Threshold Temperature Coefficient (Negative)		$V_{CE(th)}$	1.0	1.5 4.4	2.0	V mV/°C
Collector–Emitter On–Voltage (V_{GE} = 5 V, I_C = 10 A) (V_{GE} = 5 V, I_C = 10 Adc, T_J = 175°C)		$V_{CE(on)}$	— —		1.9 1.8	V
Forward Transconductance (V_{CE} > 15 V, I_C = 10 A)		g_{fs}	8.0	15	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	430	600	pF
Output Capacitance		C_{oss}	—	182	250	
Transfer Capacitance		C_{rss}	—	48	100	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 68 V, I_C = 20 A, V_{GE} = 5 V, R_G = 9.1 Ω)	$t_{d(on)}$	—	TBD	TBD	ns
Rise Time		t_r	—	TBD	TBD	
Turn–Off Delay Time		$t_{d(off)}$	—	TBD	TBD	
Fall Time		t_f	—	TBD	TBD	
Total Gate Charge	(V_{CC} = 108 V, I_C = 20 A, V_{GE} = 5 V)	Q_g	—	14	20	nC
Gate–Emitter Charge		Q_{gs}	—	3.0	—	
Gate–Collector Charge		Q_{gd}	—	6.0	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

Advanced Information

SMARTDISCRETES™ Internally Clamped, N-Channel IGBT

MGP20N35CL

20 AMPERES
VOLTAGE CLAMPED
N–CHANNEL IGBT
$V_{ce(on)}$ = 1.8 VOLTS
350 VOLTS (CLAMPED)

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

- Temperature Compensated Gate–Drain Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- High Pulsed Current Capability

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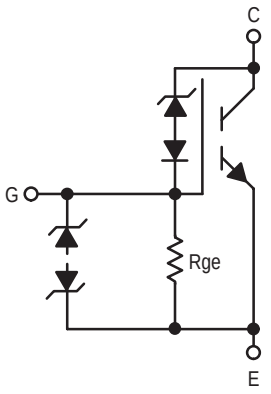

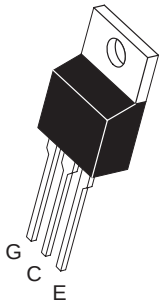

CASE 221A–06, Style 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CGR}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous @ T_C = 25°C	I_C	20	Adc
Reversed Collector Current – pulse width < 100 μs	I_{CR}	12	Apk
Total Power Dissipation @ T_C = 25°C (TO–220)	P_D	150	Watts
Electrostatic Voltage — Gate–Emitter	ESD	3.5	kV
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO–220) — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

UNCLAMPED INDUCTIVE SWITCHING CHARACTERISTICS

Single Pulse Collector–Emitter Avalanche Energy @ Starting T_J = 25°C @ Starting T_J = 150°C	E_{AS}	 550 150	mJ

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–to–Emitter Breakdown Voltage (I_{Clamp} = 10 mA, T_J = –40 to 150°C)	B_{VCES}	320	350	380	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 250 V, V_{GE} = 0 V, T_J = 125°C)	I_{CES}	—	—	1.0	mA
(V_{CE} = 15 V, V_{GE} = 0 V, T_J = 125°C)		—	—	200	μA
Resistance Gate–Emitter (T_J = –40 to 150°C)	R_{GE}	10k	16k	30k	Ω
Gate–Emitter Breakdown Voltage (I_G = 2 mA)	B_{VGES}	11	13	15	±V
Collector–Emitter Reverse Leakage (V_{CE} = –15 V, T_J = –40 to 150°C)	I_{CES}	—	8	100	mA
Collector–Emitter Reversed Breakdown Voltage (I_E = 75 mA)	B_{VCER}	26	40	120	V
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mA)	$V_{GE(th)}$	1.0	1.7	2.4	V
(V_{CE} = V_{GE}, I_C = 1 mA, T_J = 150°C)		0.75	—	1.8	
Collector–Emitter On–Voltage (V_{GE} = 5 V, I_C = 5 A)	$V_{CE(on)}$	—	1.1	1.4	V
(V_{GE} = 5 V, I_C = 10 A)		—	1.4	1.9	
(V_{GE} = 5 V, I_C = 10 Adc, T_J = 150°C)		—	1.4	1.8	
Forward Transconductance (V_{CE} > 50 V, I_C = 10 A)	g_{fs}	10	16	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	—	2800	—	pF
Output Capacitance (V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{oss}	—	200	—	
Transfer Capacitance	C_{rss}	—	25	—	
SWITCHING CHARACTERISTICS (1)					
Total Gate Charge	Q_g	—	45	80	nC
Gate–Emitter Charge (V_{CC} = 280 V, I_C = 20 A, V_{GE} = 5 V)	Q_{gs}	—	8.0	—	
Gate–Collector Charge	Q_{gd}	—	20	—	
Turn–Off Delay Time	$t_{d(off)}$	—	TBD	TBD	μs
Fall Time (V_{CC} = 320 V, I_C = 20 A, L = 200 μH, R_G = 1 KΩ)	t_f	—	TBD	TBD	
Turn–On Delay Time	$t_{d(on)}$	—	TBD	TBD	μs
Rise Time (V_{CC} = 14 V, I_C = 20 A, L = 200 μH, R_G = 1 KΩ)	t_r	—	TBD	TBD	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

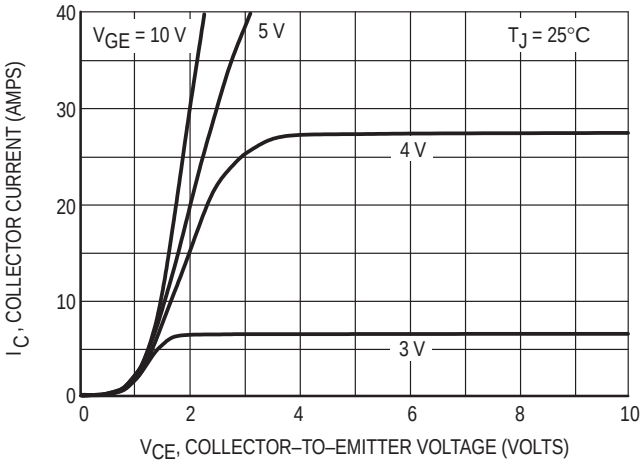

Figure 1. Output Characteristics, T_J = 25°C

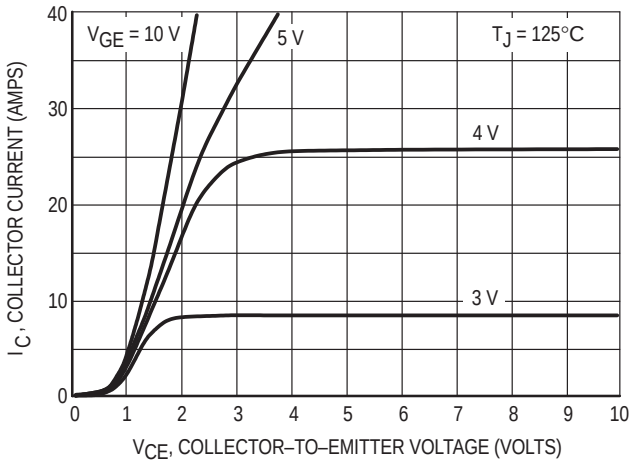

Figure 2. Output Characteristics, T_J = 125°C

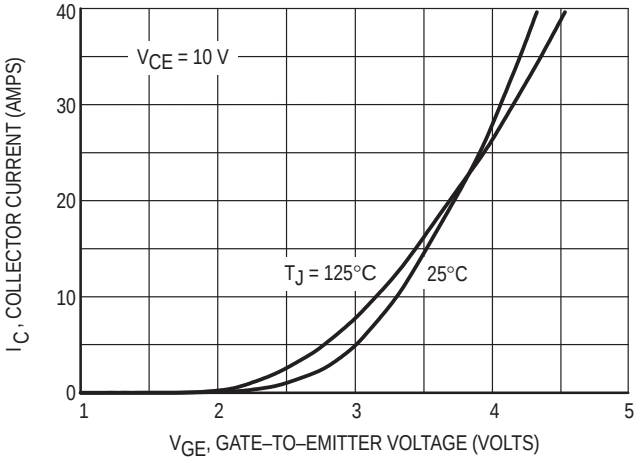

Figure 3. Transfer Characteristics

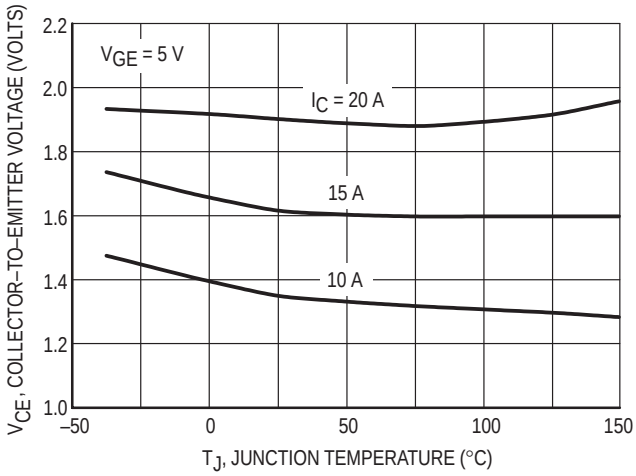

Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

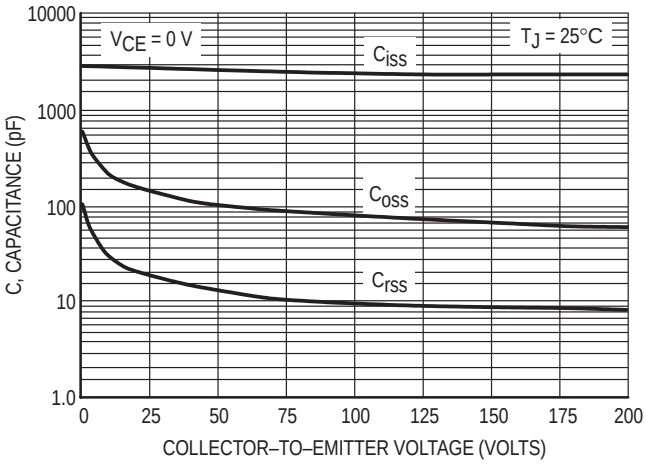

Figure 5. Capacitance Variation

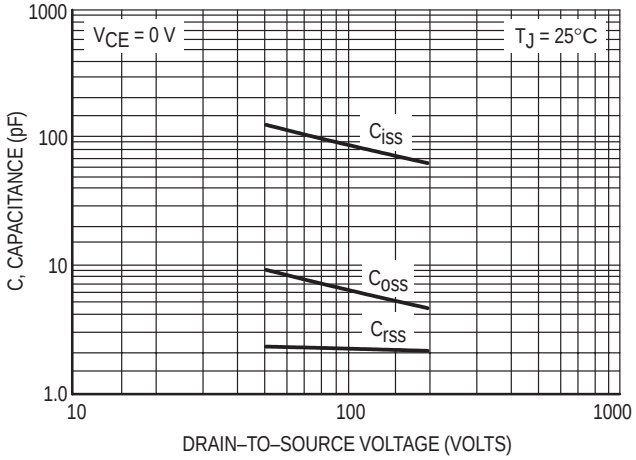

Figure 6. High Voltage Capacitance Variation

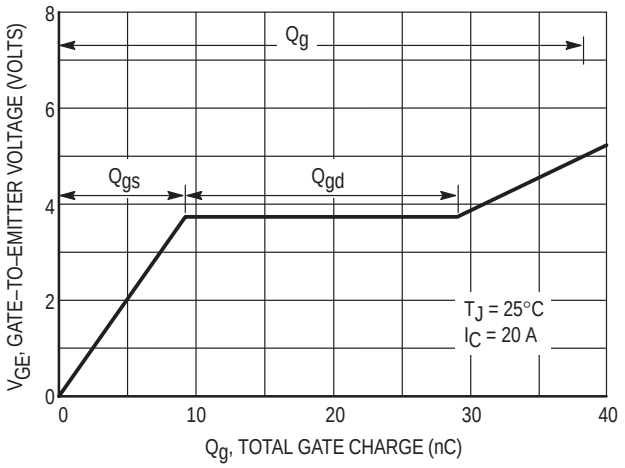

Figure 7. Gate–to–Emitter and Collector–to–Emitter Voltage vs Total Charge

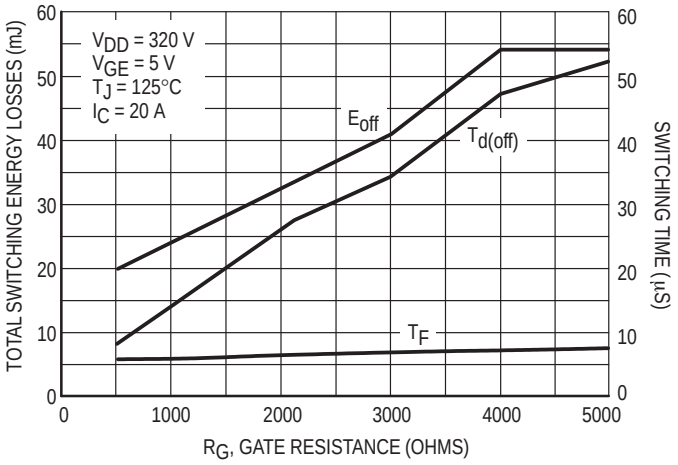

Figure 8. Total Switching Losses versus Gate Temperature

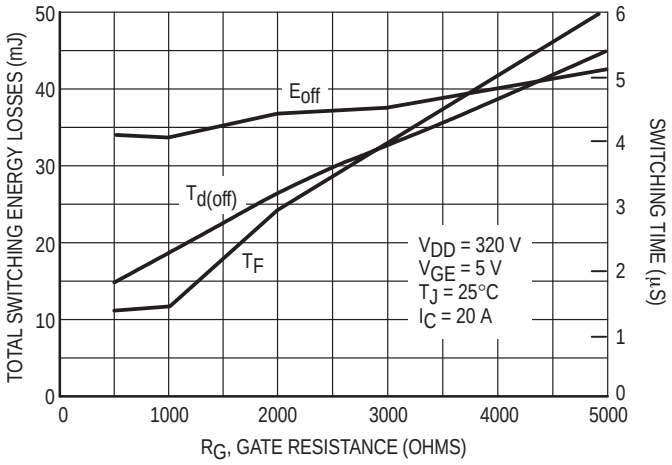

Figure 9. Total Switching Losses versus Gate Resistance

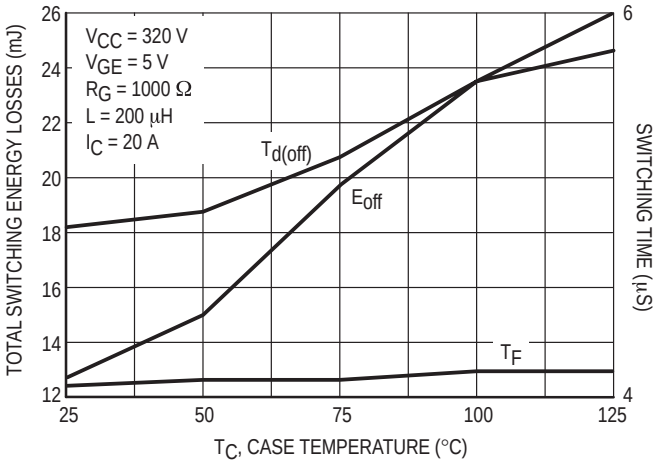

Figure 10. Total Switching Losses versus Case Temperature

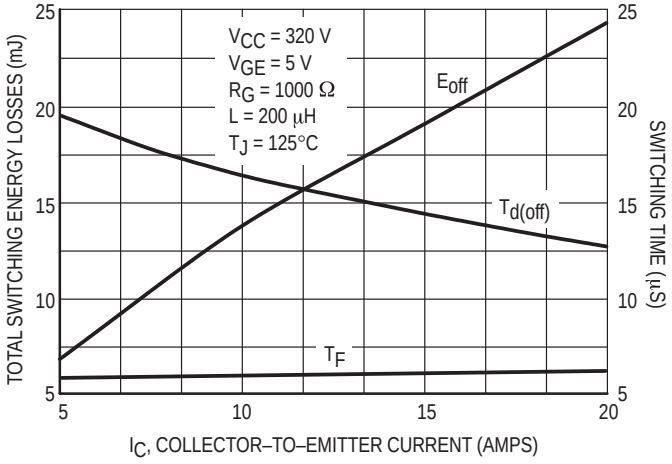

Figure 11. Total Switching Losses versus Collector Current

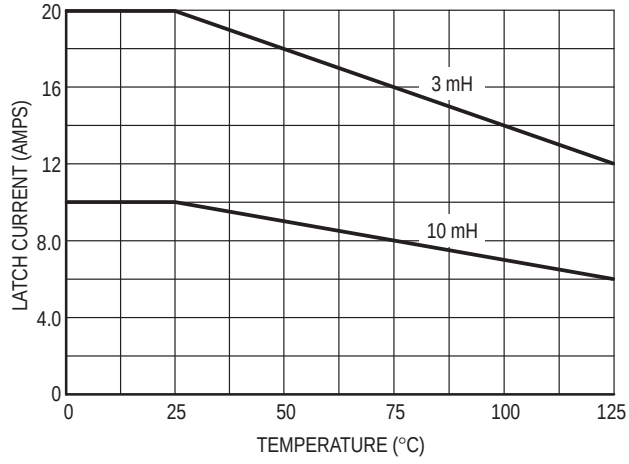

Figure 12. Latch Current versus Temperature

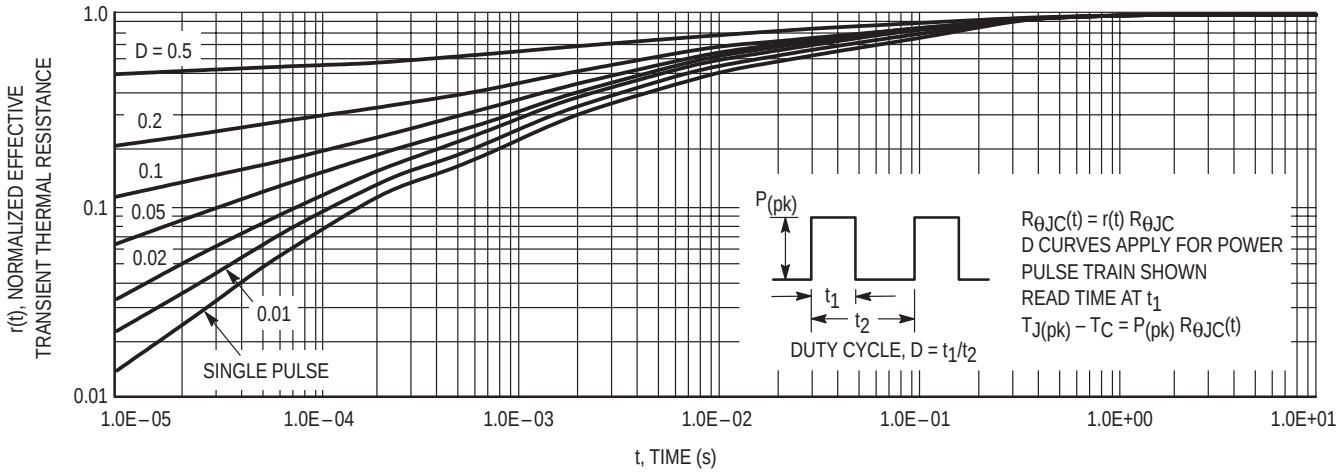

Figure 13. Thermal Response

Advanced Information

SMARTDISCRETES™ Internally Clamped, N-Channel IGBT

MGP20N40CL

20 AMPERES
VOLTAGE CLAMPED
N–CHANNEL IGBT
$V_{ce(on)}$ = 1.8 VOLTS
400 VOLTS (CLAMPED)

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features Gate–Emitter ESD protection, Gate–Collector overvoltage protection from SMARTDISCRETES™ monolithic circuitry for usage as an **Ignition Coil Driver**.

- Temperature Compensated Gate–Drain Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessors
- Low Saturation Voltage
- High Pulsed Current Capability

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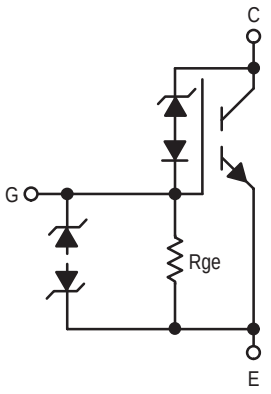
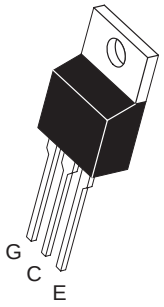




CASE 221A–06, Style 9
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	CLAMPED	Vdc
Collector–Gate Voltage	V_{CGR}	CLAMPED	Vdc
Gate–Emitter Voltage	V_{GE}	CLAMPED	Vdc
Collector Current — Continuous @ T_C = 25°C	I_C	20	Adc
Reversed Collector Current – pulse width < 100 μs	I_{CR}	12	Apk
Total Power Dissipation @ T_C = 25°C (TO–220)	P_D	150	Watts
Electrostatic Voltage — Gate–Emitter	ESD	3.5	kV
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case – (TO–220) — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

UNCLAMPED INDUCTIVE SWITCHING CHARACTERISTICS

Single Pulse Collector–Emitter Avalanche Energy @ Starting T_J = 25°C @ Starting T_J = 150°C	E_{AS}	 550 150	mJ

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–to–Emitter Breakdown Voltage (I_{Clamp} = 10 mA, T_J = –40 to 150°C)	B_{VCES}	380	405	440	Vdc
Zero Gate Voltage Collector Current (V_{CE} = 300 V, V_{GE} = 0 V, T_J = 125°C)	I_{CES}	—	—	1.0	mA
(V_{CE} = 15 V, V_{GE} = 0 V, T_J = 125°C)		—	—	200	μA
Resistance Gate–Emitter (T_J = –40 to 150°C)	R_{GE}	10k	16k	30k	Ω
Gate–Emitter Breakdown Voltage (I_G = 2 mA)	B_{VGES}	11	13	15	±V
Collector–Emitter Reverse Leakage (V_{CE} = –15 V, T_J = –40 to 150°C)	I_{CES}	—	—	—	mA
Collector–Emitter Reversed Breakdown Voltage (I_E = 75 mA)	B_{VCER}	26	40	120	V
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mA)	$V_{GE(th)}$	1.0	1.7	2.4	V
(V_{CE} = V_{GE}, I_C = 1 mA, T_J = 150°C)		0.75	—	1.8	
Collector–Emitter On–Voltage (V_{GE} = 5 V, I_C = 5 A)	$V_{CE(on)}$	—	1.1	1.4	V
(V_{GE} = 5 V, I_C = 10 A)		—	1.4	1.9	
(V_{GE} = 5 V, I_C = 10 Adc, T_J = 150°C)		—	1.4	1.8	
Forward Transconductance (V_{CE} > 50 V, I_C = 10 A)	g_{fs}	10	16	—	S
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	—	2800	—	pF
Output Capacitance (V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{oss}	—	200	—	
Transfer Capacitance	C_{rss}	—	25	—	
SWITCHING CHARACTERISTICS (1)					
Total Gate Charge	Q_g	—	45	80	nC
Gate–Emitter Charge (V_{CC} = 280 V, I_C = 20 A, V_{GE} = 5 V)	Q_{gs}	—	8.0	—	
Gate–Collector Charge	Q_{gd}	—	20	—	
Turn–Off Delay Time (V_{CC} = 320 V, I_C = 20 A, L = 200 μH, R_G = 1 KΩ)	$t_{d(off)}$	—	TBD	TBD	μs
Fall Time	t_f	—	TBD	TBD	
Turn–On Delay Time (V_{CC} = 14 V, I_C = 20 A, L = 200 μH, R_G = 1 KΩ)	$t_{d(on)}$	—	TBD	TBD	μs
Rise Time	t_r	—	TBD	TBD	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

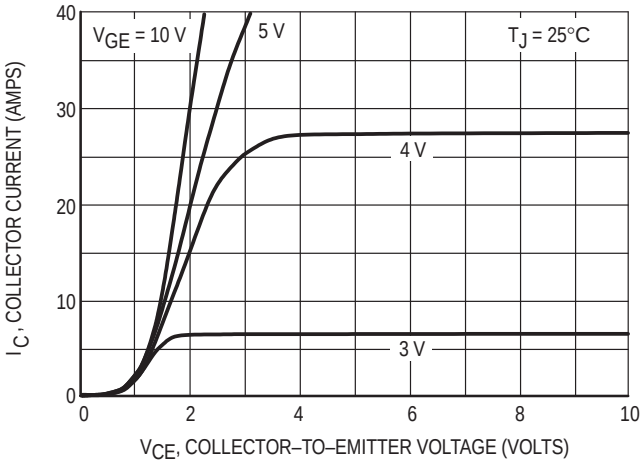


Figure 1. Output Characteristics, T_J = 25°C

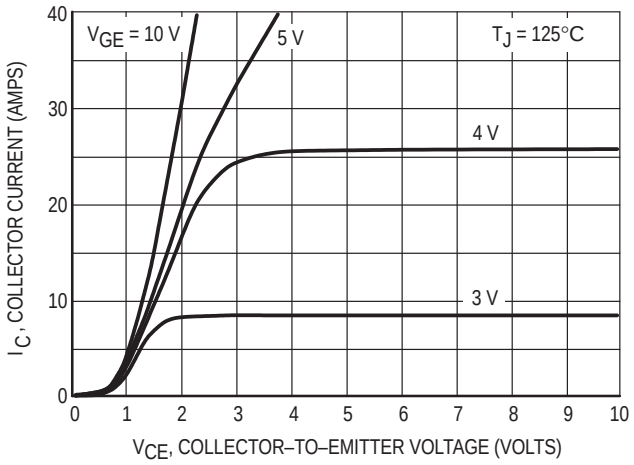


Figure 2. Output Characteristics, T_J = 125°C

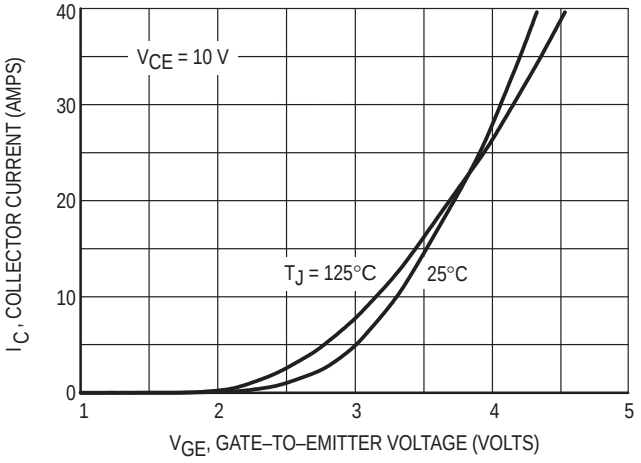


Figure 3. Transfer Characteristics

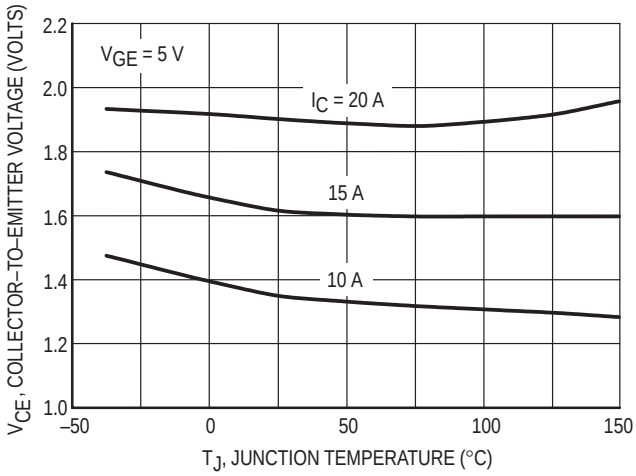


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

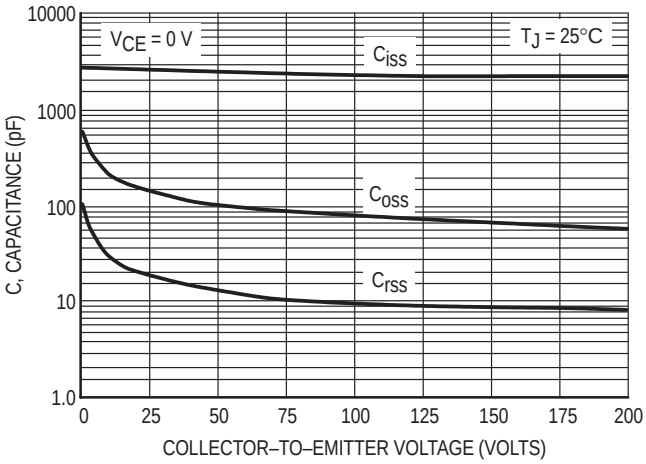


Figure 5. Capacitance Variation

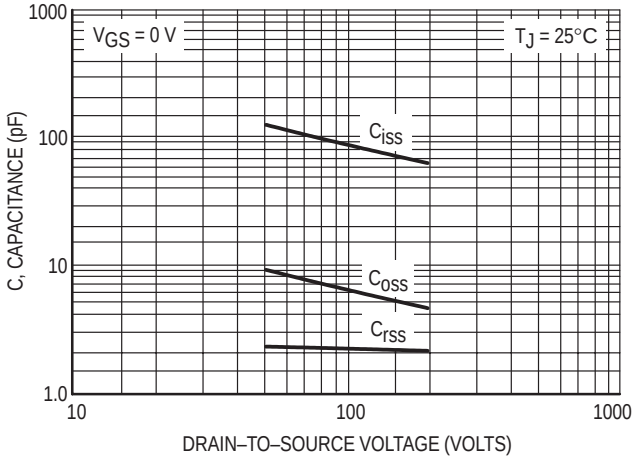


Figure 6. High Voltage Capacitance Variation

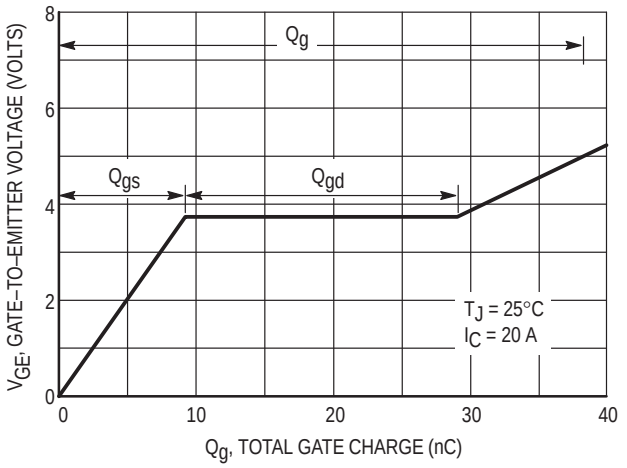


Figure 7. Gate–to–Emitter and Collector–to–Emitter Voltage vs Total Charge

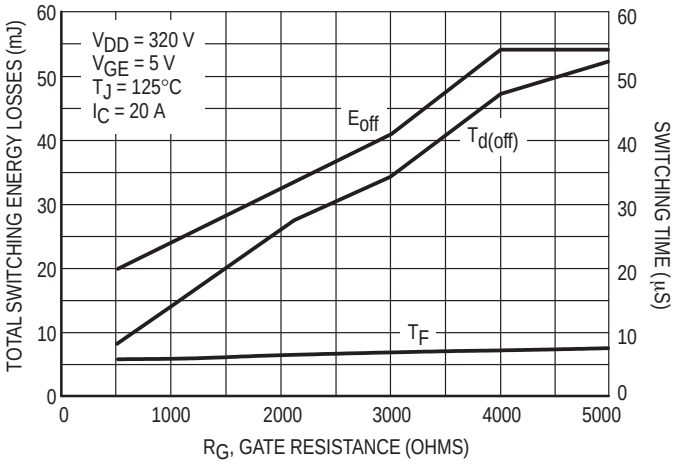


Figure 8. Total Switching Losses versus Gate Temperature

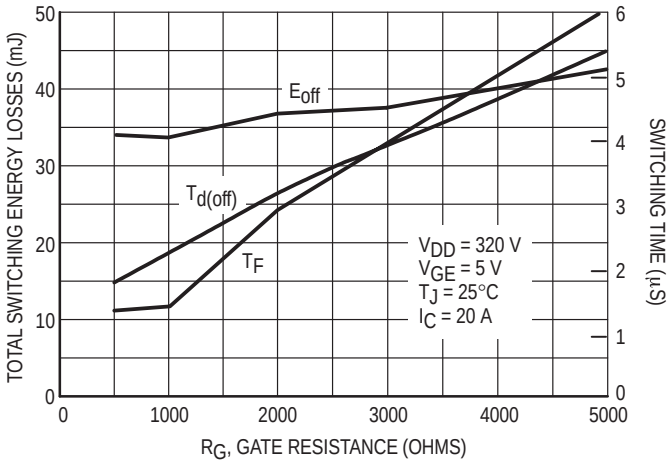


Figure 9. Total Switching Losses versus Gate Resistance

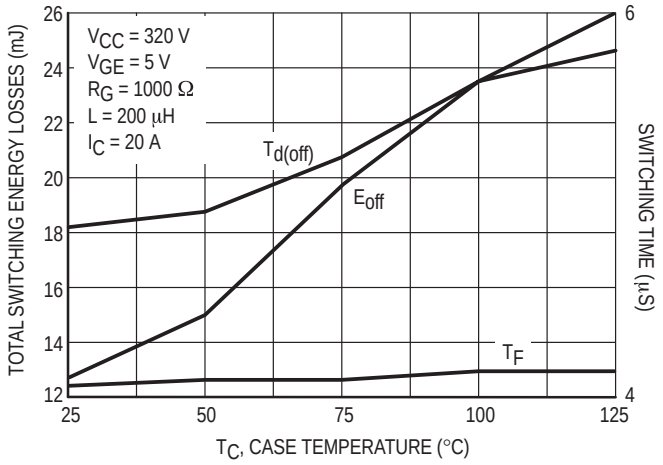


Figure 10. Total Switching Losses versus Case Temperature

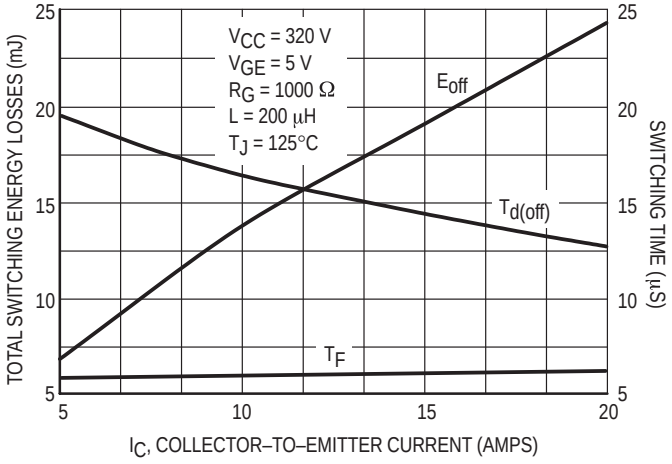


Figure 11. Total Switching Losses versus Collector Current

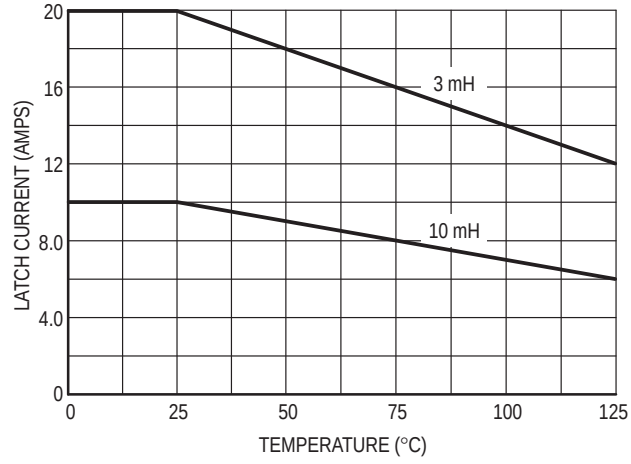


Figure 12. Latch Current versus Temperature

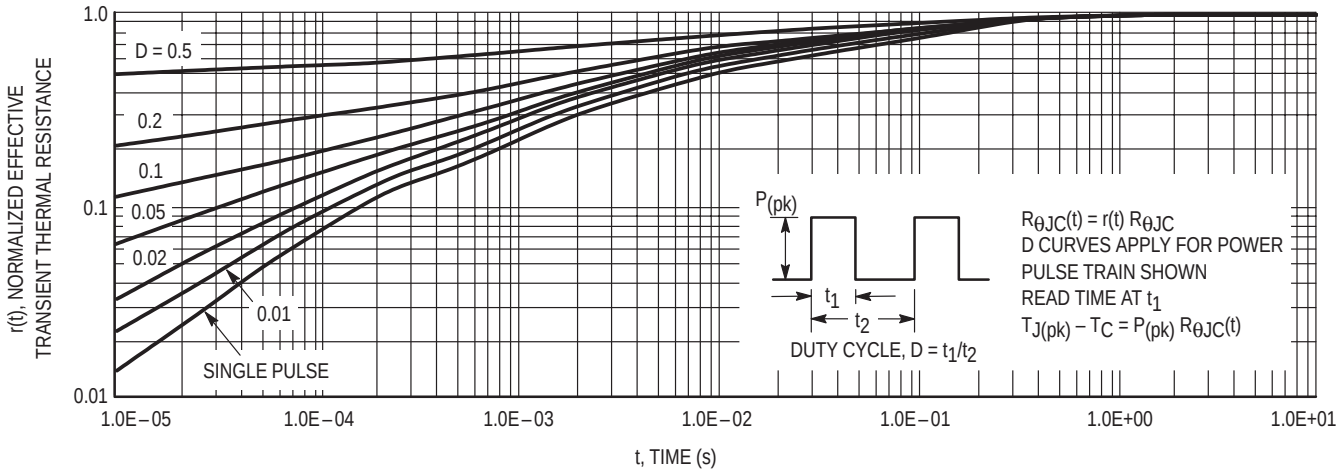


Figure 13. Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

N–Channel Enhancement–Mode Silicon Gate

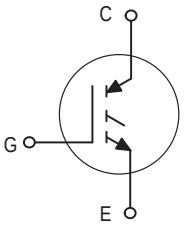
MGW12N120

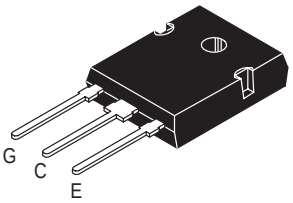
Motorola Preferred Device

IGBT IN TO–247
12 A @ 90°C
20 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies.

- Industry Standard High Power TO–247 Package with Isolated Mounting Hole
- High Speed E_{off}: 160 μJ/A typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Robust High Voltage Termination





CASE 340F–03, Style 4
TO–247AE

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	20 12 40	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	123 0.98	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		BV_{CES}	1200	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		BV_{ECS}	25	—	—	Vdc
Zero Gate Voltage Collector Current		I_{CES}				μAdc
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc)			—	—	100	
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage		$V_{CE(on)}$				Vdc
(V_{GE} = 15 Vdc, I_C = 5.0 Adc)			—	2.51	3.37	
(V_{GE} = 15 Vdc, I_C = 5.0 Adc, T_J = 125°C)			—	2.36	—	
(V_{GE} = 15 Vdc, I_C = 10 Adc)			—	3.21	4.42	
Gate Threshold Voltage		$V_{GE(th)}$				Vdc
(V_{CE} = V_{GE}, I_C = 1.0 mAdc)			4.0	6.0	8.0	
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 10 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	930	—	pF
Output Capacitance		C_{oes}	—	126	—	
Transfer Capacitance		C_{res}	—	16	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 25°C) Energy losses include “tail”	$t_{d(on)}$	—	74	—	ns
Rise Time		t_r	—	83	—	
Turn–Off Delay Time		$t_{d(off)}$	—	76	—	
Fall Time		t_f	—	231	—	
Turn–Off Switching Loss		E_{off}	—	0.55	1.33	mJ
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	66	—	ns
Rise Time		t_r	—	87	—	
Turn–Off Delay Time		$t_{d(off)}$	—	120	—	
Fall Time		t_f	—	575	—	
Turn–Off Switching Loss		E_{off}	—	1.49	—	mJ
Gate Charge	(V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc)	Q_T	—	31	—	nC
		Q_1	—	13	—	
		Q_2	—	14	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

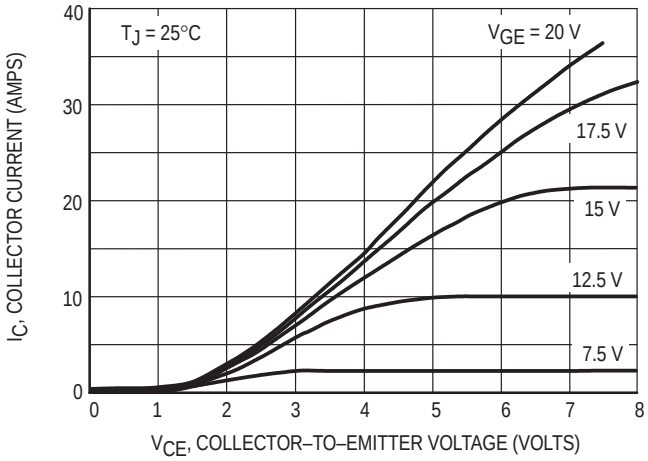


Figure 1. Output Characteristics, T_J = 25°C

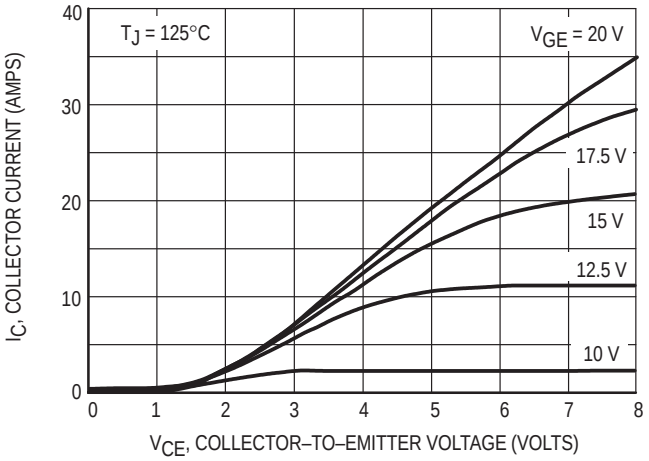


Figure 2. Output Characteristics, T_J = 125°C

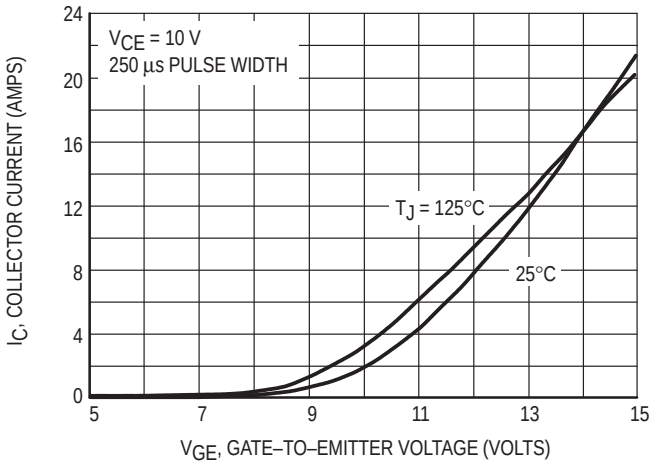


Figure 3. Transfer Characteristics

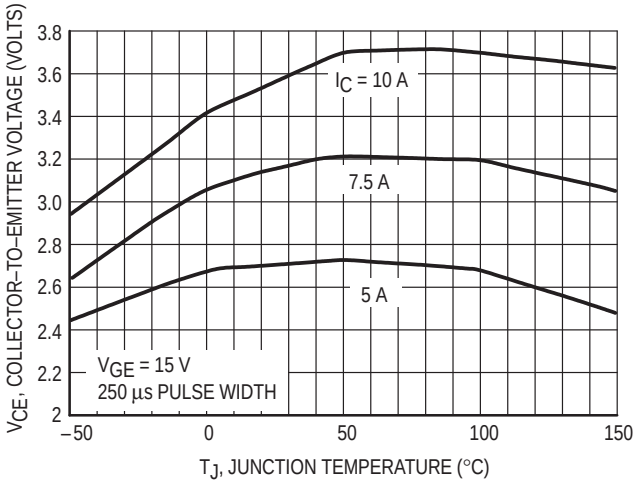


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

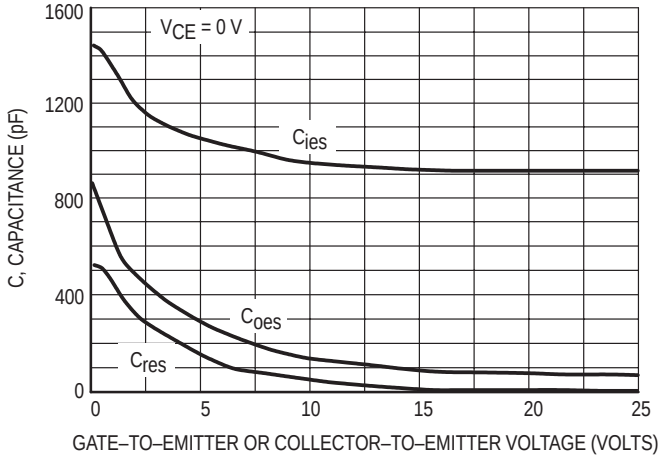


Figure 5. Capacitance Variation

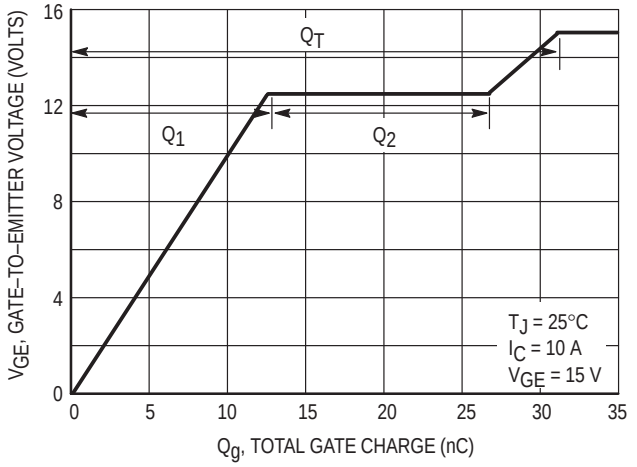


Figure 6. Gate–to–Emitter Voltage versus Total Charge

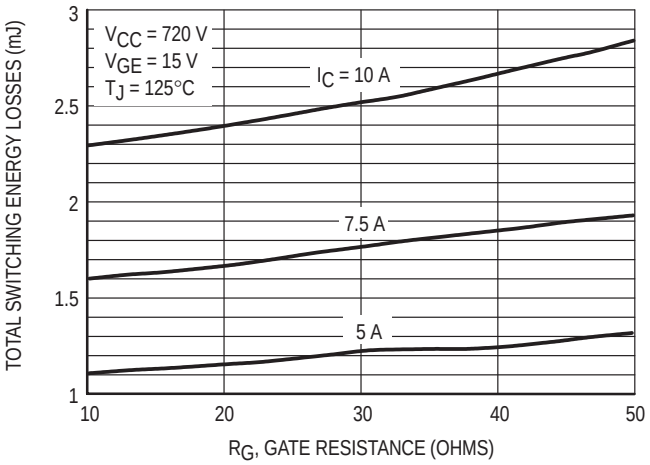


Figure 7. Total Switching Losses versus Gate Resistance

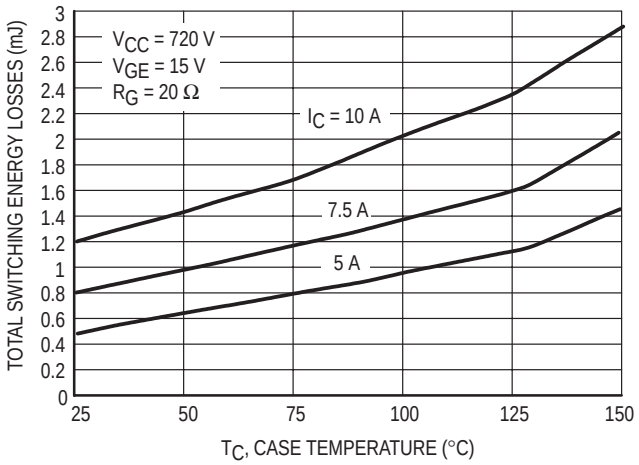


Figure 8. Total Switching Losses versus Case Temperature

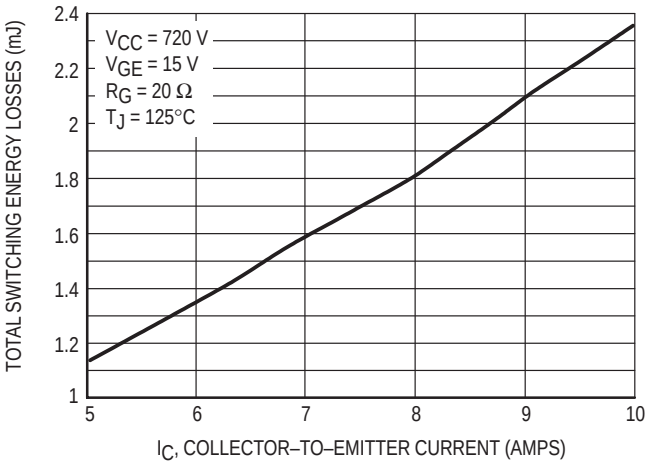


Figure 9. Total Switching Losses versus Collector–to–Emitter Current

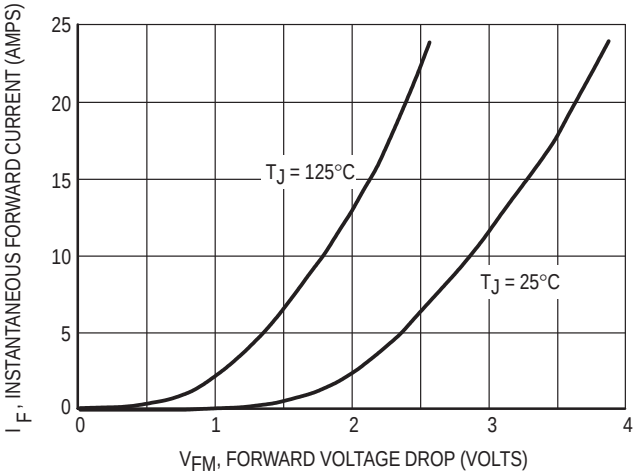


Figure 10. Maximum Forward Drop versus Instantaneous Forward Current

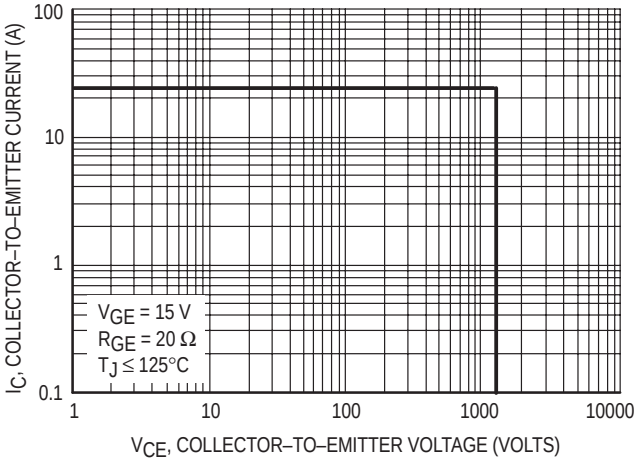


Figure 11. Reverse Biased Safe Operating Area

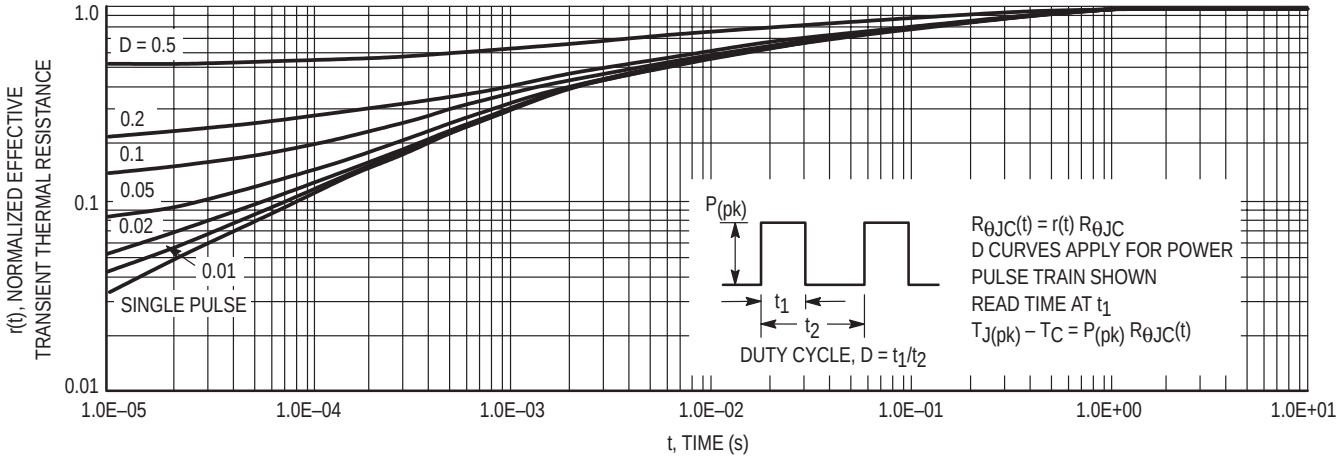


Figure 12. Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N–Channel Enhancement–Mode Silicon Gate

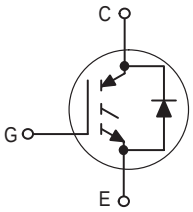
MGW12N120D

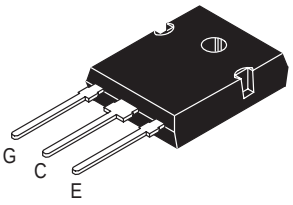
Motorola Preferred Device

IGBT & DIODE IN TO–247
12 A @ 90°C
20 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies. Co–packaged IGBT's save space, reduce assembly time and cost.

- Industry Standard High Power TO–247 Package with Isolated Mounting Hole
- High Speed E_{off}: 160 μJ per Amp typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Soft Recovery Free Wheeling Diode is included in the package
- Robust High Voltage Termination
- Robust RBSOA





CASE 340F–03, Style 4
TO–247AE

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	20 12 40	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	123 0.98	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	1.0 1.4 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)	BV_{CES}	1200	—	—	Vdc
Temperature Coefficient (Positive)		—	870	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc)	I_{CES}	—	—	100	μAdc
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)		—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)	I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)					
Collector–to–Emitter On–State Voltage	$V_{CE(on)}$				Vdc
(V_{GE} = 15 Vdc, I_C = 5.0 Adc)		—	2.71	3.37	
(V_{GE} = 15 Vdc, I_C = 5.0 Adc, T_J = 125°C)		—	3.78	—	
(V_{GE} = 15 Vdc, I_C = 10 Adc)		—	3.72	4.42	
Gate Threshold Voltage	$V_{GE(th)}$				Vdc
(V_{CE} = V_{GE}, I_C = 1.0 mAdc)		4.0	6.0	8.0	
Threshold Temperature Coefficient (Negative)		—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 10 Adc)	g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{ies}	—	1003	—	pF
Output Capacitance	C_{oes}	—	126	—	
Transfer Capacitance	C_{res}	—	106	—	
(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)					
SWITCHING CHARACTERISTICS (1)					
Turn–On Delay Time	$t_{d(on)}$	—	74	—	ns
Rise Time	t_r	—	83	—	
Turn–Off Delay Time	$t_{d(off)}$	—	76	—	
Fall Time	t_f	—	231	—	
Turn–Off Switching Loss	E_{off}	—	0.55	1.33	mJ
Turn–On Switching Loss	E_{on}	—	1.21	1.88	
Total Switching Loss	E_{ts}	—	1.76	3.21	
(V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 25°C) Energy losses include "tail"					
Turn–On Delay Time	$t_{d(on)}$	—	66	—	ns
Rise Time	t_r	—	87	—	
Turn–Off Delay Time	$t_{d(off)}$	—	120	—	
Fall Time	t_f	—	575	—	
Turn–Off Switching Loss	E_{off}	—	1.49	—	mJ
Turn–On Switching Loss	E_{on}	—	2.37	—	
Total Switching Loss	E_{ts}	—	3.86	—	
(V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include "tail"					
Gate Charge	Q_T	—	29	—	nC
(V_{CC} = 720 Vdc, I_C = 10 Adc, V_{GE} = 15 Vdc)	Q_1	—	13	—	
	Q_2	—	12	—	
DIODE CHARACTERISTICS					
Diode Forward Voltage Drop	V_{FEC}				Vdc
(I_{EC} = 5.0 Adc)		—	2.26	3.32	
(I_{EC} = 5.0 Adc, T_J = 125°C)		—	1.37	—	
(I_{EC} = 10 Adc)		—	2.86	4.18	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 10 Adc, V_R = 720 Vdc, dI_F/dt = 100 A/μs)	t_{rr}	—	116	—	ns
		t_a	—	69	—	
		t_b	—	47	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.36	—	μC
Reverse Recovery Time	(I_F = 10 Adc, V_R = 720 Vdc, dI_F/dt = 100 A/μs, T_J = 125°C)	t_{rr}	—	234	—	ns
		t_a	—	149	—	
		t_b	—	85	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.40	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

TYPICAL ELECTRICAL CHARACTERISTICS

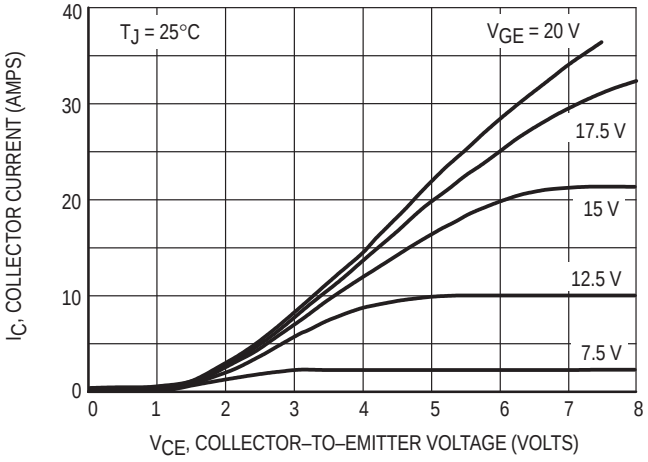


Figure 1. Output Characteristics, T_J = 25°C

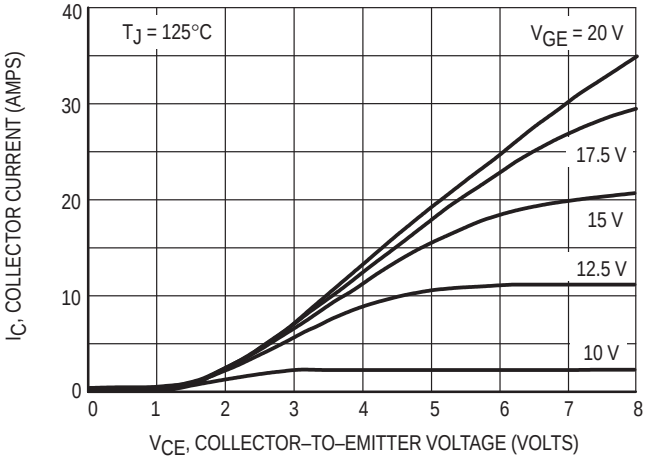


Figure 2. Output Characteristics, T_J = 125°C

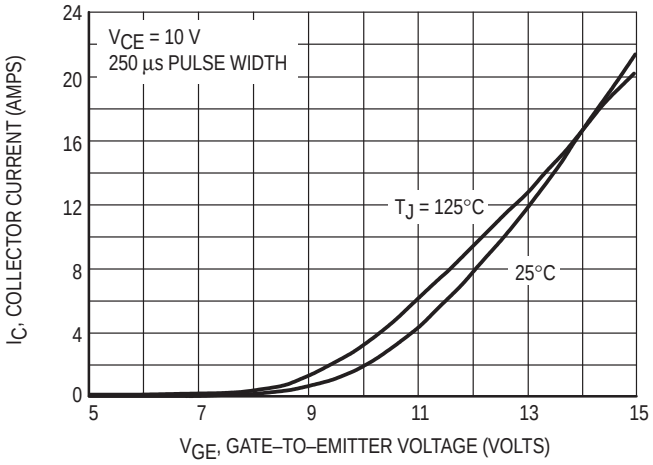


Figure 3. Transfer Characteristics

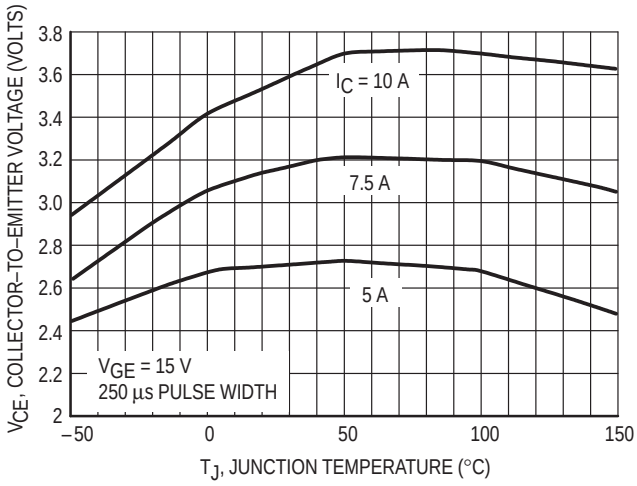


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

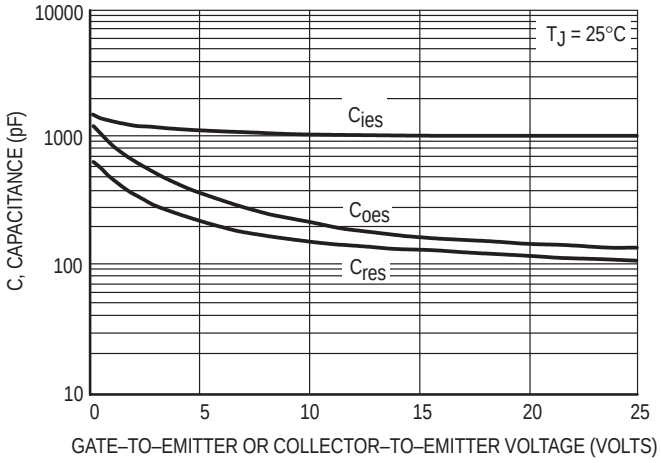


Figure 5. Capacitance Variation

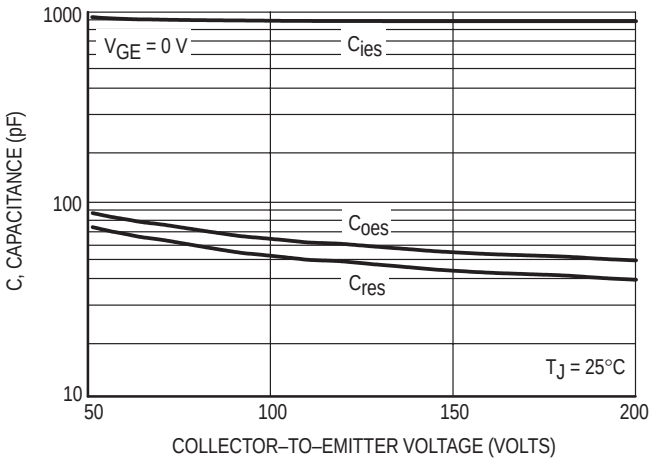


Figure 5b. High Voltage Capacitance Variation

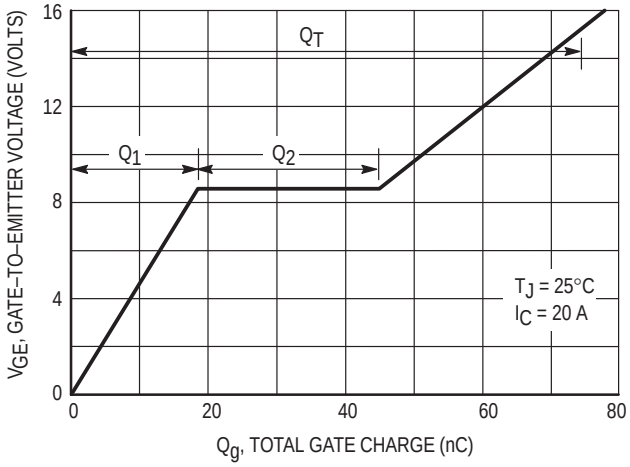


Figure 6. Gate–to–Emitter and Collector–to–Emitter Voltage versus Total Charge

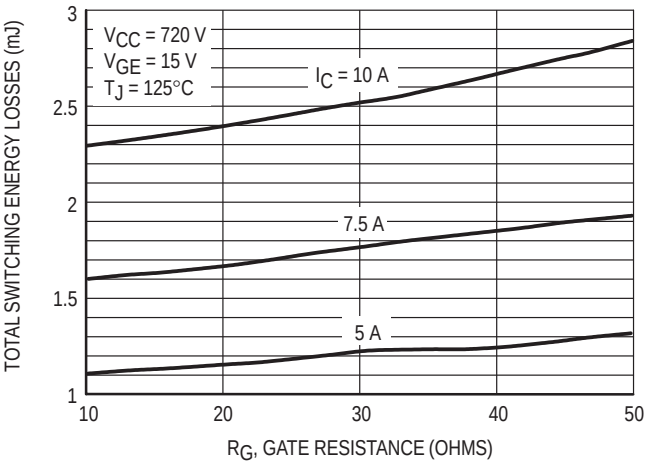


Figure 7. Total Switching Losses versus Gate Resistance

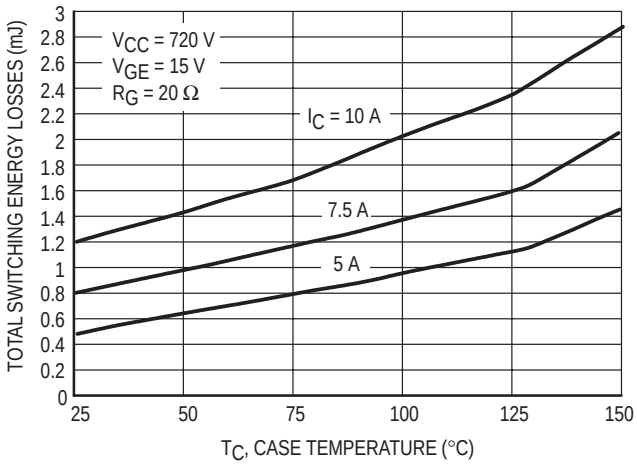


Figure 8. Total Switching Losses versus Case Temperature

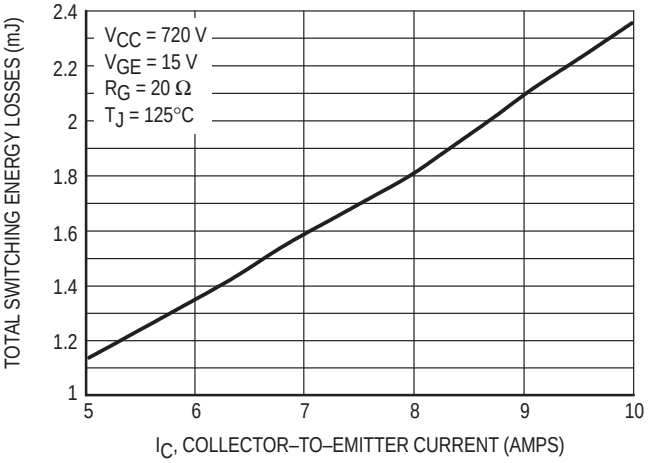


Figure 9. Total Switching Losses versus Collector–to–Emitter Current

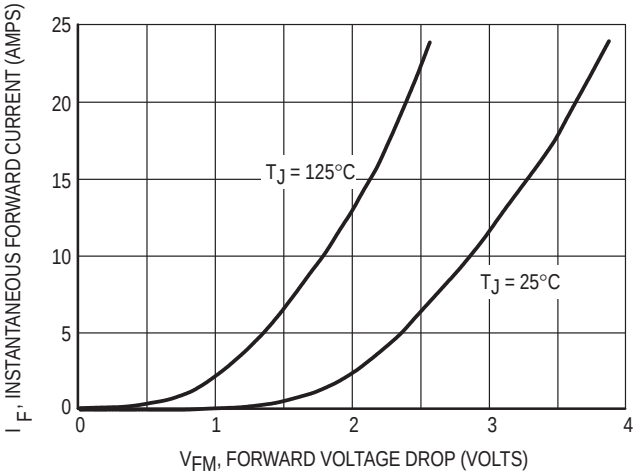


Figure 10. Maximum Forward Drop versus Instantaneous Forward Current

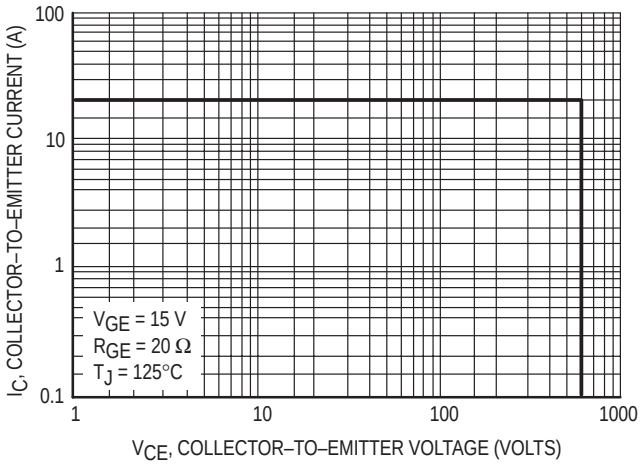


Figure 11. Reverse Biased Safe Operating Area

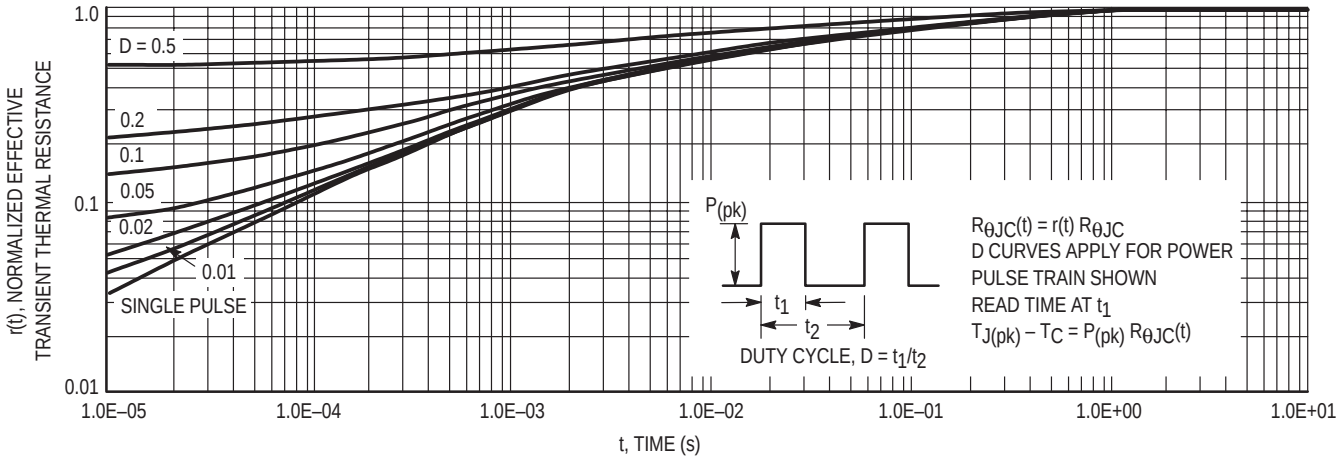


Figure 12. Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N–Channel Enhancement–Mode Silicon Gate

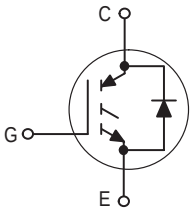
MGW20N60D

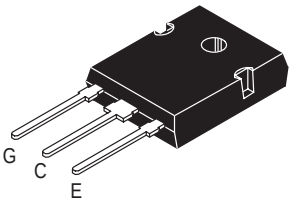
Motorola Preferred Device

IGBT & DIODE IN TO–247
20 A @ 90°C
32 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operations at high frequencies. Co–packaged IGBT's save space, reduce assembly time and cost.

- Industry Standard High Power TO–247 Package with Isolated Mounting Hole
- High Speed E_{off}: 60 μJ per Amp typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Soft Recovery Free Wheeling Diode is included in the package
- Robust High Voltage Termination
- Robust RBSOA





CASE 340F–03, Style 4
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	32 20 64	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	142 1.14	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 360 Vdc, V_{GE} = 15 Vdc, T_J = 25°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	0.88 2.00 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc)	BV_{CES}	600	—	—	Vdc
Temperature Coefficient (Positive)		—	870	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)	I_{CES}	—	—	100	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)		—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)	I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)					
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 10 Adc)	$V_{CE(on)}$	—	2.30	2.85	Vdc
(V_{GE} = 15 Vdc, I_C = 10 Adc, T_J = 125°C)		—	2.20	—	
(V_{GE} = 15 Vdc, I_C = 20 Adc)		—	2.85	3.65	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mAdc)	$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)		—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 20 Adc)	g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{ies}	—	2280	—	pF
Output Capacitance (V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{oes}	—	165	—	
Transfer Capacitance	C_{res}	—	12	—	
SWITCHING CHARACTERISTICS (1)					
Turn–On Delay Time	$t_{d(on)}$	—	59	—	ns
Rise Time	t_r	—	61	—	
Turn–Off Delay Time (V_{CC} = 360 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 25°C) Energy losses include “tail”	$t_{d(off)}$	—	150	—	
Fall Time	t_f	—	212	—	
Turn–Off Switching Loss	E_{off}	—	0.60	0.85	mJ
Turn–On Switching Loss	E_{on}	—	0.75	—	
Total Switching Loss	E_{ts}	—	1.35	—	
Turn–On Delay Time	$t_{d(on)}$	—	51	—	ns
Rise Time	t_r	—	77	—	
Turn–Off Delay Time (V_{CC} = 360 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(off)}$	—	184	—	
Fall Time	t_f	—	392	—	
Turn–Off Switching Loss	E_{off}	—	1.20	—	mJ
Turn–On Switching Loss	E_{on}	—	1.50	—	
Total Switching Loss	E_{ts}	—	2.70	—	
Gate Charge	Q_T	—	74	—	nC
(V_{CC} = 360 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc)	Q_1	—	19	—	
	Q_2	—	27	—	
DIODE CHARACTERISTICS					
Diode Forward Voltage Drop (I_{EC} = 10 Adc)	V_{FEC}	—	1.50	1.90	Vdc
(I_{EC} = 10 Adc, T_J = 125°C)		—	1.30	—	
(I_{EC} = 20 Adc)		—	1.70	2.15	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 20 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs)	t_{rr}	—	117	—	ns
		t_a	—	70	—	
		t_b	—	47	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.2	—	μC
Reverse Recovery Time	(I_F = 20 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs, T_J = 125°C)	t_{rr}	—	166	—	ns
		t_a	—	98	—	
		t_b	—	68	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.9	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

TYPICAL ELECTRICAL CHARACTERISTICS

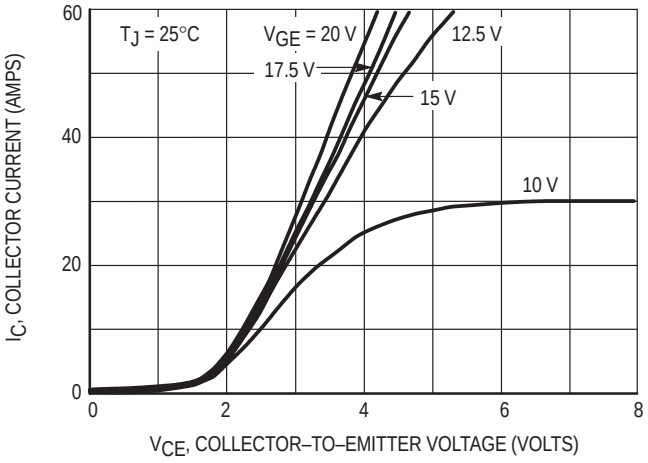


Figure 1. Output Characteristics, T_J = 25°C

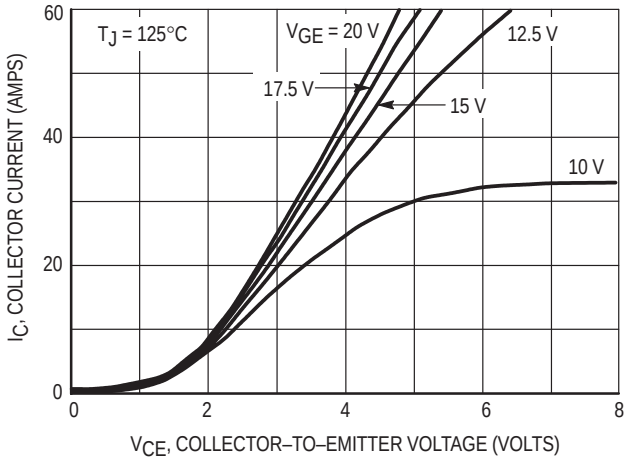


Figure 2. Output Characteristics, T_J = 125°C

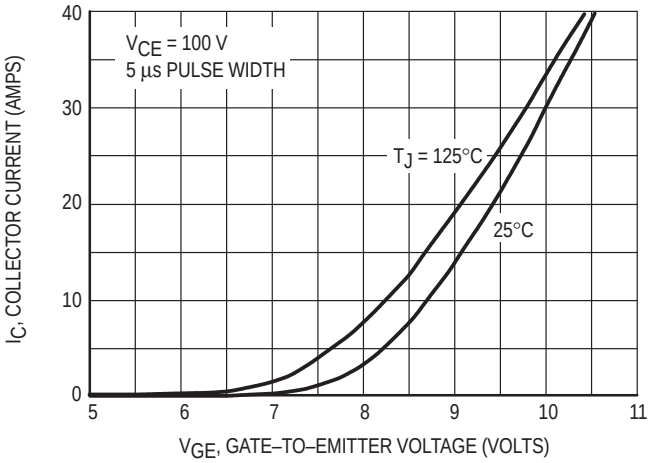


Figure 3. Transfer Characteristics

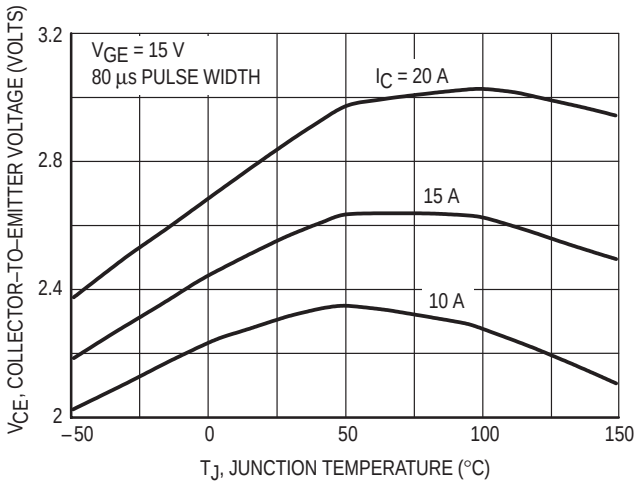


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

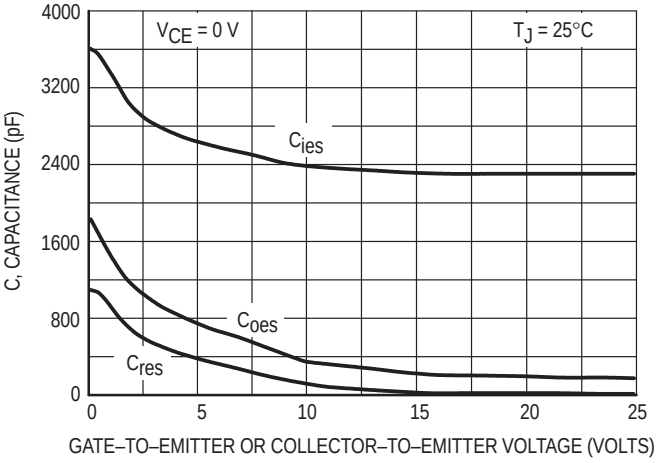


Figure 5. Capacitance Variation

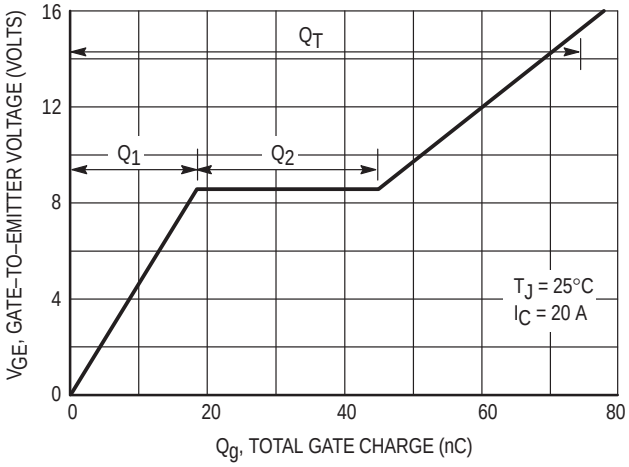


Figure 6. Gate–to–Emitter Voltage versus Total Charge

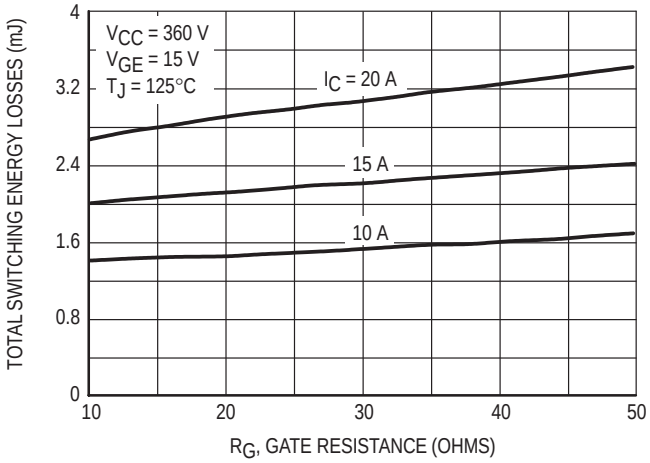


Figure 7. Total Switching Losses versus Gate Resistance

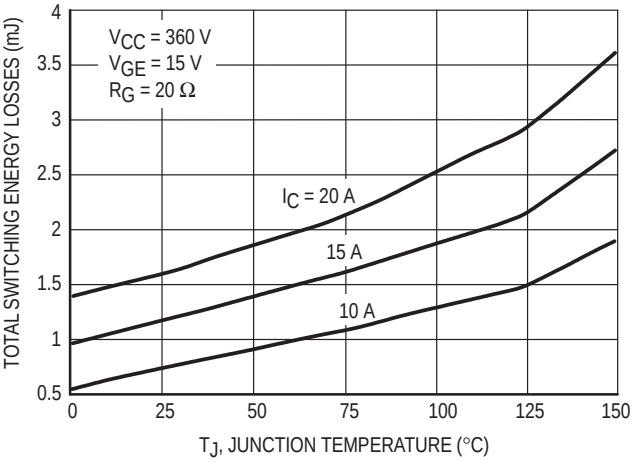


Figure 8. Total Switching Losses versus Junction Temperature

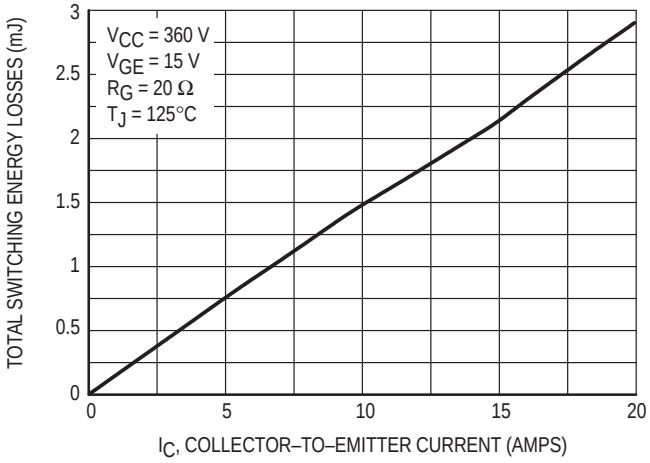


Figure 9. Total Switching Losses versus Collector–to–Emitter Current

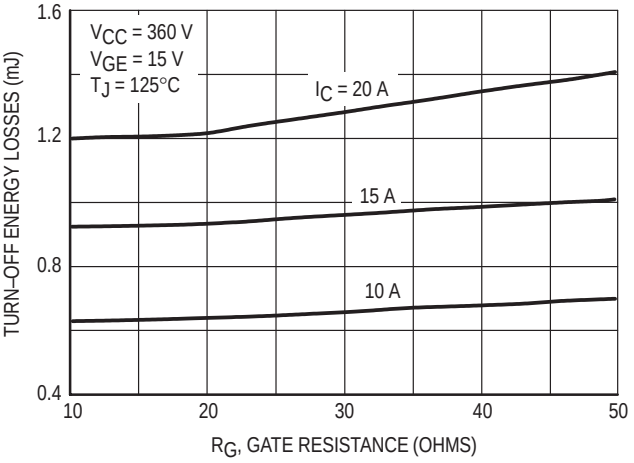


Figure 10. Turn–Off Losses versus Gate Resistance

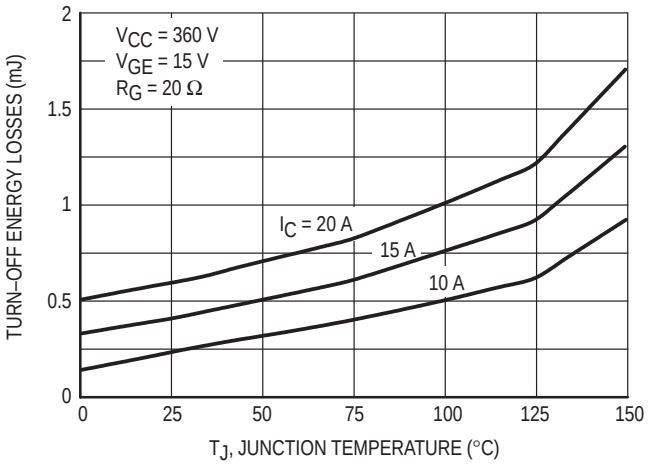


Figure 11. Turn–Off Losses versus Junction Temperature

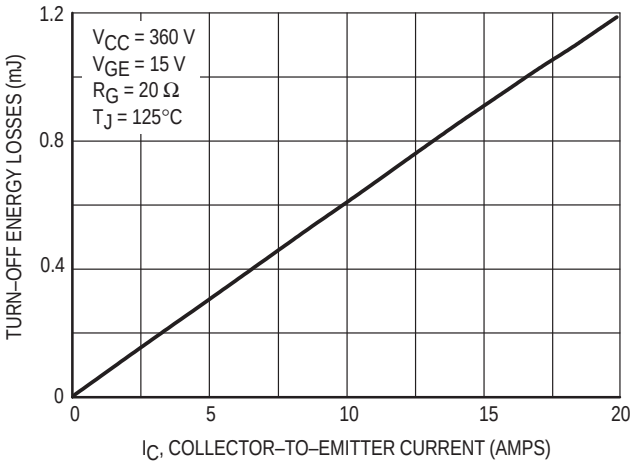


Figure 12. Turn–Off Losses versus Collector–to–Emitter Current

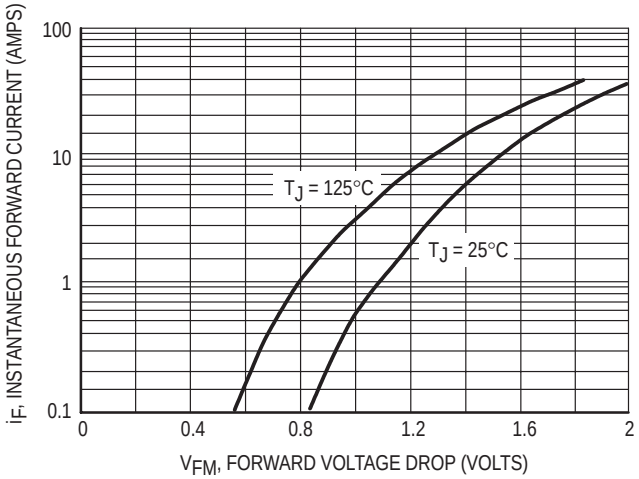


Figure 13. Typical Diode Forward Drop versus Instantaneous Forward Current

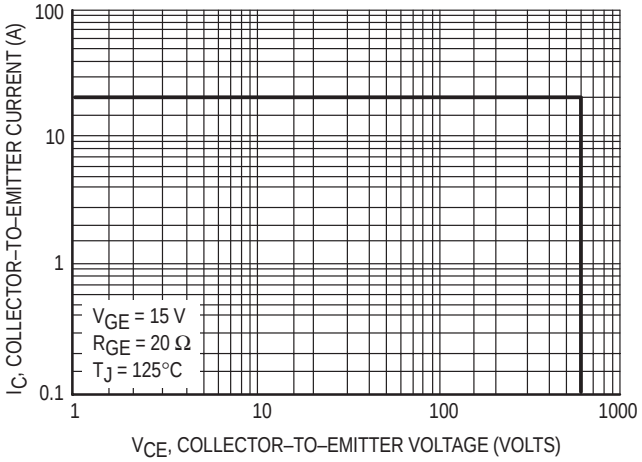


Figure 14. Reverse Biased Safe Operating Area

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

N–Channel Enhancement–Mode Silicon Gate

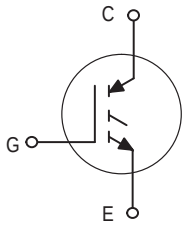
MGW20N120

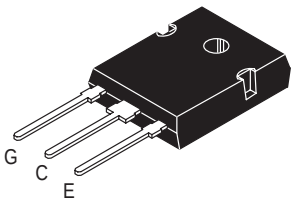
Motorola Preferred Device

IGBT IN TO–247
20 A @ 90°C
28 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time. Fast switching characteristics result in efficient operation at high frequencies.

- Industry Standard High Power TO–247 Package with Isolated Mounting Hole
- High Speed E_{off}: 160 μJ/A typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Robust High Voltage Termination





CASE 340F–03, Style 4
TO–247AE

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	28 20 56	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	174 1.39	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.7 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		BV_{CES}	1200	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		BV_{ECS}	25	—	—	Vdc
Zero Gate Voltage Collector Current		I_{CES}				μAdc
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc)			—	—	100	
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage		$V_{CE(on)}$				Vdc
(V_{GE} = 15 Vdc, I_C = 10 Adc)			—	3.00	3.54	
(V_{GE} = 15 Vdc, I_C = 10 Adc, T_J = 125°C)			—	2.36	—	
(V_{GE} = 15 Vdc, I_C = 20 Adc)			—	2.90	4.99	
Gate Threshold Voltage		$V_{GE(th)}$				Vdc
(V_{CE} = V_{GE}, I_C = 1.0 mAdc)			4.0	6.0	8.0	
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 20 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1860	—	pF
Output Capacitance		C_{oes}	—	122	—	
Transfer Capacitance		C_{res}	—	29	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 25°C) Energy losses include “tail”	$t_{d(on)}$	—	88	—	ns
Rise Time		t_r	—	103	—	
Turn–Off Delay Time		$t_{d(off)}$	—	190	—	
Fall Time		t_f	—	284	—	
Turn–Off Switching Loss		E_{off}	—	1.65	3.75	mJ
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	83	—	ns
Rise Time		t_r	—	107	—	
Turn–Off Delay Time		$t_{d(off)}$	—	216	—	
Fall Time		t_f	—	494	—	
Turn–Off Switching Loss		E_{off}	—	3.19	—	mJ
Gate Charge	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc)	Q_T	—	62	—	nC
		Q_1	—	21	—	
		Q_2	—	25	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

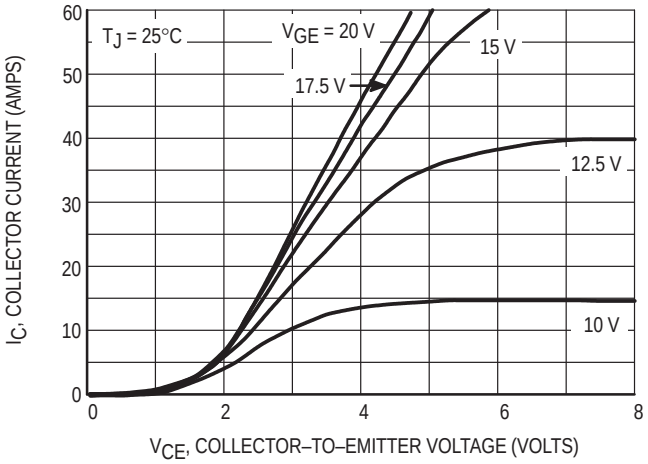


Figure 1. Output Characteristics, T_J = 25°C

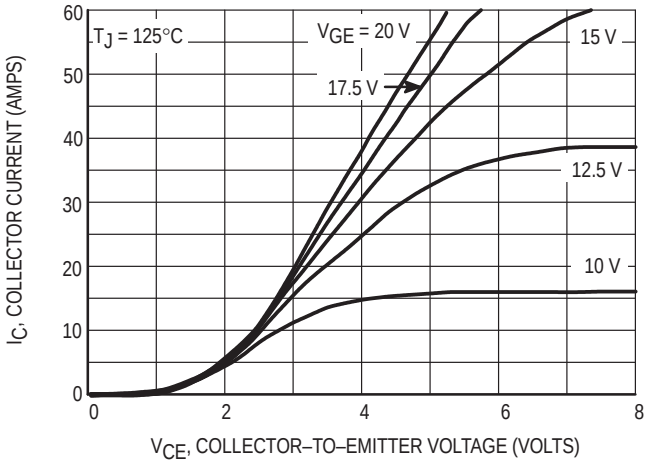


Figure 2. Output Characteristics, T_J = 125°C

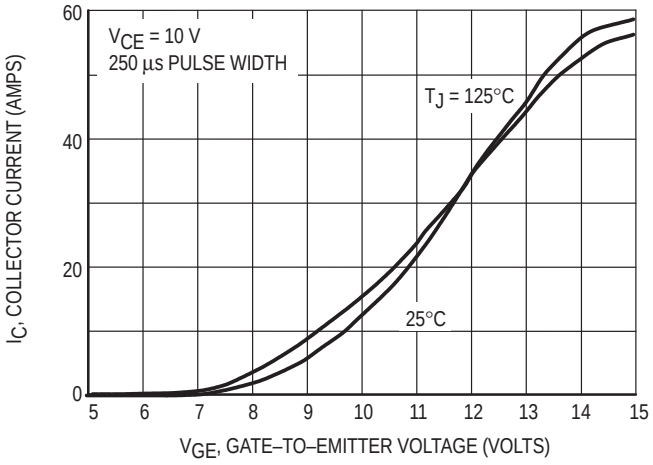


Figure 3. Transfer Characteristics

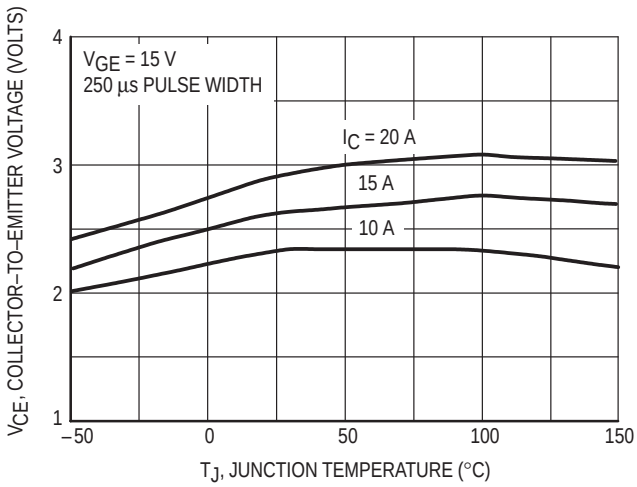


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

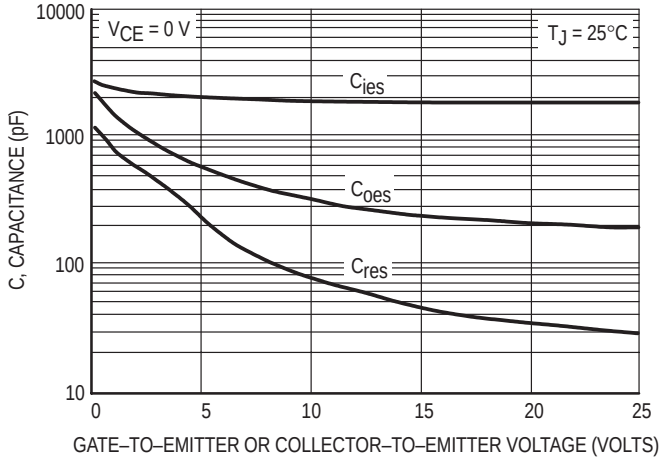


Figure 5. Capacitance Variation

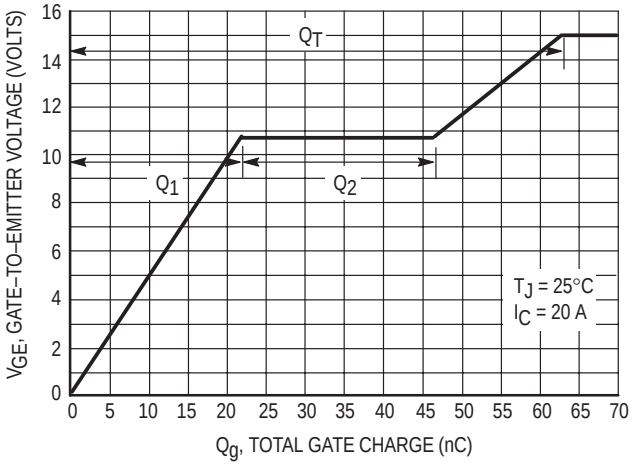


Figure 6. Gate–to–Emitter Voltage versus Total Charge

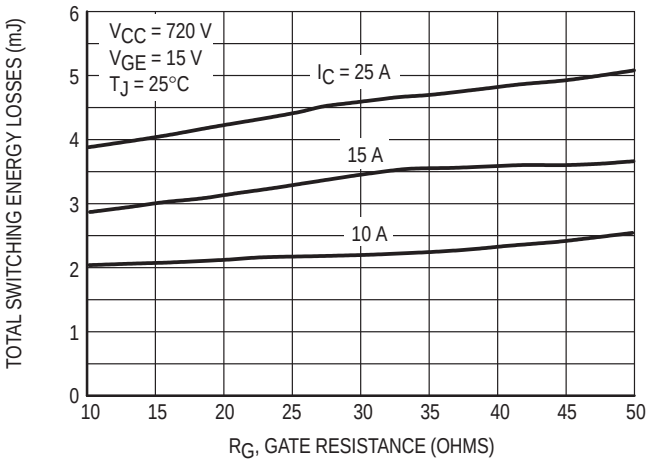


Figure 7. Total Switching Losses versus Gate Resistance

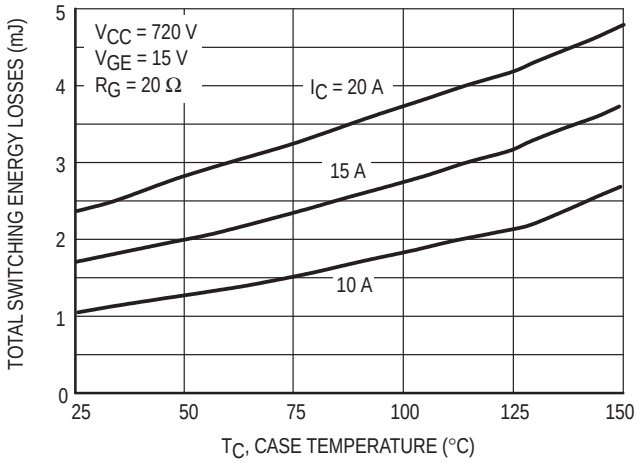


Figure 8. Total Switching Losses versus Case Temperature

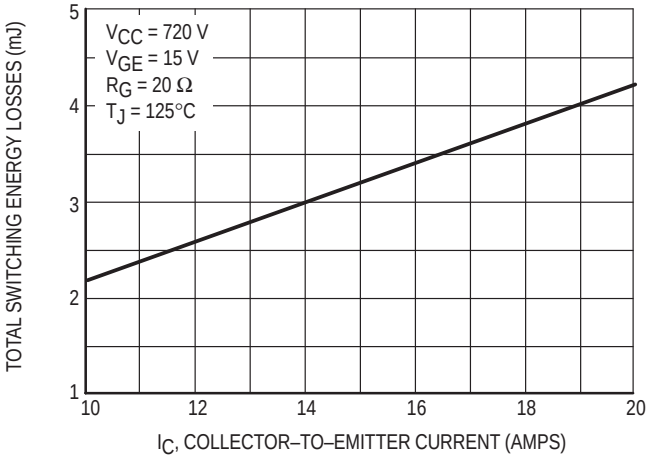


Figure 9. Turn–Off Losses versus Collector–to–Emitter Current

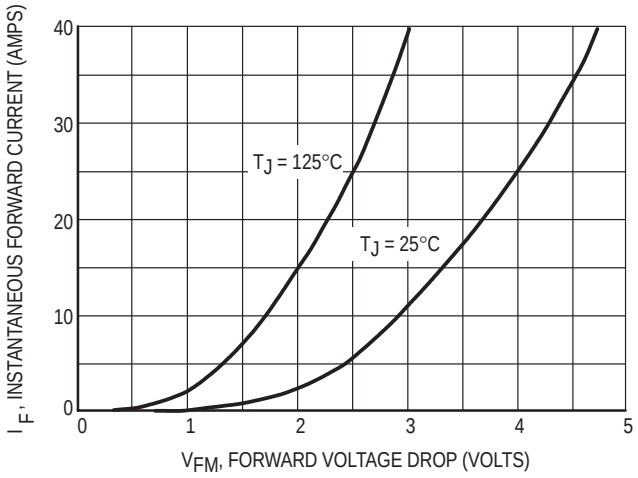


Figure 10. Maximum Forward Drop versus Instantaneous Forward Current

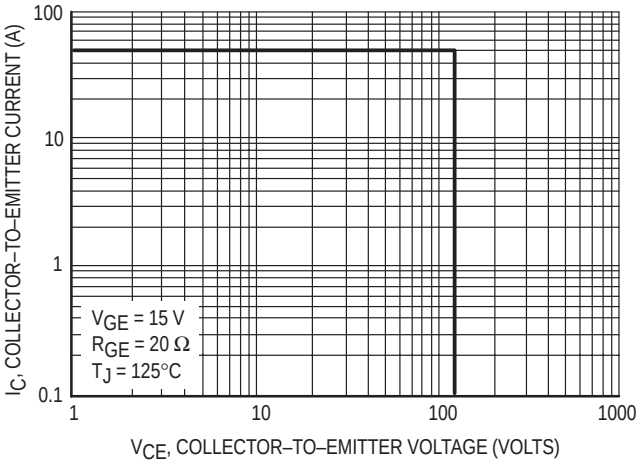


Figure 11. Reverse Biased Safe Operating Area

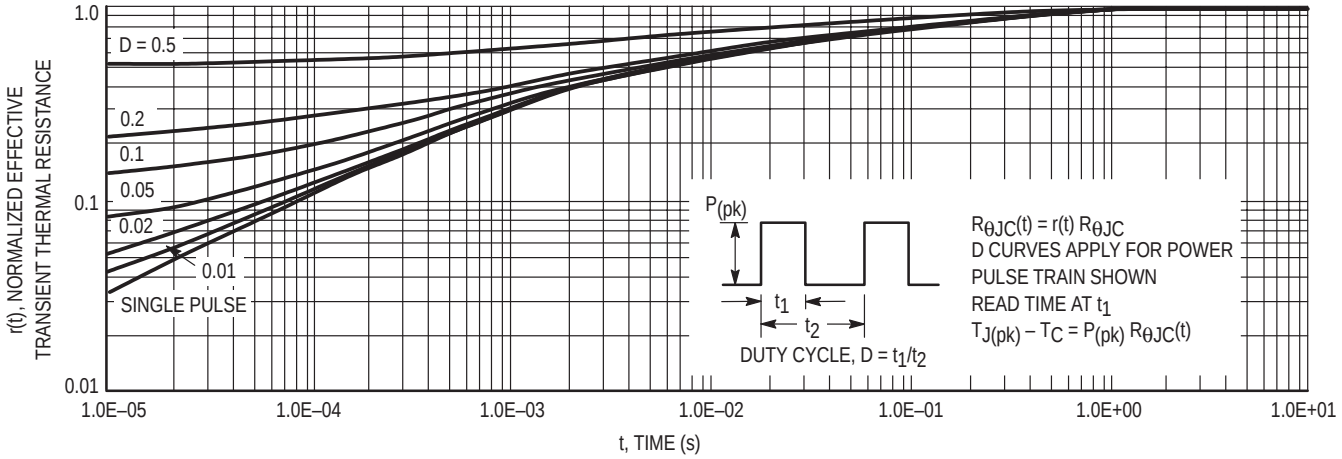


Figure 12. Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

N–Channel Enhancement–Mode Silicon Gate

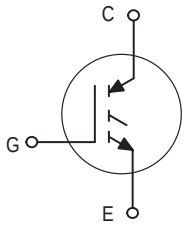
MGW30N60

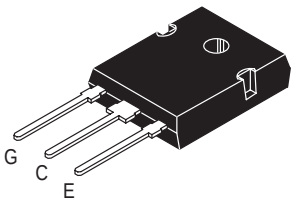
Motorola Preferred Device

IGBT IN TO–247
30 A @ 90°C
50 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies.

- Industry Standard High Power TO–247 Package with Isolated Mounting Hole
- High Speed E_{off}: 60 μJ per Amp typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Robust High Voltage Termination
- Robust RBSOA





CASE 340F–03, Style 4
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	50 30 100	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	202 1.61	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 360 Vdc, V_{GE} = 15 Vdc, T_J = 25°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.62 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc)		BV_{CES}	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		BV_{ECS}	25	—	—	Vdc
Zero Gate Voltage Collector Current		I_{CES}				μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)			—	—	100	
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage		$V_{CE(on)}$				Vdc
(V_{GE} = 15 Vdc, I_C = 15 Adc)			—	2.20	2.90	
(V_{GE} = 15 Vdc, I_C = 15 Adc, T_J = 125°C)			—	2.10	—	
(V_{GE} = 15 Vdc, I_C = 30 Adc)			—	2.60	3.45	
Gate Threshold Voltage		$V_{GE(th)}$				Vdc
(V_{CE} = V_{GE}, I_C = 1 mAdc)			4.0	6.0	8.0	
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 30 Adc)		g_{fe}	—	15	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	4280	—	pF
Output Capacitance		C_{oes}	—	275	—	
Transfer Capacitance		C_{res}	—	19	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 30 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 25°C) Energy losses include “tail”	$t_{d(on)}$	—	76	—	ns
Rise Time		t_r	—	80	—	
Turn–Off Delay Time		$t_{d(off)}$	—	348	—	
Fall Time		t_f	—	188	—	
Turn–Off Switching Loss		E_{off}	—	0.98	1.28	mJ
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 30 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	73	—	ns
Rise Time		t_r	—	95	—	
Turn–Off Delay Time		$t_{d(off)}$	—	394	—	
Fall Time		t_f	—	418	—	
Turn–Off Switching Loss		E_{off}	—	1.90	—	mJ
Gate Charge	(V_{CC} = 360 Vdc, I_C = 30 Adc, V_{GE} = 15 Vdc)	Q_T	—	150	—	nC
		Q_1	—	30	—	
		Q_2	—	45	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

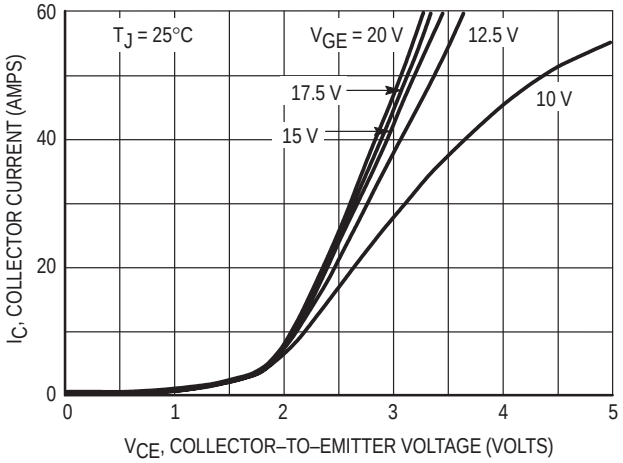


Figure 1. Output Characteristics, T_J = 25°C

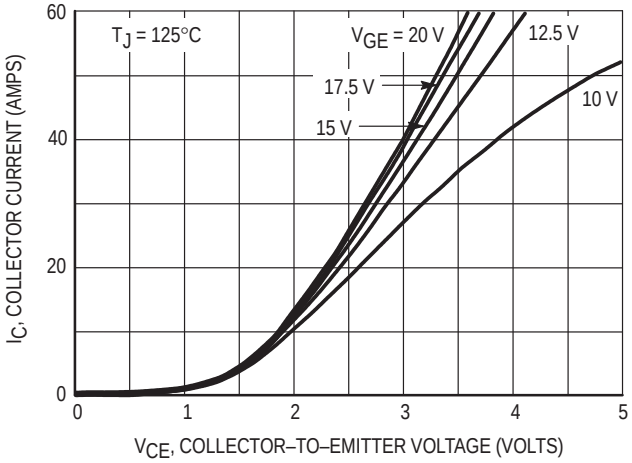


Figure 2. Output Characteristics, T_J = 125°C

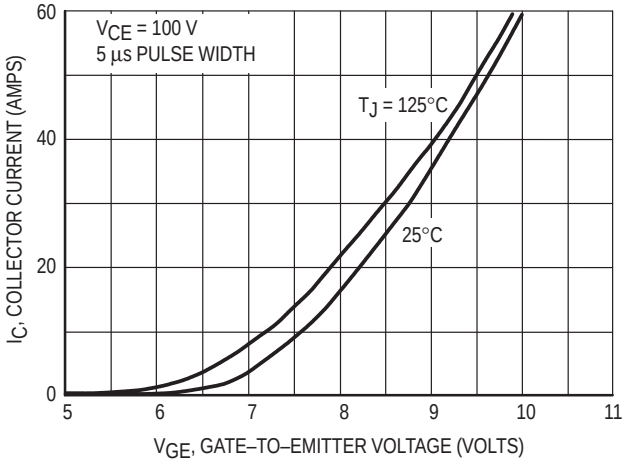


Figure 3. Transfer Characteristics

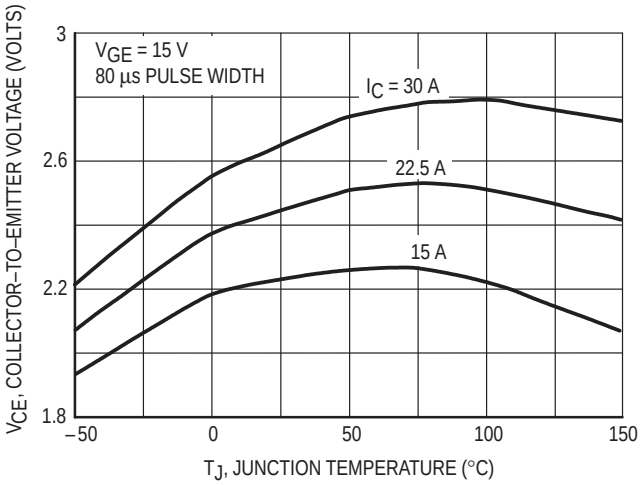


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

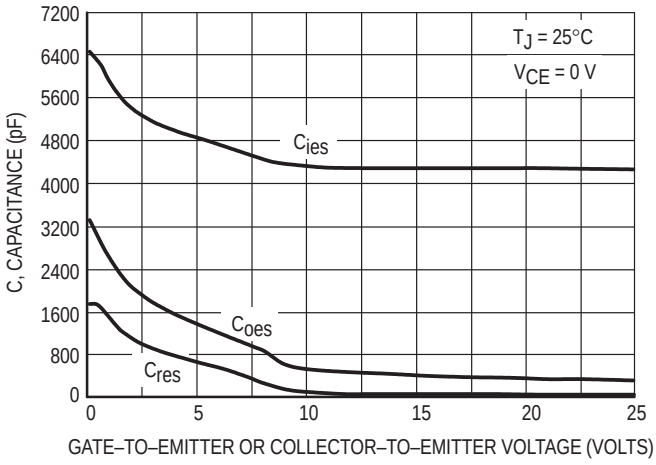


Figure 5. Capacitance Variation

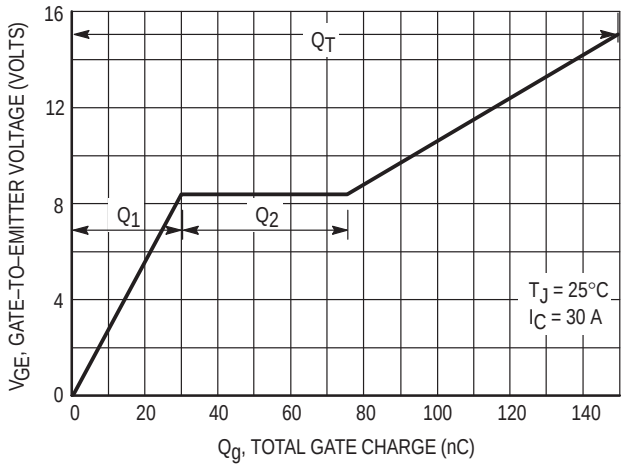


Figure 6. Gate–to–Emitter Voltage versus Total Charge

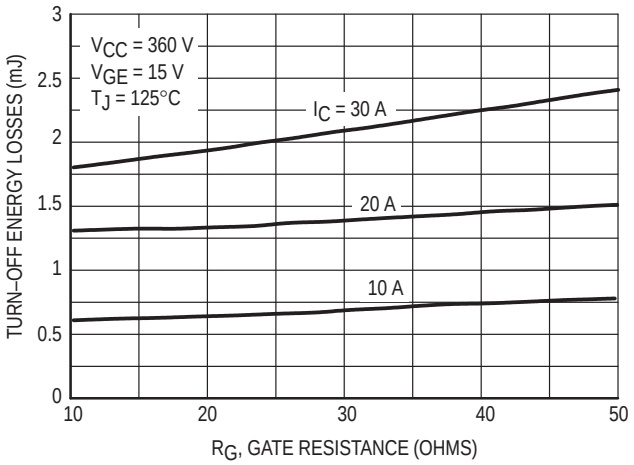


Figure 7. Turn–Off Losses versus Gate Resistance

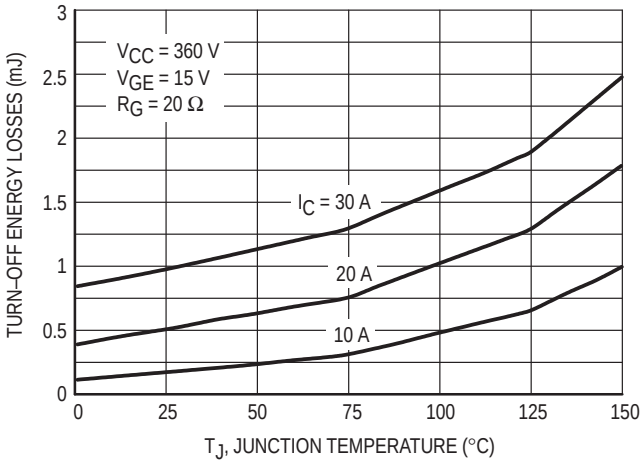


Figure 8. Turn–Off Losses versus Junction Temperature

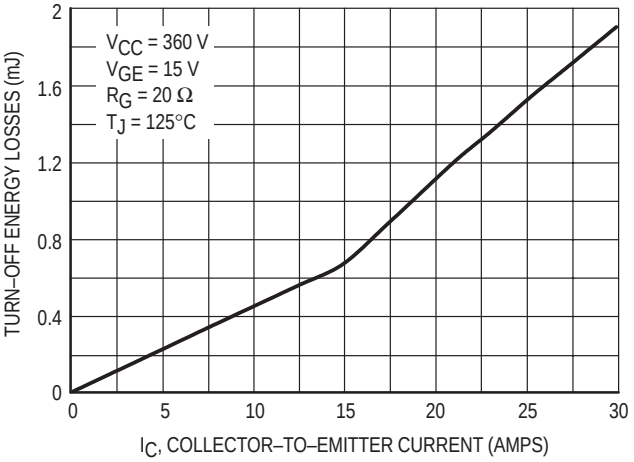


Figure 9. Turn–Off Losses versus Collector–to–Emitter Current

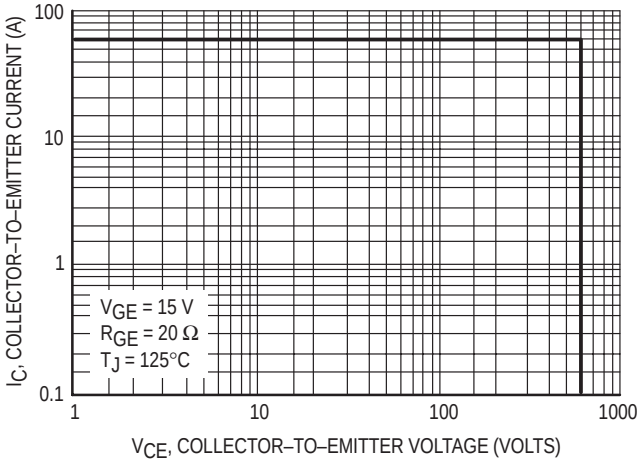


Figure 10. Reverse Biased Safe Operating Area

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N–Channel Enhancement–Mode Silicon Gate

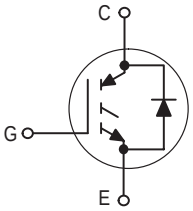
MGY20N120D

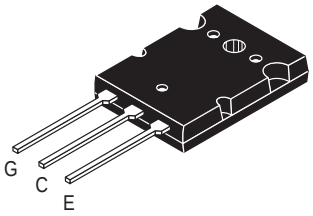
Motorola Preferred Device

IGBT & DIODE IN TO–264
20 A @ 90°C
28 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies. Co–packaged IGBT's save space, reduce assembly time and cost.

- Industry Standard High Power TO–264 Package (TO–3PBL)
- High Speed E_{off}: 160 μJ per Amp typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Soft Recovery Free Wheeling Diode is included in the package
- Robust High Voltage Termination
- Robust RBSOA





CASE 340G–02, Style 5
TO–264

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	28 20 56	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	174 1.39	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	0.7 1.1 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		BV_{CES}	1200	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	100	μAdc
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage		$V_{CE(on)}$				Vdc
(V_{GE} = 15 Vdc, I_C = 10 Adc)			—	3.00	3.54	
(V_{GE} = 15 Vdc, I_C = 10 Adc, T_J = 125°C)			—	2.36	—	
(V_{GE} = 15 Vdc, I_C = 20 Adc)			—	2.90	4.99	
Gate Threshold Voltage		$V_{GE(th)}$				Vdc
(V_{CE} = V_{GE}, I_C = 1.0 mAdc)			4.0	6.0	8.0	
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 20 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	1876	—	pF
Output Capacitance		C_{oes}	—	208	—	
Transfer Capacitance		C_{res}	—	31	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 25°C) Energy losses include "tail"	$t_{d(on)}$	—	88	—	ns
Rise Time		t_r	—	103	—	
Turn–Off Delay Time		$t_{d(off)}$	—	190	—	
Fall Time		t_f	—	284	—	
Turn–Off Switching Loss		E_{off}	—	1.65	3.75	mJ
Turn–On Switching Loss		E_{on}	—	2.42	7.68	
Total Switching Loss		E_{ts}	—	4.07	11.43	
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include "tail"	$t_{d(on)}$	—	83	—	ns
Rise Time		t_r	—	107	—	
Turn–Off Delay Time		$t_{d(off)}$	—	216	—	
Fall Time		t_f	—	494	—	
Turn–Off Switching Loss		E_{off}	—	3.19	—	mJ
Turn–On Switching Loss		E_{on}	—	4.26	—	
Total Switching Loss		E_{ts}	—	7.45	—	
Gate Charge	(V_{CC} = 720 Vdc, I_C = 20 Adc, V_{GE} = 15 Vdc)	Q_T	—	63	—	nC
		Q_1	—	20	—	
		Q_2	—	27	—	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop		V_{FEC}				Vdc
(I_{EC} = 10 Adc)			—	2.92	3.59	
(I_{EC} = 10 Adc, T_J = 125°C)			—	1.73	—	
(I_{EC} = 20 Adc)			—	3.67	4.57	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 20 Adc, V_R = 720 Vdc, dI_F/dt = 150 A/μs)	t_{rr}	—	114	—	ns
		t_a	—	74	—	
		t_b	—	40	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.68	—	μC
Reverse Recovery Time	(I_F = 20 Adc, V_R = 720 Vdc, dI_F/dt = 150 A/μs, T_J = 125°C)	t_{rr}	—	224	—	ns
		t_a	—	149	—	
		t_b	—	75	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.40	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

TYPICAL ELECTRICAL CHARACTERISTICS

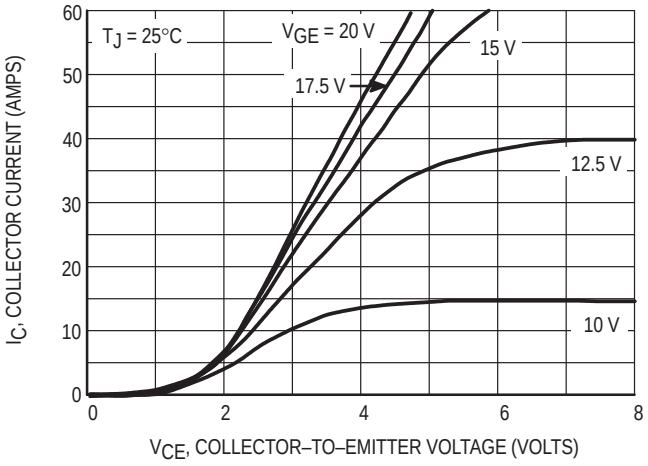


Figure 1. Output Characteristics, T_J = 25°C

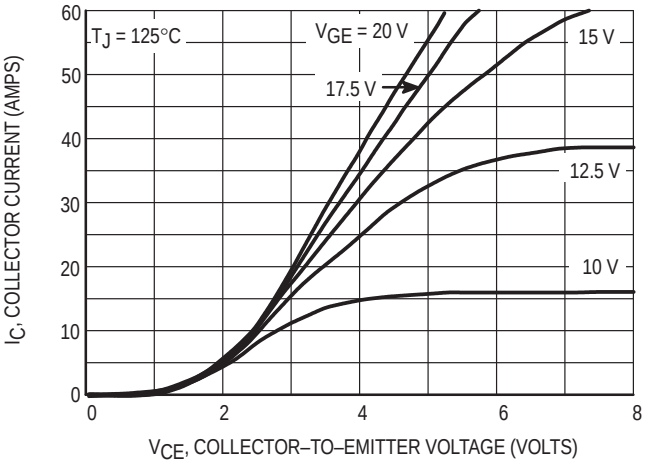


Figure 2. Output Characteristics, T_J = 125°C

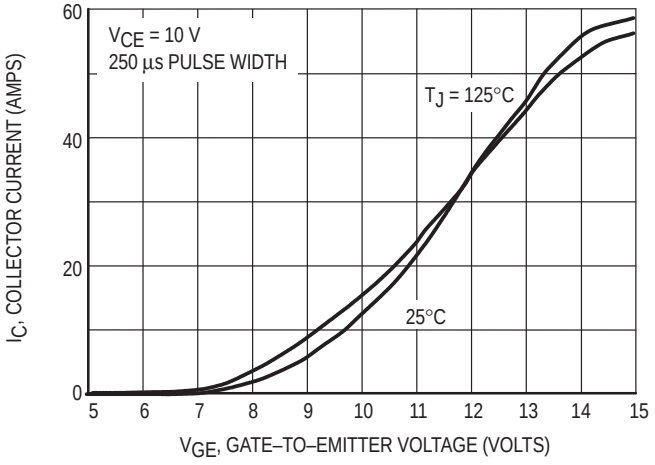


Figure 3. Transfer Characteristics

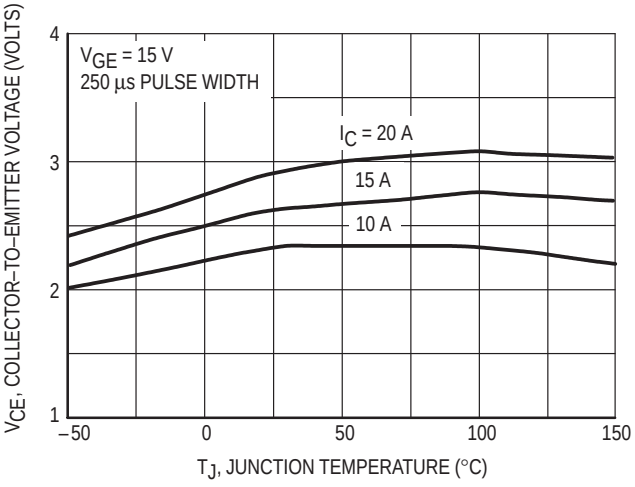


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

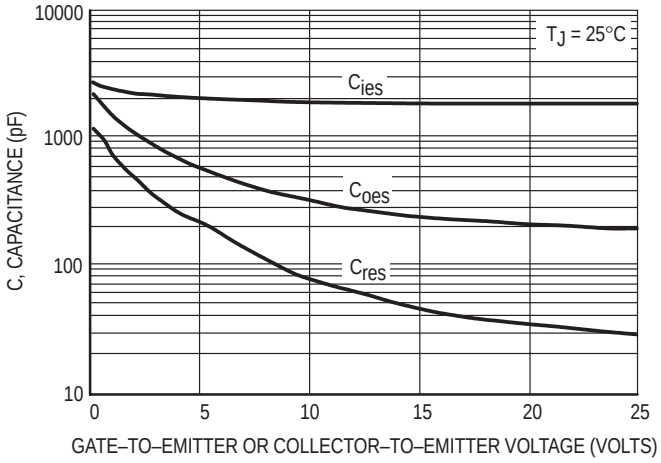


Figure 5. Capacitance Variation

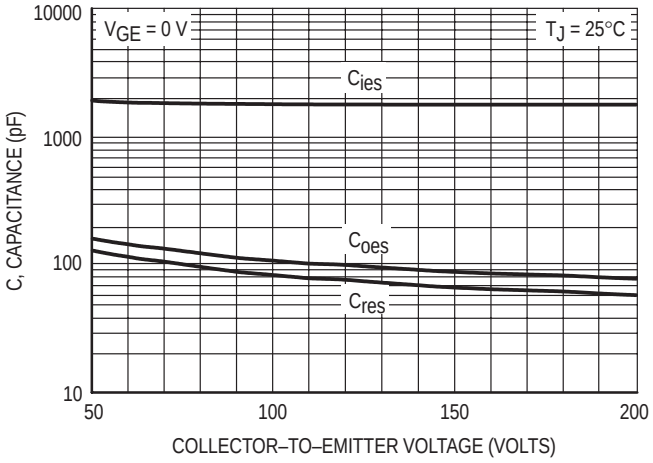


Figure 5b. High Voltage Capacitance Variation

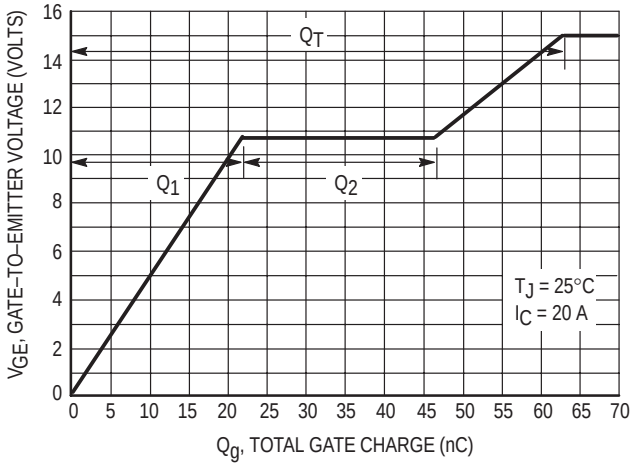


Figure 6. Gate–to–Emitter and Collector–to–Emitter Voltage versus Total Charge

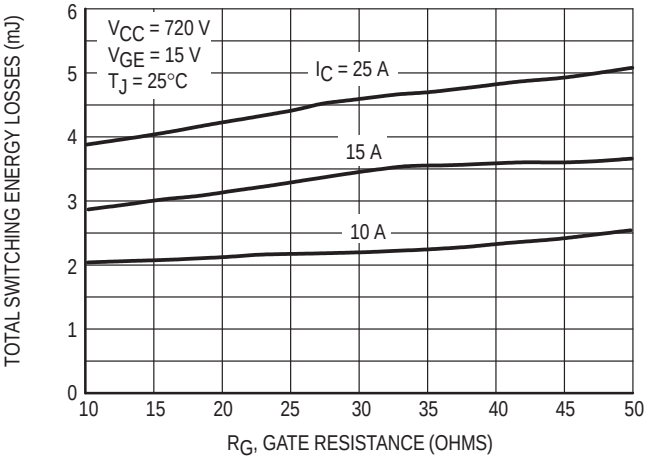


Figure 7. Total Switching Losses versus Gate Resistance

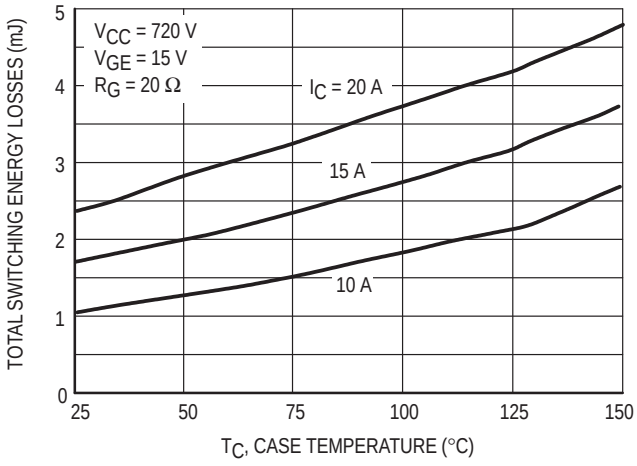


Figure 8. Total Switching Losses versus Case Temperature

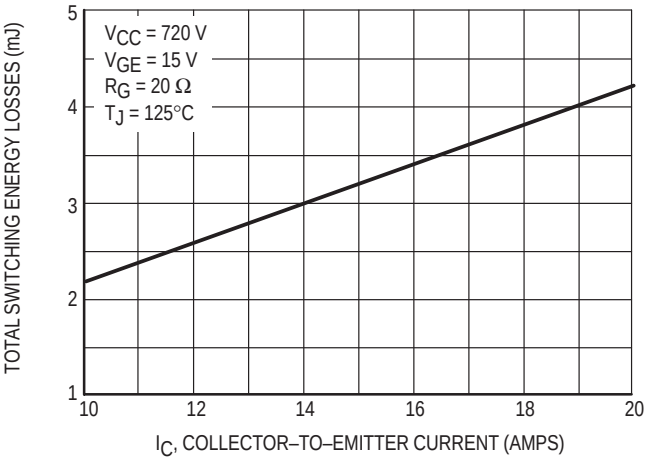


Figure 9. Total Switching Losses versus Collector–to–Emitter Current

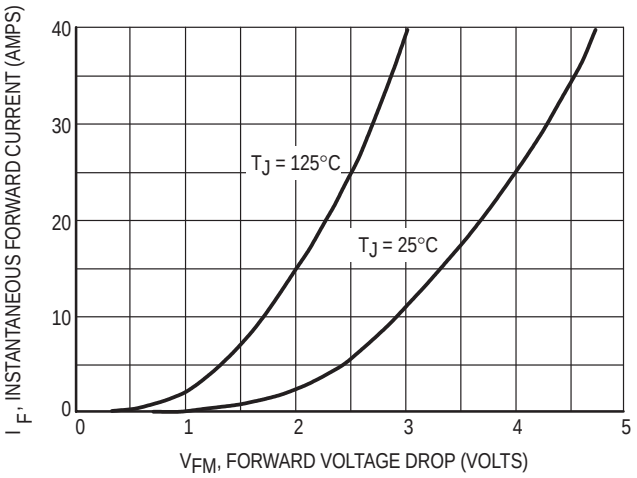


Figure 10. Maximum Forward Drop versus Instantaneous Forward Current

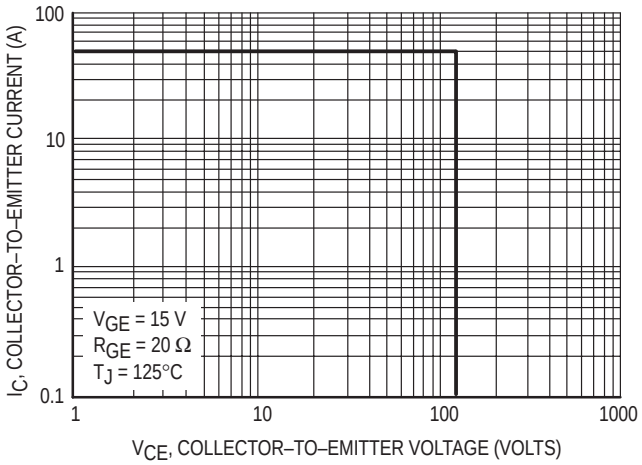


Figure 11. Reverse Biased Safe Operating Area

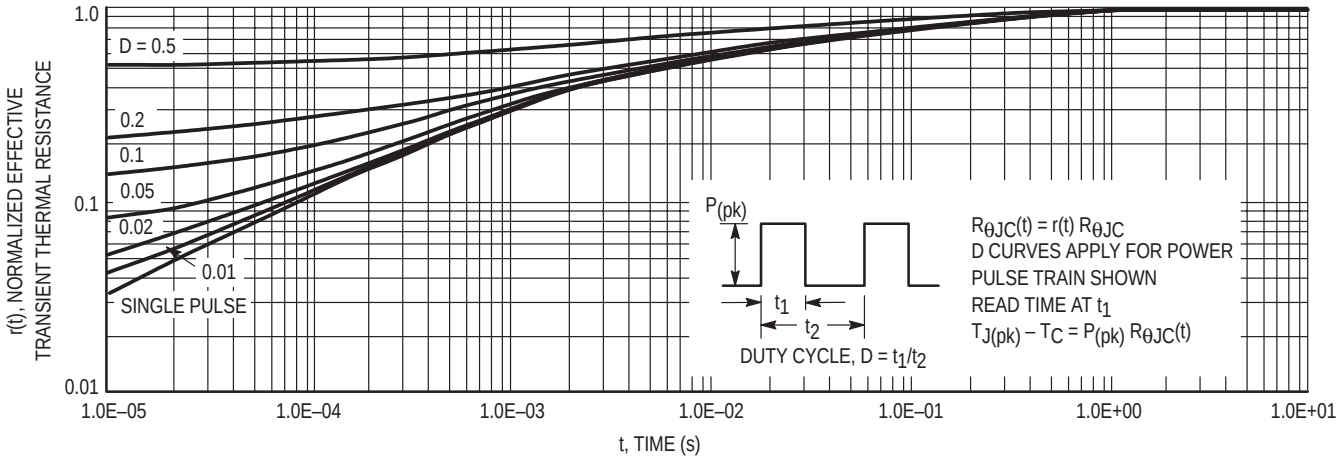


Figure 12. Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

N–Channel Enhancement–Mode Silicon Gate

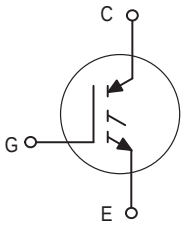
MGY25N120

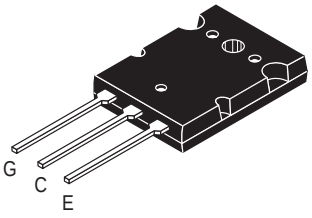
Motorola Preferred Device

IGBT IN TO–264
25 A @ 90°C
38 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time. Fast switching characteristics result in efficient operation at high frequencies.

- Industry Standard High Power TO–264 Package (TO–3PBL)
- High Speed E_{off}: 273 μJ/A typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Robust High Voltage Termination





CASE 340G–02, Style 5
TO–264

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	38 25 76	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	212 1.69	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.6 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)		BV_{CES}	1200	—	—	Vdc
Temperature Coefficient (Positive)			—	960	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		BV_{ECS}	25	—	—	Vdc
Zero Gate Voltage Collector Current		I_{CES}				μAdc
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc)			—	—	100	
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage		$V_{CE(on)}$				Vdc
(V_{GE} = 15 Vdc, I_C = 12.5 Adc)			—	2.37	3.24	
(V_{GE} = 15 Vdc, I_C = 12.5 Adc, T_J = 125°C)			—	2.15	—	
(V_{GE} = 15 Vdc, I_C = 25 Adc)			—	2.98	4.19	
Gate Threshold Voltage		$V_{GE(th)}$				Vdc
(V_{CE} = V_{GE}, I_C = 1.0 mAdc)			4.0	6.0	8.0	
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 25 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	2795	—	pF
Output Capacitance		C_{oes}	—	181	—	
Transfer Capacitance		C_{res}	—	45	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 25°C) Energy losses include “tail”	$t_{d(on)}$	—	91	—	ns
Rise Time		t_r	—	124	—	
Turn–Off Delay Time		$t_{d(off)}$	—	196	—	
Fall Time		t_f	—	310	—	
Turn–Off Switching Loss		E_{off}	—	2.44	4.69	mJ
Turn–On Delay Time	(V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	88	—	ns
Rise Time		t_r	—	126	—	
Turn–Off Delay Time		$t_{d(off)}$	—	236	—	
Fall Time		t_f	—	640	—	
Turn–Off Switching Loss		E_{off}	—	5.40	—	mJ
Gate Charge	(V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc)	Q_T	—	97	—	nC
		Q_1	—	31	—	
		Q_2	—	40	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

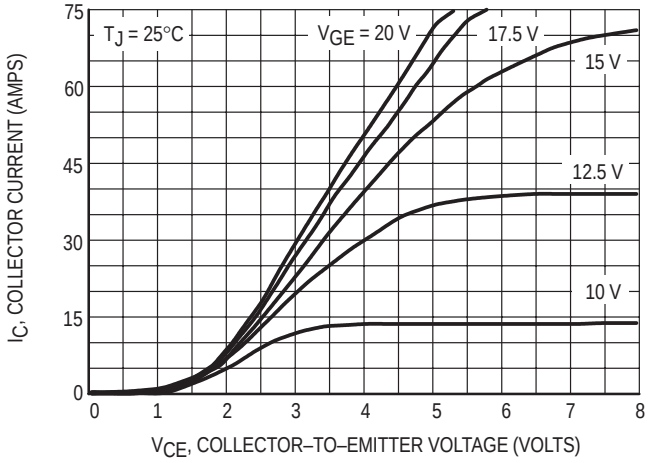


Figure 1. Output Characteristics, T_J = 25°C

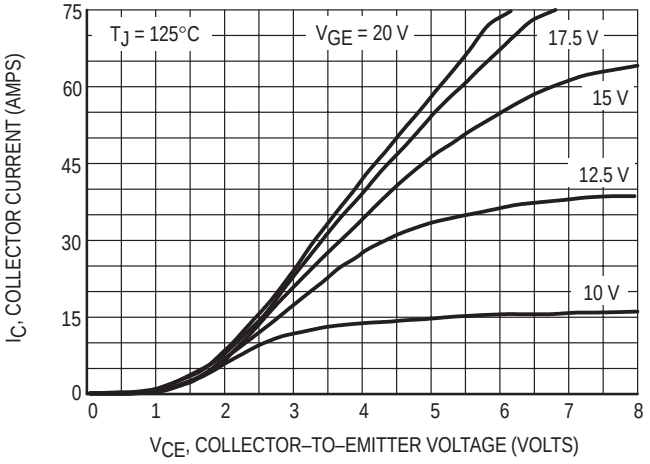


Figure 2. Output Characteristics, T_J = 125°C

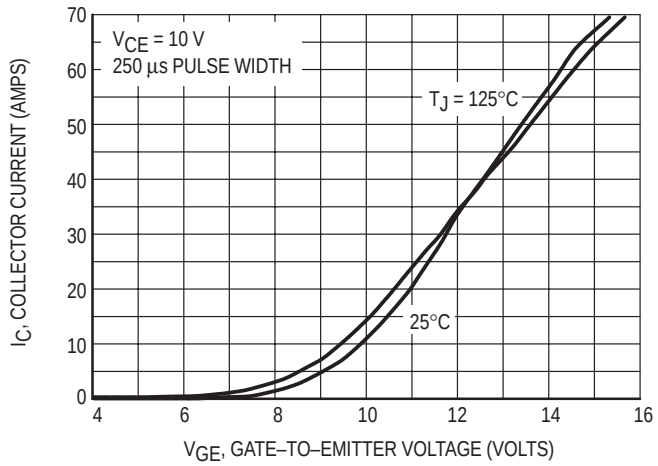


Figure 3. Transfer Characteristics

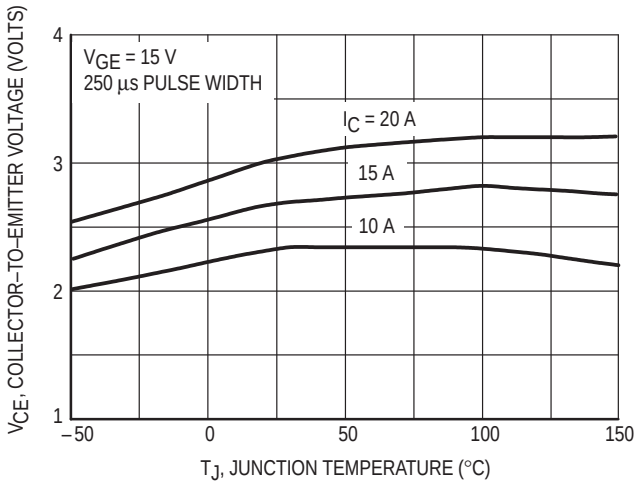


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

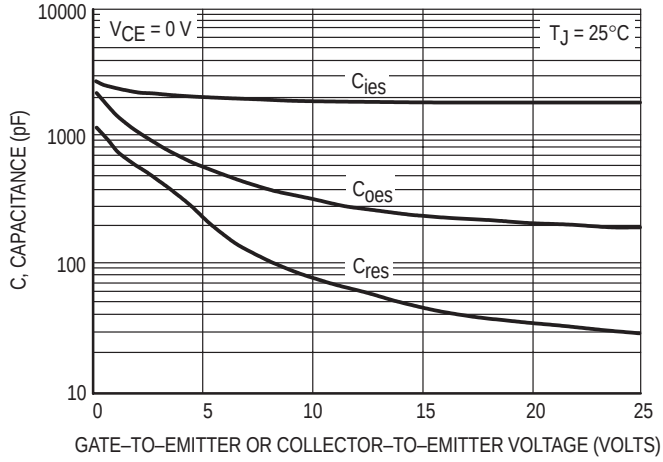


Figure 5. Capacitance Variation

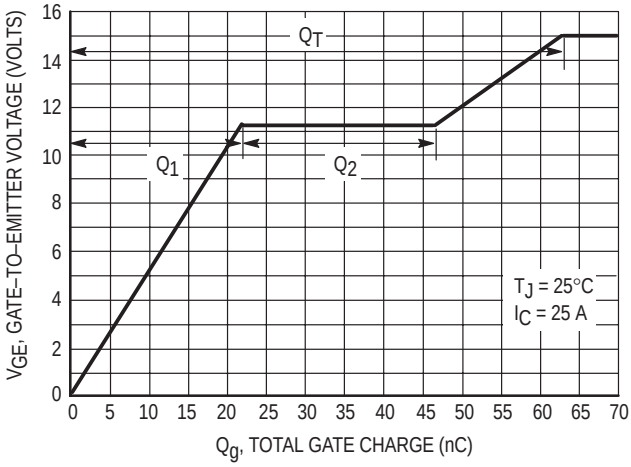


Figure 6. Gate–to–Emitter Voltage versus Total Charge

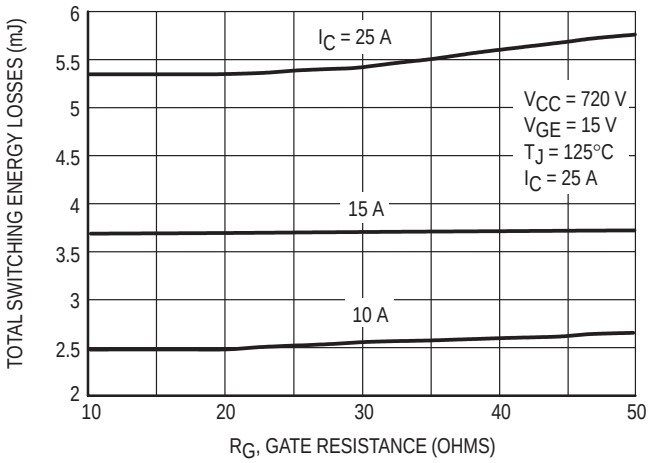


Figure 7. Total Switching Losses versus Gate Resistance

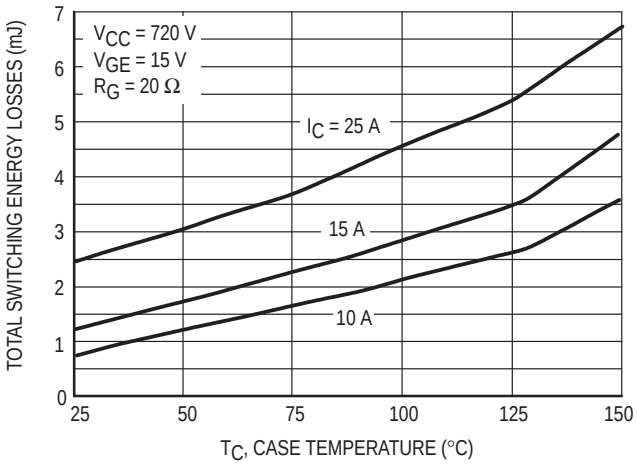


Figure 8. Total Switching Losses versus Case Temperature

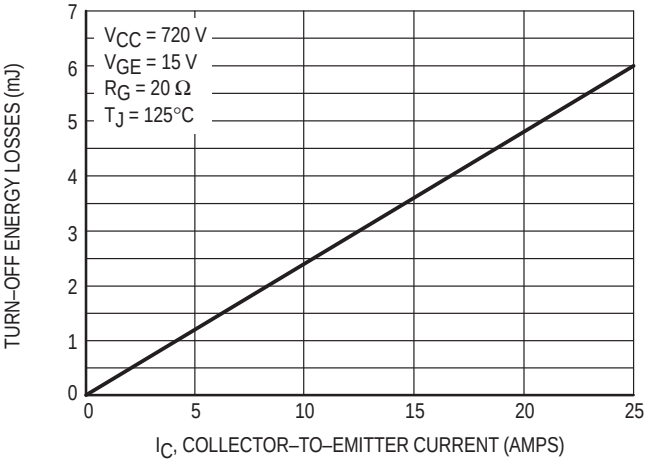


Figure 9. Turn–Off Losses versus Collector–to–Emitter Current

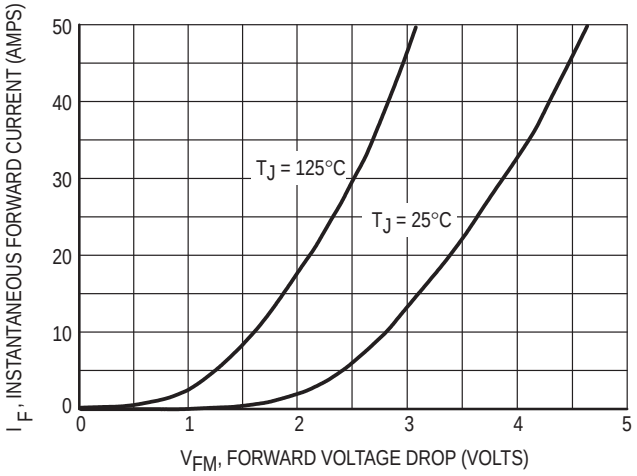


Figure 10. Maximum Forward Drop versus Instantaneous Forward Current

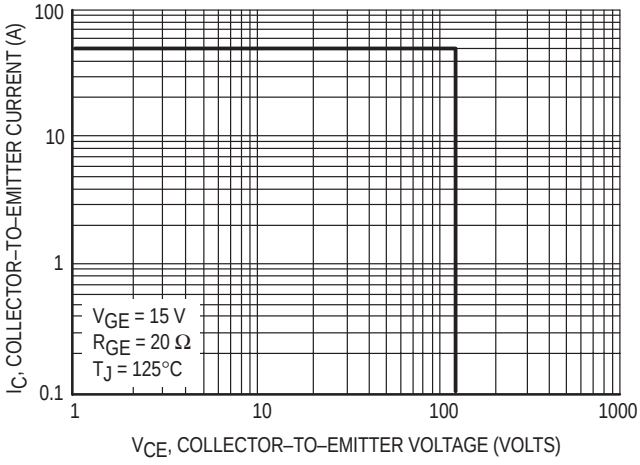


Figure 11. Reverse Biased Safe Operating Area

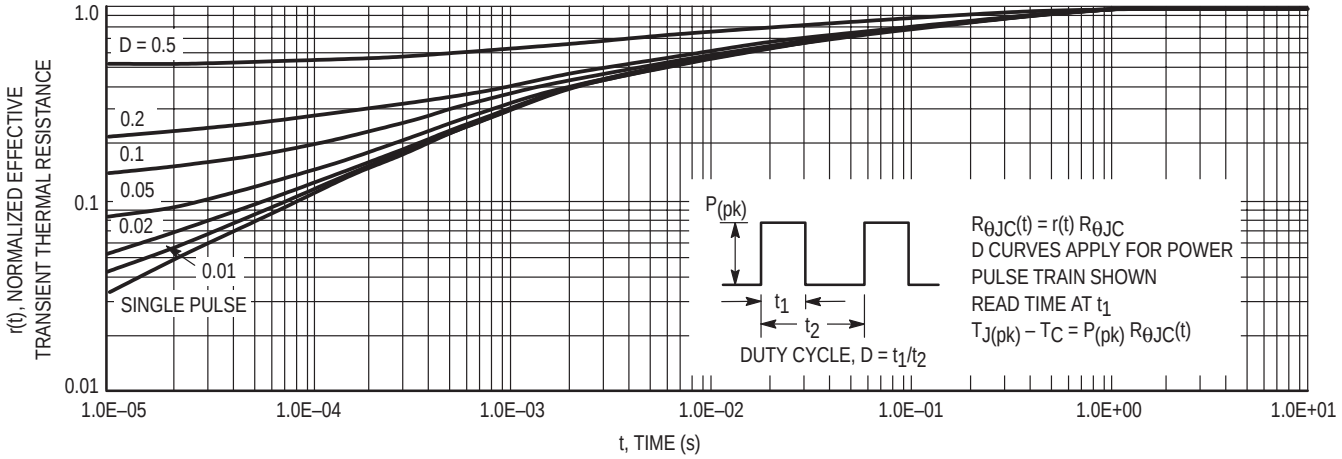


Figure 12. Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N–Channel Enhancement–Mode Silicon Gate

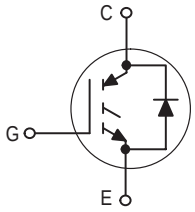
MGY25N120D

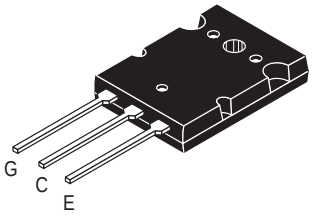
Motorola Preferred Device

IGBT & DIODE IN TO–264
25 A @ 90°C
38 A @ 25°C
1200 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies. Co–packaged IGBT's save space, reduce assembly time and cost.

- Industry Standard High Power TO–264 Package (TO–3PBL)
- High Speed E_{off}: 226 μJ per Amp typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Soft Recovery Free Wheeling Diode is included in the package
- Robust High Voltage Termination
- Robust RBSOA





CASE 340G–02, Style 5
TO–264

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	1200	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	1200	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	38 25 76	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	212 1.69	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 720 Vdc, V_{GE} = 15 Vdc, T_J = 125°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	0.6 0.9 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 25 μAdc)	BV_{CES}	1200	—	—	Vdc
Temperature Coefficient (Positive)		—	960	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc)	I_{CES}	—	—	100	μAdc
(V_{CE} = 1200 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)		—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)	I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)					
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 12.5 Adc)	$V_{CE(on)}$	—	2.37	3.24	Vdc
(V_{GE} = 15 Vdc, I_C = 12.5 Adc, T_J = 125°C)		—	2.15	—	
(V_{GE} = 15 Vdc, I_C = 25 Adc)		—	2.98	4.19	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1.0 mAdc)	$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)		—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 20 Adc)	g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{ies}	—	1859	—	pF
Output Capacitance (V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{oes}	—	198	—	
Transfer Capacitance	C_{res}	—	30	—	
SWITCHING CHARACTERISTICS (1)					
Turn–On Delay Time	$t_{d(on)}$	—	91	—	ns
Rise Time	t_r	—	124	—	
Turn–Off Delay Time (V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 25°C) Energy losses include “tail”	$t_{d(off)}$	—	196	—	
Fall Time	t_f	—	310	—	
Turn–Off Switching Loss	E_{off}	—	2.44	4.69	mJ
Turn–On Switching Loss	E_{on}	—	3.14	9.69	
Total Switching Loss	E_{ts}	—	5.58	14.38	
Turn–On Delay Time	$t_{d(on)}$	—	88	—	ns
Rise Time	t_r	—	126	—	
Turn–Off Delay Time (V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(off)}$	—	236	—	
Fall Time	t_f	—	640	—	
Turn–Off Switching Loss	E_{off}	—	5.40	—	mJ
Turn–On Switching Loss	E_{on}	—	5.03	—	
Total Switching Loss	E_{ts}	—	10.43	—	
Gate Charge	Q_T	—	62	—	nC
(V_{CC} = 720 Vdc, I_C = 25 Adc, V_{GE} = 15 Vdc)	Q_1	—	22	—	
	Q_2	—	25	—	
DIODE CHARACTERISTICS					
Diode Forward Voltage Drop (I_{EC} = 12.5 Adc)	V_{FEC}	—	2.89	3.50	Vdc
(I_{EC} = 12.5 Adc, T_J = 125°C)		—	1.75	—	
(I_{EC} = 25 Adc)		—	3.65	4.45	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 25 Adc, V_R = 720 Vdc, dI_F/dt = 150 A/μs)	t_{rr}	—	114	—	ns
		t_a	—	71	—	
		t_b	—	43	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.65	—	μC
Reverse Recovery Time	(I_F = 25 Adc, V_R = 720 Vdc, dI_F/dt = 150 A/μs, T_J = 125°C)	t_{rr}	—	226	—	ns
		t_a	—	165	—	
		t_b	—	61	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.90	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

TYPICAL ELECTRICAL CHARACTERISTICS

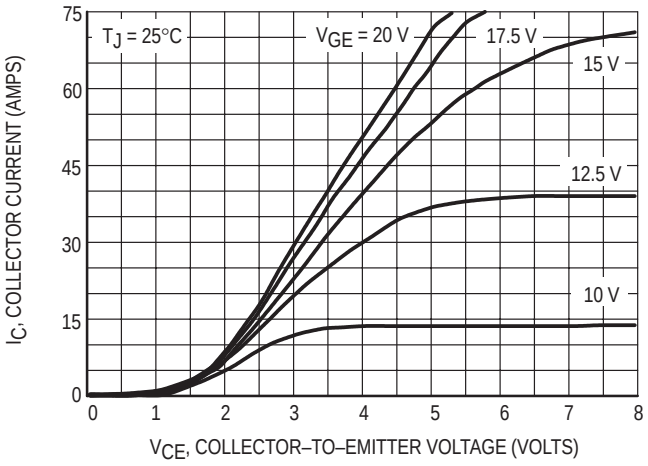


Figure 1. Output Characteristics, T_J = 25°C

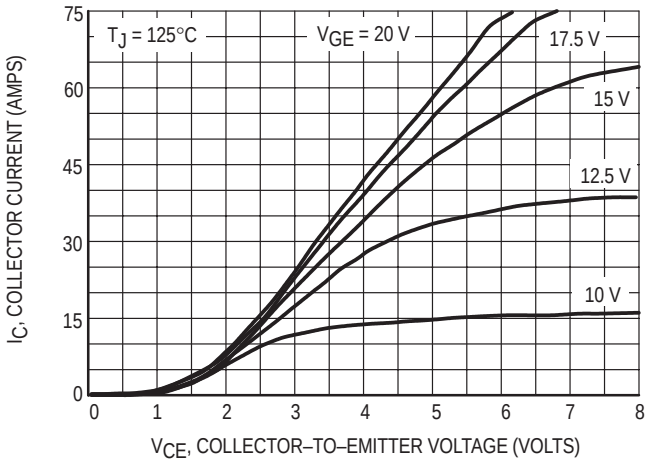


Figure 2. Output Characteristics, T_J = 125°C

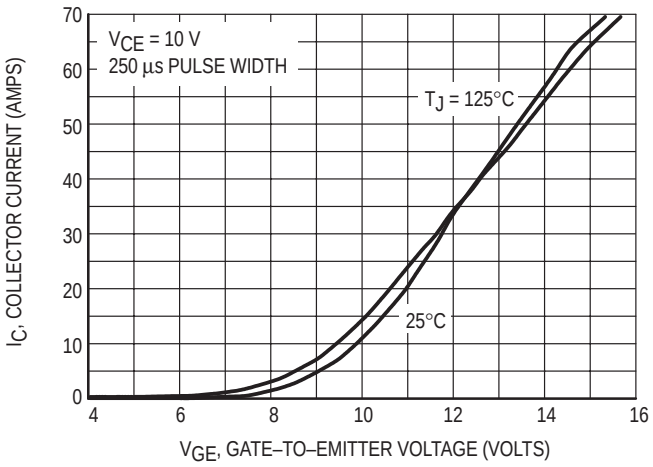


Figure 3. Transfer Characteristics

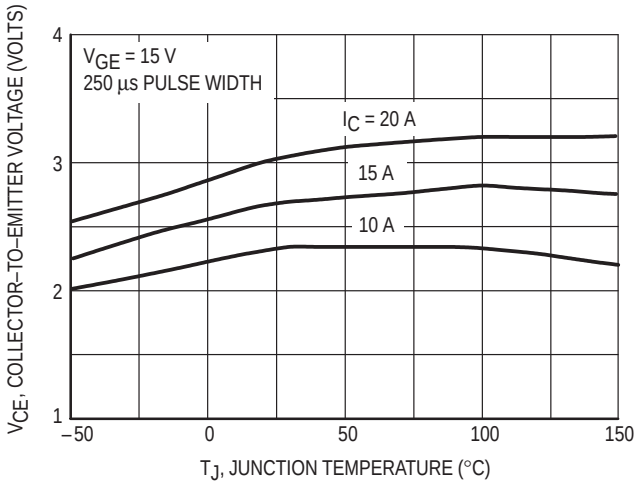


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

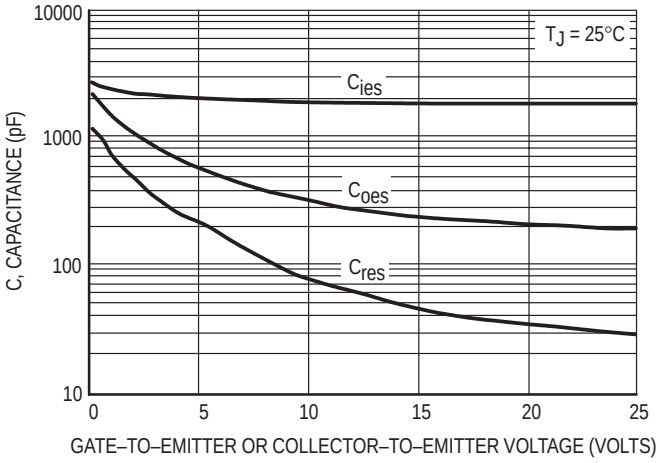


Figure 5. Capacitance Variation

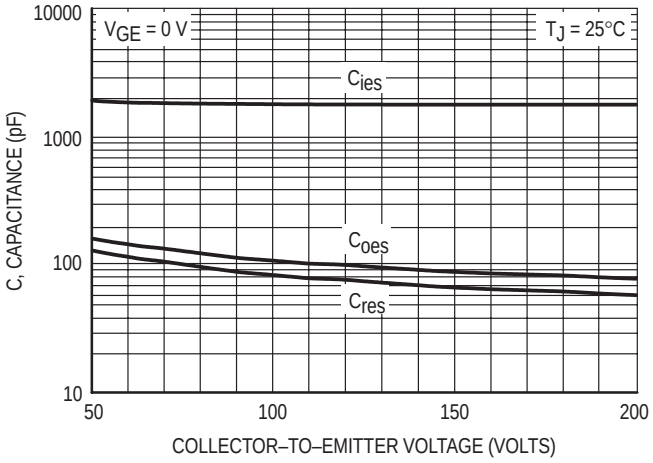


Figure 5b. High Voltage Capacitance Variation

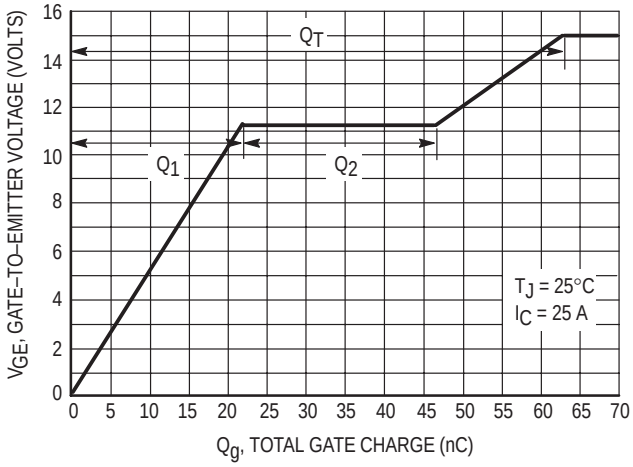


Figure 6. Gate–to–Emitter and Collector–to–Emitter Voltage versus Total Charge

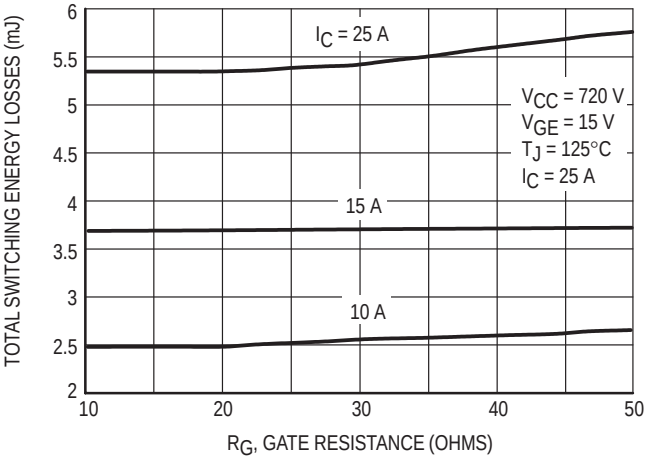


Figure 7. Total Switching Losses versus Gate Resistance

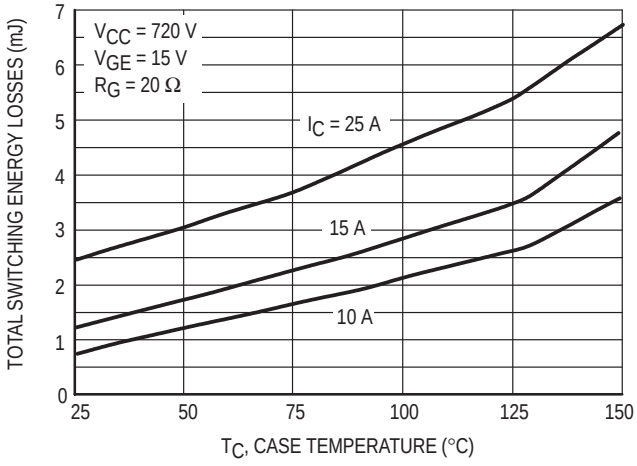


Figure 8. Total Switching Losses versus Case Temperature

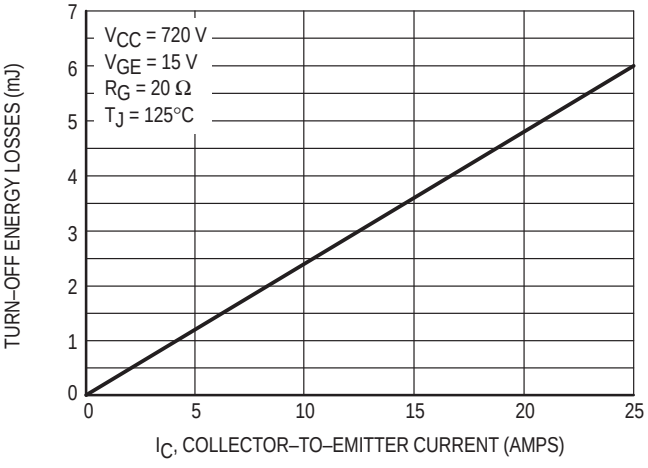


Figure 9. Turn–Off Losses versus Collector–to–Emitter Current

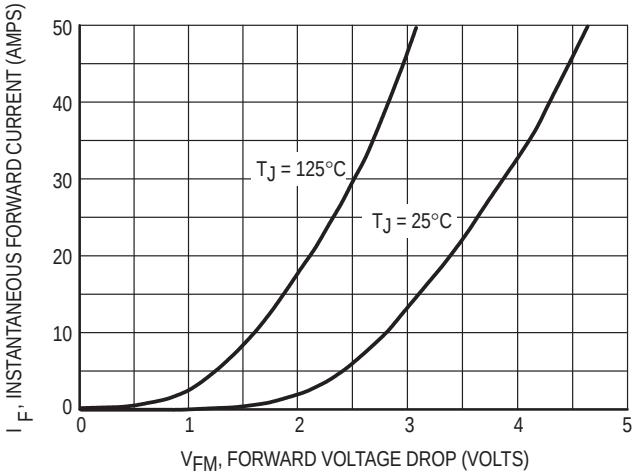


Figure 10. Maximum Forward Drop versus Instantaneous Forward Current

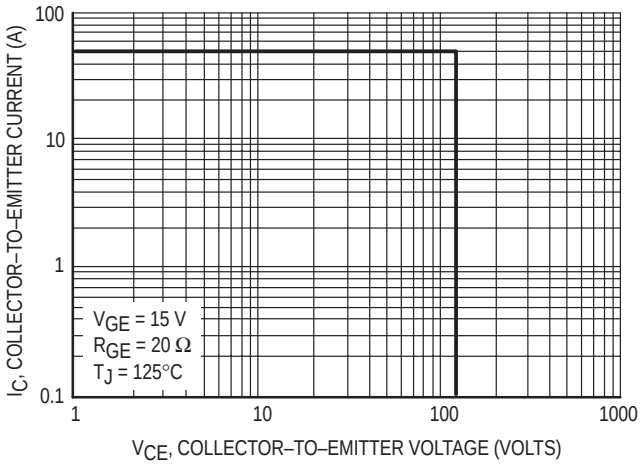


Figure 11. Reverse Biased Safe Operating Area

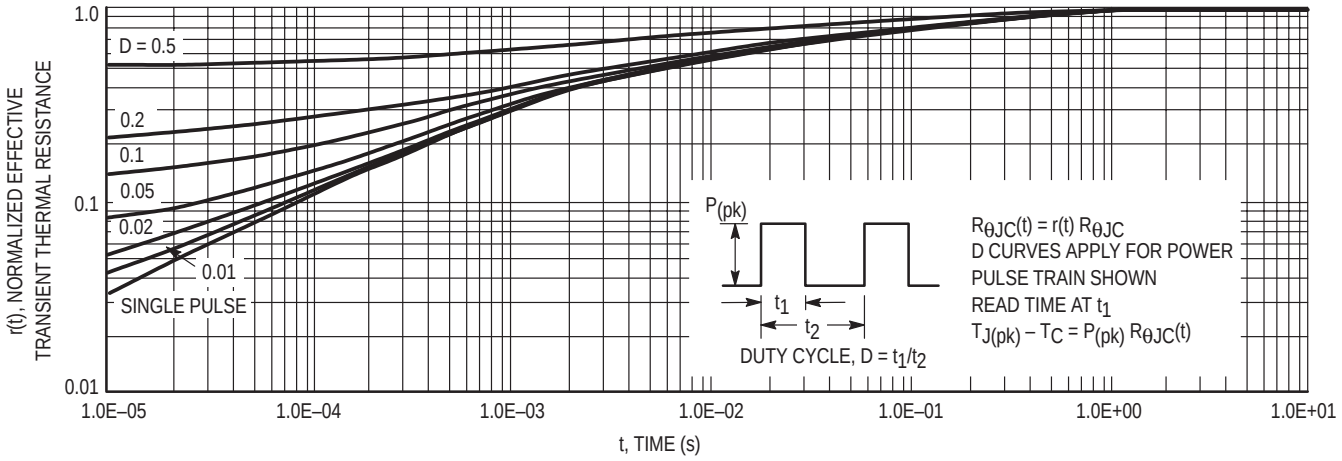


Figure 12. Thermal Response

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N–Channel Enhancement–Mode Silicon Gate

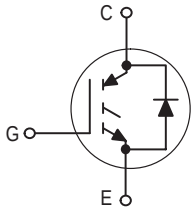
MGY30N60D

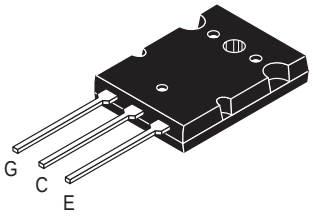
Motorola Preferred Device

IGBT & DIODE IN TO–264
30 A @ 90°C
50 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operations at high frequencies. Co–packaged IGBT's save space, reduce assembly time and cost.

- Industry Standard High Power TO–264 Package (TO–3PBL)
- High Speed E_{off}: 60 μJ per Amp typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Soft Recovery Free Wheeling Diode is included in the package
- Robust High Voltage Termination
- Robust RBSOA





CASE 340G–02, Style 5
TO–264

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	50 30 100	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	202 1.61	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 360 Vdc, V_{GE} = 15 Vdc, T_J = 25°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	0.62 1.41 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc)		BV_{CES}	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	100	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 15 Adc)		$V_{CE(on)}$	—	2.20	2.90	Vdc
(V_{GE} = 15 Vdc, I_C = 15 Adc, T_J = 125°C)			—	2.10	—	
(V_{GE} = 15 Vdc, I_C = 30 Adc)			—	2.60	3.45	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 30 Adc)		g_{fe}	—	15	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	4280	—	pF
Output Capacitance		C_{oes}	—	225	—	
Transfer Capacitance		C_{res}	—	19	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 30 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 25°C) Energy losses include “tail”	$t_{d(on)}$	—	76	—	ns
Rise Time		t_r	—	80	—	
Turn–Off Delay Time		$t_{d(off)}$	—	348	—	
Fall Time		t_f	—	188	—	
Turn–Off Switching Loss		E_{off}	—	0.98	1.28	mJ
Turn–On Switching Loss		E_{on}	—	2.00	—	
Total Switching Loss		E_{ts}	—	2.98	—	
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 30 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	73	—	ns
Rise Time		t_r	—	95	—	
Turn–Off Delay Time		$t_{d(off)}$	—	394	—	
Fall Time		t_f	—	418	—	
Turn–Off Switching Loss		E_{off}	—	1.90	—	mJ
Turn–On Switching Loss		E_{on}	—	3.10	—	
Total Switching Loss		E_{ts}	—	5.00	—	
Gate Charge	(V_{CC} = 360 Vdc, I_C = 30 Adc, V_{GE} = 15 Vdc)	Q_T	—	150	—	nC
		Q_1	—	30	—	
		Q_2	—	45	—	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 15 Adc)		V_{FEC}	—	1.30	1.80	Vdc
(I_{EC} = 15 Adc, T_J = 125°C)			—	1.10	—	
(I_{EC} = 30 Adc)			—	1.45	2.05	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 30 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs)	t_{rr}	—	153	—	ns
		t_a	—	82	—	
		t_b	—	71	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.3	—	μC
Reverse Recovery Time	(I_F = 30 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs, T_J = 125°C)	t_{rr}	—	208	—	ns
		t_a	—	117	—	
		t_b	—	91	—	
Reverse Recovery Stored Charge		Q_{RR}	—	3.8	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

TYPICAL ELECTRICAL CHARACTERISTICS

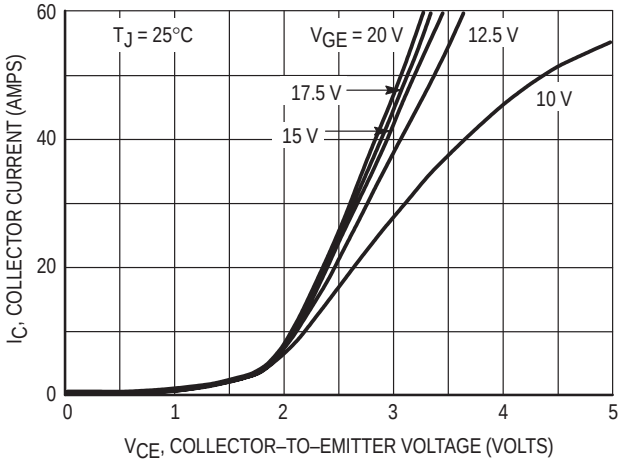


Figure 1. Output Characteristics, T_J = 25°C

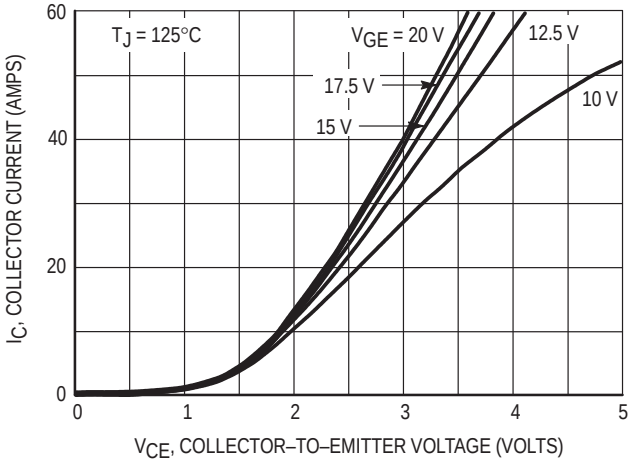


Figure 2. Output Characteristics, T_J = 125°C

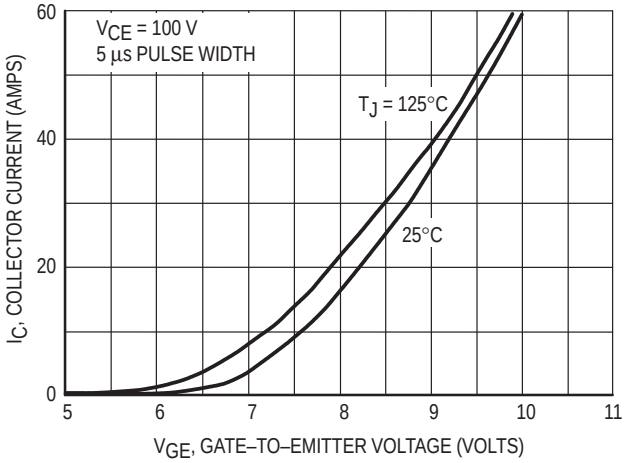


Figure 3. Transfer Characteristics

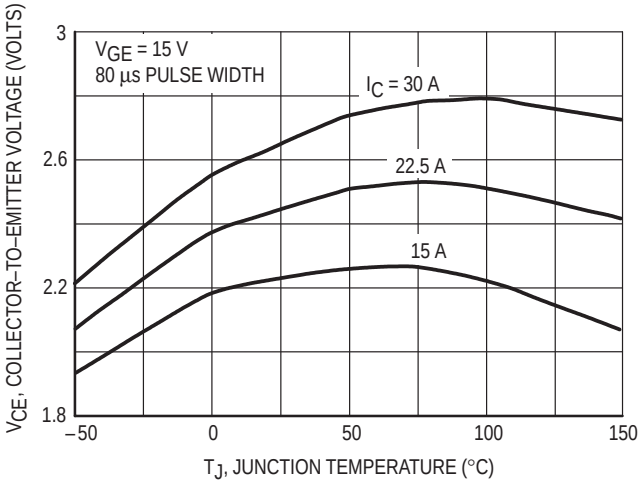


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

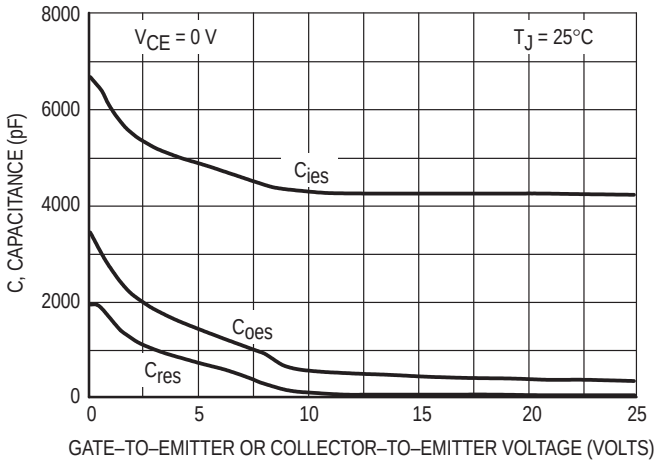


Figure 5. Capacitance Variation

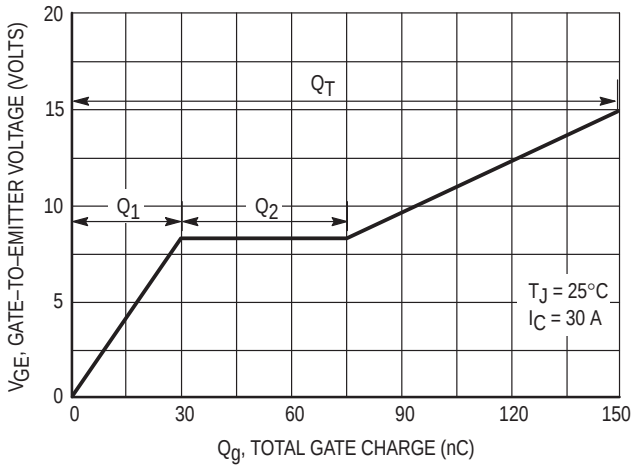


Figure 6. Gate–to–Emitter Voltage versus Total Charge

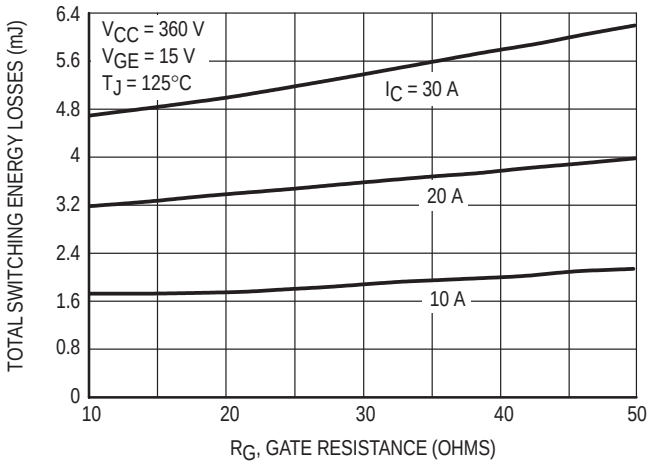


Figure 7. Total Switching Losses versus Gate Resistance

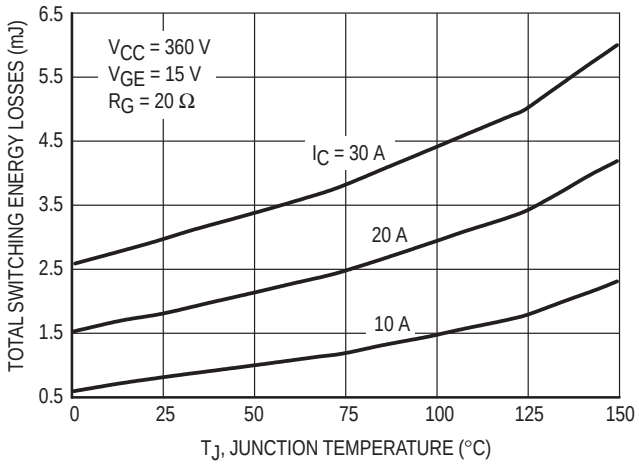


Figure 8. Total Switching Losses versus Junction Temperature

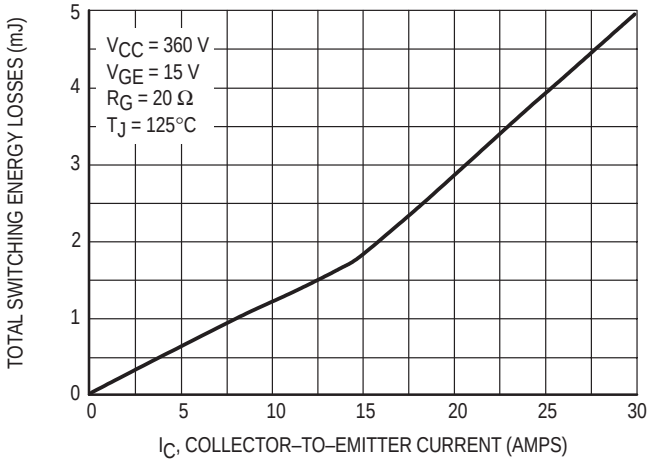


Figure 9. Total Switching Losses versus Collector–to–Emitter Current

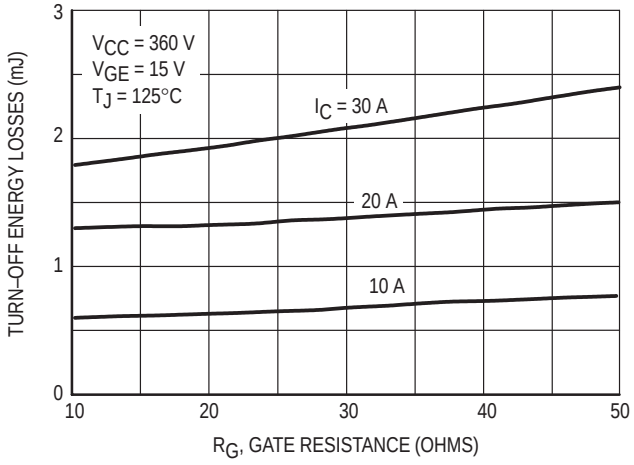


Figure 10. Turn–Off Losses versus Gate Resistance

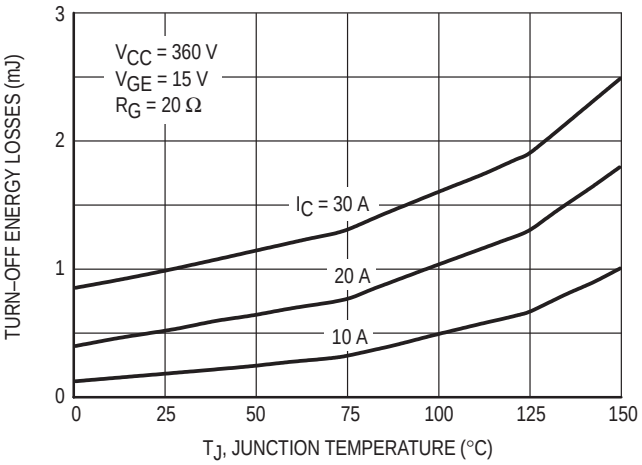


Figure 11. Turn–Off Losses versus Junction Temperature

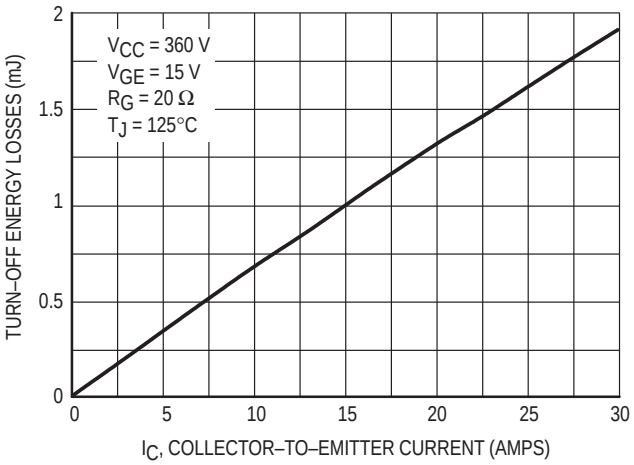


Figure 12. Turn–Off Losses versus Collector–to–Emitter Current

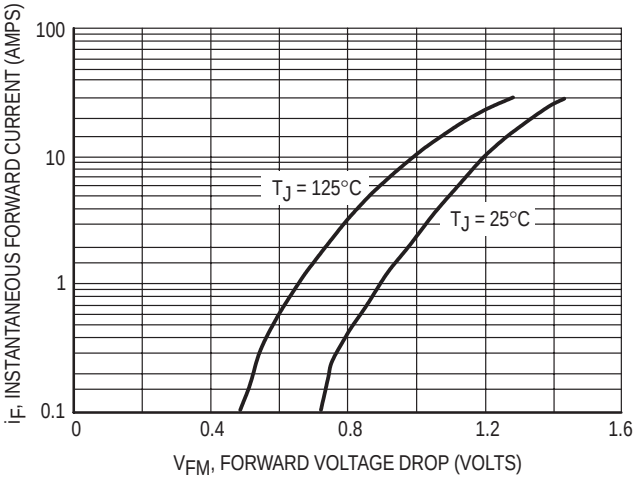


Figure 13. Typical Diode Forward Drop versus Instantaneous Forward Current

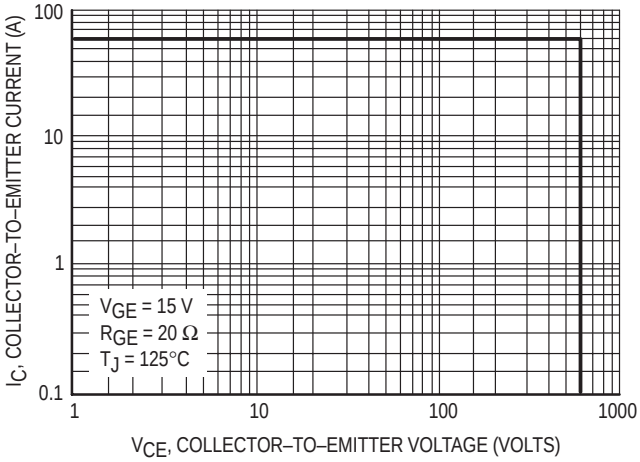


Figure 14. Reverse Biased Safe Operating Area

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor

N–Channel Enhancement–Mode Silicon Gate

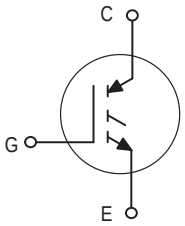
MGY40N60

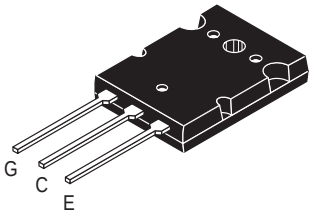
Motorola Preferred Device

IGBT IN TO–264
40 A @ 90°C
66 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operations at high frequencies.

- Industry Standard High Power TO–264 Package (TO–3PBL)
- High Speed E_{off}: 60 μJ per Amp typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Robust High Voltage Termination
- Robust RBSOA





CASE 340G–02, Style 5
TO–264

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	66 40 132	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	260 2.08	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 360 Vdc, V_{GE} = 15 Vdc, T_J = 25°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.48 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc)		BV_{CES}	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Emitter–to–Collector Breakdown Voltage (V_{GE} = 0 Vdc, I_{EC} = 100 mAdc)		BV_{ECS}	25	—	—	Vdc
Zero Gate Voltage Collector Current		I_{CES}				μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)			—	—	100	
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage		$V_{CE(on)}$				Vdc
(V_{GE} = 15 Vdc, I_C = 20 Adc)			—	2.20	2.80	
(V_{GE} = 15 Vdc, I_C = 20 Adc, T_J = 125°C)			—	2.10	—	
(V_{GE} = 15 Vdc, I_C = 40 Adc)			—	2.60	3.25	
Gate Threshold Voltage		$V_{GE(th)}$				Vdc
(V_{CE} = V_{GE}, I_C = 1 mAdc)			4.0	6.0	8.0	
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 40 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	6810	—	pF
Output Capacitance		C_{oes}	—	464	—	
Transfer Capacitance		C_{res}	—	15	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 40 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 25°C) Energy losses include “tail”	$t_{d(on)}$	—	126	—	ns
Rise Time		t_r	—	95	—	
Turn–Off Delay Time		$t_{d(off)}$	—	530	—	
Fall Time		t_f	—	180	—	
Turn–Off Switching Loss		E_{off}	—	1.50	2.10	mJ
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 40 Adc, V_{GE} = 15 Vdc, L = 300 μH, R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	113	—	ns
Rise Time		t_r	—	104	—	
Turn–Off Delay Time		$t_{d(off)}$	—	588	—	
Fall Time		t_f	—	346	—	
Turn–Off Switching Loss		E_{off}	—	2.70	—	mJ
Gate Charge	(V_{CC} = 360 Vdc, I_C = 40 Adc, V_{GE} = 15 Vdc)	Q_T	—	248	—	nC
		Q_1	—	49	—	
		Q_2	—	81	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

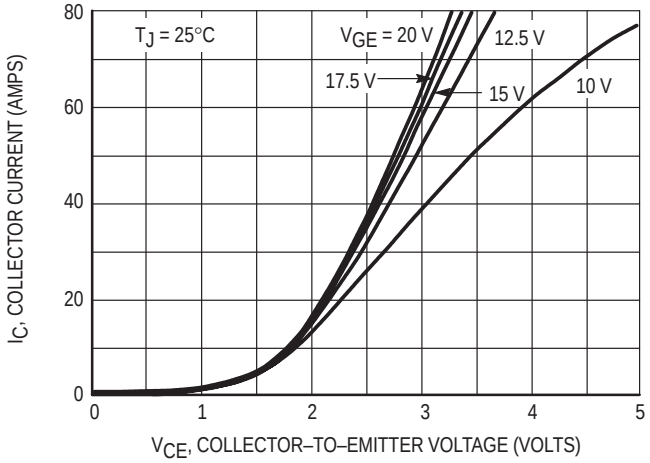


Figure 1. Output Characteristics, T_J = 25°C

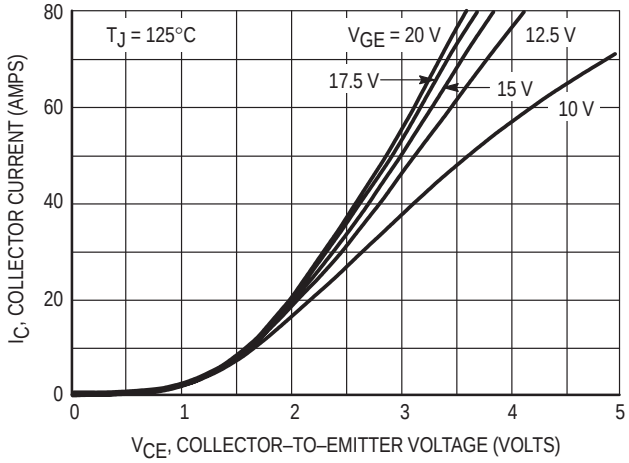


Figure 2. Output Characteristics, T_J = 125°C

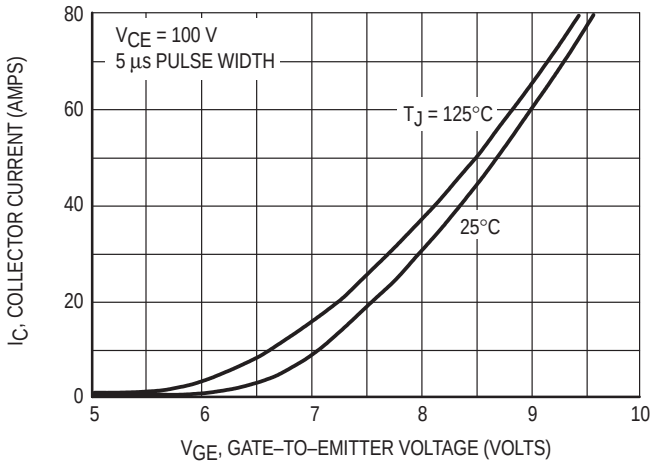


Figure 3. Transfer Characteristics

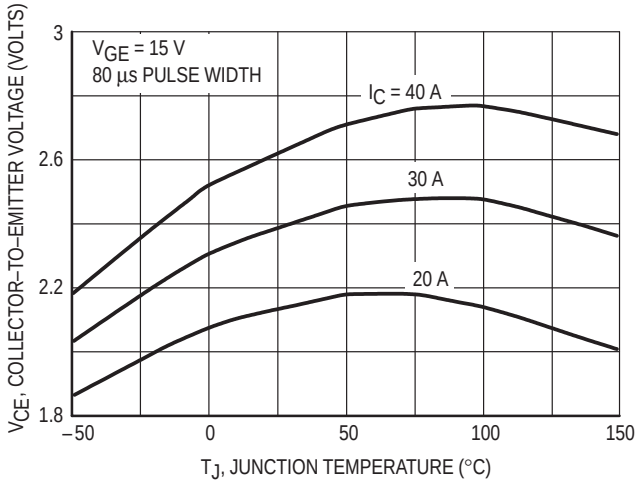


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

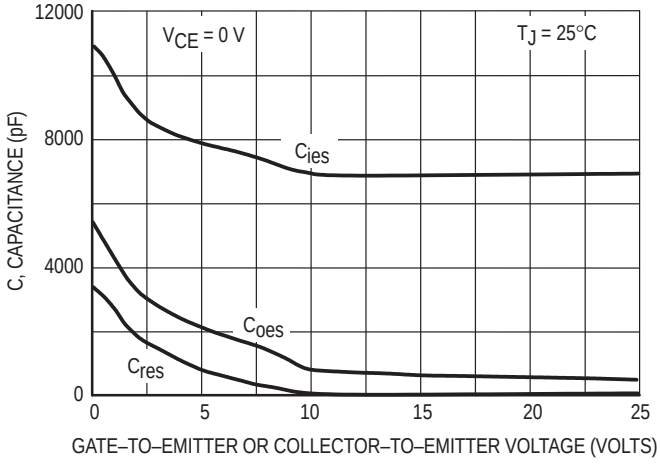


Figure 5. Capacitance Variation

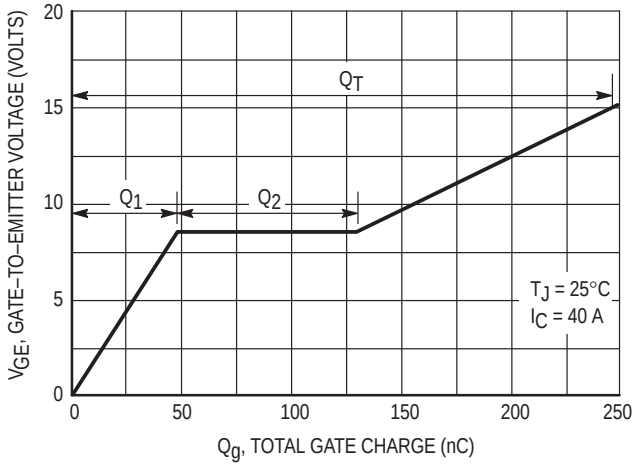


Figure 6. Gate–to–Emitter Voltage versus Total Charge

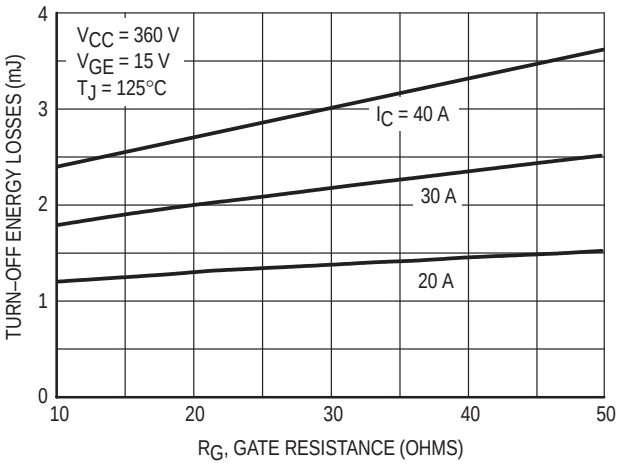


Figure 7. Turn–Off Losses versus Gate Resistance

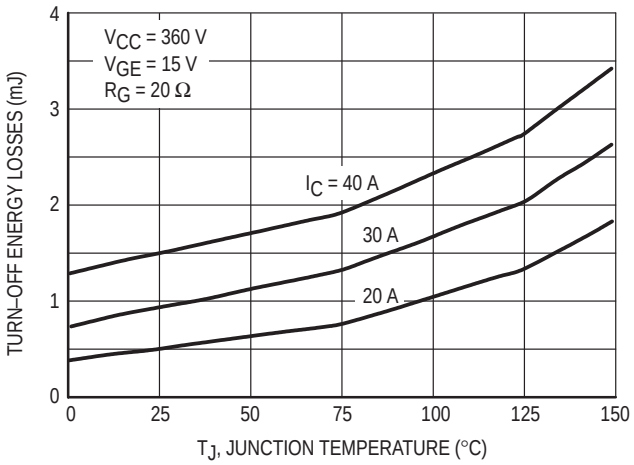


Figure 8. Turn–Off Losses versus Junction Temperature

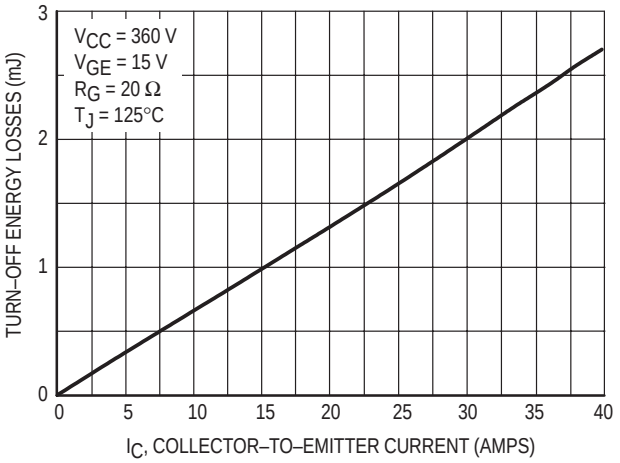


Figure 9. Turn–Off Losses versus Collector–to–Emitter Current

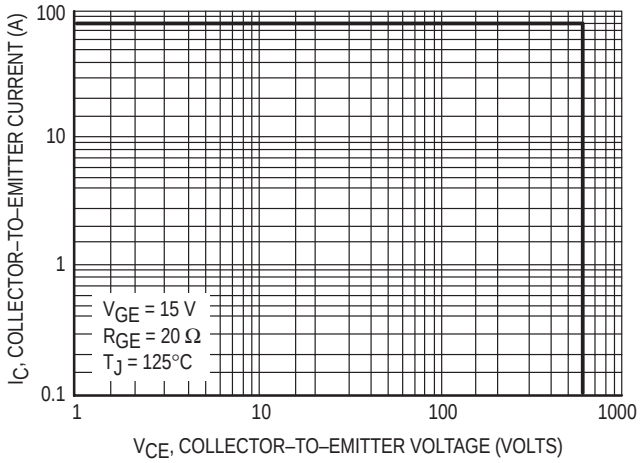


Figure 10. Reverse Biased Safe Operating Area

Designer's™ Data Sheet

Insulated Gate Bipolar Transistor with Anti-Parallel Diode

N–Channel Enhancement–Mode Silicon Gate

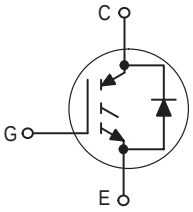
MGY40N60D

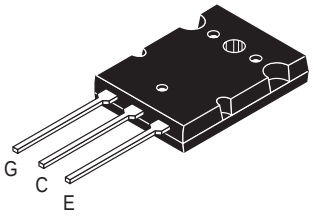
Motorola Preferred Device

IGBT & DIODE IN TO–264
40 A @ 90°C
66 A @ 25°C
600 VOLTS
SHORT CIRCUIT RATED

This Insulated Gate Bipolar Transistor (IGBT) is co–packaged with a soft recovery ultra–fast rectifier and uses an advanced termination scheme to provide an enhanced and reliable high voltage–blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operations at high frequencies. Co–packaged IGBT's save space, reduce assembly time and cost.

- Industry Standard High Power TO–264 Package (TO–3PBL)
- High Speed E_{off}: 60 μJ per Amp typical at 125°C
- High Short Circuit Capability – 10 μs minimum
- Soft Recovery Free Wheeling Diode is included in the package
- Robust High Voltage Termination
- Robust RBSOA





CASE 340G–02, Style 5
TO–264

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CES}	600	Vdc
Collector–Gate Voltage (R_{GE} = 1.0 MΩ)	V_{CGR}	600	Vdc
Gate–Emitter Voltage — Continuous	V_{GE}	±20	Vdc
Collector Current — Continuous @ T_C = 25°C — Continuous @ T_C = 90°C — Repetitive Pulsed Current (1)	I_{C25} I_{C90} I_{CM}	66 40 132	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	260 2.08	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to 150	°C
Short Circuit Withstand Time (V_{CC} = 360 Vdc, V_{GE} = 15 Vdc, T_J = 25°C, R_G = 20 Ω)	t_{sc}	10	μs
Thermal Resistance — Junction to Case – IGBT — Junction to Case – Diode — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JC}$ $R_{\theta JA}$	0.48 1.13 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C
Mounting Torque, 6–32 or M3 screw	10 lbf•in (1.13 N•m)		

(1) Pulse width is limited by maximum junction temperature.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector–to–Emitter Breakdown Voltage (V_{GE} = 0 Vdc, I_C = 250 μAdc)		BV_{CES}	600	—	—	Vdc
Temperature Coefficient (Positive)			—	870	—	mV/°C
Zero Gate Voltage Collector Current (V_{CE} = 600 Vdc, V_{GE} = 0 Vdc)		I_{CES}	—	—	100	μAdc
(V_{CE} = 600 Vdc, V_{GE} = 0 Vdc, T_J = 125°C)			—	—	2500	
Gate–Body Leakage Current (V_{GE} = ± 20 Vdc, V_{CE} = 0 Vdc)		I_{GES}	—	—	250	nAdc
ON CHARACTERISTICS (1)						
Collector–to–Emitter On–State Voltage (V_{GE} = 15 Vdc, I_C = 20 Adc)		$V_{CE(on)}$	—	2.20	2.80	Vdc
(V_{GE} = 15 Vdc, I_C = 20 Adc, T_J = 125°C)			—	2.10	—	
(V_{GE} = 15 Vdc, I_C = 40 Adc)			—	2.60	3.25	
Gate Threshold Voltage (V_{CE} = V_{GE}, I_C = 1 mAdc)		$V_{GE(th)}$	4.0	6.0	8.0	Vdc
Threshold Temperature Coefficient (Negative)			—	10	—	mV/°C
Forward Transconductance (V_{CE} = 10 Vdc, I_C = 40 Adc)		g_{fe}	—	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{CE} = 25 Vdc, V_{GE} = 0 Vdc, f = 1.0 MHz)	C_{ies}	—	6810	—	pF
Output Capacitance		C_{oes}	—	464	—	
Transfer Capacitance		C_{res}	—	15	—	
SWITCHING CHARACTERISTICS (1)						
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 40 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 25°C) Energy losses include “tail”	$t_{d(on)}$	—	126	—	ns
Rise Time		t_r	—	95	—	
Turn–Off Delay Time		$t_{d(off)}$	—	530	—	
Fall Time		t_f	—	180	—	
Turn–Off Switching Loss		E_{off}	—	1.50	2.10	mJ
Turn–On Switching Loss		E_{on}	—	2.30	—	
Total Switching Loss		E_{ts}	—	3.80	—	
Turn–On Delay Time	(V_{CC} = 360 Vdc, I_C = 40 Adc, V_{GE} = 15 Vdc, L = 300 μH R_G = 20 Ω, T_J = 125°C) Energy losses include “tail”	$t_{d(on)}$	—	113	—	ns
Rise Time		t_r	—	104	—	
Turn–Off Delay Time		$t_{d(off)}$	—	588	—	
Fall Time		t_f	—	346	—	
Turn–Off Switching Loss		E_{off}	—	2.70	—	mJ
Turn–On Switching Loss		E_{on}	—	3.80	—	
Total Switching Loss		E_{ts}	—	6.50	—	
Gate Charge	(V_{CC} = 360 Vdc, I_C = 40 Adc, V_{GE} = 15 Vdc)	Q_T	—	248	—	nC
		Q_1	—	49	—	
		Q_2	—	81	—	
DIODE CHARACTERISTICS						
Diode Forward Voltage Drop (I_{EC} = 20 Adc)		V_{FEC}	—	1.19	1.70	Vdc
(I_{EC} = 20 Adc, T_J = 125°C)			—	1.04	—	
(I_{EC} = 40 Adc)			—	1.36	2.00	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
DIODE CHARACTERISTICS — continued						
Reverse Recovery Time	(I_F = 40 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs)	t_{rr}	—	138	—	ns
		t_a	—	78	—	
		t_b	—	60	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.1	—	μC
Reverse Recovery Time	(I_F = 40 Adc, V_R = 360 Vdc, dI_F/dt = 200 A/μs, T_J = 125°C)	t_{rr}	—	213	—	ns
		t_a	—	122	—	
		t_b	—	91	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4.9	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Emitter Inductance (Measured from the emitter lead 0.25″ from package to emitter bond pad)		L_E	—	13	—	nH

TYPICAL ELECTRICAL CHARACTERISTICS

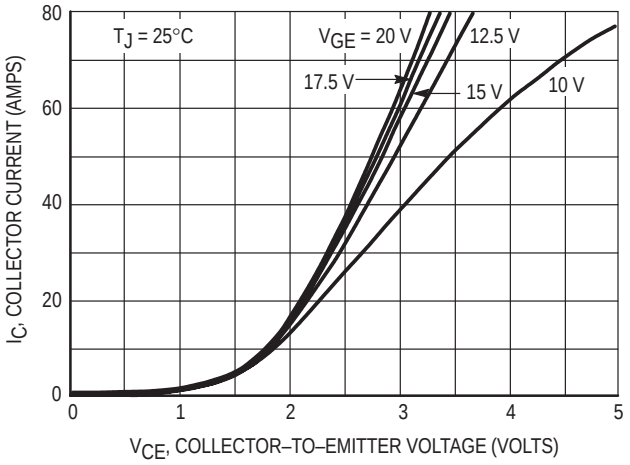


Figure 1. Output Characteristics, T_J = 25°C

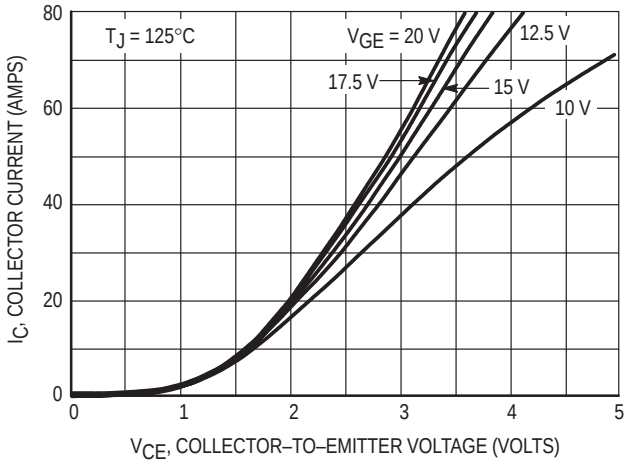


Figure 2. Output Characteristics, T_J = 125°C

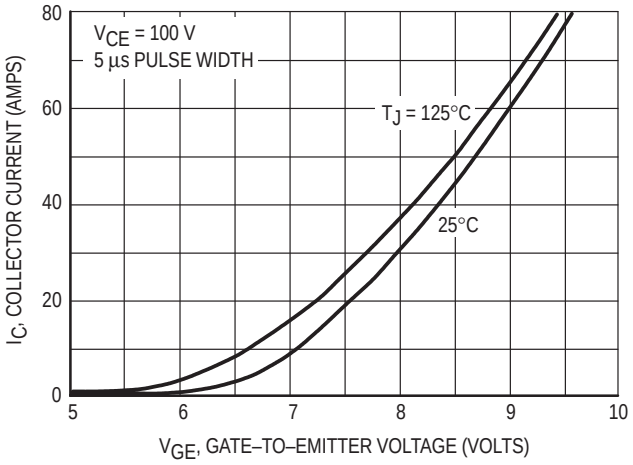


Figure 3. Transfer Characteristics

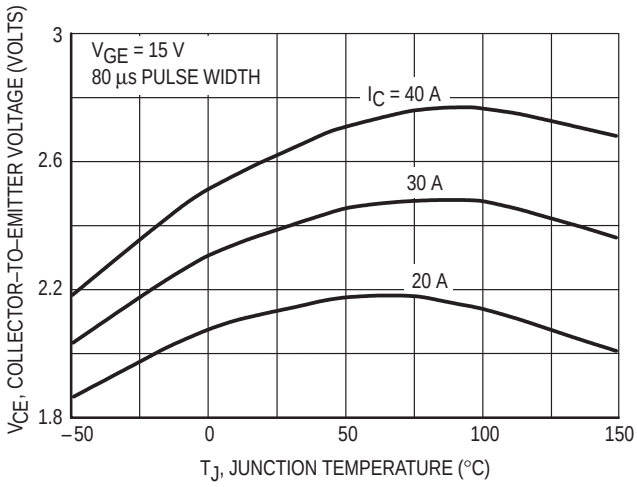


Figure 4. Collector–to–Emitter Saturation Voltage versus Junction Temperature

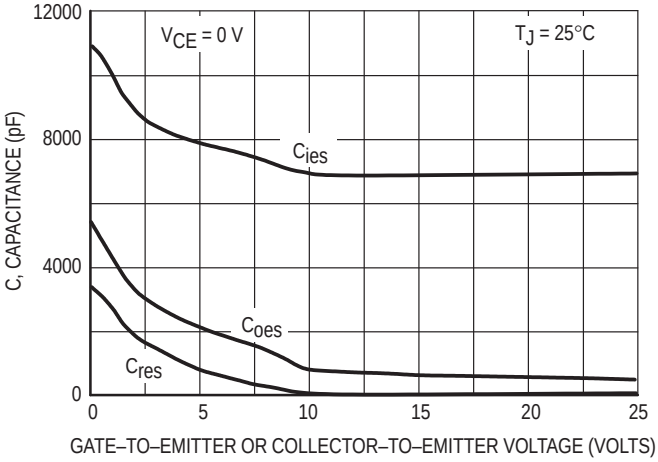


Figure 5. Capacitance Variation

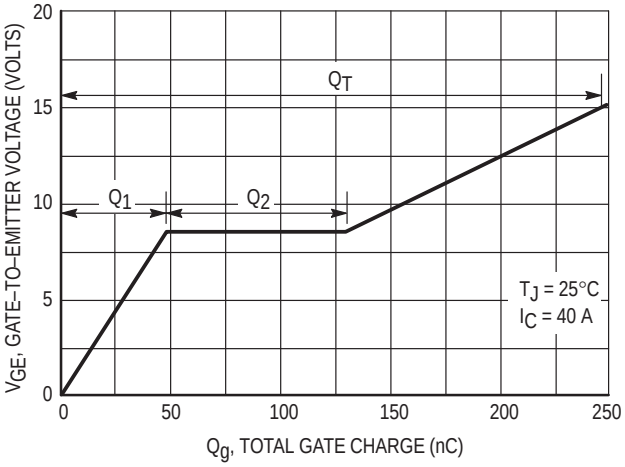


Figure 6. Gate–to–Emitter Voltage versus Total Charge

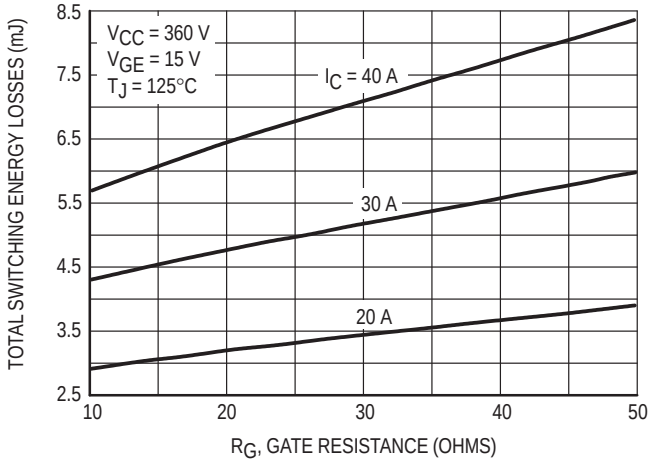


Figure 7. Total Switching Losses versus Gate Resistance

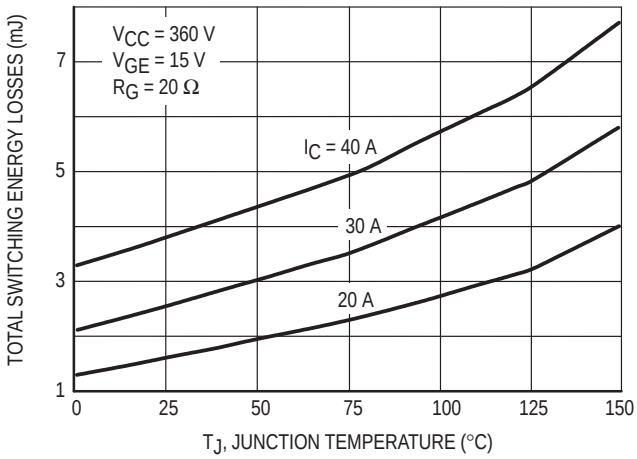


Figure 8. Total Switching Losses versus Junction Temperature

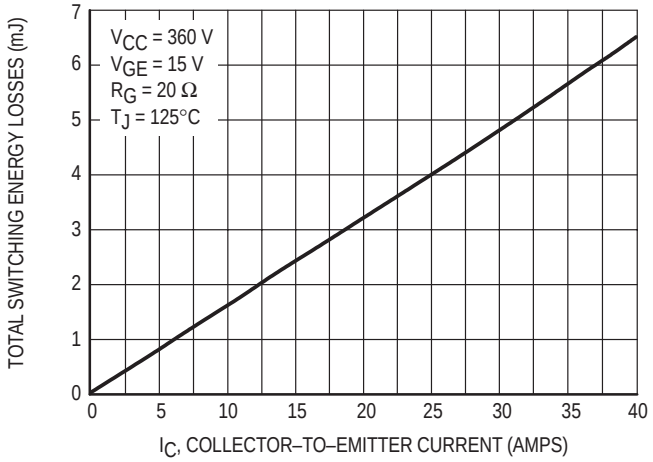


Figure 9. Total Switching Losses versus Collector–to–Emitter Current

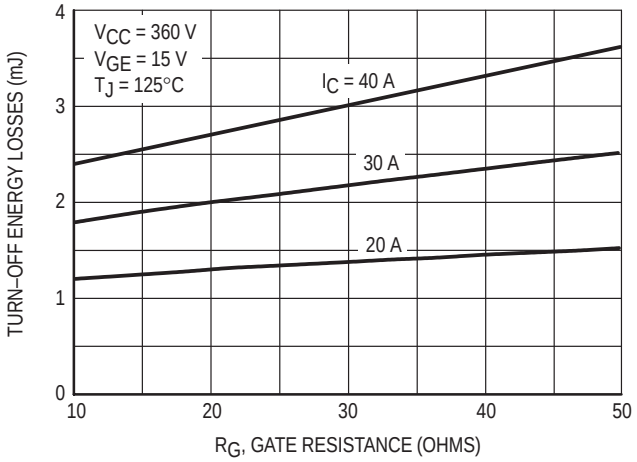


Figure 10. Turn–Off Losses versus Gate Resistance

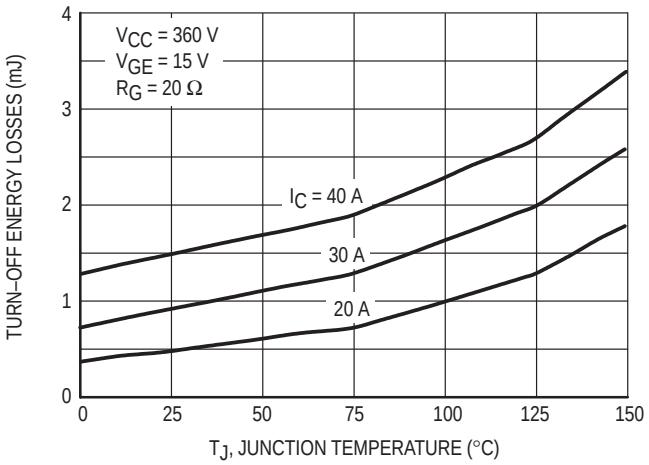


Figure 11. Turn–Off Losses versus Junction Temperature

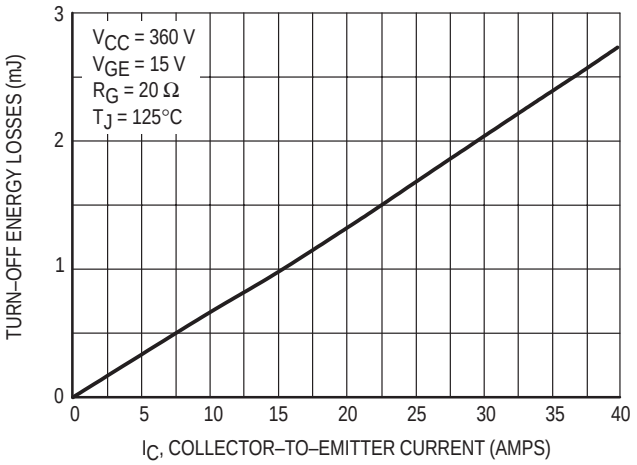


Figure 12. Turn–Off Losses versus Collector–to–Emitter Current

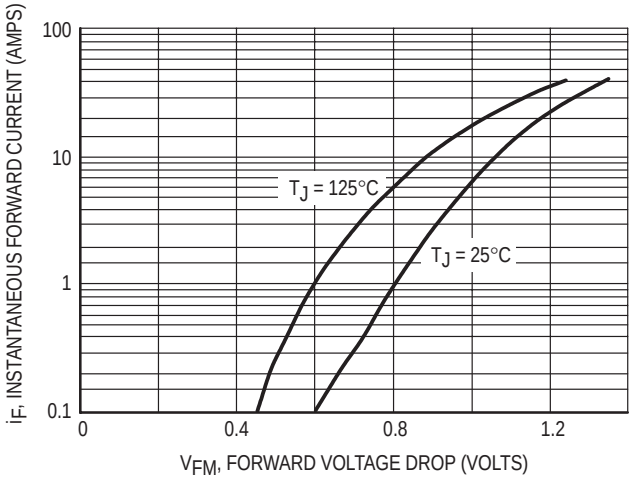


Figure 13. Typical Diode Forward Drop versus Instantaneous Forward Current

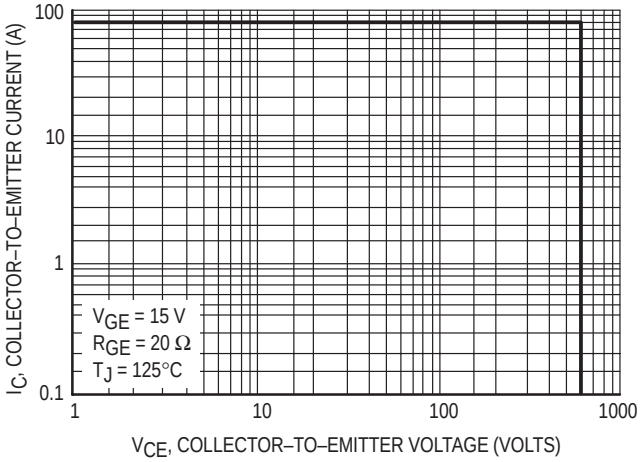


Figure 14. Reverse Biased Safe Operating Area

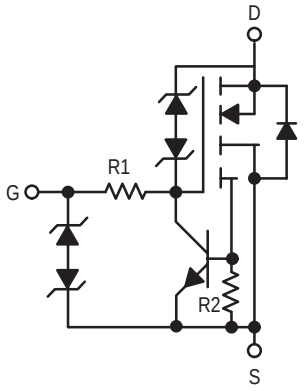
Designer's™ Data Sheet
SMARTDISCRETES™

Internally Clamped, Current Limited N–Channel Logic Level Power MOSFET

MLD1N06CL

Motorola Preferred Device

VOLTAGE CLAMPED
CURRENT LIMITING
MOSFET
62 VOLTS (CLAMPED)
$R_{DS(on)}$ = 0.75 OHMS



The MLD1N06CL is designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontrol unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in–rush current or a shorted load condition could occur.

This logic level power MOSFET features current limiting for short circuit protection, integrated Gate–Source clamping for ESD protection and integral Gate–Drain clamping for over–voltage protection and Sensefet technology for low on–resistance. No additional gate series resistance is required when interfacing to the output of a MCU, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition.

The internal Gate–Source and Gate–Drain clamps allow the device to be applied without use of external transient suppression components. The Gate–Source clamp protects the MOSFET input from electrostatic voltage stress up to 2.0 kV. The Gate–Drain clamp protects the MOSFET drain from the avalanche stress that occurs with inductive loads. Their unique design provides voltage clamping that is essentially independent of operating temperature.

The MLD1N06CL is fabricated using Motorola's SMARTDISCRETES™ technology which combines the advantages of a power MOSFET output device with the on–chip protective circuitry that can be obtained from a standard MOSFET process. This approach offers an economical means of providing protection to power MOSFETs from harsh automotive and industrial environments. SMARTDISCRETES™ devices are specified over a wide temperature range from –50°C to 150°C.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

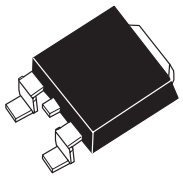
Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	Clamped	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	Clamped	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±10	Vdc
Drain Current — Continuous — Single Pulse	I_D I_{DM}	Self–limited 1.8	Adc Apk
Total Power Dissipation	P_D	40	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–50 to 150	°C
Electrostatic Discharge Voltage (Human Model)	ESD	2.0	kV

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.12 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 sec.	T_L	260	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS

Single Pulse Drain–to–Source Avalanche Energy Starting T_J = 25°C	E_{AS}	80	mJ



CASE 369A–13, Style 2
DPAK Surface Mount

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (Internally Clamped) (I_D = 20 mAdc, V_{GS} = 0 Vdc) (I_D = 20 mAdc, V_{GS} = 0 Vdc, T_J = 150°C)	$V_{(BR)DSS}$	 59 59	 62 62	 65 65	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 45 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 45 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)	I_{DSS}	 — —	 0.6 6.0	 5.0 20	μAdc
Gate–Source Leakage Current (V_G = 5.0 Vdc, V_{DS} = 0 Vdc) (V_G = 5.0 Vdc, V_{DS} = 0 Vdc, T_J = 150°C)	I_{GSS}	 — —	 0.5 1.0	 5.0 20	μAdc
ON CHARACTERISTICS(1)					
Gate Threshold Voltage (I_D = 250 μAdc, V_{DS} = V_{GS}) (I_D = 250 μAdc, V_{DS} = V_{GS}, T_J = 150°C)	$V_{GS(th)}$	 1.0 0.6	 1.5 —	 2.0 1.6	Vdc
Static Drain–to–Source On–Resistance (I_D = 1.0 Adc, V_{GS} = 4.0 Vdc) (I_D = 1.0 Adc, V_{GS} = 5.0 Vdc) (I_D = 1.0 Adc, V_{GS} = 4.0 Vdc, T_J = 150°C) (I_D = 1.0 Adc, V_{GS} = 5.0 Vdc, T_J = 150°C)	$R_{DS(on)}$	 — — — —	 0.63 0.59 1.1 1.0	 0.75 0.75 1.9 1.8	Ohms
Static Source–to–Drain Diode Voltage (I_S = 1.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.1	1.5	Vdc
Static Drain Current Limit (V_{GS} = 5.0 Vdc, V_{DS} = 10 Vdc) (V_{GS} = 5.0 Vdc, V_{DS} = 10 Vdc, T_J = 150°C)	$I_{D(lim)}$	 2.0 1.1	 2.3 1.3	 2.75 1.8	Adc
Forward Transconductance (I_D = 1.0 Adc, V_{DS} = 10 Vdc)	g_{FS}	1.0	1.4	—	mhos
RESISTIVE SWITCHING CHARACTERISTICS(2)					
Turn–On Delay Time	(V_{DD} = 25 Vdc, I_D = 1.0 Adc, $V_{GS(on)}$ = 5.0 Vdc, R_{GS} = 50 Ohms)	$t_{d(on)}$	—	1.2	2.0	ns
Rise Time		t_r	—	4.0	6.0	
Turn–Off Delay Time		$t_{d(off)}$	—	4.0	6.0	
Fall Time		t_f	—	3.0	5.0	
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from drain lead 0.25” from package to center of die)	L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25” from package to source bond pad)	L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

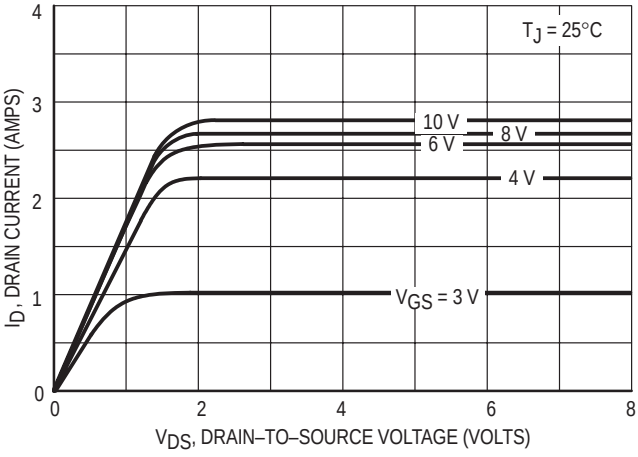


Figure 1. Output Characteristics

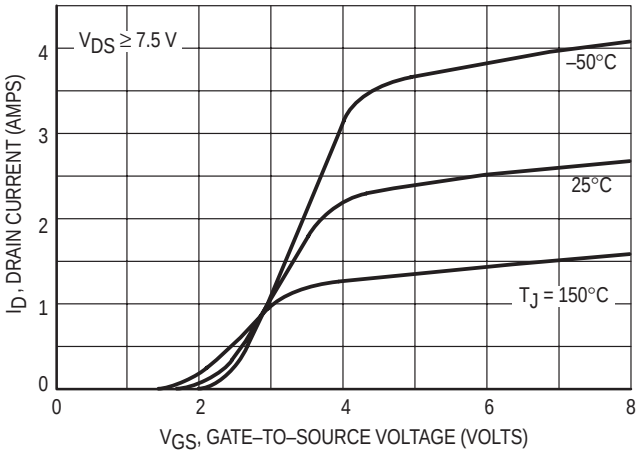


Figure 2. Transfer Function

THE SMARTDISCRETES CONCEPT

From a standard power MOSFET process, several active and passive elements can be obtained that provide on–chip protection to the basic power device. Such elements require only a small increase in silicon area and/or the addition of one masking layer to the process. The resulting device exhibits significant improvements in ruggedness and reliability as well as system cost reduction. The SMARTDISCRETES device functions can now provide an economical alternative to smart power ICs for power applications requiring low on–resistance, high voltage and high current.

These devices are designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontroller unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in–rush current or a shorted load condition could occur.

OPERATION IN THE CURRENT LIMIT MODE

The amount of time that an unprotected device can withstand the current stress resulting from a shorted load before its maximum junction temperature is exceeded is dependent upon a number of factors that include the amount of heatsinking that is provided, the size or rating of the device, its initial junction temperature, and the supply voltage. Without some form of current limiting, a shorted load can raise a device's junction temperature beyond the maximum rated operating temperature in only a few milliseconds.

Even with no heatsink, the MLD1N06CL can withstand a shorted load powered by an automotive battery (10 to 14 Volts) for almost a second if its initial operating temperature is under 100°C. For longer periods of operation in the current–limited mode, device heatsinking can extend operation from several seconds to indefinitely depending on the amount of heatsinking provided.

SHORT CIRCUIT PROTECTION AND THE EFFECT OF TEMPERATURE

The on–chip circuitry of the MLD1N06CL offers an integrated means of protecting the MOSFET component from high in–rush current or a shorted load. As shown in the schematic diagram, the current limiting feature is provided by an NPN transistor and integral resistors R1 and R2. R2 senses the current through the MOSFET and forward biases the NPN transistor's base as the current increases. As the NPN turns on, it begins to pull gate drive current through R1, dropping the gate drive voltage across it, and thus lowering the voltage across the gate–to–source of the power MOSFET and limiting the current. The current limit is temperature dependent as shown in Figure 3, and decreases from about 2.3 Amps at 25°C to about 1.3 Amps at 150°C.

Since the MLD1N06CL continues to conduct current and dissipate power during a shorted load condition, it is important to provide sufficient heatsinking to limit the device junction temperature to a maximum of 150°C.

The metal current sense resistor R2 adds about 0.4 ohms to the power MOSFET's on–resistance, but the effect of temperature on the combination is less than on a standard MOSFET due to the lower temperature coefficient of R2. The on–resistance variation with temperature for gate voltages of 4 and 5 Volts is shown in Figure 5.

Back–to–back polysilicon diodes between gate and source provide ESD protection to greater than 2 kV, HBM. This on–chip protection feature eliminates the need for an external Zener diode for systems with potentially heavy line transients.

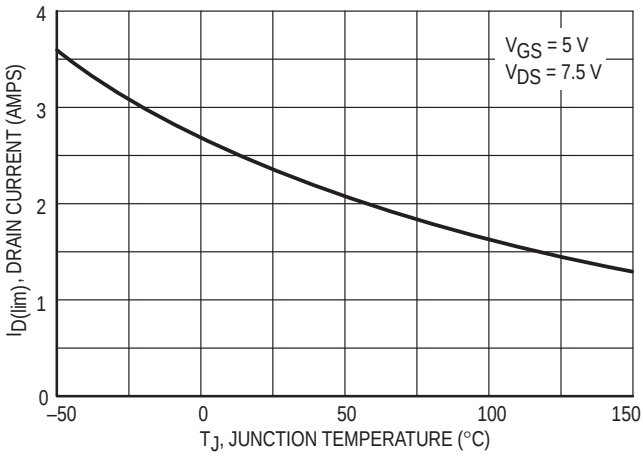


Figure 3. $I_{D(lim)}$ Variation With Temperature

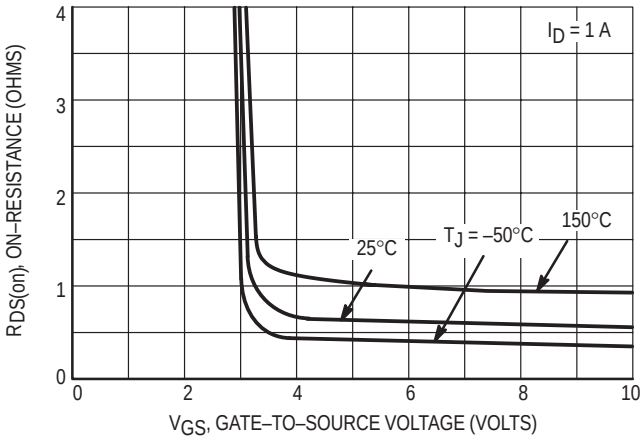


Figure 4. $R_{DS(on)}$ Variation With Gate–To–Source Voltage

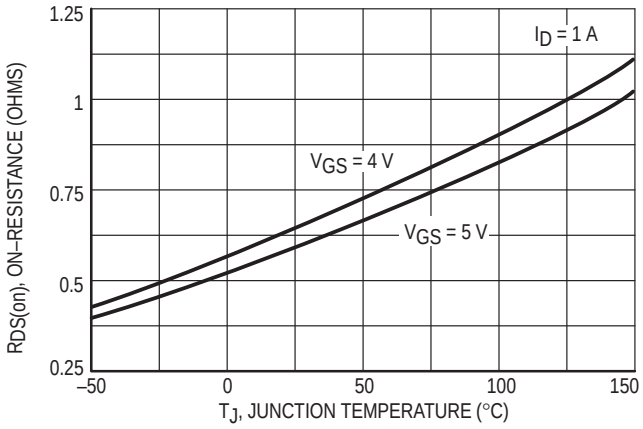


Figure 5. On–Resistance Variation With Temperature

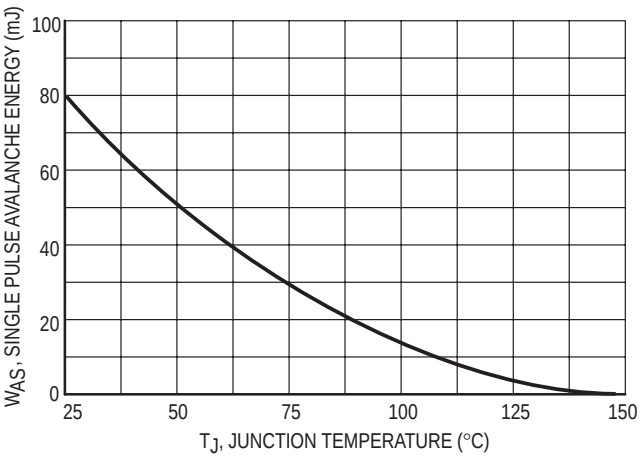


Figure 6. Single Pulse Avalanche Energy versus Junction Temperature

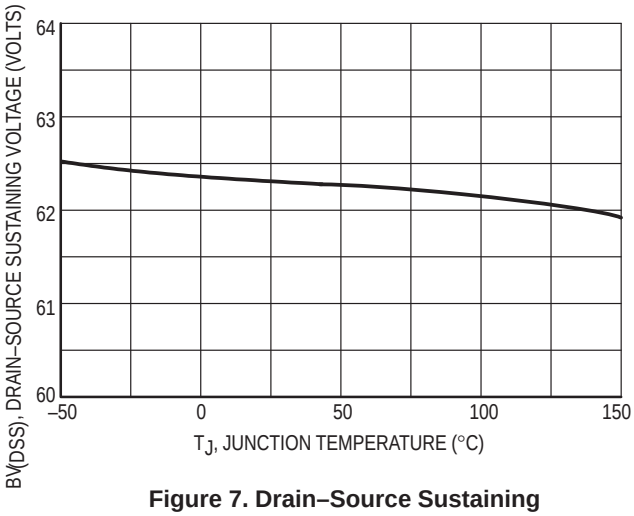


Figure 7. Drain–Source Sustaining Voltage Variation With Temperature

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance — General Data and Its Use” provides detailed instructions.

MAXIMUM DC VOLTAGE CONSIDERATIONS

The maximum drain–to–source voltage that can be continuously applied across the MLD1N06CL when it is in current limit is a function of the power that must be dissipated. This power is determined by the maximum current limit at maximum rated operating temperature (1.8 A at 150°C) and not the $R_{DS(on)}$. The maximum voltage can be calculated by the following equation:

$$V_{supply} = \frac{(150 - T_A)}{I_{D(lim)} (R_{\theta JC} + R_{\theta CA})}$$

where the value of $R_{\theta CA}$ is determined by the heatsink that is being used in the application.

DUTY CYCLE OPERATION

When operating in the duty cycle mode, the maximum drain voltage can be increased. The maximum operating temperature is related to the duty cycle (DC) by the following equation:

$$T_C = (V_{DS} \times I_D \times DC \times R_{\theta CA}) + T_A$$

The maximum value of V_{DS} applied when operating in a duty cycle mode can be approximated by:

$$V_{DS} = \frac{150 - T_C}{I_{D(lim)} \times DC \times R_{\theta JC}}$$

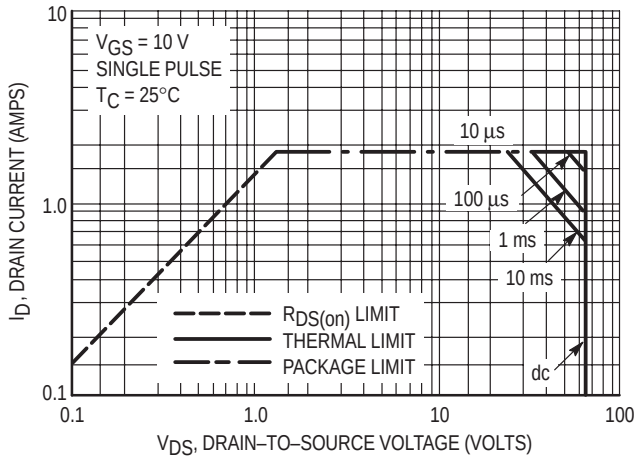


Figure 8. Maximum Rated Forward Bias Safe Operating Area (MLD1N06CL)

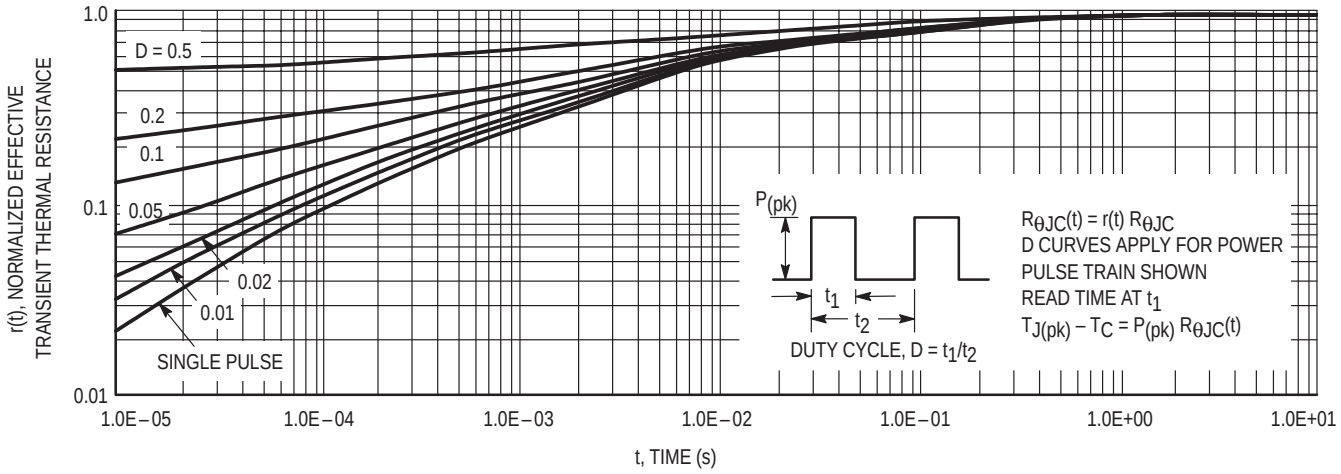


Figure 9. Thermal Response (MLD1N06CL)

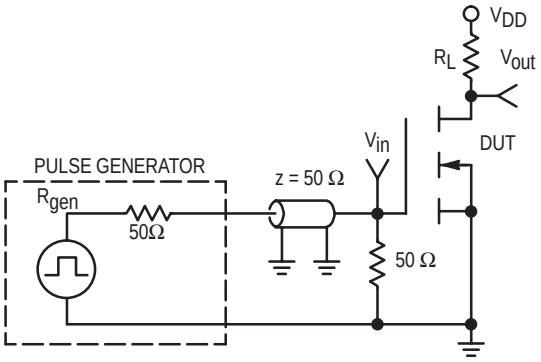


Figure 10. Switching Test Circuit

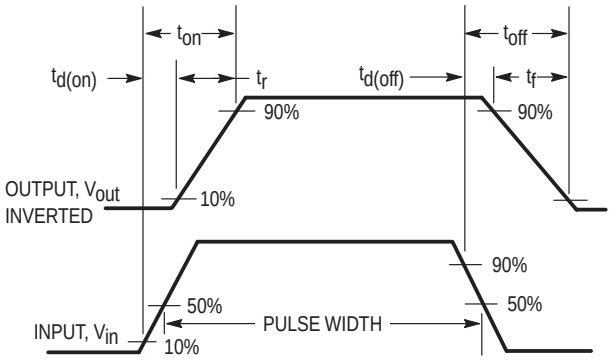


Figure 11. Switching Waveforms

ACTIVE CLAMPING

SMARTDISCRETES technology can provide on–chip realization of the popular gate–to–source and gate–to–drain Zener diode clamp elements. Until recently, such features have been implemented only with discrete components which consume board space and add system cost. The SMARTDISCRETES technology approach economically melds these features and the power chip with only a slight increase in chip area.

In practice, back–to–back diode elements are formed in a polysilicon region monolithicly integrated with, but electrically isolated from, the main device structure. Each back–to–back diode element provides a temperature compensated voltage element of about 7.2 volts. As the polysilicon region is formed on top of silicon dioxide, the diode elements are free from direct interaction with the conduction regions of the power device, thus eliminating parasitic electrical effects while maintaining excellent thermal coupling.

To achieve high gate–to–drain clamp voltages, several voltage elements are strung together; the MLD1N06CL uses 8 such elements. Customarily, two voltage elements are used to provide a 14.4 volt gate–to–source voltage clamp. For the MLD1N06CL, the integrated gate–to–source voltage elements provide greater than 2.0 kV electrostatic voltage protection.

The avalanche voltage of the gate–to–drain voltage clamp is set less than that of the power MOSFET device. As soon as the drain–to–source voltage exceeds this avalanche voltage, the resulting gate–to–drain Zener current builds a gate voltage across the gate–to–source impedance, turning on the power device which then conducts the current. Since virtually all of the current is carried by the power device, the gate–to–drain voltage clamp element may be small in size. This technique of establishing a temperature compensated drain–to–source sustaining voltage (Figure 7) effectively removes the possibility of drain–to–source avalanche in the power device.

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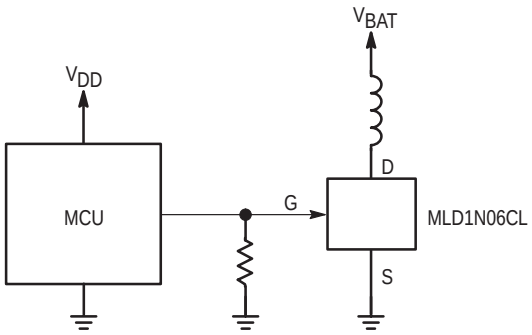
TYPICAL APPLICATIONS: INJECTOR DRIVER, SOLENOIDS, LAMPS, RELAY COILS

The MLD1N06CL has been designed to allow direct interface to the output of a microcontrol unit to control an isolated load. No additional series gate resistance is required, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition in the event of an MCU failure. The internal clamps allow the device to be used without any external transistent suppressing components.



Designer's™ Data Sheet
SMARTDISCRETES™

Internally Clamped, Current Limited N–Channel Logic Level Power MOSFET

MLD2N06CL

Motorola Preferred Device

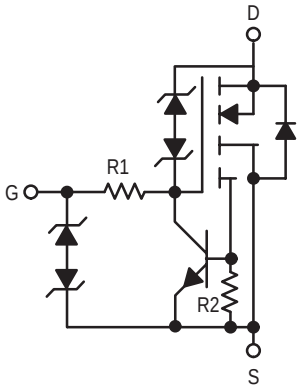
VOLTAGE CLAMPED
CURRENT LIMITING
MOSFET
62 VOLTS (CLAMPED)
$R_{DS(on)}$ = 0.4 OHMS

The MLD2N06CL is designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontrol unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in–rush current or a shorted load condition could occur.

This logic level power MOSFET features current limiting for short circuit protection, integrated Gate–Source clamping for ESD protection and integral Gate–Drain clamping for over–voltage protection and Sensefet technology for low on–resistance. No additional gate series resistance is required when interfacing to the output of a MCU, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition.

The internal Gate–Source and Gate–Drain clamps allow the device to be applied without use of external transient suppression components. The Gate–Source clamp protects the MOSFET input from electrostatic voltage stress up to 2.0 kV. The Gate–Drain clamp protects the MOSFET drain from the avalanche stress that occurs with inductive loads. Their unique design provides voltage clamping that is essentially independent of operating temperature.

The MLD2N06CL is fabricated using Motorola's SMARTDISCRETES™ technology which combines the advantages of a power MOSFET output device with the on–chip protective circuitry that can be obtained from a standard MOSFET process. This approach offers an economical means of providing protection to power MOSFETs from harsh automotive and industrial environments. SMARTDISCRETES™ devices are specified over a wide temperature range from –50°C to 150°C.



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

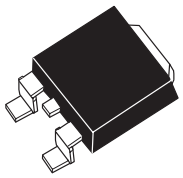
Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	Clamped	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	Clamped	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±10	Vdc
Drain Current — Continuous @ T_C = 25°C	I_D	Self–limited	Adc
Total Power Dissipation @ T_C = 25°C	P_D	40	Watts
Electrostatic Voltage	ESD	2.0	kV
Operating and Storage Temperature Range	T_J, T_{stg}	–50 to 150	°C

THERMAL CHARACTERISTICS

Maximum Junction Temperature	$T_{J(max)}$	150	°C
Thermal Resistance – Junction to Case	$R_{\theta JC}$	3.12	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 sec.	T_L	260	°C

DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS

Single Pulse Drain–to–Source Avalanche Energy (Starting T_J = 25°C, I_D = 2.0 A, L = 40 mH)	E_{AS}	80	mJ



CASE 369A–13, Style 2
DPAK Surface Mount

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$				Vdc
(I_D = 20 mAdc, V_{GS} = 0 Vdc)		58	62	66	
(I_D = 20 mAdc, V_{GS} = 0 Vdc, T_J = 150°C)		58	62	66	
Zero Gate Voltage Drain Current	I_{DSS}				μAdc
(V_{DS} = 40 Vdc, V_{GS} = 0 Vdc)		—	0.6	5.0	
(V_{DS} = 40 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		—	6.0	20	
Gate–Source Leakage Current	I_{GSS}				μAdc
(V_G = 5.0 Vdc, V_{DS} = 0 Vdc)		—	0.5	5.0	
(V_G = 5.0 Vdc, V_{DS} = 0 Vdc, T_J = 150°C)		—	1.0	20	
ON CHARACTERISTICS(1)					
Gate Threshold Voltage	$V_{GS(th)}$				Vdc
(I_D = 250 μAdc, V_{DS} = V_{GS})		1.0	1.5	2.0	
(I_D = 250 μAdc, V_{DS} = V_{GS}, T_J = 150°C)		0.6	1	1.6	
Static Drain Current Limit	$I_{D(lim)}$				Adc
(V_{GS} = 5.0 Vdc, V_{DS} = 10 Vdc)		3.8	4.4	5.2	
(V_{GS} = 5.0 Vdc, V_{DS} = 10 Vdc, T_J = 150°C)		1.6	2.4	2.9	
Static Drain–to–Source On–Resistance	$R_{DS(on)}$				Ohms
(I_D = 1.0 Adc, V_{GS} = 5.0 Vdc)		—	0.3	0.4	
(I_D = 1.0 Adc, V_{GS} = 5.0 Vdc, T_J = 150°C)		—	0.53	0.7	
Forward Transconductance (I_D = 1.0 Adc, V_{DS} = 10 Vdc)	g_{FS}	1.0	1.4	—	mhos
Static Source–to–Drain Diode Voltage	V_{SD}				Vdc
(I_S = 1.0 Adc, V_{GS} = 0 Vdc)		—	1.1	1.5	
SWITCHING CHARACTERISTICS(2)					
Turn–On Delay Time	$t_{d(on)}$	—	1.0	1.5	μs
Rise Time	t_r	—	3.0	5.0	
Turn–Off Delay Time	$t_{d(off)}$	—	5.0	8.0	
Fall Time	t_f	—	3.0	5.0	

(V_{DD} = 30 Vdc, I_D = 1.0 Adc, $V_{GS(on)}$ = 5.0 Vdc, R_{GS} = 25 Ohms)

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

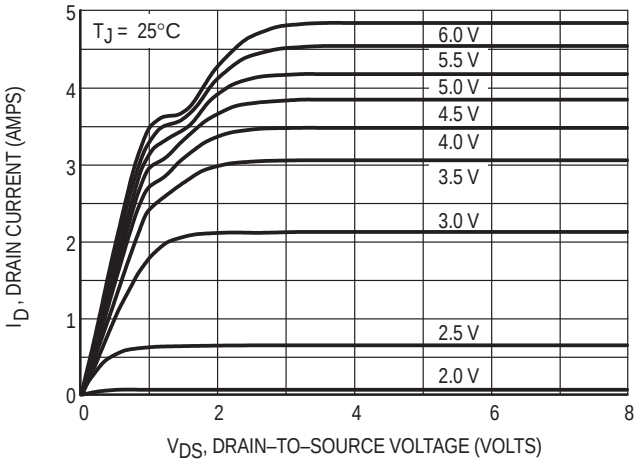


Figure 1. Output Characteristics

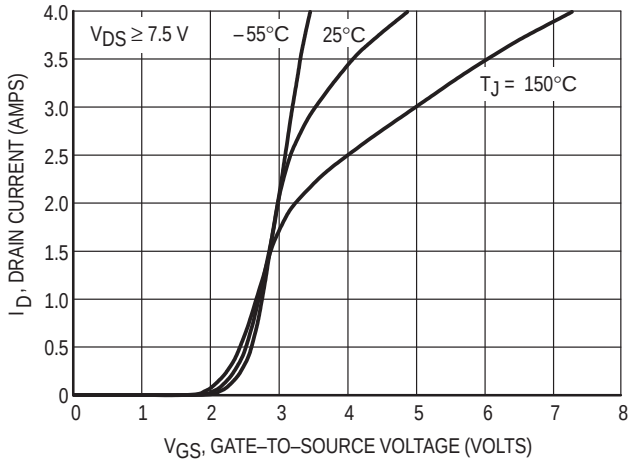


Figure 2. Transfer Function

THE SMARTDISCRETES CONCEPT

From a standard power MOSFET process, several active and passive elements can be obtained that provide on–chip protection to the basic power device. Such elements require only a small increase in silicon area and/or the addition of one masking layer to the process. The resulting device exhibits significant improvements in ruggedness and reliability as well as system cost reduction. The SMARTDISCRETES device functions can now provide an economical alternative to smart power ICs for power applications requiring low on–resistance, high voltage and high current.

These devices are designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontroller unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in–rush current or a shorted load condition could occur.

OPERATION IN THE CURRENT LIMIT MODE

The amount of time that an unprotected device can withstand the current stress resulting from a shorted load before its maximum junction temperature is exceeded is dependent upon a number of factors that include the amount of heatsinking that is provided, the size or rating of the device, its initial junction temperature, and the supply voltage. Without some form of current limiting, a shorted load can raise a device's junction temperature beyond the maximum rated operating temperature in only a few milliseconds.

Even with no heatsink, the MLD2N06CL can withstand a shorted load powered by an automotive battery (10 to 14 Volts) for almost a second if its initial operating temperature is under 100°C. For longer periods of operation in the current–limited mode, device heatsinking can extend operation from several seconds to indefinitely depending on the amount of heatsinking provided.

SHORT CIRCUIT PROTECTION AND THE EFFECT OF TEMPERATURE

The on–chip circuitry of the MLD2N06CL offers an integrated means of protecting the MOSFET component from high in–rush current or a shorted load. As shown in the schematic diagram, the current limiting feature is provided by an NPN transistor and integral resistors R1 and R2. R2 senses the current through the MOSFET and forward biases the NPN transistor's base as the current increases. As the NPN turns on, it begins to pull gate drive current through R1, dropping the gate drive voltage across it, and thus lowering the voltage across the gate–to–source of the power MOSFET and limiting the current. The current limit is temperature dependent as shown in Figure 3, and decreases from about 2.3 Amps at 25°C to about 1.3 Amps at 150°C.

Since the MLD2N06CL continues to conduct current and dissipate power during a shorted load condition, it is important to provide sufficient heatsinking to limit the device junction temperature to a maximum of 150°C.

The metal current sense resistor R2 adds about 0.4 ohms to the power MOSFET's on–resistance, but the effect of temperature on the combination is less than on a standard MOSFET due to the lower temperature coefficient of R2. The on–resistance variation with temperature for gate voltages of 4 and 5 Volts is shown in Figure 5.

Back–to–back polysilicon diodes between gate and source provide ESD protection to greater than 2 kV, HBM. This on–chip protection feature eliminates the need for an external Zener diode for systems with potentially heavy line transients.

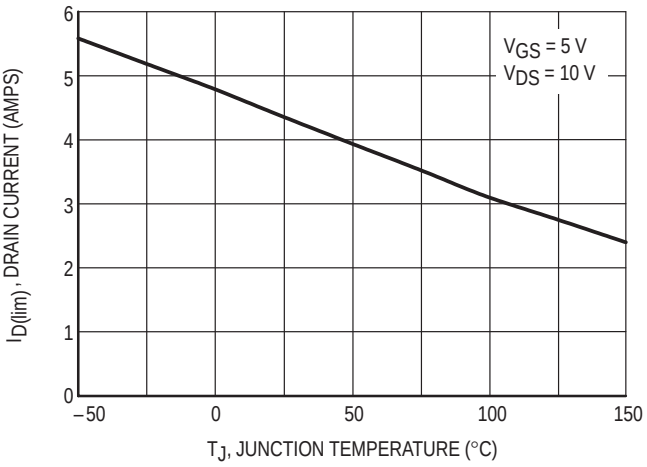


Figure 3. $I_{D(lim)}$ Variation With Temperature

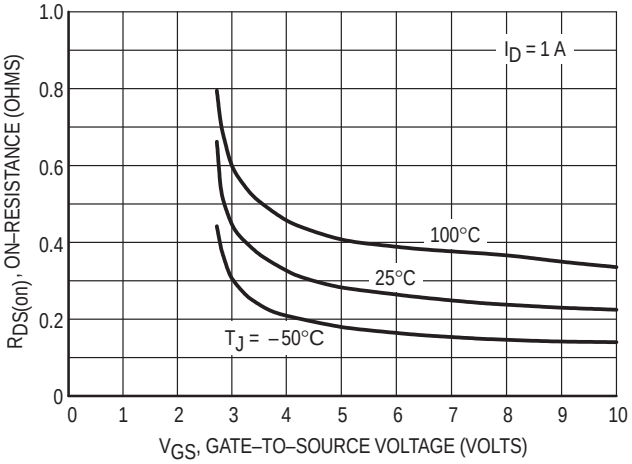


Figure 4. $R_{DS(on)}$ Variation With Gate–To–Source Voltage

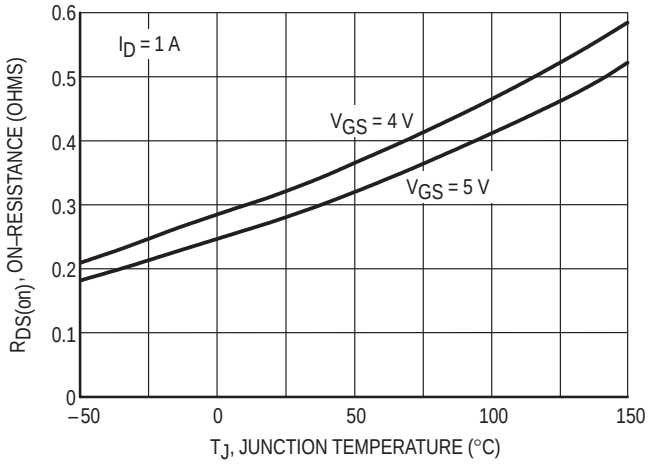


Figure 5. On–Resistance Variation With Temperature

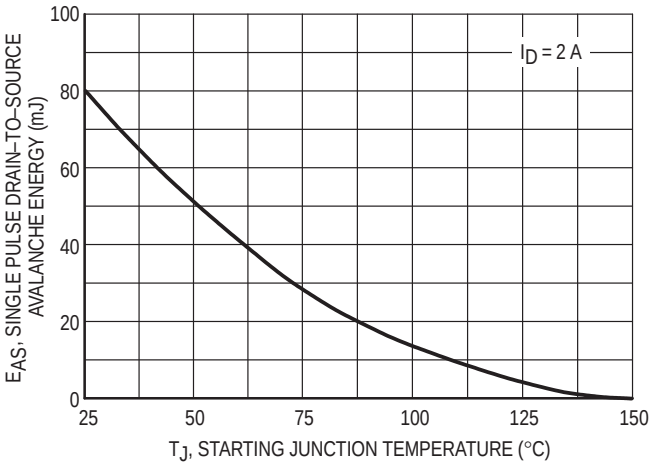


Figure 6. Maximum Avalanche Energy versus Starting Junction Temperature

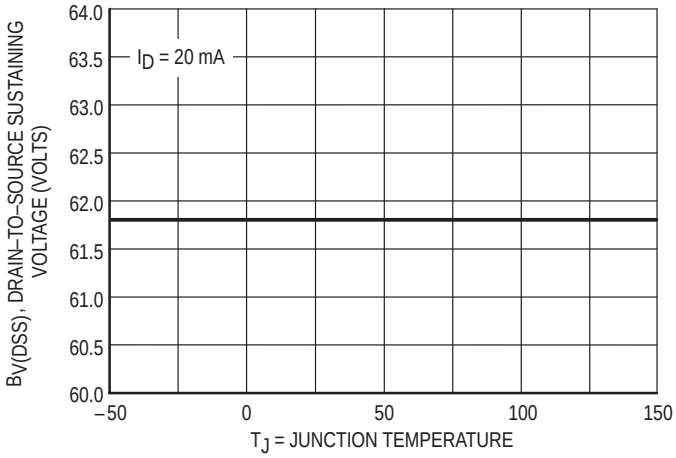


Figure 7. Drain–Source Sustaining Voltage Variation With Temperature

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance — General Data and Its Use” provides detailed instructions.

MAXIMUM DC VOLTAGE CONSIDERATIONS

The maximum drain–to–source voltage that can be continuously applied across the MLD2N06CL when it is in current limit is a function of the power that must be dissipated. This power is determined by the maximum current limit at maximum rated operating temperature (1.8 A at 150°C) and not the $R_{DS(on)}$. The maximum voltage can be calculated by the following equation:

$$V_{supply} = \frac{(150 - T_A)}{I_{D(lim)} (R_{\theta JC} + R_{\theta CA})}$$

where the value of $R_{\theta CA}$ is determined by the heatsink that is being used in the application.

DUTY CYCLE OPERATION

When operating in the duty cycle mode, the maximum drain voltage can be increased. The maximum operating temperature is related to the duty cycle (DC) by the following equation:

$$T_C = (V_{DS} \times I_D \times DC \times R_{\theta CA}) + T_A$$

The maximum value of V_{DS} applied when operating in a duty cycle mode can be approximated by:

$$V_{DS} = \frac{150 - T_C}{I_{D(lim)} \times DC \times R_{\theta JC}}$$

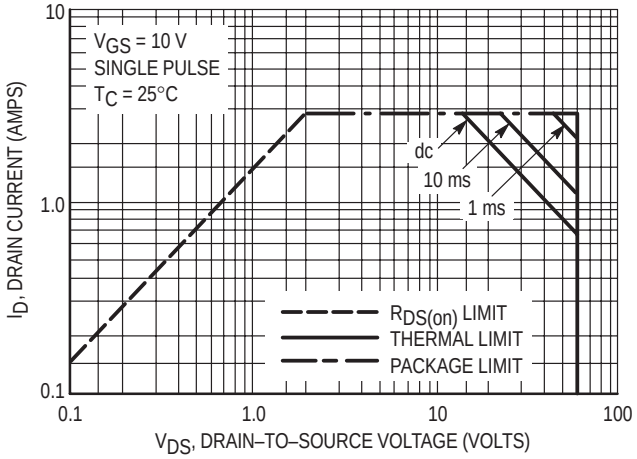


Figure 8. Maximum Rated Forward Bias Safe Operating Area (MLD2N06CL)

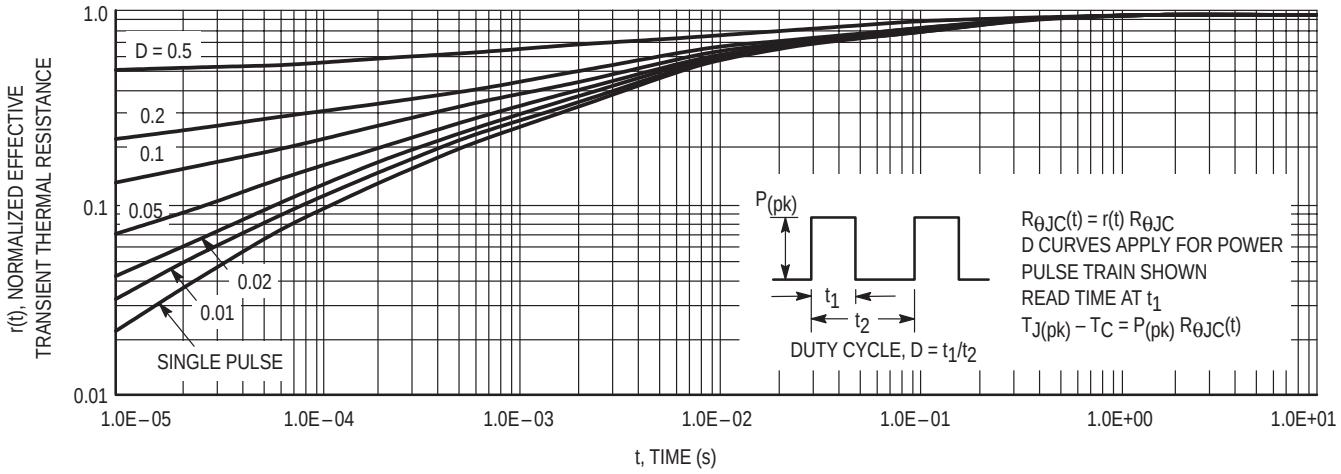
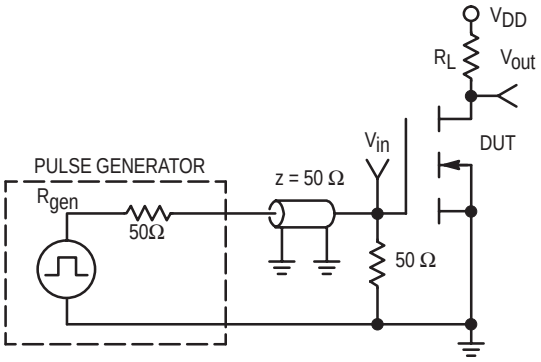


Figure 9. Thermal Response (MLD2N06CL)



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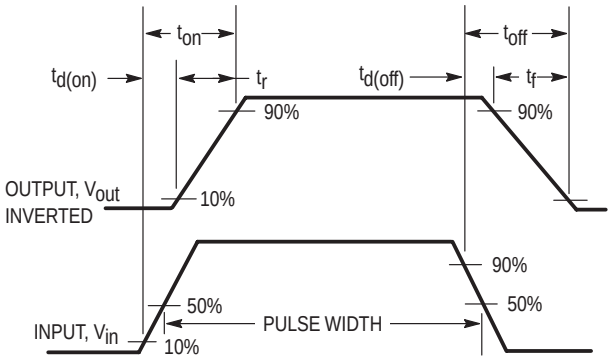

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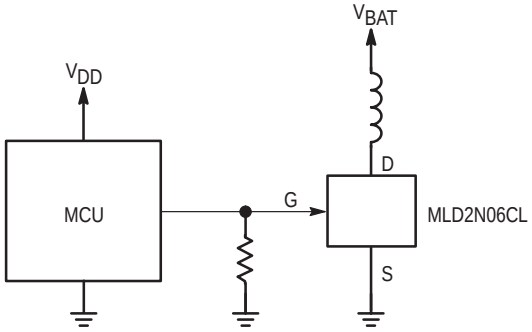


SMARTDISCRETES™
Internally Clamped, Current Limited N–Channel Logic Level Power MOSFET

MLP1N06CL

Motorola Preferred Device

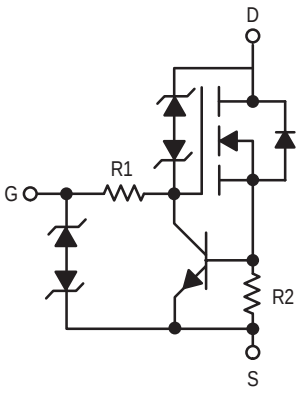
VOLTAGE CLAMPED
CURRENT LIMITING
MOSFET
62 VOLTS (CLAMPED)
$R_{DS(on)}$ = 0.75 OHMS

These SMARTDISCRETES devices feature current limiting for short circuit protection, an integral gate–to–source clamp for ESD protection and gate–to–drain clamp for over–voltage protection. No additional gate series resistance is required when interfacing to the output of a MCU, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition.

The internal gate–to–source and gate–to–drain clamps allow the devices to be applied without use of external transient suppression components. The gate–to–source clamp protects the MOSFET input from electrostatic gate voltage stresses up to 2.0 kV. The gate–to–drain clamp protects the MOSFET drain from drain avalanche stresses that occur with inductive loads. This unique design provides voltage clamping that is essentially independent of operating temperature.

The MLP1N06CL is fabricated using Motorola's SMARTDISCRETES technology which combines the advantages of a power MOSFET output device with on–chip protective circuitry. This approach offers an economical means for providing additional functions that protect a power MOSFET in harsh automotive and industrial environments. SMARTDISCRETES devices are specified over a wide temperature range from –50°C to 150°C.

- Temperature Compensated Gate–to–Drain Clamp Limits Voltage Stress Applied to the Device and Protects the Load From Overvoltage
- Integrated ESD Diode Protection
- Controlled Switching Minimizes RFI
- Low Threshold Voltage Enables Interfacing Power Loads to Microprocessors



MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

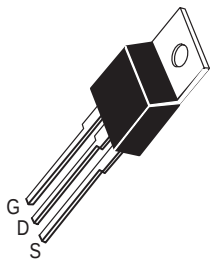
Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	Clamped	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	Clamped	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±10	Vdc
Drain Current — Continuous — Single Pulse	I_D I_{DM}	Self–limited 1.8	Adc
Total Power Dissipation	P_D	40	Watts
Electrostatic Discharge Voltage (Human Body Model)	ESD	2.0	kV
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–50 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Case Thermal Resistance, Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.12 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case	T_L	260	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS

Single Pulse Drain–to–Source Avalanche Energy (Starting T_J = 25°C, I_D = 2.0 A, L = 40 mH) (Figure 6)	E_{AS}	80	mJ



CASE 221A–06, Style 5
TO–220AB

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Sustaining Voltage (Internally Clamped)	$V_{(BR)DSS}$				Vdc
(I_D = 20 mA, V_{GS} = 0)		59	62	65	
(I_D = 20 mA, V_{GS} = 0, T_J = 150°C)		59	62	65	
Zero Gate Voltage Drain Current	I_{DSS}				μAdc
(V_{DS} = 45 V, V_{GS} = 0)		—	0.6	5.0	
(V_{DS} = 45 V, V_{GS} = 0, T_J = 150°C)		—	6.0	20	
Gate–Body Leakage Current	I_{GSS}				μAdc
(V_G = 5.0 V, V_{DS} = 0)		—	0.5	5.0	
(V_G = 5.0 V, V_{DS} = 0, T_J = 150°C)		—	1.0	20	
ON CHARACTERISTICS*					
Gate Threshold Voltage	$V_{GS(th)}$				Vdc
(I_D = 250 μA, V_{DS} = V_{GS})		1.0	1.5	2.0	
(I_D = 250 μA, V_{DS} = V_{GS}, T_J = 150°C)		0.6	—	1.6	
Static Drain–to–Source On–Resistance	$R_{DS(on)}$				Ohms
(I_D = 1.0 A, V_{GS} = 4.0 V)		—	0.63	0.75	
(I_D = 1.0 A, V_{GS} = 5.0 V)		—	0.59	0.75	
(I_D = 1.0 A, V_{GS} = 4.0 V, T_J = 150°C)		—	1.1	1.9	
(I_D = 1.0 A, V_{GS} = 5.0 V, T_J = 150°C)		—	1.0	1.8	
Forward Transconductance (I_D = 1.0 A, V_{DS} = 10 V)	g_{FS}	1.0	1.4	—	mhos
Static Source–to–Drain Diode Voltage (I_S = 1.0 A, V_{GS} = 0)	V_{SD}	—	1.1	1.5	Vdc
Static Drain Current Limit	$I_{D(lim)}$				A
(V_{GS} = 5.0 V, V_{DS} = 10 V)		2.0	2.3	2.75	
(V_{GS} = 5.0 V, V_{DS} = 10 V, T_J = 150°C)		1.1	1.3	1.8	
RESISTIVE SWITCHING CHARACTERISTICS*					
Turn–On Delay Time	(V_{DD} = 25 V, I_D = 1.0 A, V_{GS} = 5.0 V, R_G = 50 Ohms)	$t_{d(on)}$	—	1.2	2.0	μs
Rise Time		t_r	—	4.0	6.0	
Turn–Off Delay Time		$t_{d(off)}$	—	4.0	6.0	
Fall Time		t_f	—	3.0	5.0	

* Indicates Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

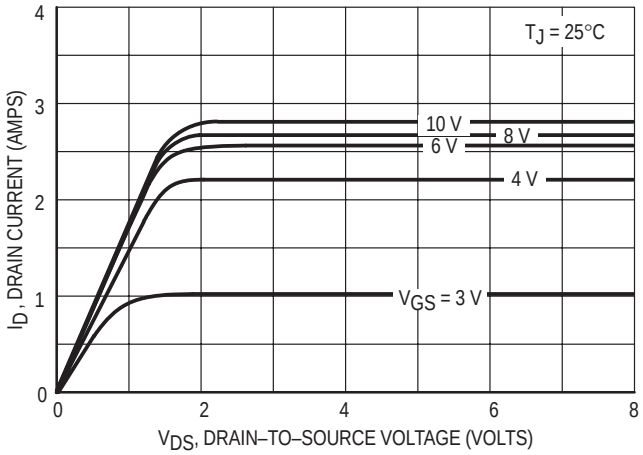


Figure 1. Output Characteristics

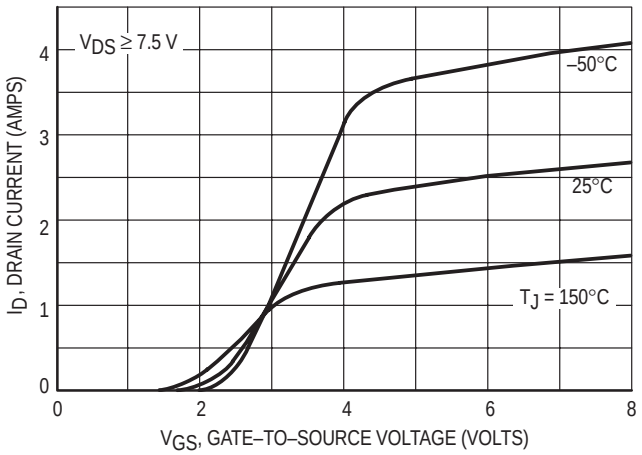


Figure 2. Transfer Function

THE SMARTDISCRETES CONCEPT

From a standard power MOSFET process, several active and passive elements can be obtained that provide on–chip protection to the basic power device. Such elements require only a small increase in silicon area and/or the addition of one masking layer to the process. The resulting device exhibits significant improvements in ruggedness and reliability as well as system cost reduction. The SMARTDISCRETES device functions can now provide an economical alternative to smart power ICs for power applications requiring low on–resistance, high voltage and high current.

These devices are designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontroller unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in–rush current or a shorted load condition could occur.

OPERATION IN THE CURRENT LIMIT MODE

The amount of time that an unprotected device can withstand the current stress resulting from a shorted load before its maximum junction temperature is exceeded is dependent upon a number of factors that include the amount of heatsinking that is provided, the size or rating of the device, its initial junction temperature, and the supply voltage. Without some form of current limiting, a shorted load can raise a device's junction temperature beyond the maximum rated operating temperature in only a few milliseconds.

Even with no heatsink, the MLP1N06CL can withstand a shorted load powered by an automotive battery (10 to 14 Volts) for almost a second if its initial operating temperature is under 100°C. For longer periods of operation in the current–limited mode, device heatsinking can extend operation from several seconds to indefinitely depending on the amount of heatsinking provided.

SHORT CIRCUIT PROTECTION AND THE EFFECT OF TEMPERATURE

The on–chip circuitry of the MLP1N06CL offers an integrated means of protecting the MOSFET component from high in–rush current or a shorted load. As shown in the schematic diagram, the current limiting feature is provided by an NPN transistor and integral resistors R1 and R2. R2 senses the current through the MOSFET and forward biases the NPN transistor's base as the current increases. As the NPN turns on, it begins to pull gate drive current through R1, dropping the gate drive voltage across it, and thus lowering the voltage across the gate–to–source of the power MOSFET and limiting the current. The current limit is temperature dependent as shown in Figure 3, and decreases from about 2.3 Amps at 25°C to about 1.3 Amps at 150°C.

Since the MLP1N06CL continues to conduct current and dissipate power during a shorted load condition, it is important to provide sufficient heatsinking to limit the device junction temperature to a maximum of 150°C.

The metal current sense resistor R2 adds about 0.4 ohms to the power MOSFET's on–resistance, but the effect of temperature on the combination is less than on a standard MOSFET due to the lower temperature coefficient of R2. The on–resistance variation with temperature for gate voltages of 4 and 5 Volts is shown in Figure 5.

Back–to–back polysilicon diodes between gate and source provide ESD protection to greater than 2 kV, HBM. This on–chip protection feature eliminates the need for an external Zener diode for systems with potentially heavy line transients.

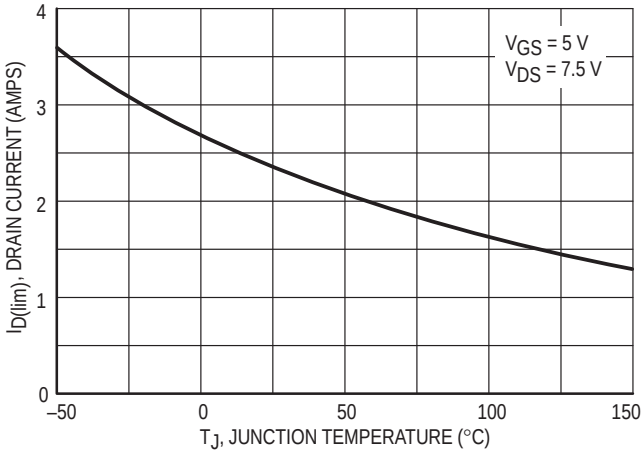


Figure 3. $I_{D(lim)}$ Variation With Temperature

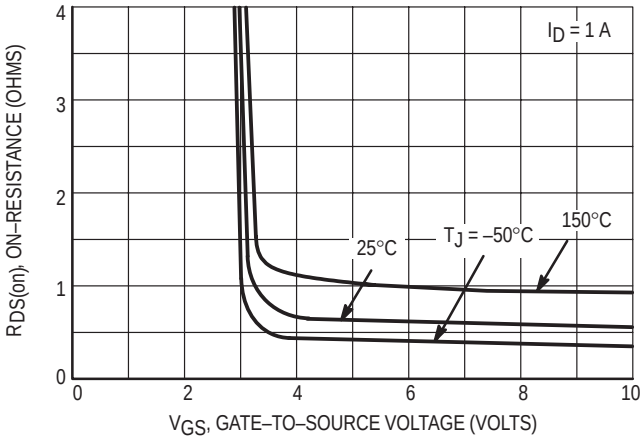


Figure 4. $R_{DS(on)}$ Variation With Gate–To–Source Voltage

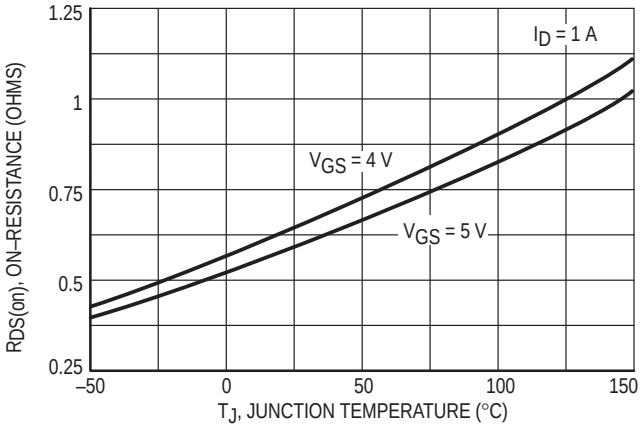


Figure 5. On–Resistance Variation With Temperature

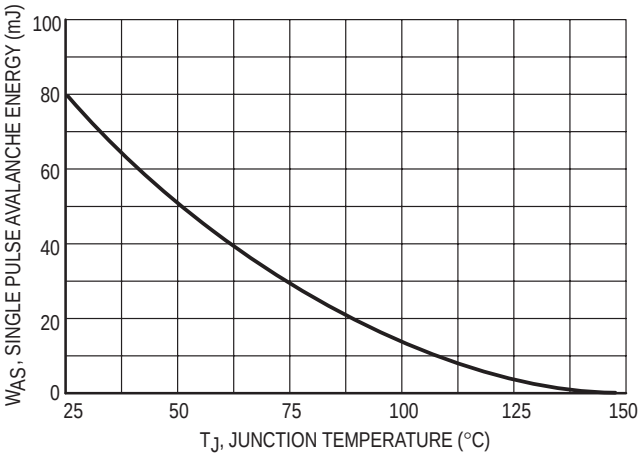


Figure 6. Single Pulse Avalanche Energy versus Junction Temperature

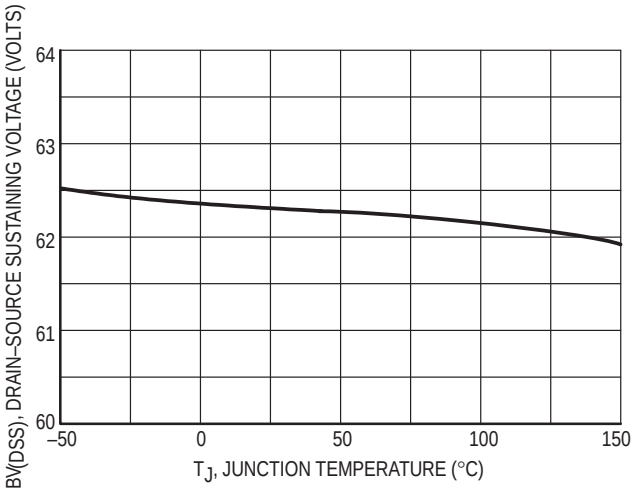


Figure 7. Drain–Source Sustaining Voltage Variation With Temperature

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance — General Data and Its Use” provides detailed instructions.

MAXIMUM DC VOLTAGE CONSIDERATIONS

The maximum drain–to–source voltage that can be continuously applied across the MLP1N06CL when it is in current limit is a function of the power that must be dissipated. This power is determined by the maximum current limit at maximum rated operating temperature (1.8 A at 150°C) and not the $R_{DS(on)}$. The maximum voltage can be calculated by the following equation:

$$V_{supply} = \frac{(150 - T_A)}{I_{D(lim)} (R_{\theta JC} + R_{\theta CA})}$$

where the value of $R_{\theta CA}$ is determined by the heatsink that is being used in the application.

DUTY CYCLE OPERATION

When operating in the duty cycle mode, the maximum drain voltage can be increased. The maximum operating temperature is related to the duty cycle (DC) by the following equation:

$$T_C = (V_{DS} \times I_D \times DC \times R_{\theta CA}) + T_A$$

The maximum value of V_{DS} applied when operating in a duty cycle mode can be approximated by:

$$V_{DS} = \frac{150 - T_C}{I_{D(lim)} \times DC \times R_{\theta JC}}$$

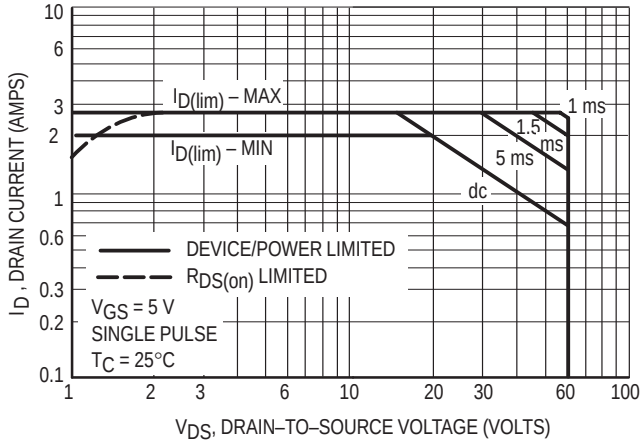


Figure 8. Maximum Rated Forward Bias Safe Operating Area (MLP1N06CL)

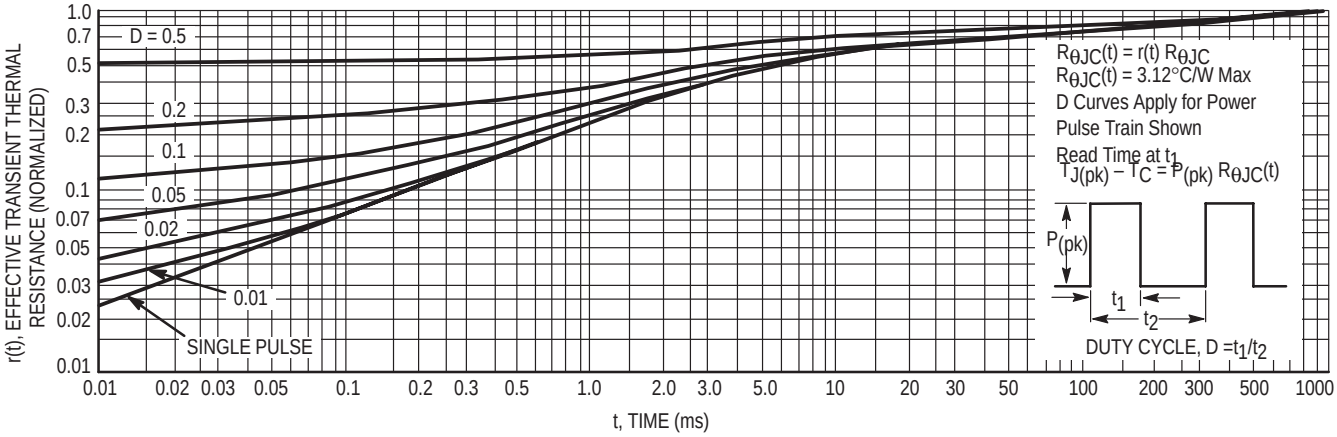


Figure 9. Thermal Response (MLP1N06CL)

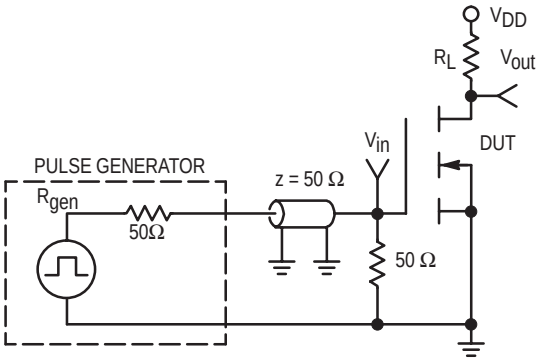


Figure 10. Switching Test Circuit

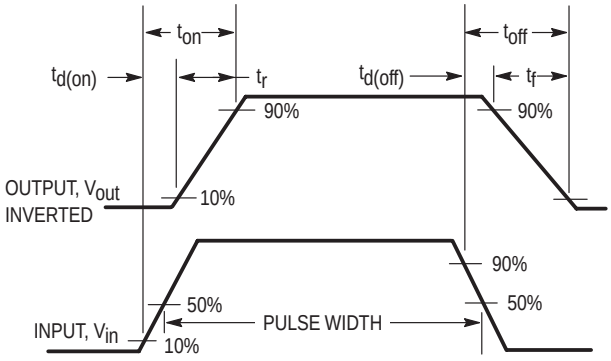


Figure 11. Switching Waveforms

ACTIVE CLAMPING

SMARTDISCRETES technology can provide on–chip realization of the popular gate–to–source and gate–to–drain Zener diode clamp elements. Until recently, such features have been implemented only with discrete components which consume board space and add system cost. The SMARTDISCRETES technology approach economically melds these features and the power chip with only a slight increase in chip area.

In practice, back–to–back diode elements are formed in a polysilicon region monolithicly integrated with, but electrically isolated from, the main device structure. Each back–to–back diode element provides a temperature compensated voltage element of about 7.2 volts. As the polysilicon region is formed on top of silicon dioxide, the diode elements are free from direct interaction with the conduction regions of the power device, thus eliminating parasitic electrical effects while maintaining excellent thermal coupling.

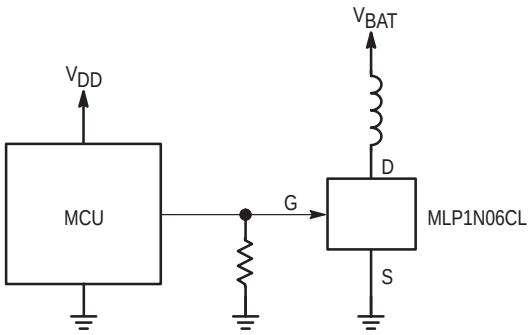
To achieve high gate–to–drain clamp voltages, several voltage elements are strung together; the MLP1N06CL uses 8 such elements. Customarily, two voltage elements are used to provide a 14.4 volt gate–to–source voltage clamp. For the MLP1N06CL, the integrated gate–to–source voltage elements provide greater than 2.0 kV electrostatic voltage protection.

The avalanche voltage of the gate–to–drain voltage clamp is set less than that of the power MOSFET device. As soon as the drain–to–source voltage exceeds this avalanche voltage, the resulting gate–to–drain Zener current builds a gate voltage across the gate–to–source impedance, turning on the power device which then conducts the current. Since virtually all of the current is carried by the power device, the gate–to–drain voltage clamp element may be small in size. This technique of establishing a temperature compensated drain–to–source sustaining voltage (Figure 7) effectively removes the possibility of drain–to–source avalanche in the power device.

The gate–to–drain voltage clamp technique is particularly useful for snubbing loads where the inductive energy would otherwise avalanche the power device. An improvement in ruggedness of at least four times has been observed when inductive energy is dissipated in the gate–to–drain clamped conduction mode rather than in the more stressful gate–to–source avalanche mode.

TYPICAL APPLICATIONS: INJECTOR DRIVER, SOLENOIDS, LAMPS, RELAY COILS

The MLP1N06CL has been designed to allow direct interface to the output of a microcontrol unit to control an isolated load. No additional series gate resistance is required, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition in the event of an MCU failure. The internal clamps allow the device to be used without any external transistent suppressing components.



Designer's™ Data Sheet
SMARTDISCRETES™

Internally Clamped, Current Limited N–Channel Logic Level Power MOSFET

MLP2N06CL

Motorola Preferred Device

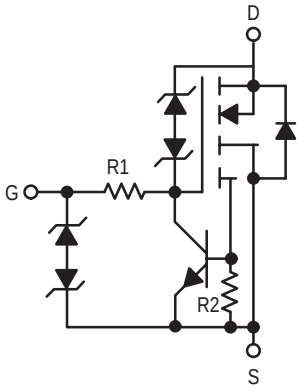
VOLTAGE CLAMPED
CURRENT LIMITING
MOSFET
62 VOLTS (CLAMPED)
$R_{DS(on)}$ = 0.4 OHMS

The MLP2N06CL is designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontrol unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in–rush current or a shorted load condition could occur.

This logic level power MOSFET features current limiting for short circuit protection, integrated Gate–Source clamping for ESD protection and integral Gate–Drain clamping for over–voltage protection and Sensefet technology for low on–resistance. No additional gate series resistance is required when interfacing to the output of a MCU, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition.

The internal Gate–Source and Gate–Drain clamps allow the device to be applied without use of external transient suppression components. The Gate–Source clamp protects the MOSFET input from electrostatic voltage stress up to 2.0 kV. The Gate–Drain clamp protects the MOSFET drain from the avalanche stress that occurs with inductive loads. Their unique design provides voltage clamping that is essentially independent of operating temperature.

The MLP2N06CL is fabricated using Motorola's SMARTDISCRETES™ technology which combines the advantages of a power MOSFET output device with the on–chip protective circuitry that can be obtained from a standard MOSFET process. This approach offers an economical means of providing protection to power MOSFETs from harsh automotive and industrial environments. SMARTDISCRETES™ devices are specified over a wide temperature range from –50°C to 150°C.



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

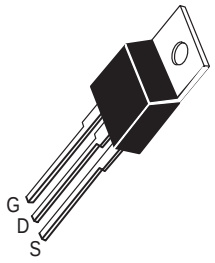
Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	Clamped	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	Clamped	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±10	Vdc
Drain Current — Continuous @ T_C = 25°C	I_D	Self–limited	Adc
Total Power Dissipation @ T_C = 25°C	P_D	40	Watts
Electrostatic Voltage	ESD	2.0	kV
Operating and Storage Temperature Range	T_J, T_{stg}	–50 to 150	°C

THERMAL CHARACTERISTICS

Maximum Junction Temperature	$T_{J(max)}$	150	°C
Thermal Resistance – Junction to Case	$R_{\theta JC}$	3.12	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 sec.	T_L	260	°C

DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS

Single Pulse Drain–to–Source Avalanche Energy (Starting T_J = 25°C, I_D = 2.0 A, L = 40 mH)	E_{AS}	80	mJ



CASE 221A–06, Style 5
TO–220AB

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

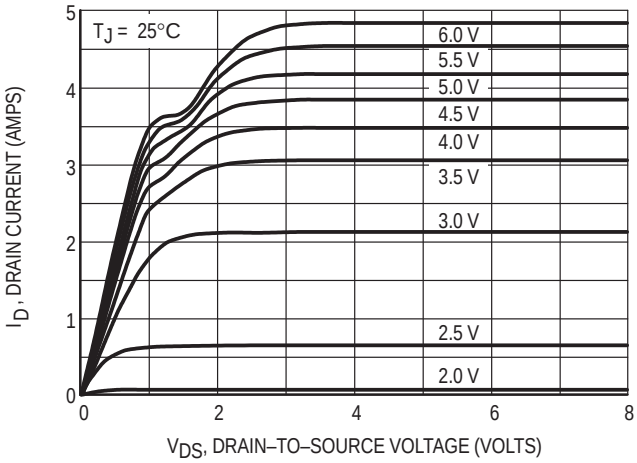
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$				Vdc
(I_D = 20 mAdc, V_{GS} = 0 Vdc)		58	62	66	
(I_D = 20 mAdc, V_{GS} = 0 Vdc, T_J = 150°C)		58	62	66	
Zero Gate Voltage Drain Current	I_{DSS}				μAdc
(V_{DS} = 40 Vdc, V_{GS} = 0 Vdc)		—	0.6	5.0	
(V_{DS} = 40 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		—	6.0	20	
Gate–Source Leakage Current	I_{GSS}				μAdc
(V_G = 5.0 Vdc, V_{DS} = 0 Vdc)		—	0.5	5.0	
(V_G = 5.0 Vdc, V_{DS} = 0 Vdc, T_J = 150°C)		—	1.0	20	
ON CHARACTERISTICS(1)					
Gate Threshold Voltage	$V_{GS(th)}$				Vdc
(I_D = 250 μAdc, V_{DS} = V_{GS})		1.0	1.5	2.0	
(I_D = 250 μAdc, V_{DS} = V_{GS}, T_J = 150°C)		0.6	1	1.6	
Static Drain Current Limit	$I_{D(lim)}$				Adc
(V_{GS} = 5.0 Vdc, V_{DS} = 10 Vdc)		3.8	4.4	5.2	
(V_{GS} = 5.0 Vdc, V_{DS} = 10 Vdc, T_J = 150°C)		1.6	2.4	2.9	
Static Drain–to–Source On–Resistance	$R_{DS(on)}$				Ohms
(I_D = 1.0 Adc, V_{GS} = 5.0 Vdc)		—	0.3	0.4	
(I_D = 1.0 Adc, V_{GS} = 5.0 Vdc, T_J = 150°C)		—	0.53	0.7	
Forward Transconductance (I_D = 1.0 Adc, V_{DS} = 10 Vdc)	g_{FS}	1.0	1.4	—	mhos
Static Source–to–Drain Diode Voltage	V_{SD}				Vdc
(I_S = 1.0 Adc, V_{GS} = 0 Vdc)		—	1.1	1.5	
SWITCHING CHARACTERISTICS(2)					
Turn–On Delay Time	$t_{d(on)}$	—	1.0	1.5	μs
Rise Time	t_r	—	3.0	5.0	
Turn–Off Delay Time	$t_{d(off)}$	—	5.0	8.0	
Fall Time	t_f	—	3.0	5.0	

(V_{DD} = 30 Vdc, I_D = 1.0 Adc, $V_{GS(on)}$ = 5.0 Vdc, R_{GS} = 25 Ohms)

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.



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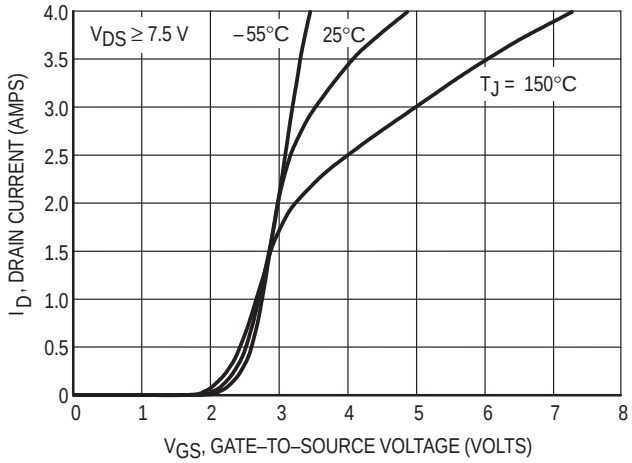

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Back–to–back polysilicon diodes between gate and source provide ESD protection to greater than 2 kV, HBM. This on–chip protection feature eliminates the need for an external Zener diode for systems with potentially heavy line transients.

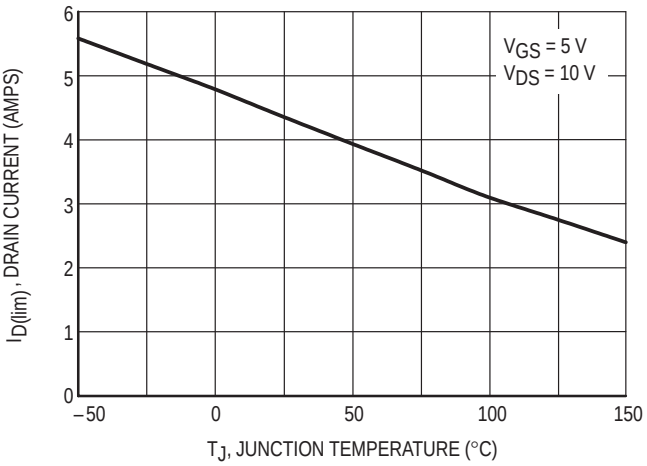


Figure 3. $I_{D(lim)}$ Variation With Temperature

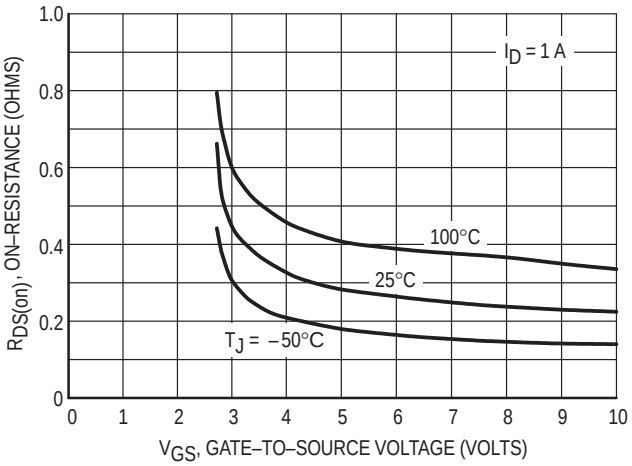


Figure 4. $R_{DS(on)}$ Variation With Gate–To–Source Voltage

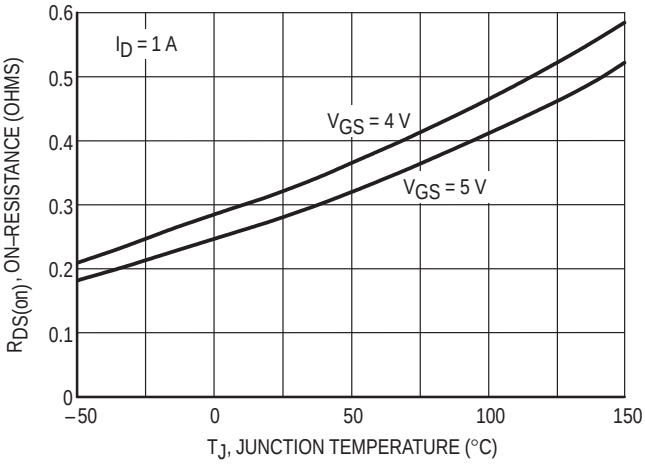


Figure 5. On–Resistance Variation With Temperature

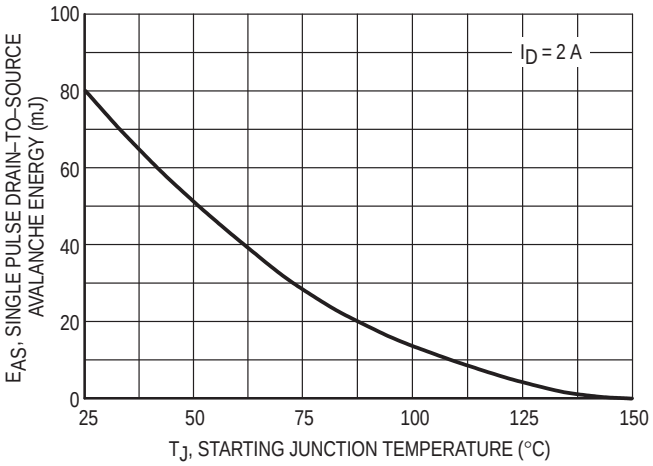


Figure 6. Maximum Avalanche Energy versus Starting Junction Temperature

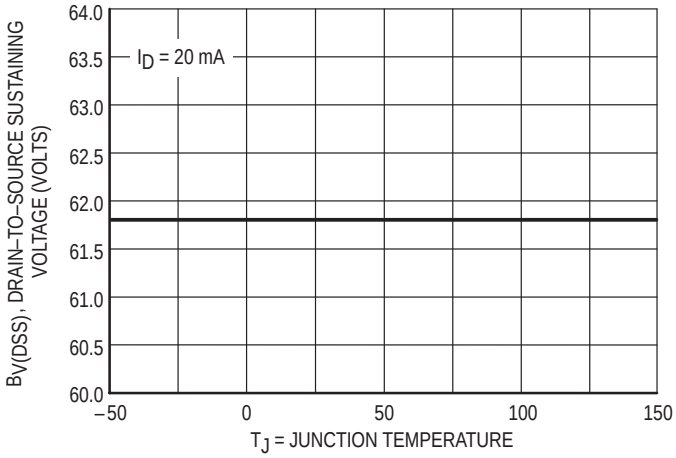


Figure 7. Drain–Source Sustaining Voltage Variation With Temperature

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance — General Data and Its Use” provides detailed instructions.

MAXIMUM DC VOLTAGE CONSIDERATIONS

The maximum drain–to–source voltage that can be continuously applied across the MLP2N06CL when it is in current limit is a function of the power that must be dissipated. This power is determined by the maximum current limit at maximum rated operating temperature (1.8 A at 150°C) and not the $R_{DS(on)}$. The maximum voltage can be calculated by the following equation:

$$V_{supply} = \frac{(150 - T_A)}{I_{D(lim)} (R_{\theta JC} + R_{\theta CA})}$$

where the value of $R_{\theta CA}$ is determined by the heatsink that is being used in the application.

DUTY CYCLE OPERATION

When operating in the duty cycle mode, the maximum drain voltage can be increased. The maximum operating temperature is related to the duty cycle (DC) by the following equation:

$$T_C = (V_{DS} \times I_D \times DC \times R_{\theta CA}) + T_A$$

The maximum value of V_{DS} applied when operating in a duty cycle mode can be approximated by:

$$V_{DS} = \frac{150 - T_C}{I_{D(lim)} \times DC \times R_{\theta JC}}$$

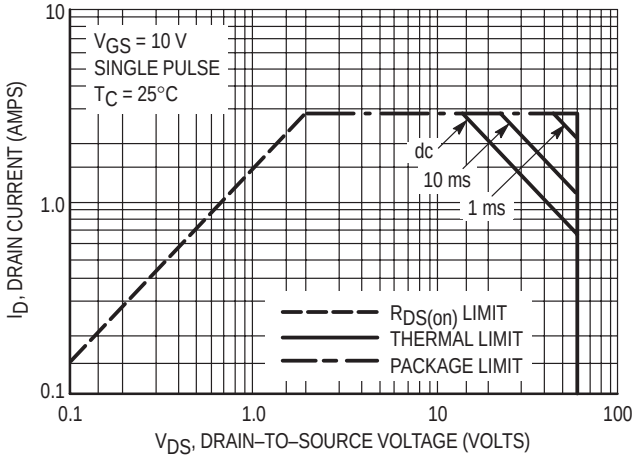


Figure 8. Maximum Rated Forward Bias Safe Operating Area (MLP2N06CL)

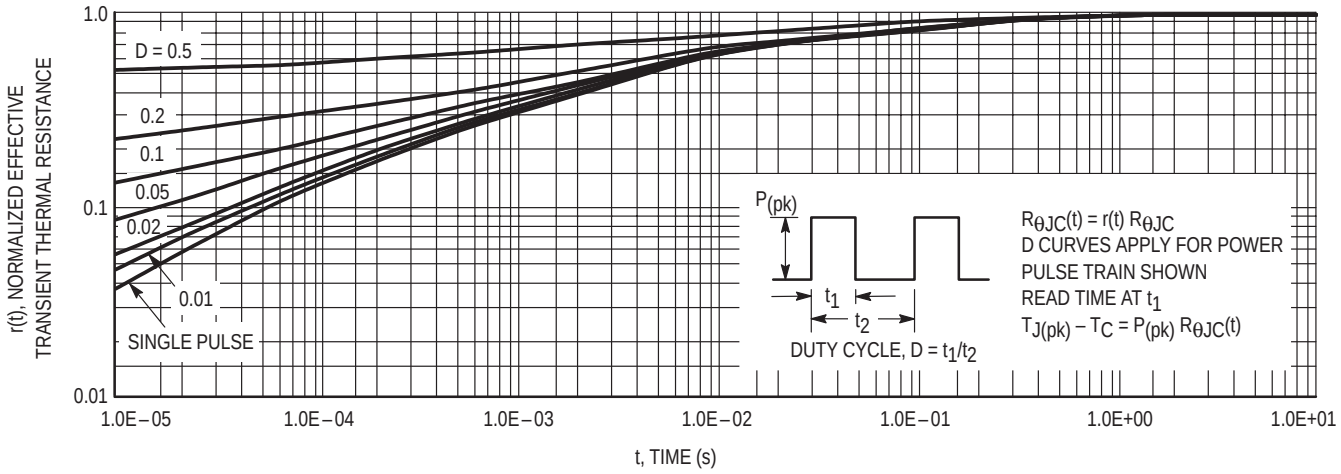


Figure 9. Thermal Response (MLP2N06CL)

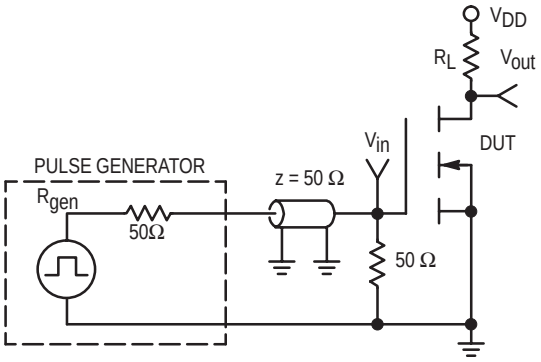


Figure 10. Switching Test Circuit

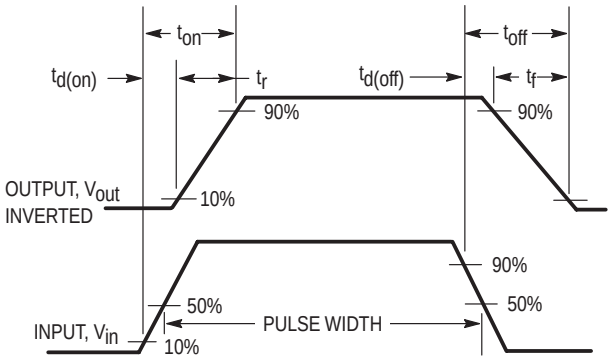


Figure 11. Switching Waveforms

ACTIVE CLAMPING

SMARTDISCRETES technology can provide on–chip realization of the popular gate–to–source and gate–to–drain Zener diode clamp elements. Until recently, such features have been implemented only with discrete components which consume board space and add system cost. The SMARTDISCRETES technology approach economically melds these features and the power chip with only a slight increase in chip area.

In practice, back–to–back diode elements are formed in a polysilicon region monolithicly integrated with, but electrically isolated from, the main device structure. Each back–to–back diode element provides a temperature compensated voltage element of about 7.2 volts. As the polysilicon region is formed on top of silicon dioxide, the diode elements are free from direct interaction with the conduction regions of the power device, thus eliminating parasitic electrical effects while maintaining excellent thermal coupling.

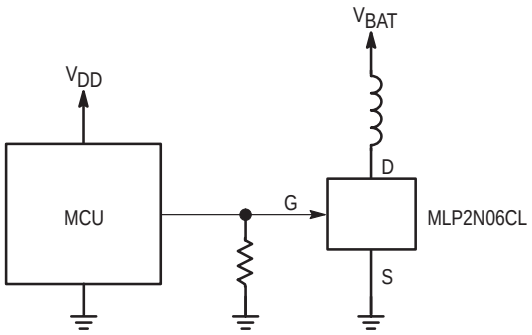
To achieve high gate–to–drain clamp voltages, several voltage elements are strung together; the MLP2N06CL uses 8 such elements. Customarily, two voltage elements are used to provide a 14.4 volt gate–to–source voltage clamp. For the MLP2N06CL, the integrated gate–to–source voltage elements provide greater than 2.0 kV electrostatic voltage protection.

The avalanche voltage of the gate–to–drain voltage clamp is set less than that of the power MOSFET device. As soon as the drain–to–source voltage exceeds this avalanche voltage, the resulting gate–to–drain Zener current builds a gate voltage across the gate–to–source impedance, turning on the power device which then conducts the current. Since virtually all of the current is carried by the power device, the gate–to–drain voltage clamp element may be small in size. This technique of establishing a temperature compensated drain–to–source sustaining voltage (Figure 7) effectively removes the possibility of drain–to–source avalanche in the power device.

The gate–to–drain voltage clamp technique is particularly useful for snubbing loads where the inductive energy would otherwise avalanche the power device. An improvement in ruggedness of at least four times has been observed when inductive energy is dissipated in the gate–to–drain clamped conduction mode rather than in the more stressful gate–to–source avalanche mode.

TYPICAL APPLICATIONS: INJECTOR DRIVER, SOLENOIDS, LAMPS, RELAY COILS

The MLP2N06CL has been designed to allow direct interface to the output of a microcontrol unit to control an isolated load. No additional series gate resistance is required, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition in the event of an MCU failure. The internal clamps allow the device to be used without any external transistent suppressing components.



Medium Power Surface Mount Products

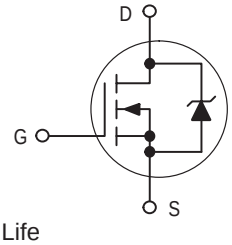
TMOS Dual N-Channel Field Effect Transistors

MMDF1N05E

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's TMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

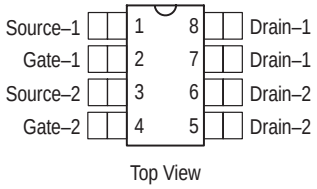
TMOS®

DUAL TMOS MOSFET
50 VOLTS
1.5 AMPERE
$R_{DS(on)}$ = 0.30 OHM



CASE 751–05, Style 11
SO–8

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided
- I_{DSS} Specified at Elevated Temperature



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DS}	50	Volts
Gate–to–Source Voltage — Continuous	V_{GS}	±20	Volts
Drain Current — Continuous — Pulsed	I_D I_{DM}	2.0 10	Amps
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 V, V_{GS} = 10 V, I_L = 2 Apk)	E_{AS}	300	mJ
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Total Power Dissipation @ T_A = 25°C	P_D	2.0	Watts
Thermal Resistance – Junction to Ambient (1)	$R_{\theta JA}$	62.5	°C/W
Maximum Temperature for Soldering, Time in Solder Bath	T_L	260 10	°C Sec

DEVICE MARKING

F1N05

(1) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF1N05ER2	13″	12 mm embossed tape	2500

REV 4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA)		$V_{(BR)DSS}$	50	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 V, V_{GS} = 0)		I_{DSS}	—	—	250	μAdc
Gate–Body Leakage Current (V_{GS} = 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	—	3.0	Vdc
Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc) (V_{GS} = 4.5 Vdc, I_D = 0.6 Adc)		$R_{DS(on)}$ $R_{DS(on)}$	— —	— —	0.30 0.50	Ohms
Forward Transconductance (V_{DS} = 15 V, I_D = 1.5 A)		g_{FS}	—	1.5	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	330	—	pF
Output Capacitance		C_{oss}	—	160	—	
Reverse Transfer Capacitance		C_{rss}	—	50	—	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 10 V, I_D = 1.5 A, R_L = 10 Ω, V_G = 10 V, R_G = 50 Ω)	$t_{d(on)}$	—	—	20	ns
Rise Time		t_r	—	—	30	
Turn–Off Delay Time		$t_{d(off)}$	—	—	40	
Fall Time		t_f	—	—	25	
Total Gate Charge	(V_{DS} = 10 V, I_D = 1.5 A, V_{GS} = 10 V)	Q_g	—	12.5	—	nC
Gate–Source Charge		Q_{gs}	—	1.9	—	
Gate–Drain Charge		Q_{gd}	—	3.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS (T_C = 25°C)						
Forward Voltage(1)	(I_S = 1.5 A, V_{GS} = 0 V) (dI_S/dt = 100 A/μs)	V_{SD}	—	—	1.6	V
Reverse Recovery Time		t_{rr}	—	45	—	ns

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

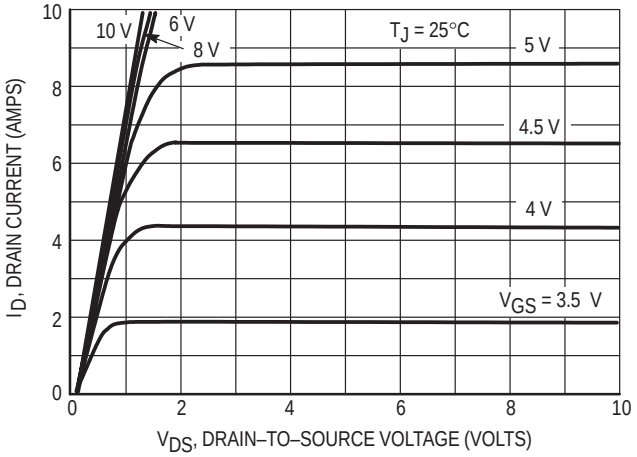


Figure 1. On–Region Characteristics

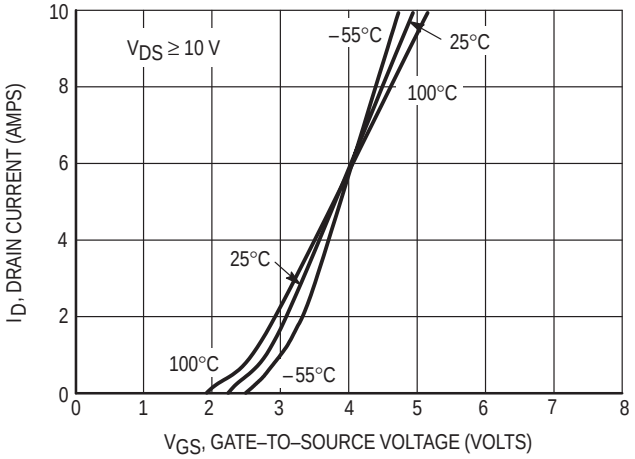


Figure 2. Transfer Characteristics

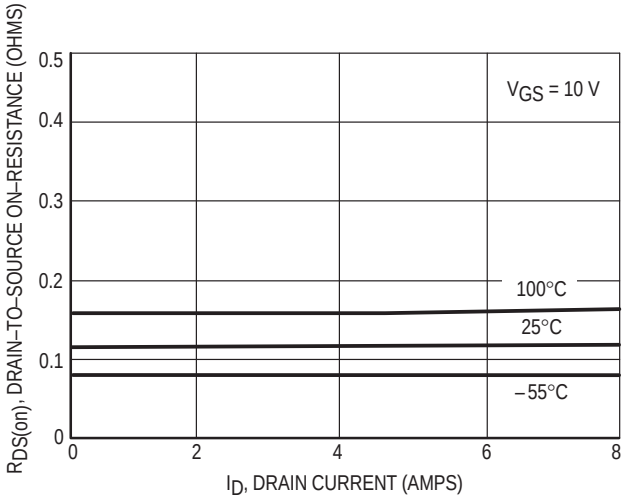


Figure 3. On–Resistance versus Drain Current

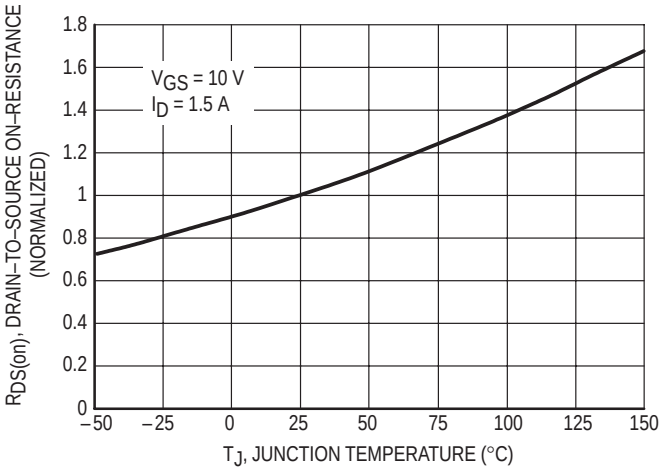


Figure 4. On–Resistance Variation with Temperature

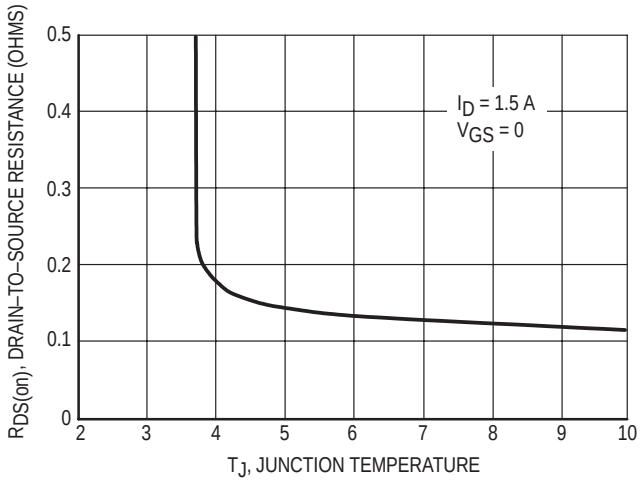


Figure 5. On Resistance versus Gate–To–Source Voltage

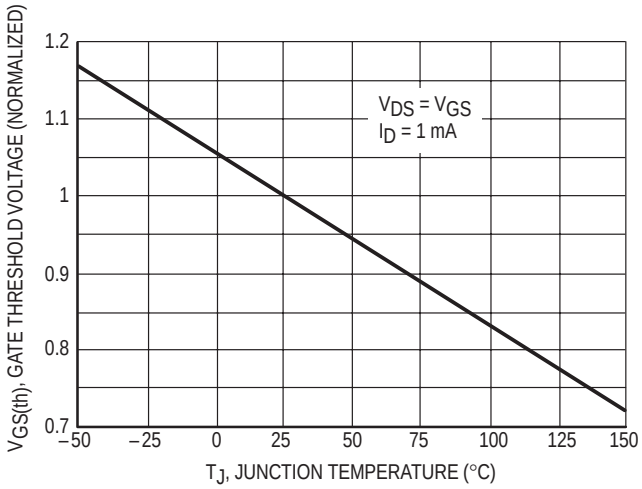


Figure 6. Gate Threshold Voltage Variation with Temperature

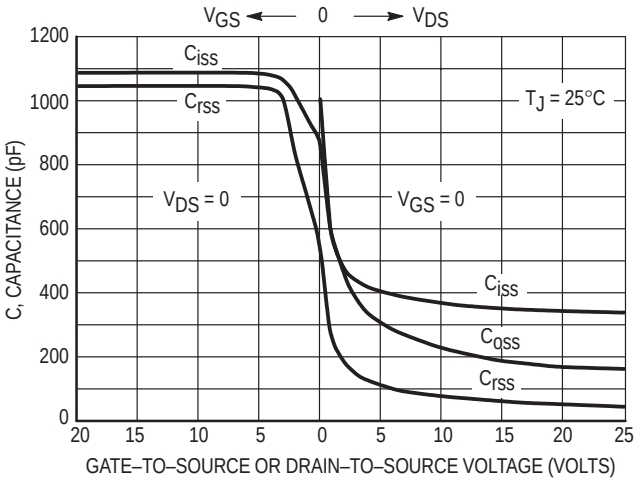


Figure 7. Capacitance Variation

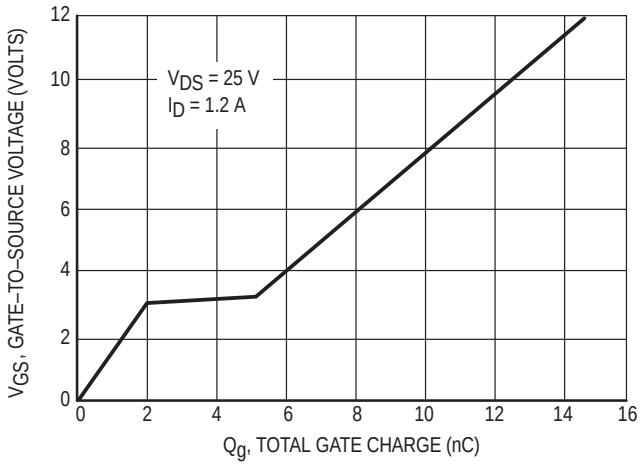


Figure 8. Gate Charge versus Gate–To–Source Voltage

SAFE OPERATING AREA INFORMATION

Forward Biased Safe Operating Area

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance — General Data and Its Use” provides detailed instructions.

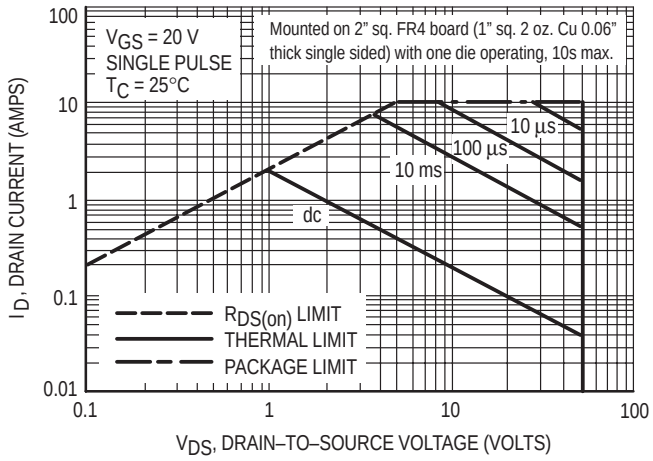


Figure 9. Maximum Rated Forward Biased Safe Operating Area

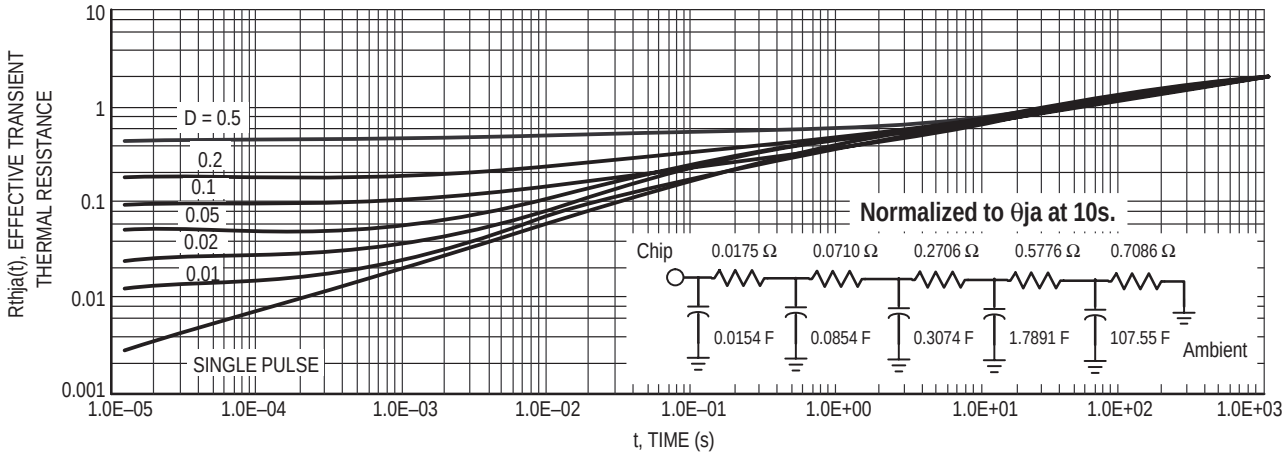


Figure 10. Thermal Response

Designer's™ Data Sheet

Medium Power Surface Mount Products

Complementary TMOS Field Effect Transistors

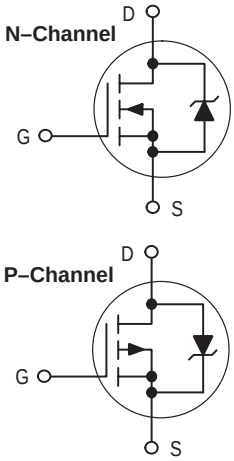
MMDF2C01HD

Motorola Preferred Device

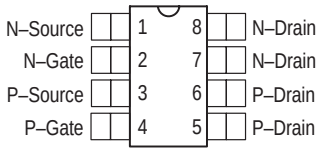
COMPLEMENTARY DUAL TMOS POWER FET
2.0 AMPERES
12 VOLTS
$R_{DS(on)}$ = 0.045 OHM (N–CHANNEL)
$R_{DS(on)}$ = 0.18 OHM (P–CHANNEL)

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided



CASE 751–05, Style 14
SO–8



Top View

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating		Symbol	Value	Unit
Drain–to–Source Voltage	N–Channel P–Channel	V_{DSS}	20 12	Vdc
Gate–to–Source Voltage		V_{GS}	± 8.0	Vdc
Drain Current — Continuous	N–Channel P–Channel	I_D	5.2 3.4	A
— Pulsed	N–Channel P–Channel	I_{DM}	48 17	
Operating and Storage Temperature Range		T_J and T_{stg}	–55 to 150	°C
Total Power Dissipation @ T_A= 25°C (2)		P_D	2.0	Watts
Thermal Resistance — Junction to Ambient (2)		$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds.		T_L	260	°C

DEVICE MARKING

D2C01

(1) Negative signs for P–Channel device omitted for clarity.
(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF2C01HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Polarity	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	(N) (P)	20 12	— —	— —	Vdc
Zero Gate Voltage Drain Current (V_{GS} = 0 Vdc, V_{DS} = 20 Vdc) (V_{GS} = 0 Vdc, V_{DS} = 12 Vdc)		I_{DSS}	(N) (P)	— —	— —	1.0 1.0	μAdc
Gate–Body Leakage Current (V_{GS} = ±8.0 Vdc, V_{DS} = 0)		I_{GSS}	—	—	—	100	nAdc
ON CHARACTERISTICS(2)							
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	(N) (P)	0.7 0.7	0.8 1.0	1.1 1.1	Vdc
Drain–to–Source On–Resistance (V_{GS} = 4.5 Vdc, I_D = 4.0 Adc) (V_{GS} = 4.5 Vdc, I_D = 2.0 Adc)		$R_{DS(on)}$	(N) (P)	— —	0.035 0.16	0.045 0.18	Ohm
Drain–to–Source On–Resistance (V_{GS} = 2.7 Vdc, I_D = 2.0 Adc) (V_{GS} = 2.7 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	(N) (P)	— —	0.043 0.2	0.055 0.22	Ohm
Forward Transconductance (V_{DS} = 2.5 Adc, I_D = 2.0 Adc) (V_{DS} = 2.5 Adc, I_D = 1.0 Adc)		g_{FS}	(N) (P)	3.0 3.0	6.0 4.75	— —	mhos
DYNAMIC CHARACTERISTICS							
Input Capacitance	(V_{DS} = 10 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	(N) (P)	— —	425 530	595 740	pF
Output Capacitance		C_{oss}	(N) (P)	— —	270 410	378 570	
Transfer Capacitance		C_{rss}	(N) (P)	— —	115 177	230 250	
SWITCHING CHARACTERISTICS(3)							
Turn–On Delay Time	(V_{DD} = 6.0 Vdc, I_D = 4.0 Adc, V_{GS} = 2.7 Vdc, R_G = 2.3 Ω)	$t_{d(on)}$	(N) (P)	— —	13 21	26 45	ns
Rise Time		t_r	(N) (P)	— —	60 156	120 315	
Turn–Off Delay Time	(V_{DD} = 6.0 Vdc, I_D = 2.0 Adc, V_{GS} = 2.7 Vdc, R_G = 6.0 Ω)	$t_{d(off)}$	(N) (P)	— —	20 38	40 75	
Fall Time		t_f	(N) (P)	— —	29 68	58 135	
Turn–On Delay Time	(V_{DS} = 6.0 Vdc, I_D = 4.0 Adc, V_{GS} = 4.5 Vdc, R_G = 2.3 Ω)	$t_{d(on)}$	(N) (P)	— —	10 16	20 35	
Rise Time		t_r	(N) (P)	— —	42 44	84 90	
Turn–Off Delay Time	(V_{DS} = 6.0 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(off)}$	(N) (P)	— —	24 68	48 135	
Fall Time		t_f	(N) (P)	— —	28 54	56 110	
Total Gate Charge	(V_{DS} = 10 Vdc, I_D = 4.0 Adc, V_{GS} = 4.5 Vdc)	Q_T	(N) (P)	— —	9.2 9.3	13 13	nC
Gate–Source Charge		Q_1	(N) (P)	— —	1.3 0.8	— —	
Gate–Drain Charge	(V_{DS} = 6.0 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc)	Q_2	(N) (P)	— —	3.5 4.0	— —	
		Q_3	(N) (P)	— —	3.0 3.0	— —	

(1) Negative signs for P–Channel device omitted for clarity.

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(3) Switching characteristics are independent of operating junction temperature.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Polarity	Min	Typ	Max	Unit
SOURCE–DRAIN DIODE CHARACTERISTICS (T_C = 25°C)							
Forward Voltage(2)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	(N) (P)	— —	0.95 1.69	1.1 2.0	Vdc
Reverse Recovery Time	($I_F = I_S$, dI_S/dt = 100 A/μs)	t_{rr}	(N) (P)	— —	38 48	— —	ns
		t_a	(N) (P)	— —	17 23	— —	
		t_b	(N) (P)	— —	22 25	— —	
Reverse Recovery Stored Charge		Q_{RR}	(N) (P)	— —	0.028 0.05	— —	μC

(1) Negative signs for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

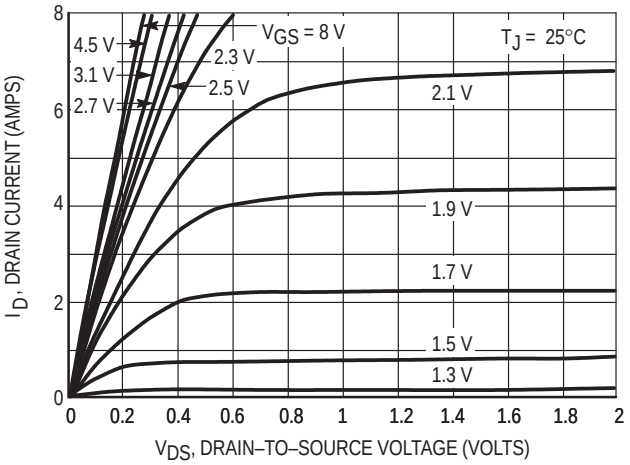


Figure 1. On–Region Characteristics

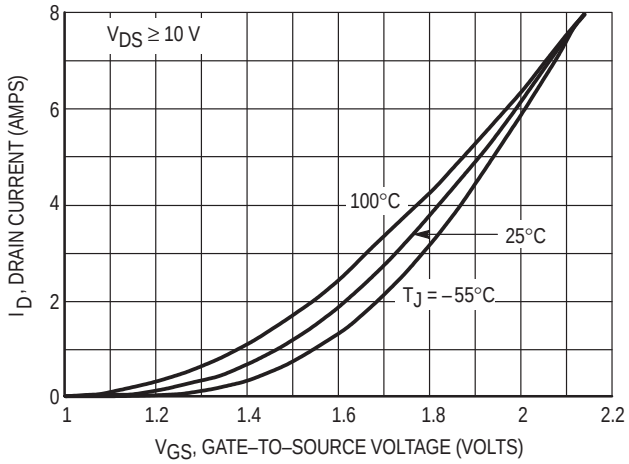


Figure 2. Transfer Characteristics

P–Channel

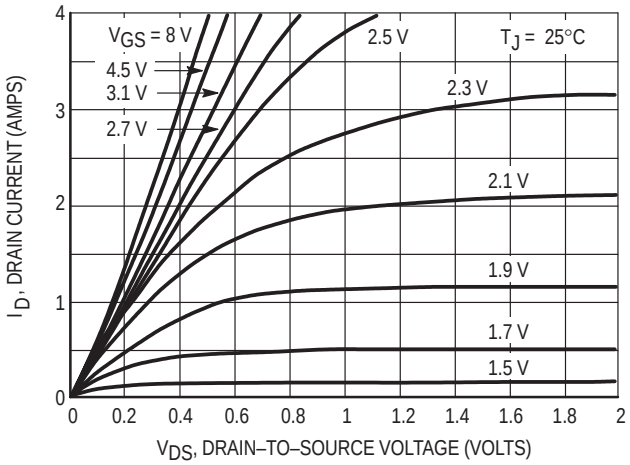


Figure 1. On–Region Characteristics

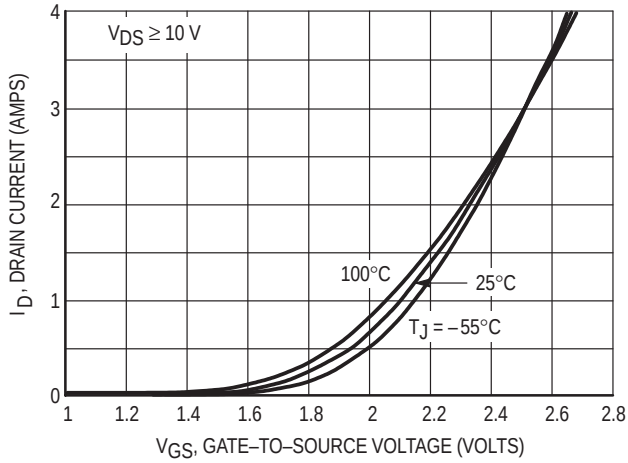


Figure 2. Transfer Characteristics

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

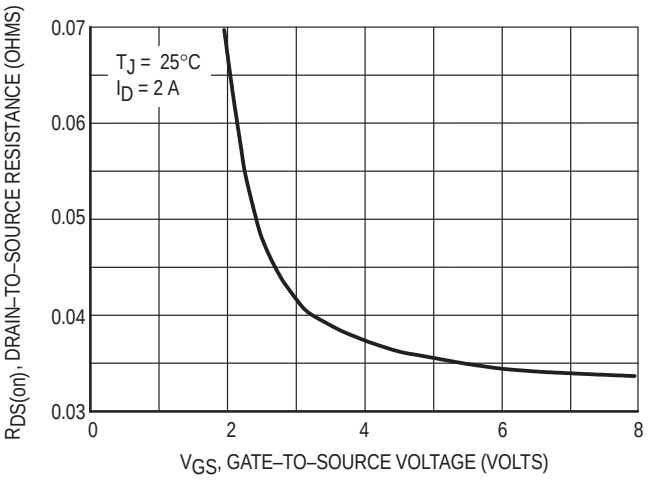


Figure 3. On–Resistance versus Gate–To–Source Voltage

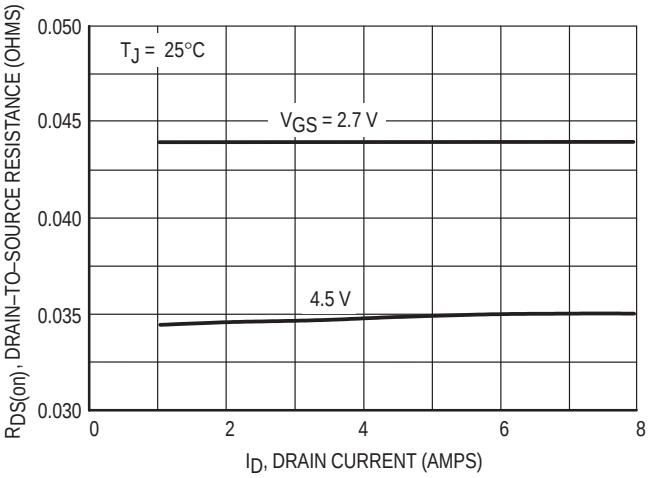


Figure 4. On–Resistance versus Drain Current and Gate Voltage

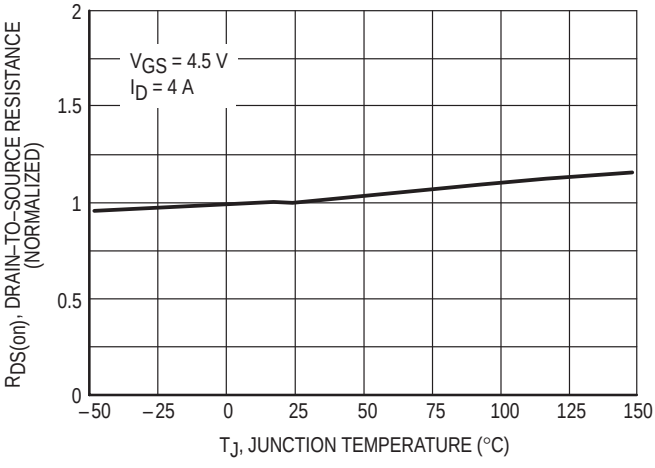


Figure 5. On–Resistance Variation with Temperature

P–Channel

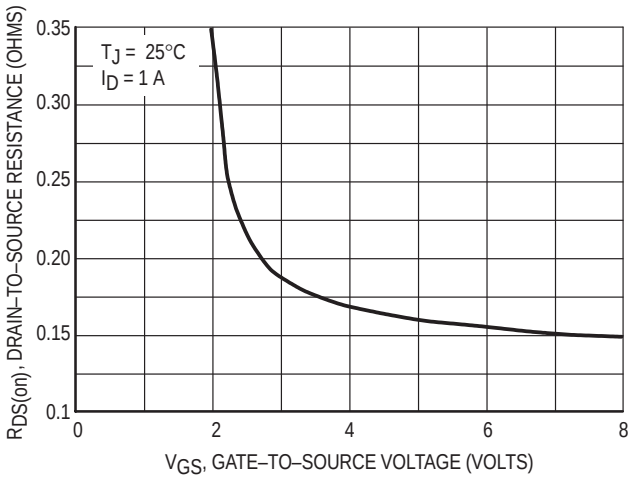


Figure 3. On–Resistance versus Gate–To–Source Voltage

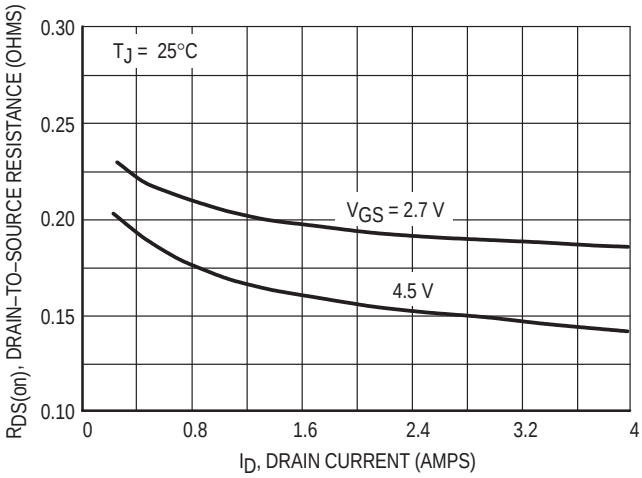


Figure 4. On–Resistance versus Drain Current and Gate Voltage

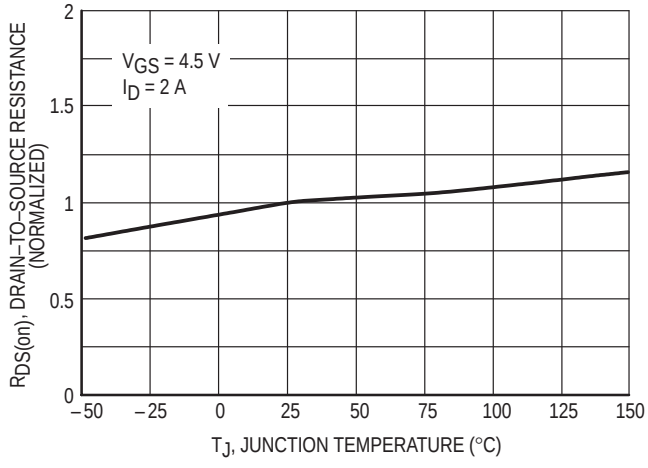


Figure 5. On–Resistance Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

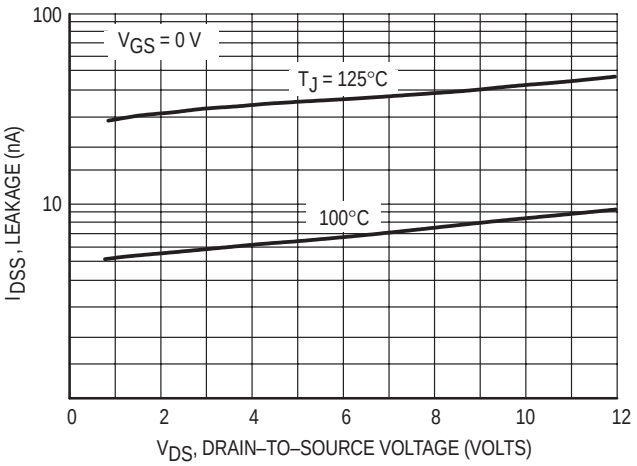


Figure 6. Drain–To–Source Leakage Current versus Voltage

P–Channel

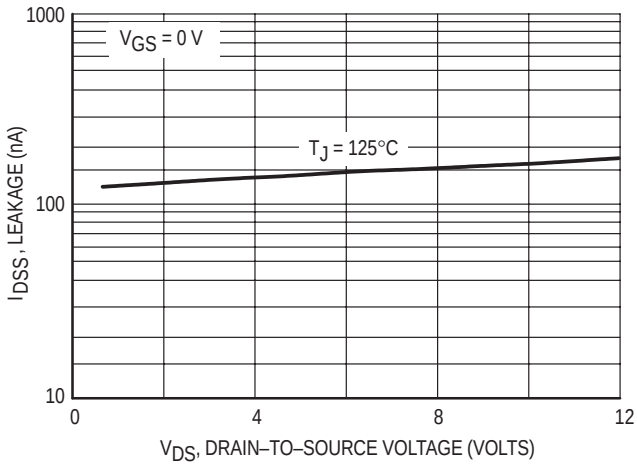


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

N–Channel

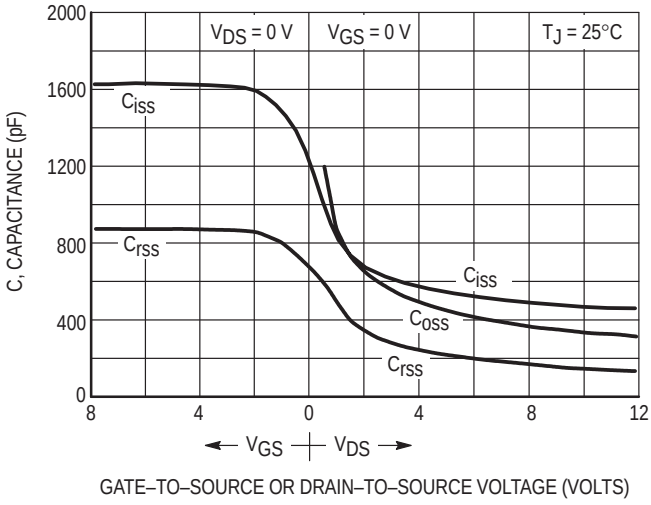


Figure 7. Capacitance Variation

P–Channel

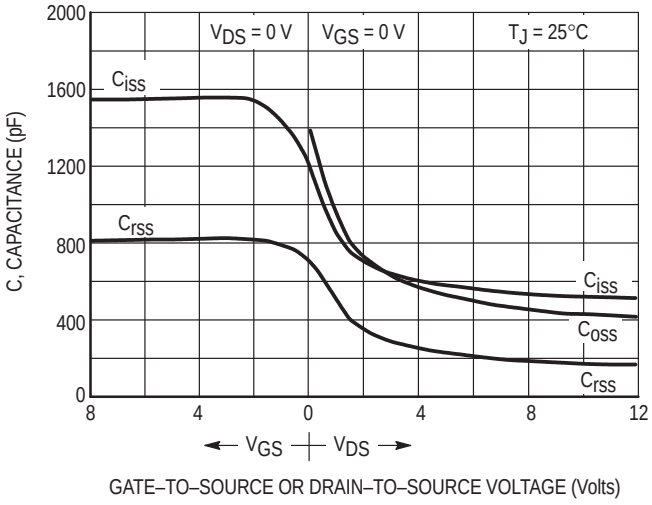


Figure 7. Capacitance Variation

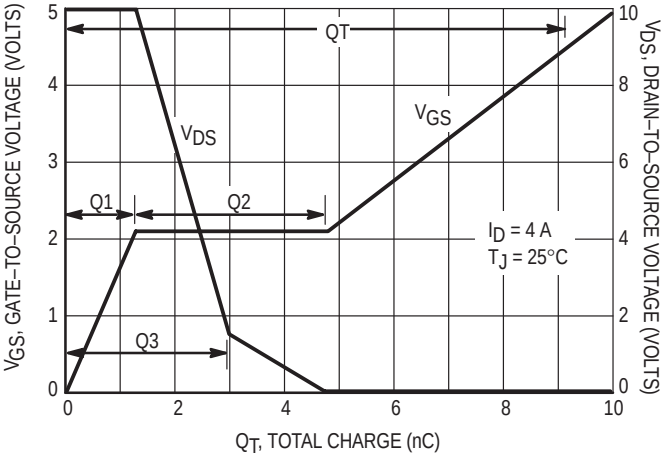


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

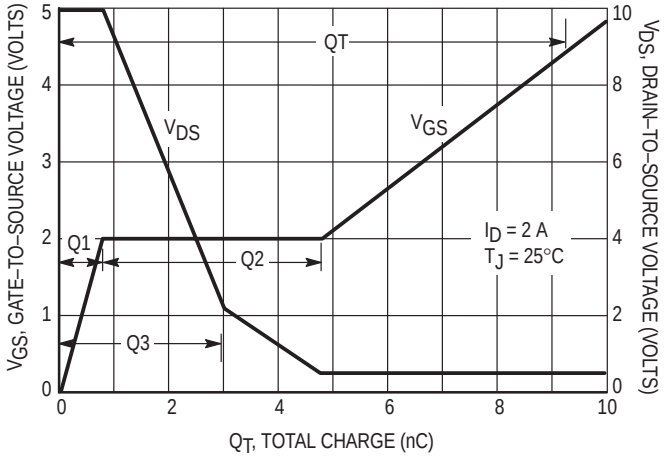


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

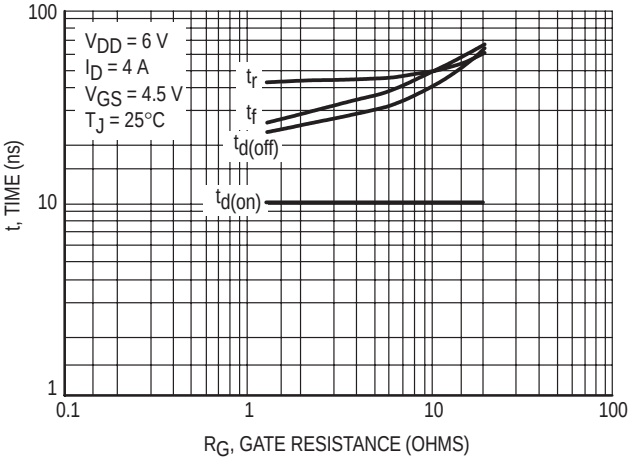


Figure 9. Resistive Switching Time Variation versus Gate Resistance

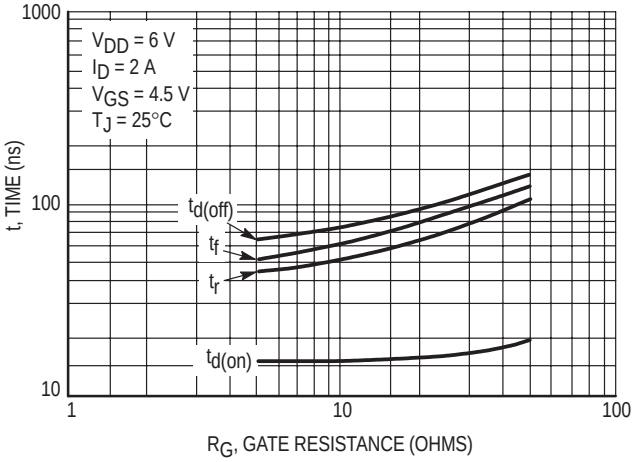


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 14. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

N–Channel

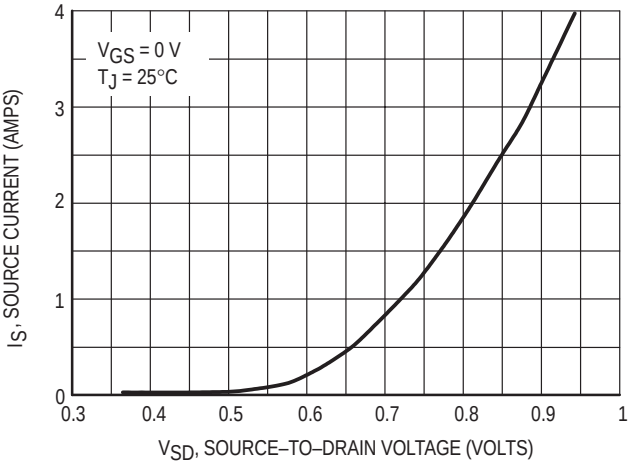


Figure 10. Diode Forward Voltage versus Current

P–Channel

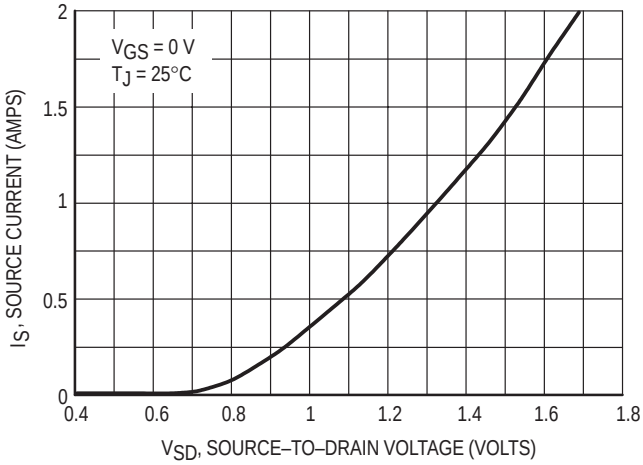


Figure 10. Diode Forward Voltage versus Current

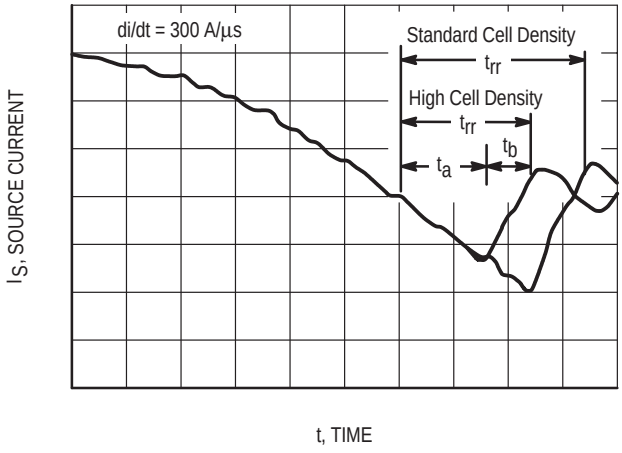


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

N–Channel

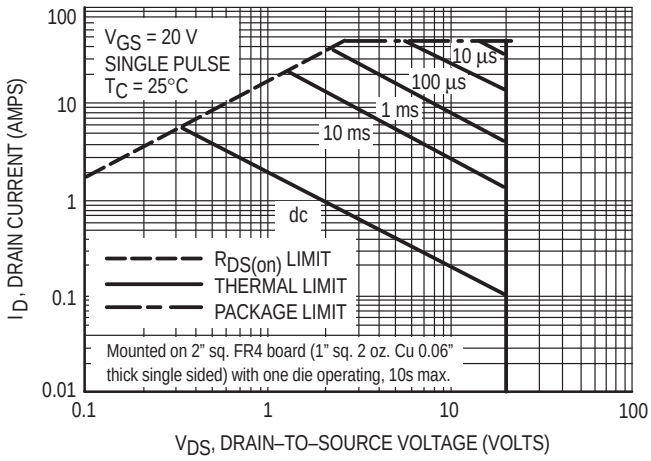


Figure 12. Maximum Rated Forward Biased Safe Operating Area

P–Channel

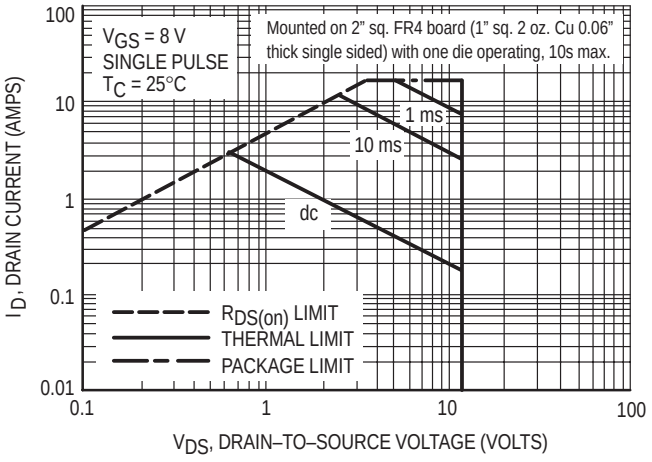


Figure 12. Maximum Rated Forward Biased Safe Operating Area

TYPICAL ELECTRICAL CHARACTERISTICS

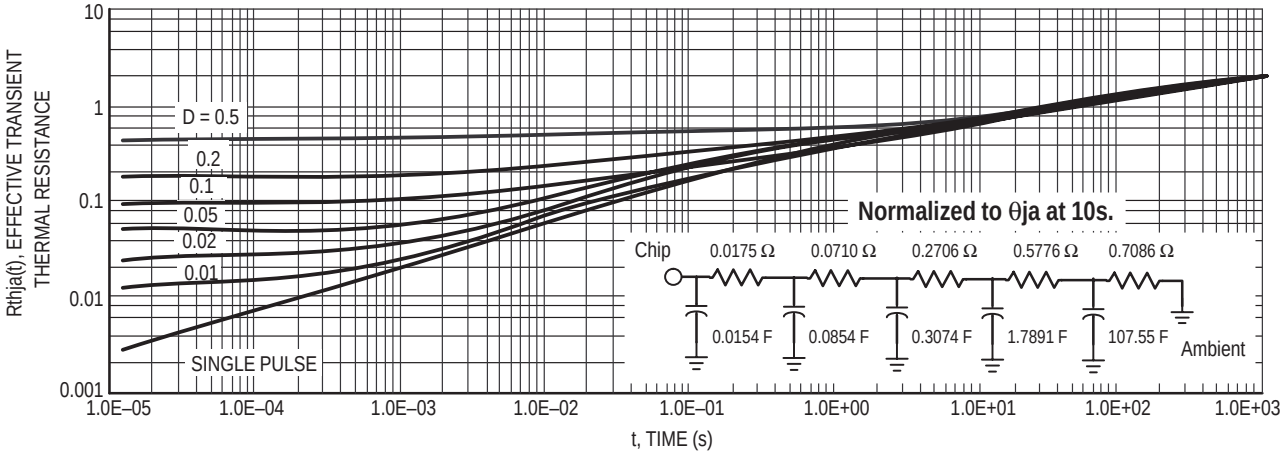


Figure 13. Thermal Response

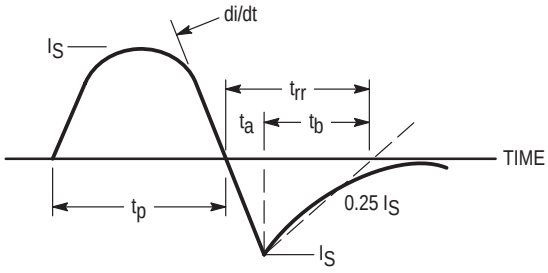


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

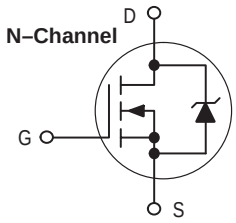
Complementary TMOS Field Effect Transistors

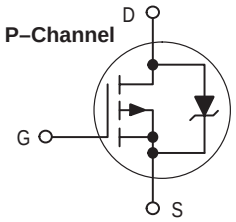
MMDF2C02E

COMPLEMENTARY DUAL TMOS POWER FET
2.5 AMPERES
25 VOLTS
$R_{DS(on)}$ = 0.100 OHM (N–CHANNEL)
$R_{DS(on)}$ = 0.25 OHM (P–CHANNEL)

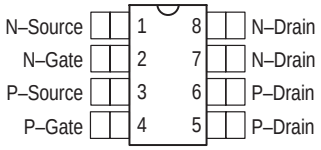
MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's TMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided





CASE 751–05, Style 14
SO–8



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating		Symbol	Value	Unit
Drain–to–Source Voltage		V_{DSS}	25	Vdc
Gate–to–Source Voltage		V_{GS}	± 20	Vdc
Drain Current — Continuous	N–Channel	I_D	3.6	Adc
	P–Channel		2.5	
— Pulsed	N–Channel	I_{DM}	18	
	P–Channel		13	
Operating and Storage Temperature Range		T_J and T_{stg}	– 55 to 150	°C
Total Power Dissipation @ T_A= 25°C (2)		P_D	2.0	Watts
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C		E_{AS}		mJ
(V_{DD} = 20 V, V_{GS} = 10 V, Peak I_L = 9.0 A, L = 6.0 mH, R_G = 25 Ω)	N–Channel		245	
(V_{DD} = 20 V, V_{GS} = 10 V, Peak I_L = 7.0 A, L = 10 mH, R_G = 25 Ω)	P–Channel		245	
Thermal Resistance — Junction to Ambient (2)		$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering, 0.0625″ from case. Time in Solder Bath is 10 seconds.		T_L	260	°C

DEVICE MARKING

F2C02

(1) Negative signs for P–Channel device omitted for clarity.
(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF2C02ER2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic	Symbol	Polarity	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)	$V_{(BR)DSS}$	—	25	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	(N) (P)	— —	— —	1.0 1.0	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	—	100	nAdc
ON CHARACTERISTICS(2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)	$V_{GS(th)}$	—	1.0	2.0	3.0	Vdc
Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.2 Adc) (V_{GS} = 10 Vdc, I_D = 2.0 Adc)	$R_{DS(on)}$	(N) (P)	— —	— —	0.100 0.250	Ohm
Drain–to–Source On–Resistance (V_{GS} = 4.5 Vdc, I_D = 1.0 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.0 Adc)	$R_{DS(on)}$	(N) (P)	— —	— —	0.200 0.400	Ohm
On–State Drain Current (V_{DS} = 5.0 Vdc, V_{GS} = 4.5 Vdc)	$I_{D(on)}$	(N) (P)	2.0 2.0	— —	— —	Adc
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.5 Adc) (V_{DS} = 3.0 Vdc, I_D = 1.0 Adc)	g_{FS}	(N) (P)	1.0 1.0	2.6 2.8	— —	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	(N) (P)	— —	380 340	532 475	pF
Output Capacitance (V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{oss}	(N) (P)	— —	235 220	329 300	
Transfer Capacitance	C_{rss}	(N) (P)	— —	55 75	110 150	
SWITCHING CHARACTERISTICS(3)						
Turn–On Delay Time	$t_{d(on)}$	(N) (P)	— —	10 20	30 40	ns
Rise Time (V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 9.1 Ω)	t_r	(N) (P)	— —	35 40	70 80	
Turn–Off Delay Time	$t_{d(off)}$	(N) (P)	— —	19 53	38 106	
Fall Time (V_{DD} = 10 Vdc, I_D = 1.0 Adc, V_{GS} = 5.0 Vdc, R_G = 25 Ω)	t_f	(N) (P)	— —	25 41	50 82	
Turn–On Delay Time	$t_{d(on)}$	(N) (P)	— —	7.0 13	21 26	
Rise Time (V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	t_r	(N) (P)	— —	17 29	30 58	
Turn–Off Delay Time	$t_{d(off)}$	(N) (P)	— —	27 30	48 60	
Fall Time (V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	t_f	(N) (P)	— —	18 28	30 56	
Total Gate Charge	Q_T	(N) (P)	— —	10.6 10	30 15	nC
Gate–Source Charge	Q_1	(N) (P)	— —	1.3 1.0	— —	
Gate–Drain Charge (V_{DS} = 16 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_2	(N) (P)	— —	2.9 3.5	— —	
	Q_3	(N) (P)	— —	2.7 3.0	— —	

(1) Negative signs for P–Channel device omitted for clarity.

(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(3) Switching characteristics are independent of operating junction temperature.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Polarity	Min	Typ	Max	Unit
SOURCE–DRAIN DIODE CHARACTERISTICS (T_C = 25°C)							
Forward Voltage(2)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	(N) (P)	— —	1.0 1.5	1.4 2.0	Vdc
Reverse Recovery Time see Figure 7	(I_F = I_S, dI_S/dt = 100 A/μs)	t_{rr}	(N) (P)	— —	34 32	66 64	ns
		t_a	(N) (P)	— —	17 19	— —	
		t_b	(N) (P)	— —	17 12	— —	
		Q_{RR}	(N) (P)	— —	0.025 0.035	— —	μC

(1) Negative signs for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

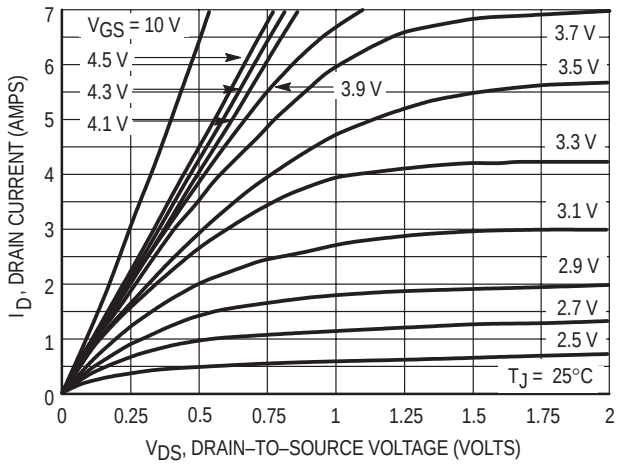


Figure 1. On–Region Characteristics

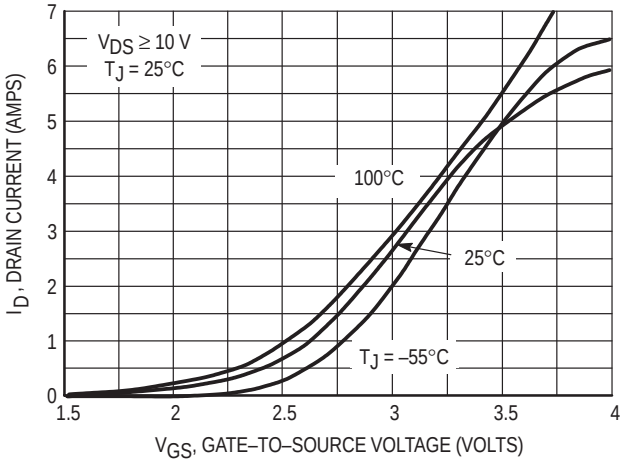


Figure 2. Transfer Characteristics

P–Channel

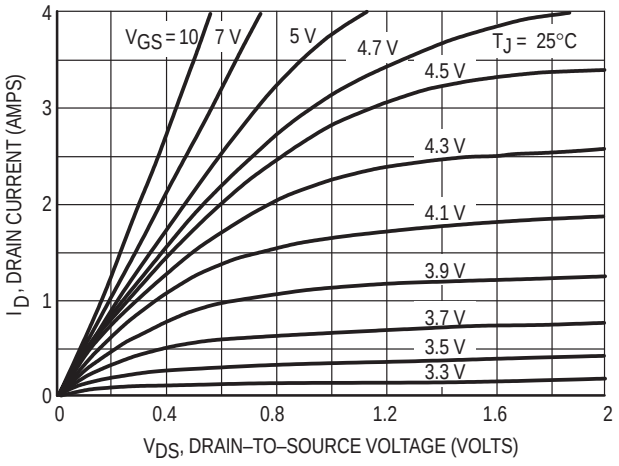


Figure 1. On–Region Characteristics

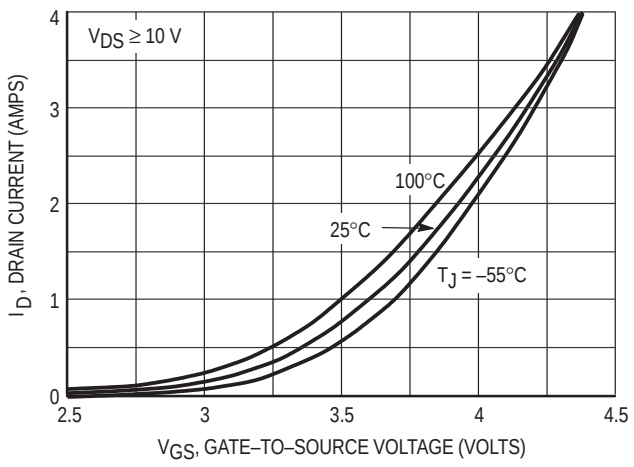


Figure 2. Transfer Characteristics

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

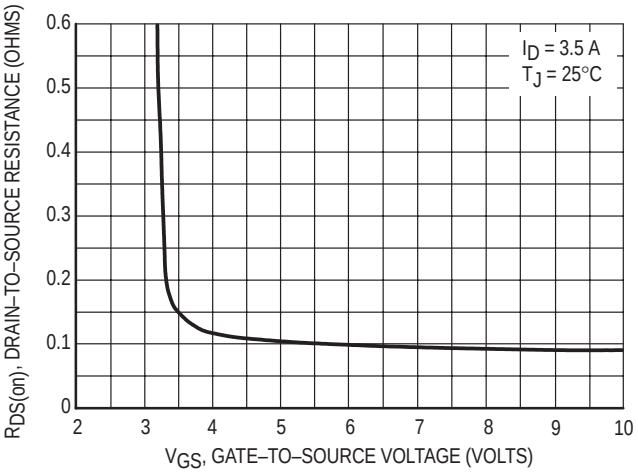


Figure 3. On–Resistance versus Gate–to–Source Voltage

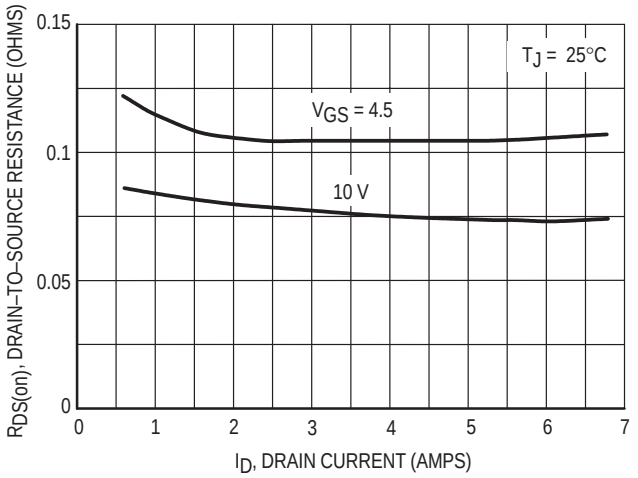


Figure 4. On–Resistance versus Drain Current and Gate Voltage

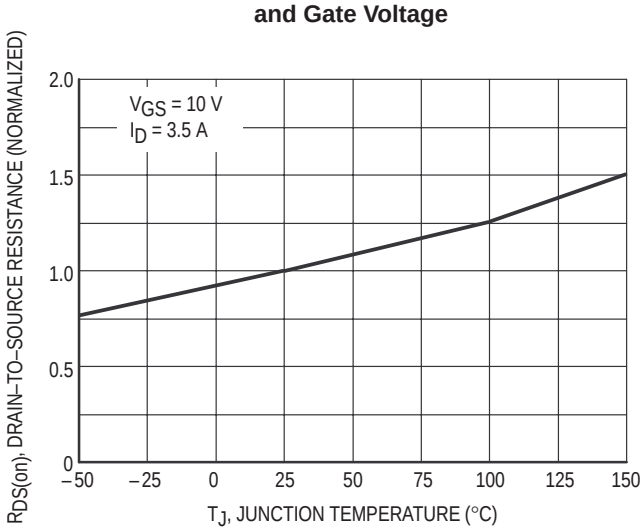


Figure 5. On–Resistance Variation with Temperature

P–Channel

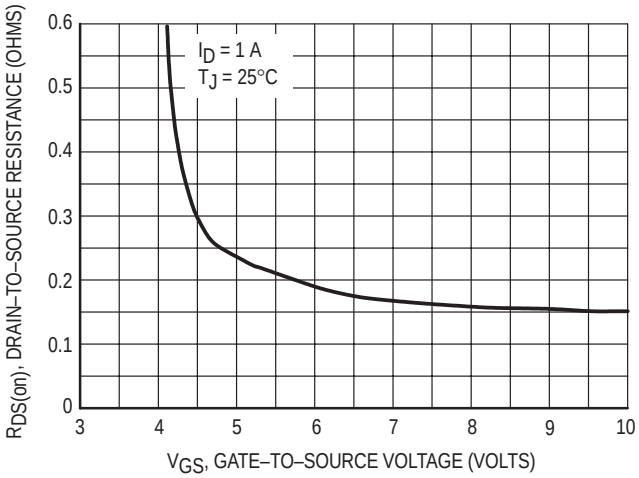


Figure 3. On–Resistance versus Gate–to–Source Voltage

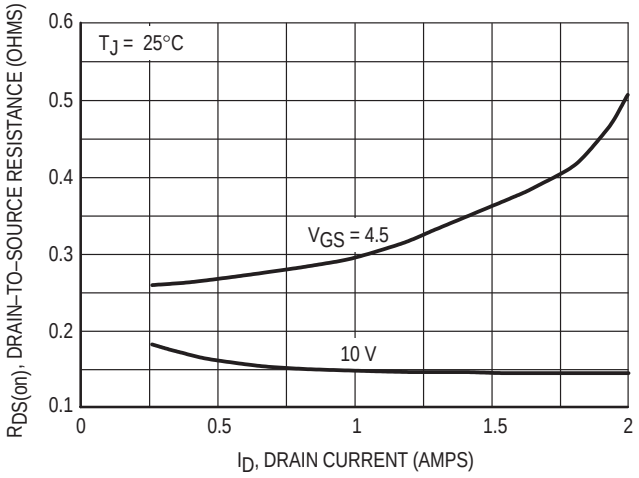


Figure 4. On–Resistance versus Drain Current and Gate Voltage

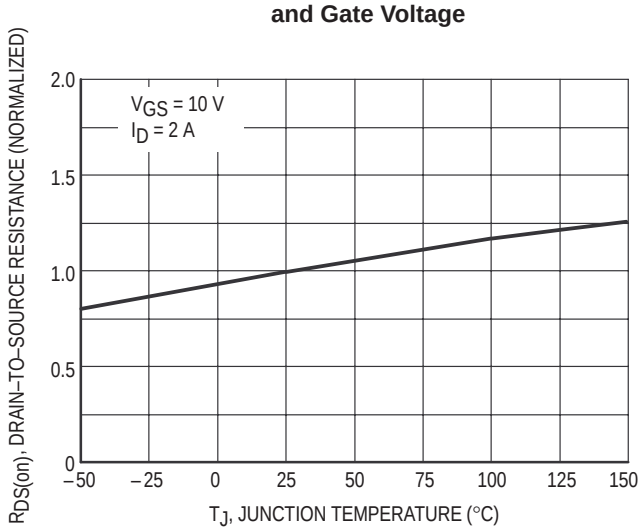


Figure 5. On–Resistance Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

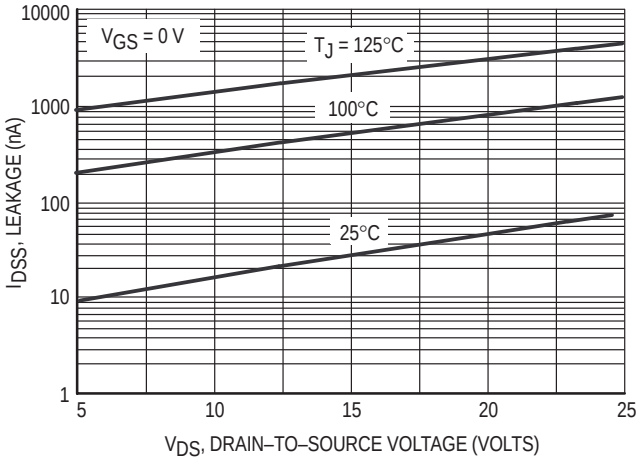


Figure 6. Drain–to–Source Leakage Current versus Voltage

P–Channel

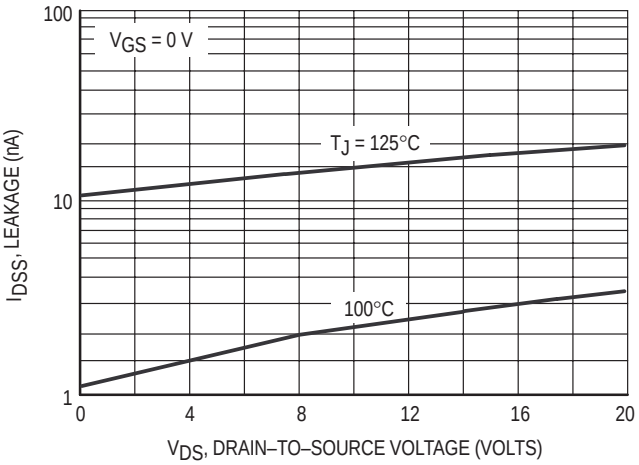


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

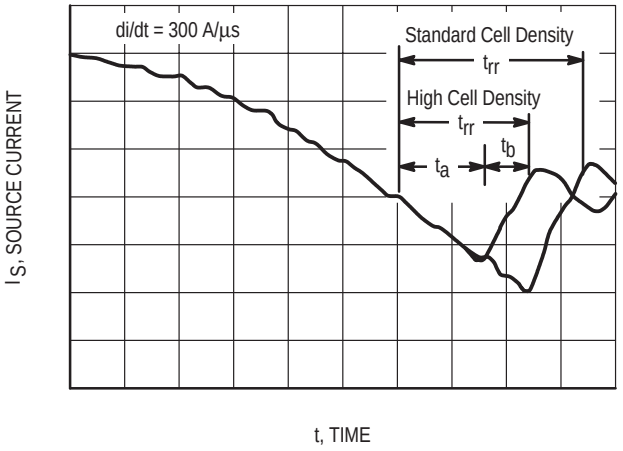


Figure 7. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 9). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

N–Channel

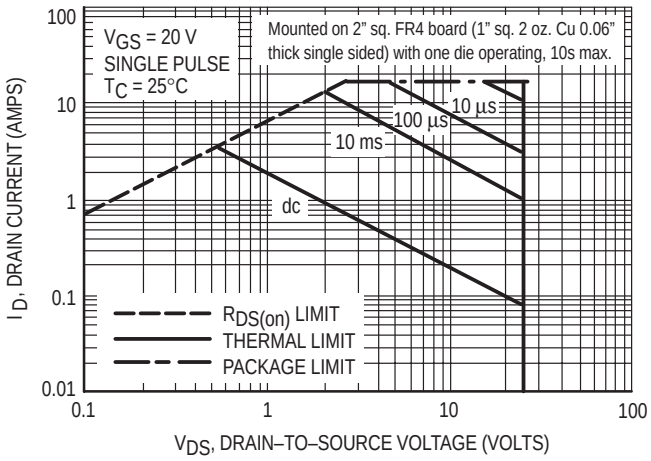


Figure 8. Maximum Rated Forward Biased Safe Operating Area

P–Channel

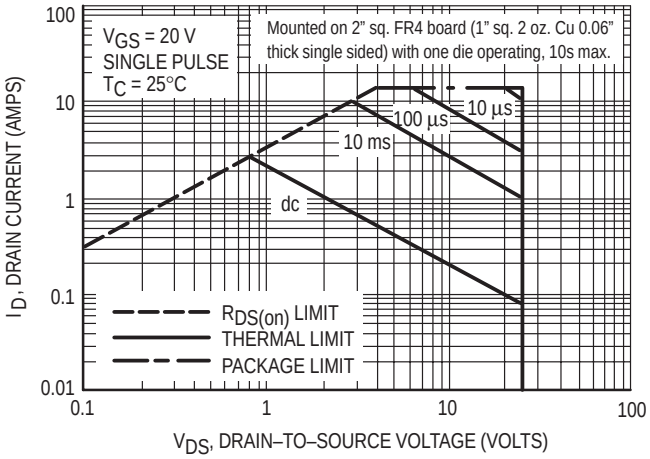


Figure 8. Maximum Rated Forward Biased Safe Operating Area

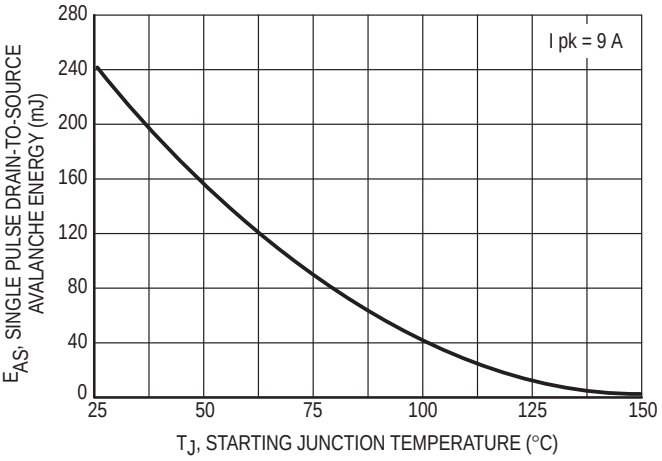


Figure 9. Maximum Avalanche Energy versus Starting Junction Temperature

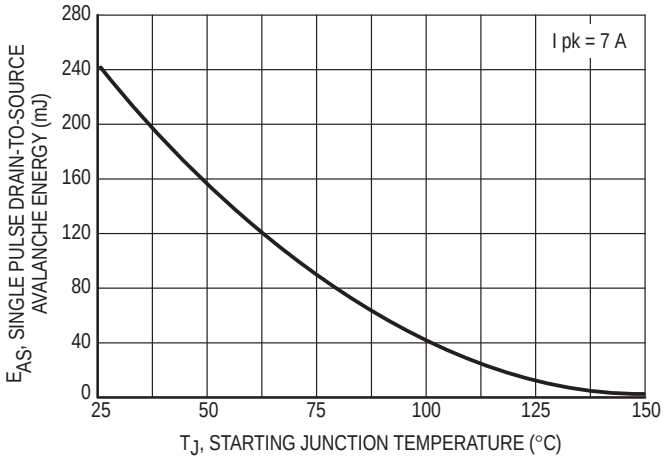


Figure 9. Maximum Avalanche Energy versus Starting Junction Temperature

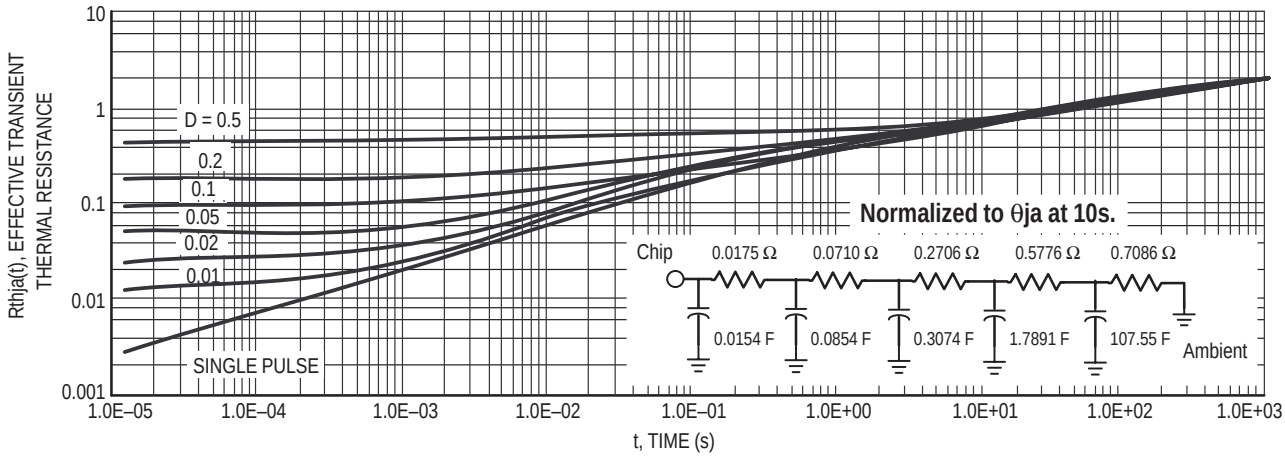


Figure 10. Thermal Response

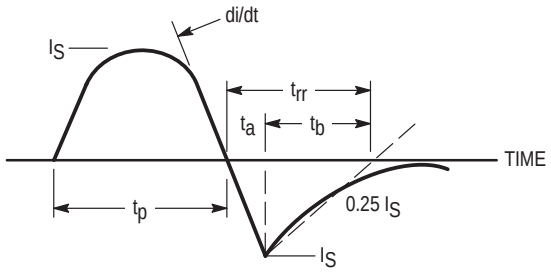


Figure 11. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

Complementary TMOS Field Effect Transistors

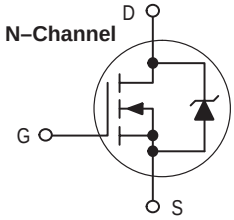
MMDF2C02HD

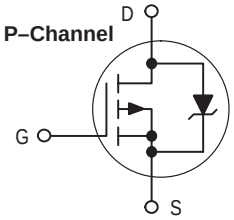
Motorola Preferred Device

COMPLEMENTARY DUAL TMOS POWER FET
2.0 AMPERES
20 VOLTS
$R_{DS(on)}$ = 0.090 OHM (N–CHANNEL)
$R_{DS(on)}$ = 0.160 OHM (P–CHANNEL)

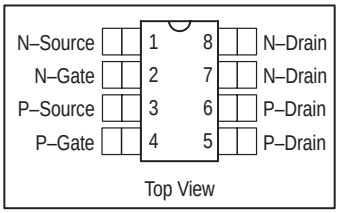
MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided





CASE 751–05, Style 14
SO–8



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating		Symbol	Value	Unit
Drain–to–Source Voltage		V_{DSS}	20	Vdc
Gate–to–Source Voltage		V_{GS}	± 20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 mΩ)		V_{DGR}	20	Vdc
Drain Current — Continuous	N–Channel	I_D	3.8	A
	P–Channel		3.3	
— Pulsed	N–Channel	I_{DM}	19	
	P–Channel		20	
Operating and Storage Temperature Range		T_J, T_{stg}	– 55 to 150	°C
Total Power Dissipation @ T_A= 25°C (2)		P_D	2.0	Watts
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C		E_{AS}		mJ
(V_{DD} = 20 V, V_{GS} = 5.0 V, Peak I_L = 9.0 A, L = 10 mH, R_G = 25 Ω)	N–Channel		405	
(V_{DD} = 20 V, V_{GS} = 5.0 V, Peak I_L = 6.0 A, L = 18 mH, R_G = 25 Ω)	P–Channel		324	
Thermal Resistance — Junction to Ambient (2)		$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering, 0.0625″ from case. Time in Solder Bath is 10 seconds.		T_L	260	°C

DEVICE MARKING

D2C02

(1) Negative signs for P–Channel device omitted for clarity.

(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF2C02HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Polarity	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	—	20	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	(N) (P)	— —	— —	1.0 1.0	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	—	100	nAdc
ON CHARACTERISTICS(2)							
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	—	1.0	1.5	2.0	Vdc
Drain–to–Source On–Resistance (V_{GS} = 4.5 Vdc, I_D = 1.5 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	(N) (P)	— —	0.074 0.152	0.100 0.180	Ohm
Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc) (V_{GS} = 10 Vdc, I_D = 2.0 Adc)		$R_{DS(on)}$	(N) (P)	— —	0.058 0.118	0.090 0.160	Ohm
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.5 Adc) (V_{DS} = 3.0 Vdc, I_D = 1.0 Adc)		g_{FS}	(N) (P)	2.0 2.0	3.88 3.0	— —	mhos
DYNAMIC CHARACTERISTICS							
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	(N) (P)	— —	455 420	630 588	pF
Output Capacitance		C_{oss}	(N) (P)	— —	184 290	250 406	
Transfer Capacitance		C_{rss}	(N) (P)	— —	45 116	90 232	
SWITCHING CHARACTERISTICS(3)							
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 3.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	(N) (P)	— —	11 19	22 38	ns
Rise Time		t_r	(N) (P)	— —	58 66	116 132	
Turn–Off Delay Time	(V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(off)}$	(N) (P)	— —	17 25	35 50	
Fall Time		t_f	(N) (P)	— —	20 37	40 74	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	(N) (P)	— —	7.0 11	21 22	
Rise Time		t_r	(N) (P)	— —	32 21	64 42	
Turn–Off Delay Time	(V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(off)}$	(N) (P)	— —	27 45	54 90	
Fall Time		t_f	(N) (P)	— —	21 36	42 72	
Total Gate Charge	(V_{DS} = 16 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc)	Q_T	(N) (P)	— —	12.5 15	18 20	nC
Gate–Source Charge		Q_1	(N) (P)	— —	1.3 1.2	— —	
Gate–Drain Charge	(V_{DS} = 16 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_2	(N) (P)	— —	2.8 5.0	— —	
		Q_3	(N) (P)	— —	2.4 4.0	— —	

(1) Negative signs for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(3) Switching characteristics are independent of operating junction temperature.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Polarity	Min	Typ	Max	Unit
SOURCE–DRAIN DIODE CHARACTERISTICS (T_C = 25°C)							
Forward Voltage(2)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	(N) (P)	— —	0.79 1.5	1.3 2.1	Vdc
Reverse Recovery Time	(I_S = 3.0 Adc, V_{AS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	(N) (P)	— —	23 38	— —	ns
		t_a	(N) (P)	— —	18 17	— —	
	(I_S = 2.0 Adc, V_{AS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_b	(N) (P)	— —	5.0 21	— —	
Reverse Recovery Stored Charge		Q_{RR}	(N) (P)	— —	0.025 0.034	— —	μC

(1) Negative signs for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

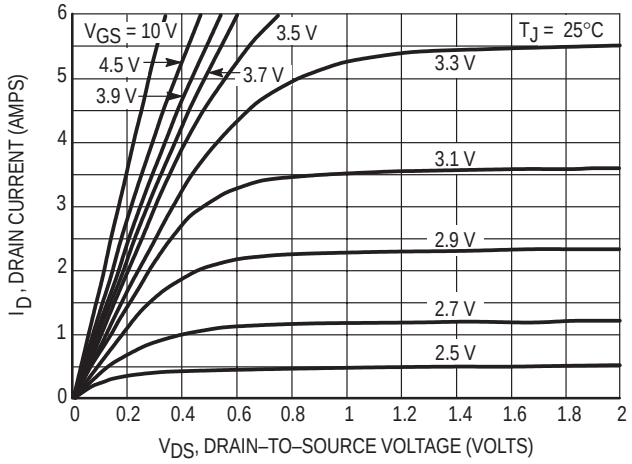


Figure 1. On–Region Characteristics

P–Channel

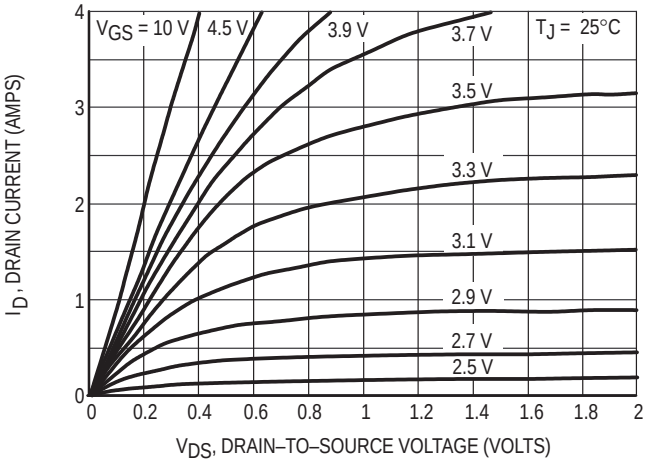


Figure 1. On–Region Characteristics

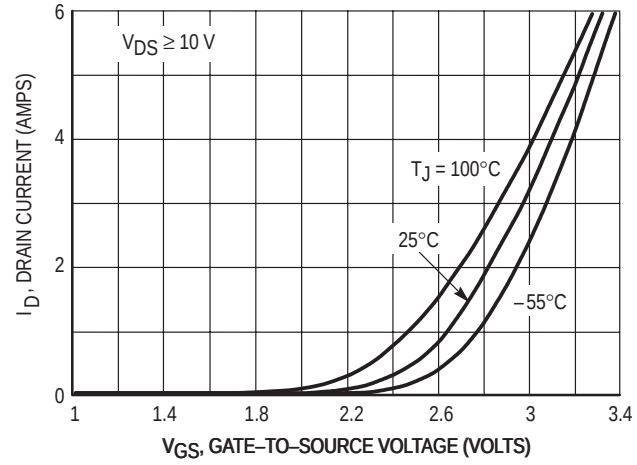


Figure 2. Transfer Characteristics

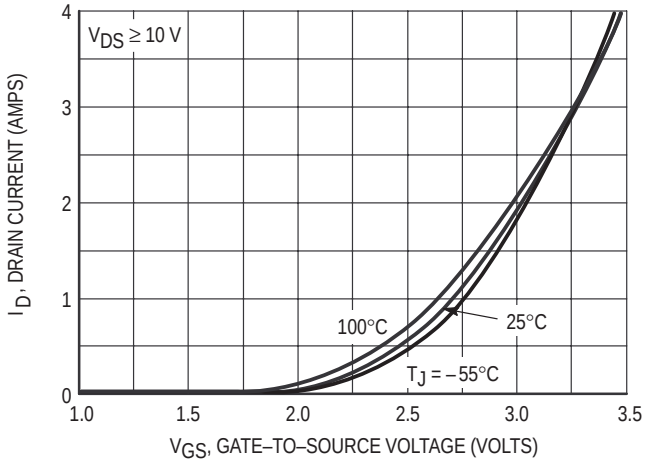


Figure 2. Transfer Characteristics

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

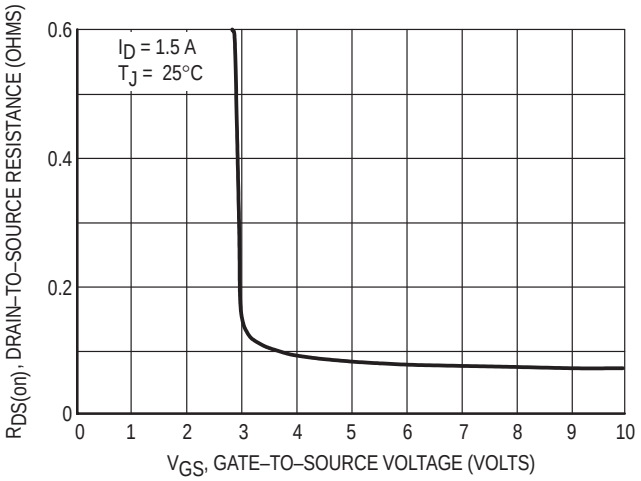


Figure 3. On–Resistance versus Gate–To–Source Voltage

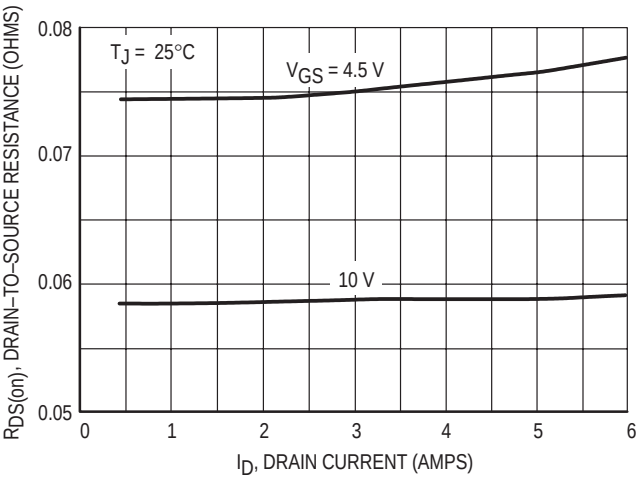


Figure 4. On–Resistance versus Drain Current and Gate Voltage

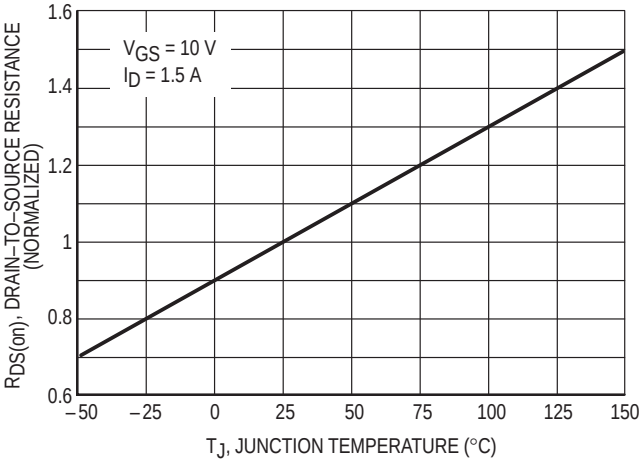


Figure 5. On–Resistance Variation with Temperature

P–Channel

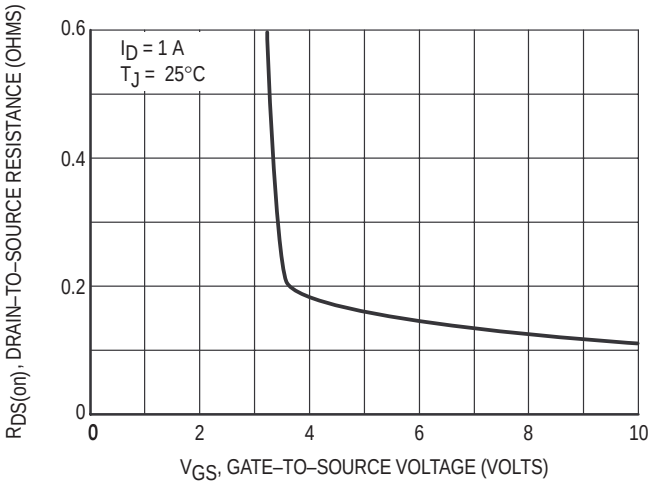


Figure 3. On–Resistance versus Gate–To–Source Voltage

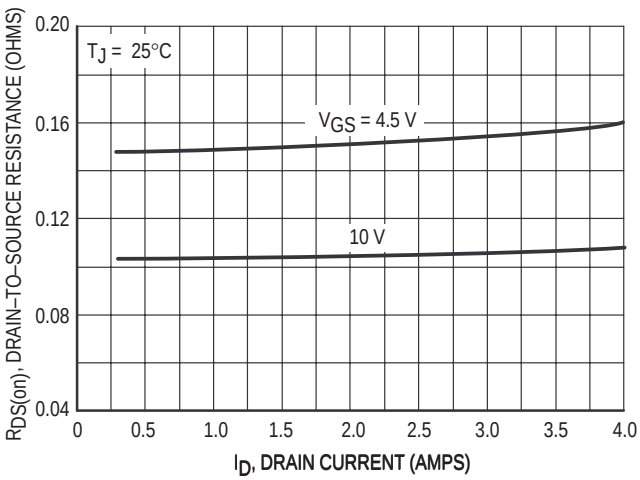


Figure 4. On–Resistance versus Drain Current and Gate Voltage

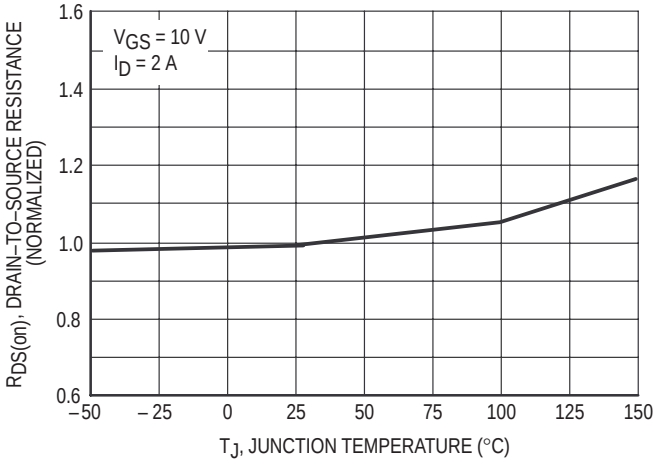


Figure 5. On–Resistance Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

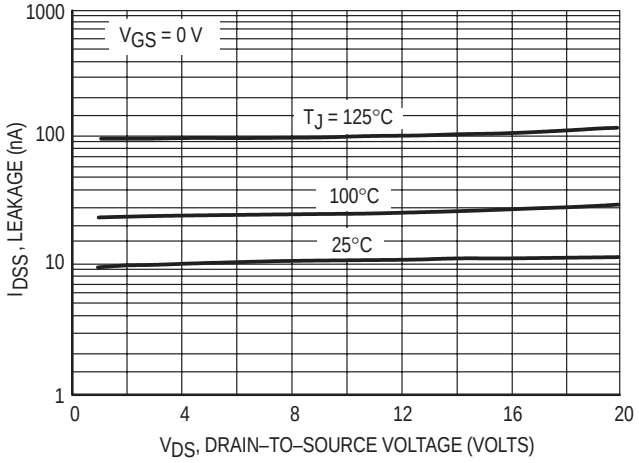


Figure 6. Drain–To–Source Leakage Current versus Voltage

P–Channel

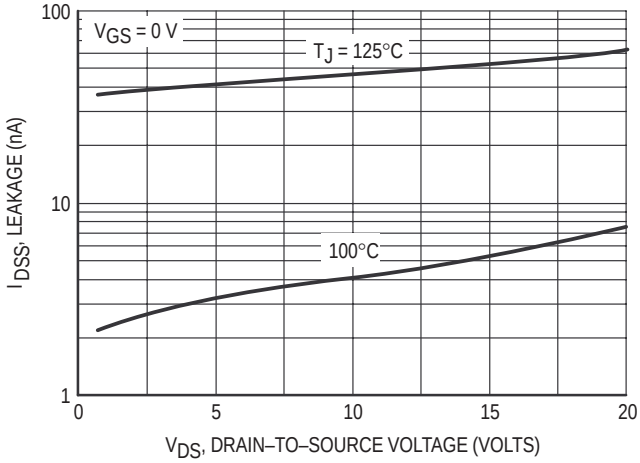


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

N–Channel

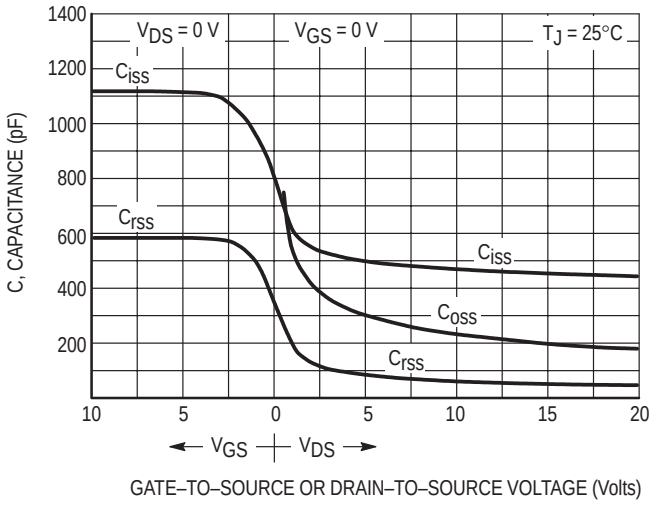


Figure 7. Capacitance Variation

P–Channel

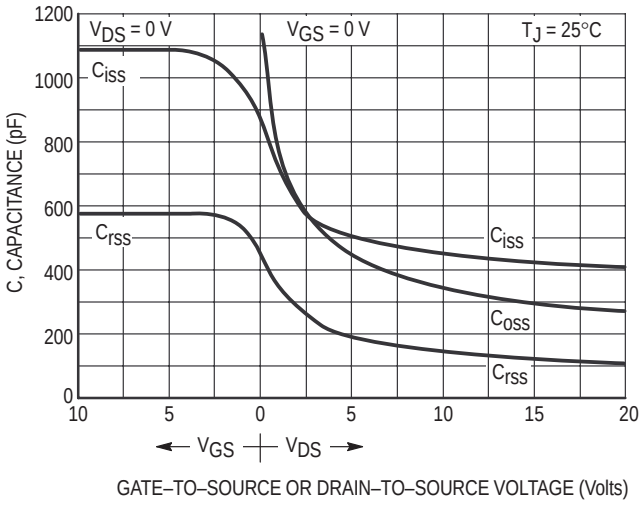


Figure 7. Capacitance Variation

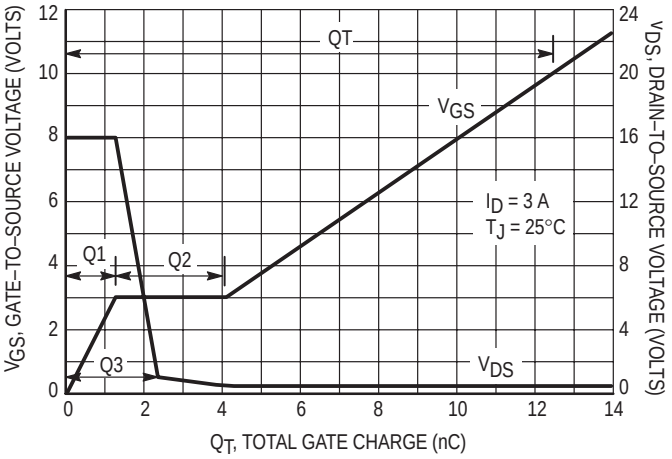


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

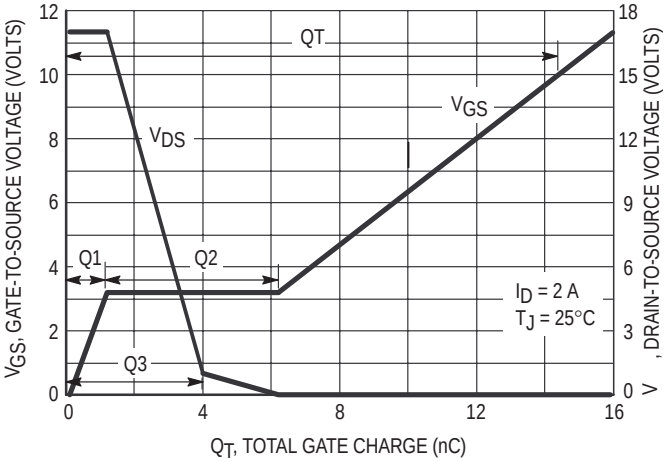


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

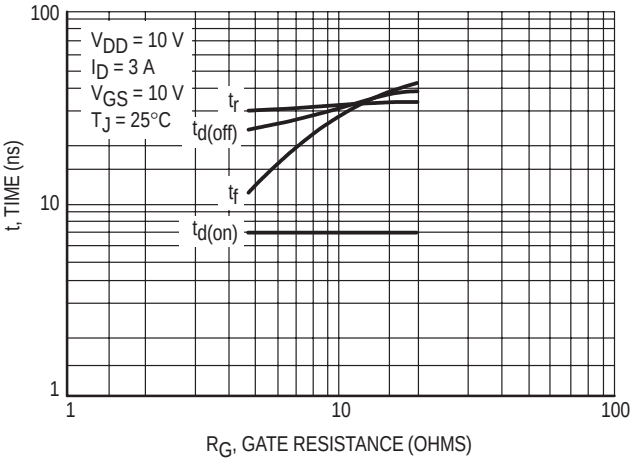


Figure 9. Resistive Switching Time Variation versus Gate Resistance

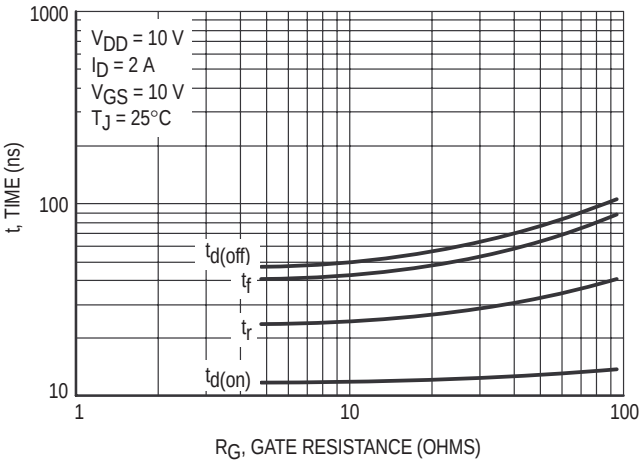


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

N–Channel

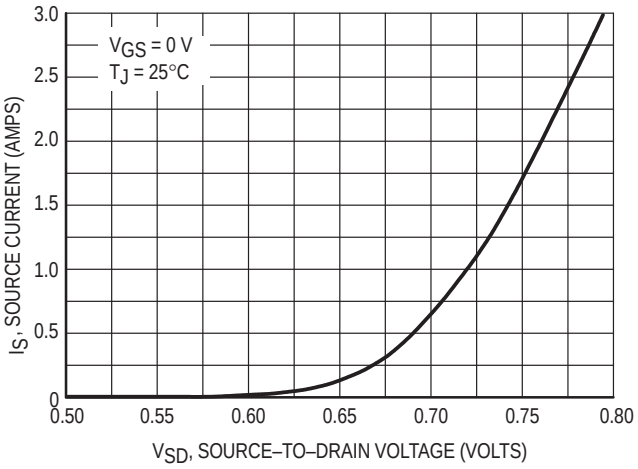


Figure 10. Diode Forward Voltage versus Current

P–Channel

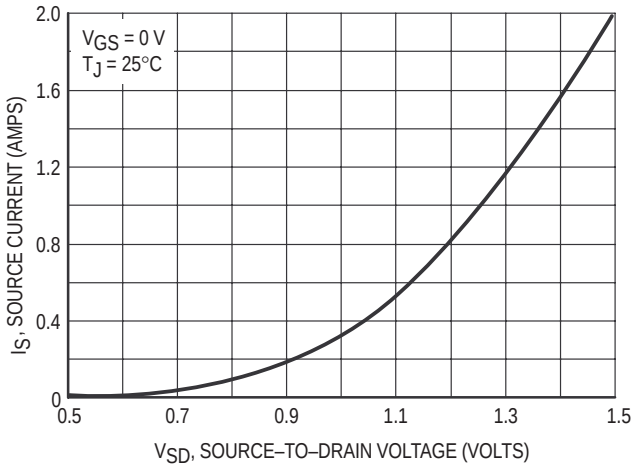


Figure 10. Diode Forward Voltage versus Current

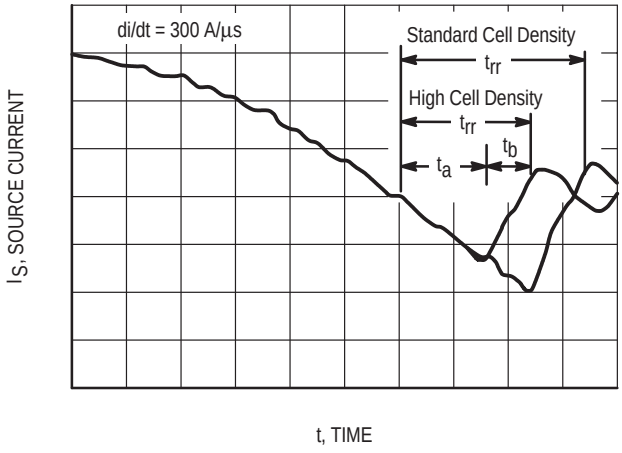


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

N–Channel

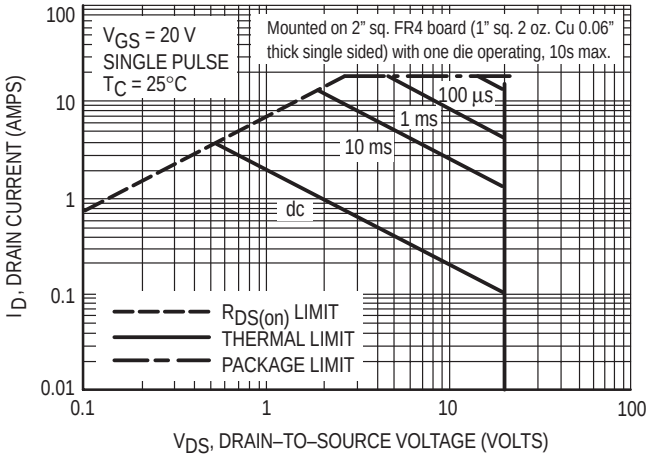


Figure 12. Maximum Rated Forward Biased Safe Operating Area

P–Channel

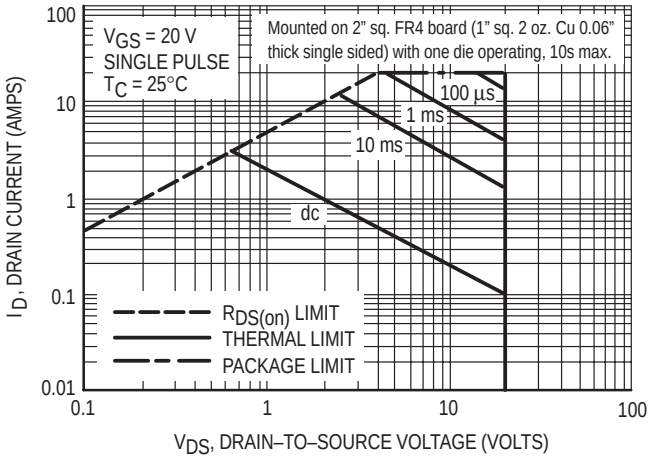


Figure 12. Maximum Rated Forward Biased Safe Operating Area

N–Channel

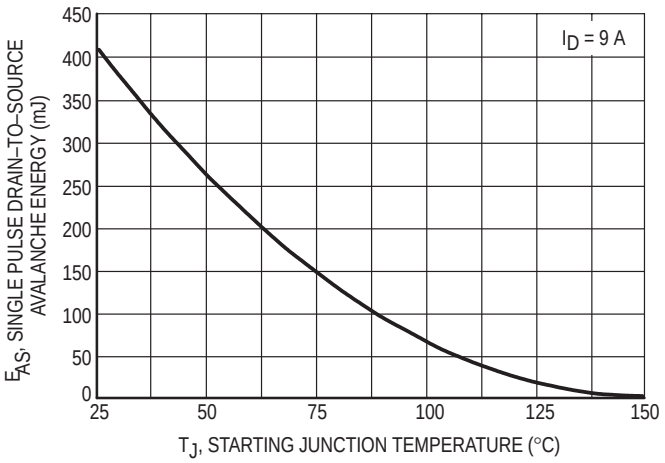


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

P–Channel

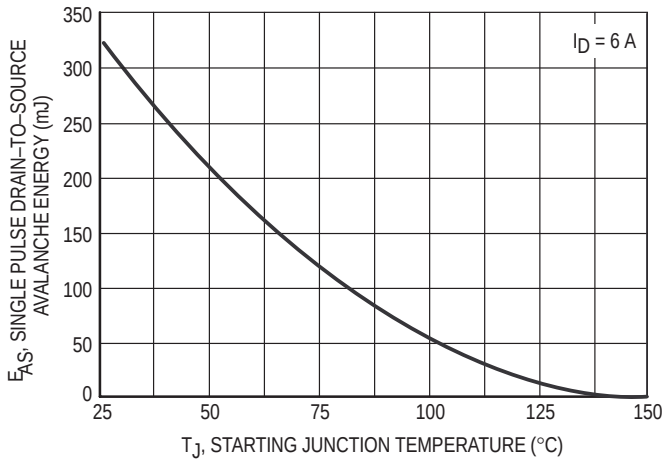


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

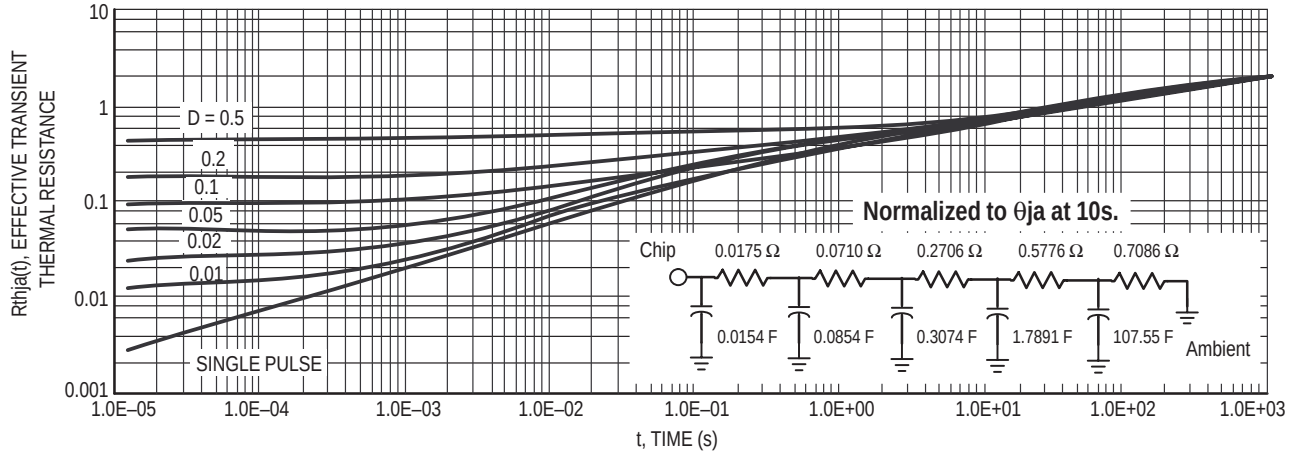


Figure 14. Thermal Response

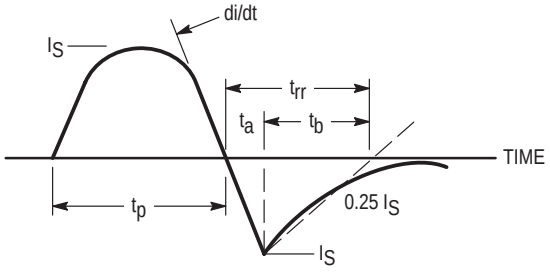


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

Complementary TMOS Field Effect Transistors

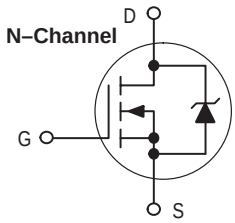
MMDF2C03HD

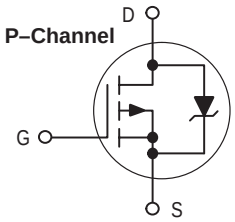
Motorola Preferred Device

COMPLEMENTARY DUAL TMOS POWER FET
2.0 AMPERES
30 VOLTS
$R_{DS(on)}$ = 0.070 OHM (N-CHANNEL)
$R_{DS(on)}$ = 0.200 OHM (P-CHANNEL)

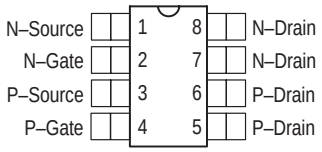
MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain-to-source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc-dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO-8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO-8 Package Provided





CASE 751–05, Style 14
SO–8



Top View

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating		Symbol	Value	Unit
Drain–to–Source Voltage		V_{DSS}	30	Vdc
Gate–to–Source Voltage		V_{GS}	± 20	Vdc
Drain Current — Continuous	N–Channel	I_D	4.1	A
	P–Channel		3.0	
— Pulsed	N–Channel	I_{DM}	21	
	P–Channel		15	
Operating and Storage Temperature Range		T_J, T_{stg}	– 55 to 150	°C
Total Power Dissipation @ T_A= 25°C (2)		P_D	2.0	Watts
Thermal Resistance — Junction to Ambient (2)		$R_{\theta JA}$	62.5	°C/W
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C		E_{AS}		mJ
(V_{DD} = 30 V, V_{GS} = 5.0 V, Peak I_L = 9.0 Apk, L = 8.0 mH, R_G = 25 Ω)	N–Channel		324	
(V_{DD} = 30 V, V_{GS} = 5.0 V, Peak I_L = 6.0 Apk, L = 18 mH, R_G = 25 Ω)	P–Channel		324	
Maximum Lead Temperature for Soldering, 0.0625″ from case. Time in Solder Bath is 10 seconds.		T_L	260	°C

DEVICE MARKING

D2C03

(1) Negative signs for P–Channel device omitted for clarity.

(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF2C03HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Polarity	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 µAdc)		$V_{(BR)DSS}$	—	30	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	(N) (P)	— —	— —	1.0 1.0	µAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	—	100	nAdc
ON CHARACTERISTICS(2)							
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 µAdc)		$V_{GS(th)}$	(N) (P)	1.0 1.0	1.7 1.5	3.0 2.0	Vdc
Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc) (V_{GS} = 10 Vdc, I_D = 2.0 Adc)		$R_{DS(on)}$	(N) (P)	— —	0.06 0.17	0.070 0.200	Ohm
Drain–to–Source On–Resistance (V_{GS} = 4.5 Vdc, I_D = 1.5 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	(N) (P)	— —	0.065 0.225	0.075 0.300	Ohm
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.5 Adc) (V_{DS} = 3.0 Vdc, I_D = 1.0 Adc)		g_{FS}	(N) (P)	2.0 2.0	3.6 3.4	— —	mhos
DYNAMIC CHARACTERISTICS							
Input Capacitance	(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	(N) (P)	— —	450 397	630 550	pF
Output Capacitance		C_{oss}	(N) (P)	— —	160 189	225 250	
Transfer Capacitance		C_{rss}	(N) (P)	— —	35 64	70 126	
SWITCHING CHARACTERISTICS(3)							
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 3.0 Adc, V_{GS} = 4.5 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	(N) (P)	— —	12 16	24 32	ns
Rise Time		t_r	(N) (P)	— —	65 18	130 36	
Turn–Off Delay Time	(V_{DD} = 15 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(off)}$	(N) (P)	— —	16 63	32 126	
Fall Time		t_f	(N) (P)	— —	19 194	38 390	
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	(N) (P)	— —	8.0 9.0	16 18	
Rise Time		t_r	(N) (P)	— —	15 10	30 20	
Turn–Off Delay Time	(V_{DD} = 15 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(off)}$	(N) (P)	— —	30 81	60 162	
Fall Time		t_f	(N) (P)	— —	23 192	46 384	
Total Gate Charge	(V_{DS} = 10 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc) (V_{DS} = 24 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	(N) (P)	— —	11.5 14.2	16 19	nC
Gate–Source Charge		Q_1	(N) (P)	— —	1.5 1.1	— —	
Gate–Drain Charge		Q_2	(N) (P)	— —	3.5 4.5	— —	
		Q_3	(N) (P)	— —	2.8 3.5	— —	

(1) Negative signs for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
(3) Switching characteristics are independent of operating junction temperature.

(continued)

ELECTRICAL CHARACTERISTICS — continued (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Polarity	Min	Typ	Max	Unit
SOURCE–DRAIN DIODE CHARACTERISTICS (T_C = 25°C)							
Forward Voltage(2)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	(N) (P)	— —	0.82 1.82	1.2 2.0	Vdc
Reverse Recovery Time	(I_F = I_S, dI_S/dt = 100 A/μs)	t_{rr}	(N) (P)	— —	24 42	— —	ns
		t_a	(N) (P)	— —	17 16	— —	
		t_b	(N) (P)	— —	7.0 26	— —	
Reverse Recovery Storage Charge		Q_{RR}	(N) (P)	— —	0.025 0.043	— —	μC

(1) Negative signs for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

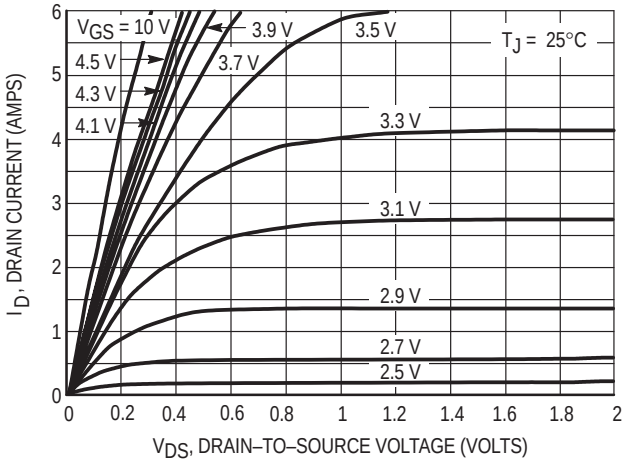


Figure 1. On–Region Characteristics

P–Channel

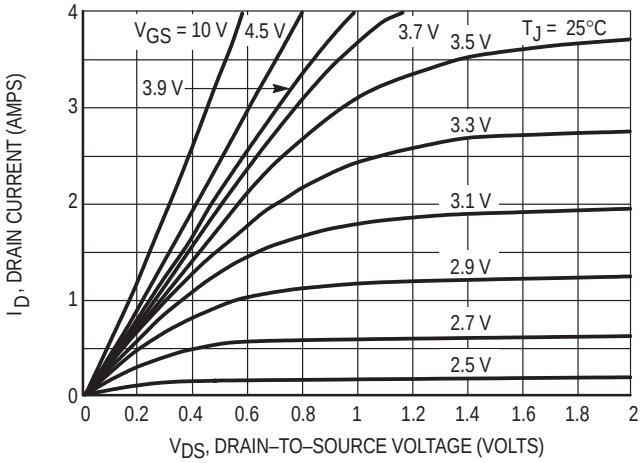


Figure 1. On–Region Characteristics

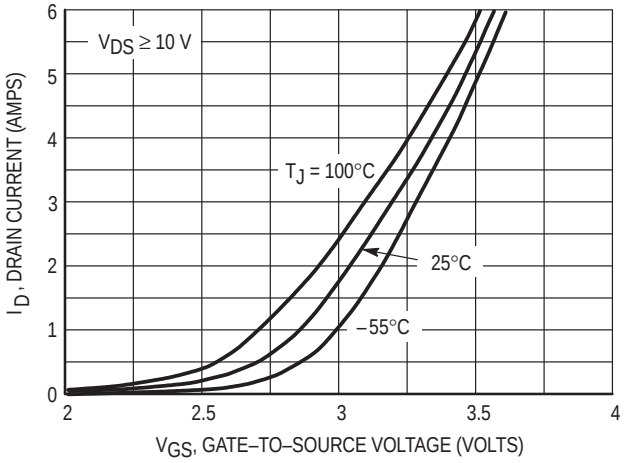


Figure 2. Transfer Characteristics

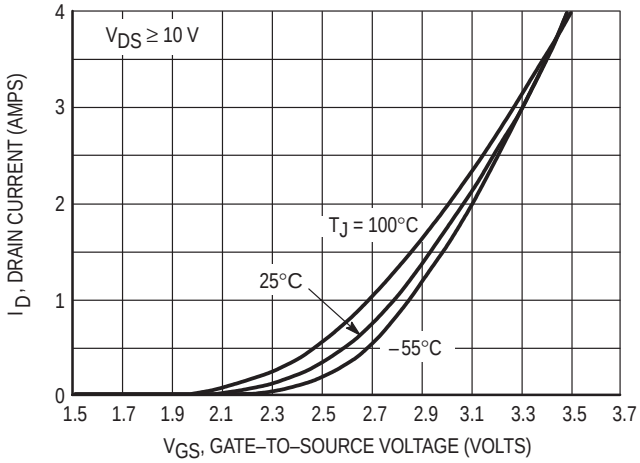


Figure 2. Transfer Characteristics

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

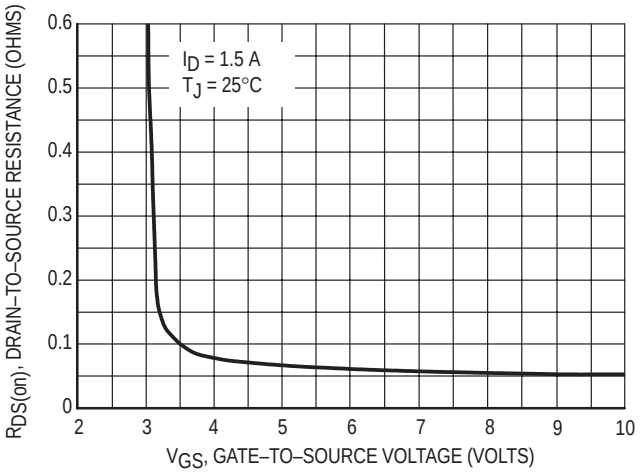


Figure 3. On–Resistance versus Gate–To–Source Voltage

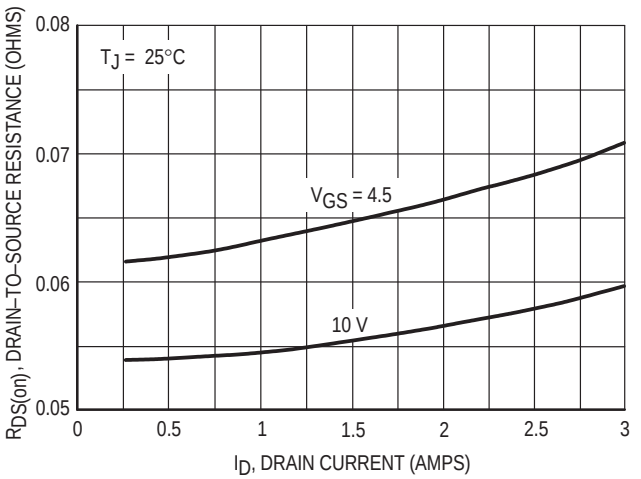


Figure 4. On–Resistance versus Drain Current and Gate Voltage

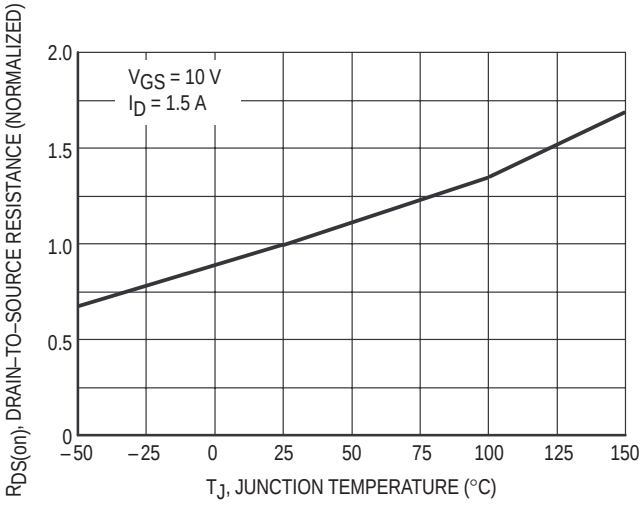


Figure 5. On–Resistance Variation with Temperature

P–Channel

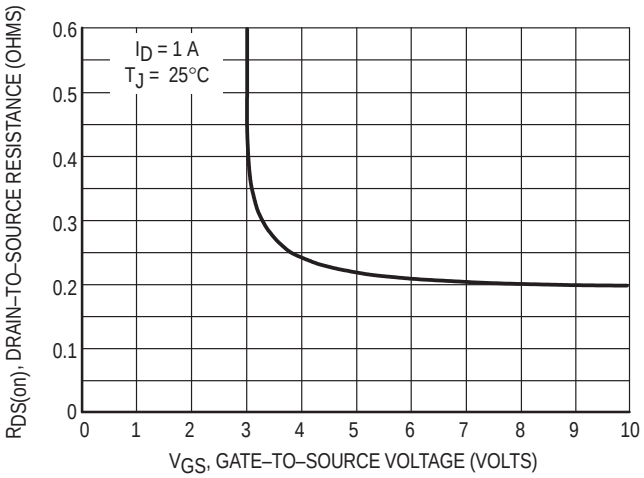


Figure 3. On–Resistance versus Gate–To–Source Voltage

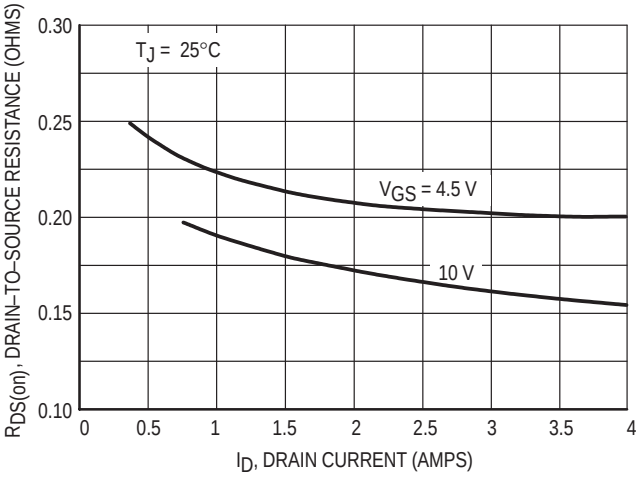


Figure 4. On–Resistance versus Drain Current and Gate Voltage

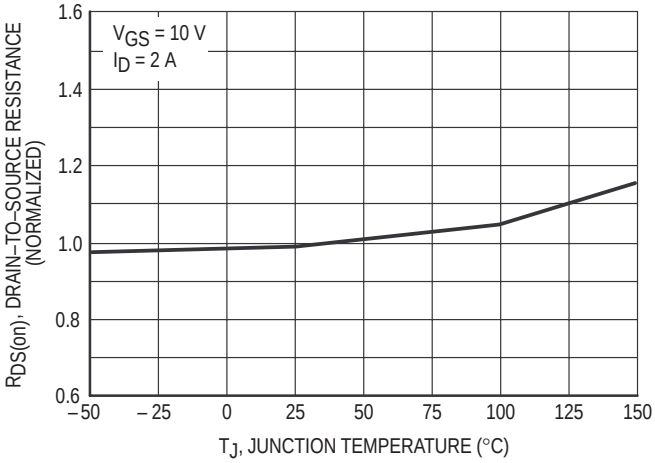


Figure 5. On–Resistance Variation with Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

N–Channel

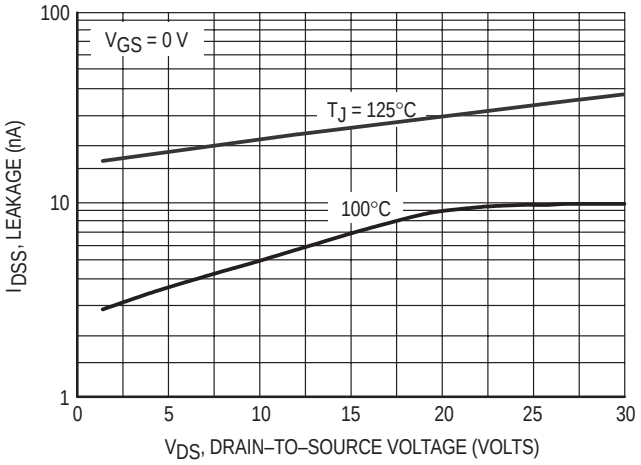


Figure 6. Drain–To–Source Leakage Current versus Voltage

P–Channel

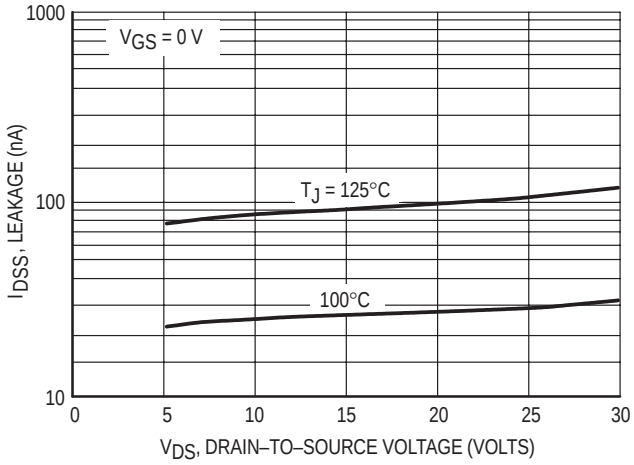


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

N–Channel

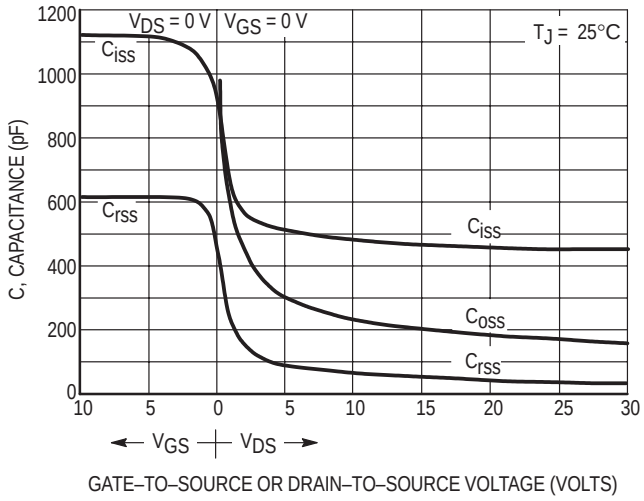


Figure 7. Capacitance Variation

P–Channel

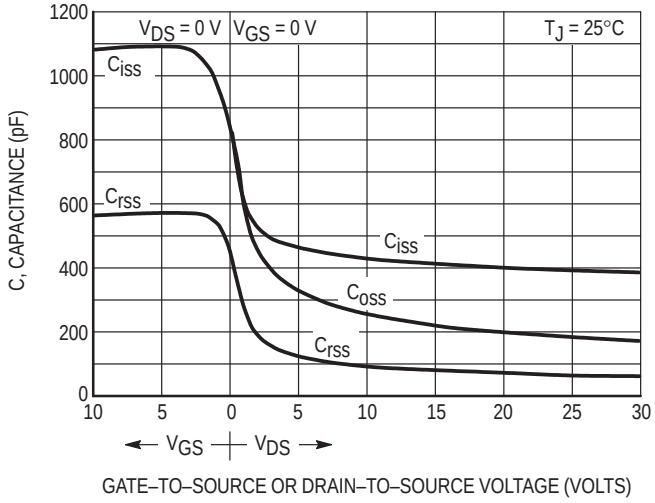


Figure 7. Capacitance Variation

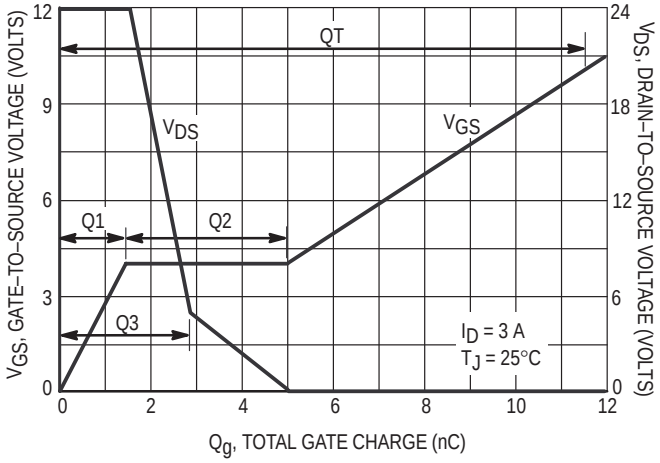


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

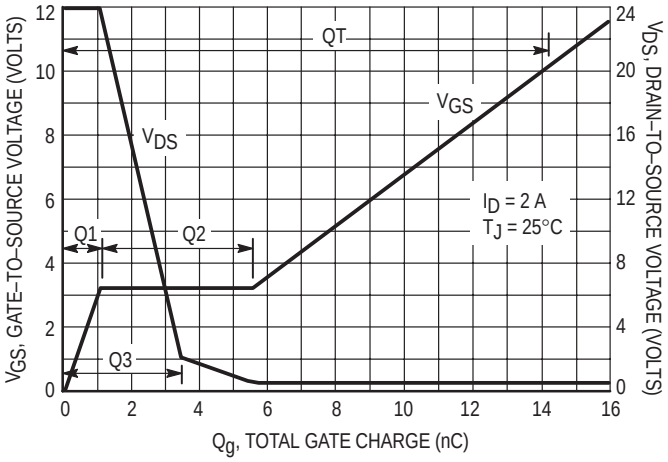


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

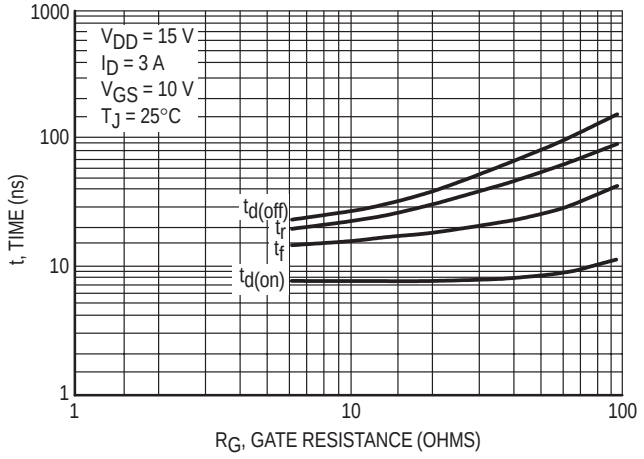


Figure 9. Resistive Switching Time Variation versus Gate Resistance

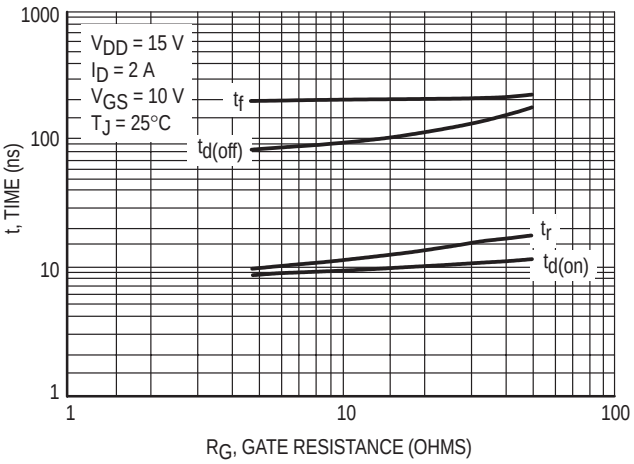


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

N–Channel

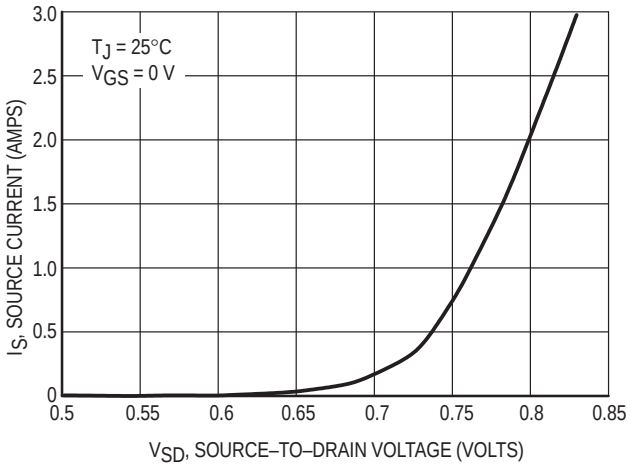


Figure 10. Diode Forward Voltage versus Current

P–Channel

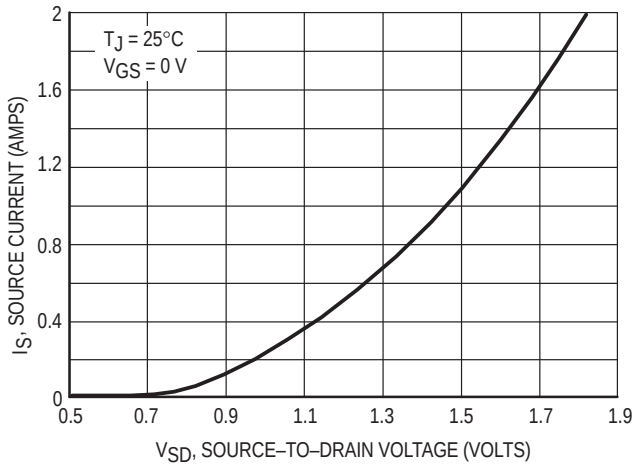


Figure 10. Diode Forward Voltage versus Current

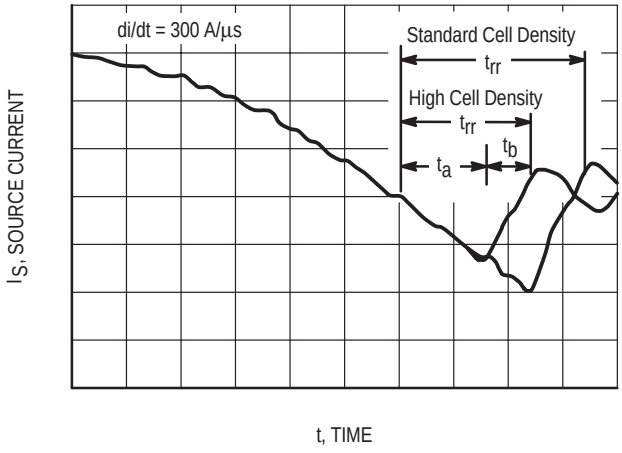


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

N–Channel

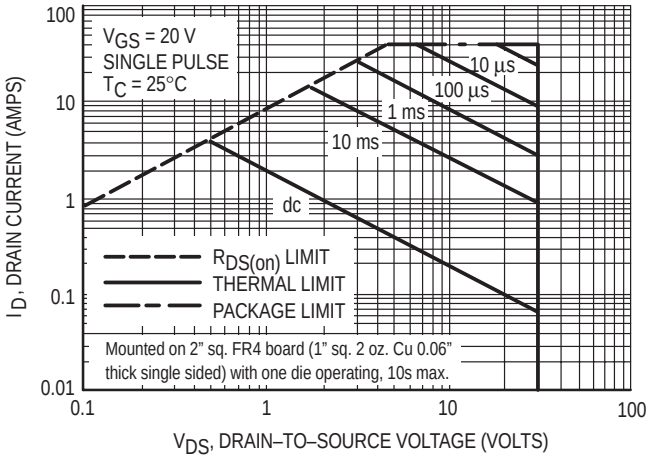


Figure 12. Maximum Rated Forward Biased Safe Operating Area

P–Channel

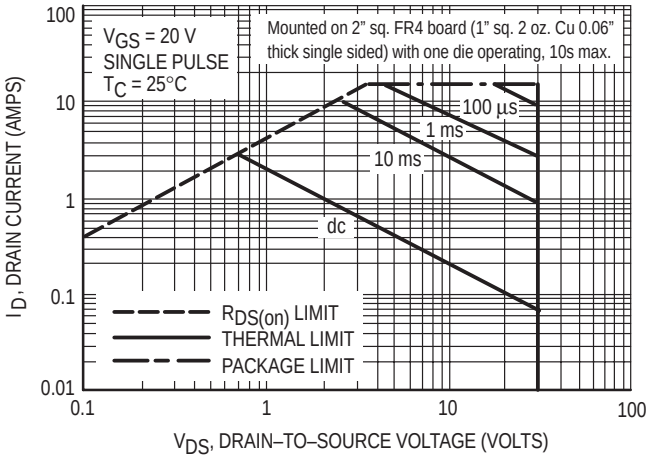


Figure 12. Maximum Rated Forward Biased Safe Operating Area

N–Channel

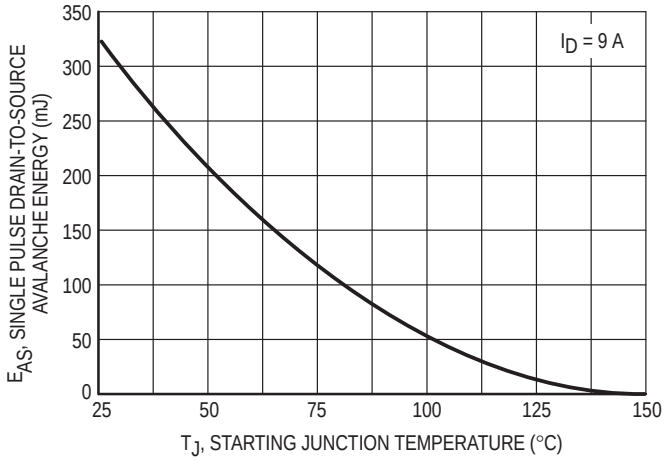


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

P–Channel

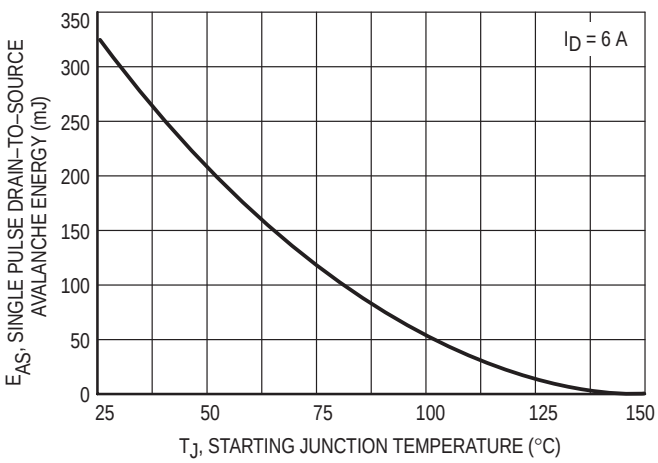


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

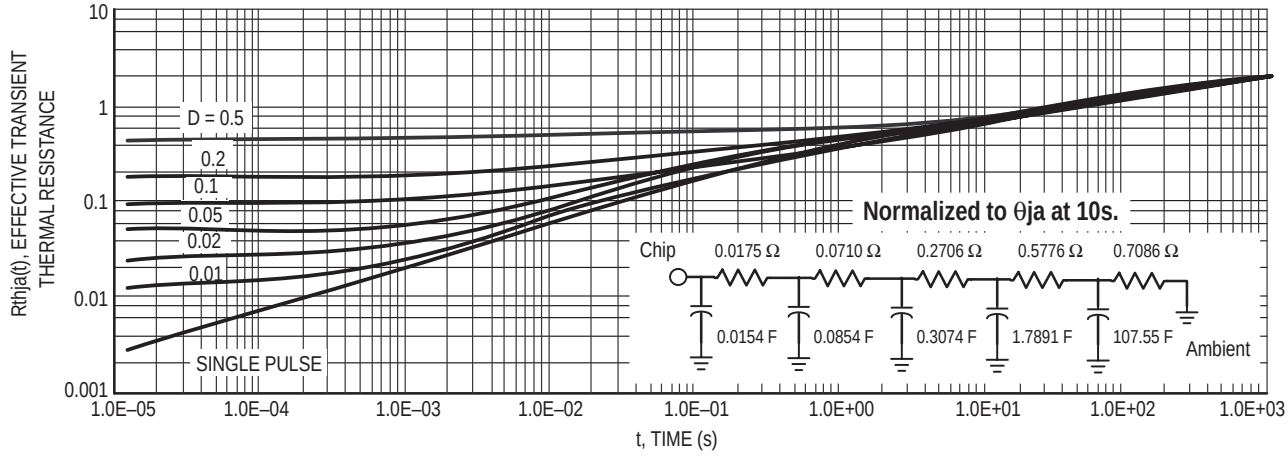


Figure 14. Thermal Response

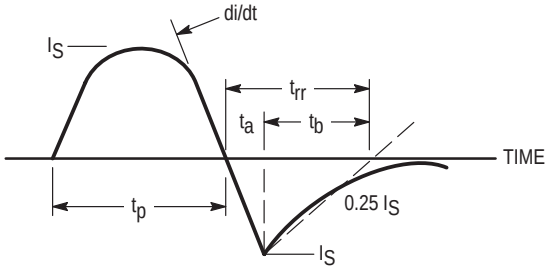


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

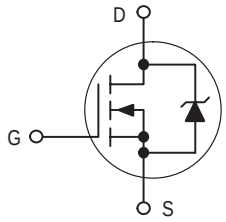
Medium Power Surface Mount Products

TMOS Dual N-Channel Field Effect Transistors

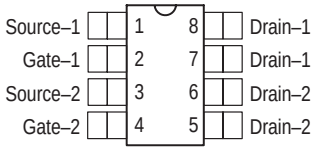
MMDF2N02E

DUAL TMOS MOSFET
3.6 AMPERES
25 VOLTS
$R_{DS(on)}$ = 0.1 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's TMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.



CASE 751–05, Style 11
SO–8



Top View

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- I_{DSS} Specified at Elevated Temperatures
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	25	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	3.6 2.5 18	Adc Apk
Total Power Dissipation @ T_A = 25°C (1)	P_D	2.0	W
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 10 Vdc, Peak I_L = 9.0 Apk, L = 6.0 mH, R_G = 25 Ω)	E_{AS}	245	mJ
Thermal Resistance, Junction to Ambient (1)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 0.0625″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

F2N02

(1) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF2N02ER2	13″	12 mm embossed tape	2500

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	25	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc		$V_{GS(th)}$	1.0	2.0	3.0	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.2 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	— —	0.083 0.110	0.100 0.200	Ohm
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.0 Adc)		g_{FS}	1.0	2.6	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	380	532	pF
Output Capacitance		C_{oss}	—	235	329	
Transfer Capacitance		C_{rss}	—	55	110	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	7.0	21	ns
Rise Time		t_r	—	17	30	
Turn–Off Delay Time		$t_{d(off)}$	—	27	48	
Fall Time		t_f	—	18	30	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	10	30	
Rise Time		t_r	—	35	70	
Turn–Off Delay Time		$t_{d(off)}$	—	19	38	
Fall Time		t_f	—	25	50	
Gate Charge	(V_{DS} = 16 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	10.6	30	nC
		Q_1	—	1.3	—	
		Q_2	—	2.9	—	
		Q_3	—	2.7	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.4	Vdc
Reverse Recovery Time See Figure 11	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	34	66	ns
		t_a	—	17	—	
		t_b	—	17	—	
Reverse Recovery Storage Charge		Q_{RR}	—	0.03	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

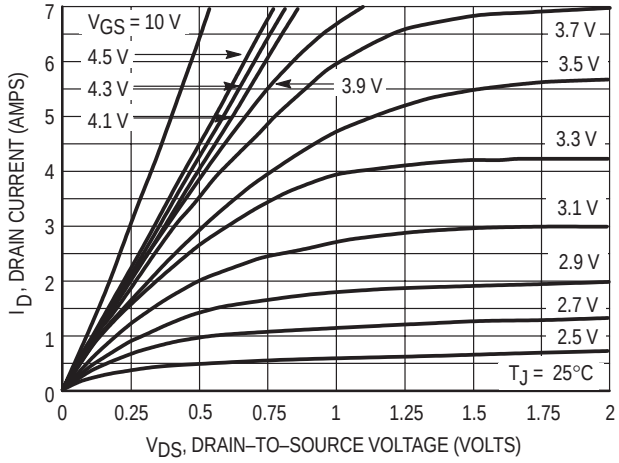


Figure 1. On–Region Characteristics

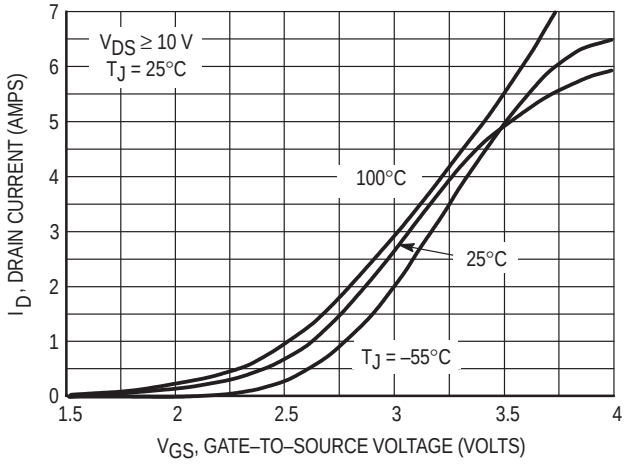


Figure 2. Transfer Characteristics

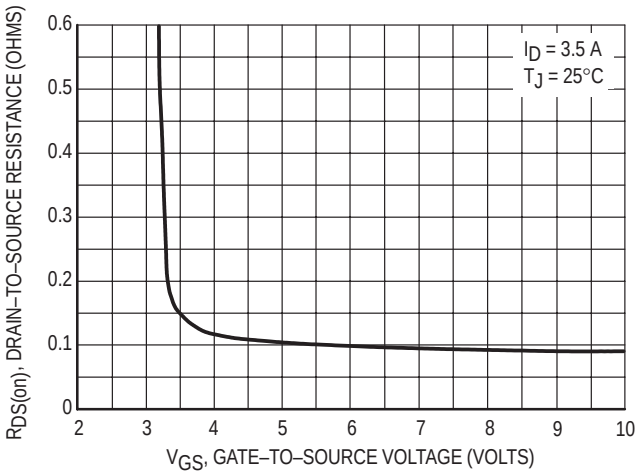


Figure 3. On–Resistance versus Gate–to–Source Voltage

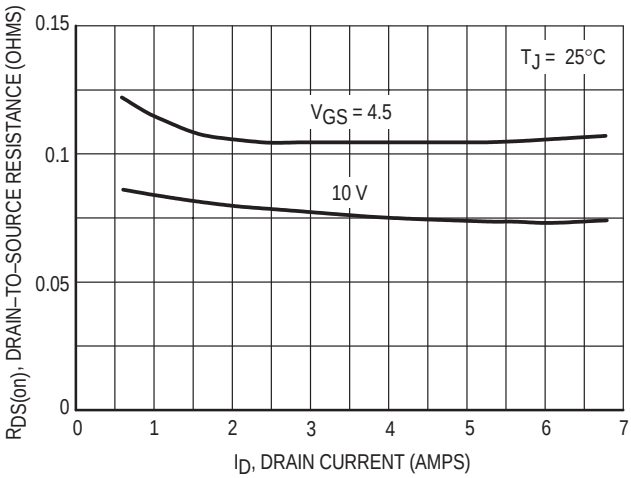


Figure 4. On–Resistance versus Drain Current and Gate Voltage

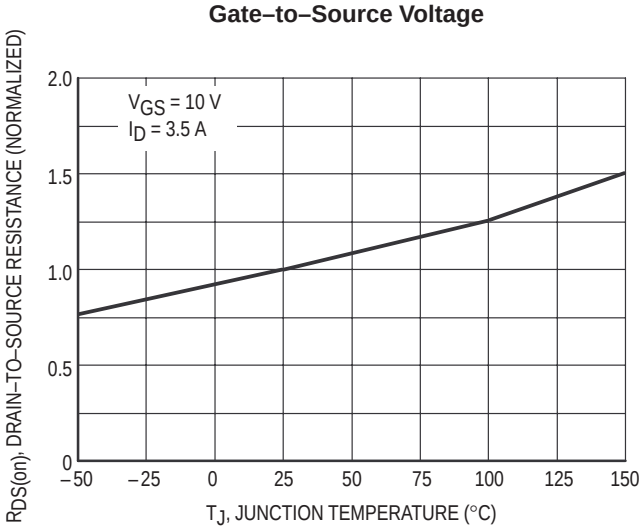


Figure 5. On–Resistance Variation with Temperature

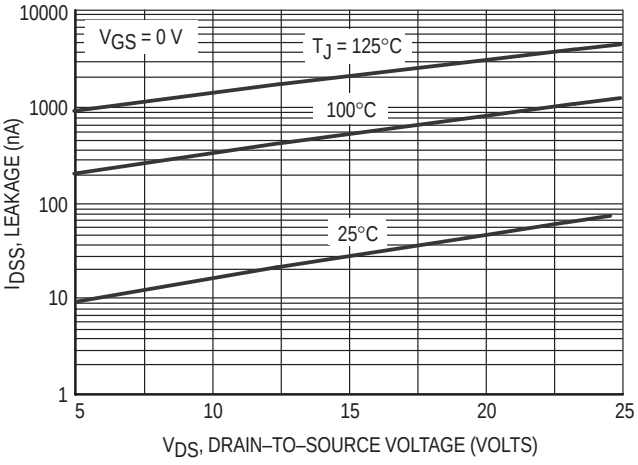


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

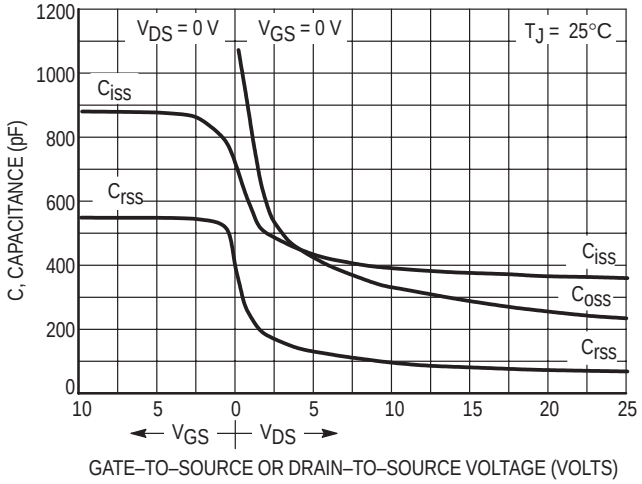


Figure 7. Capacitance Variation

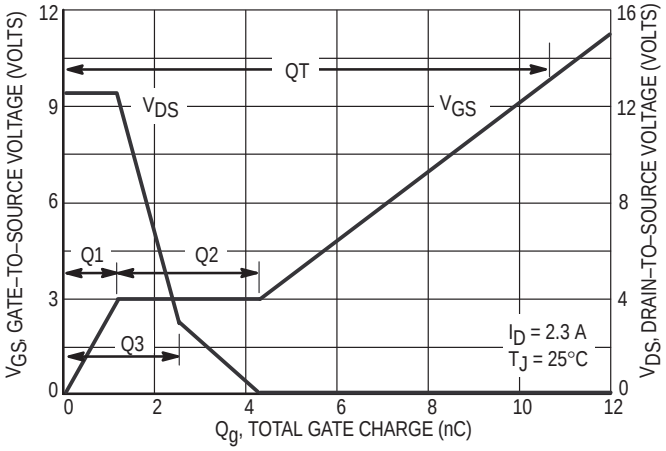


Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

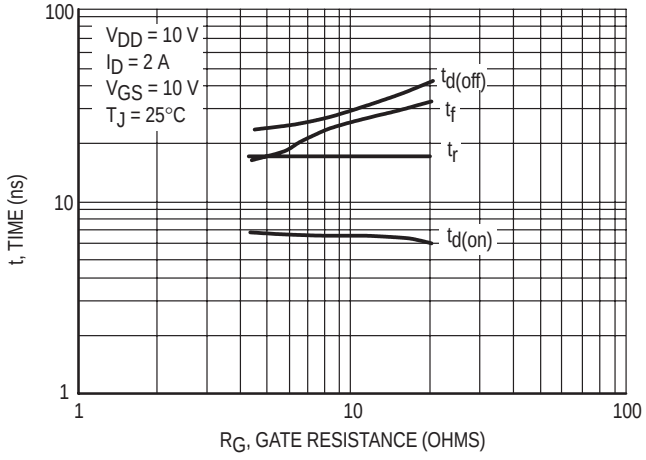


Figure 9. Resistive Switching Time Variation versus Gate Resistance

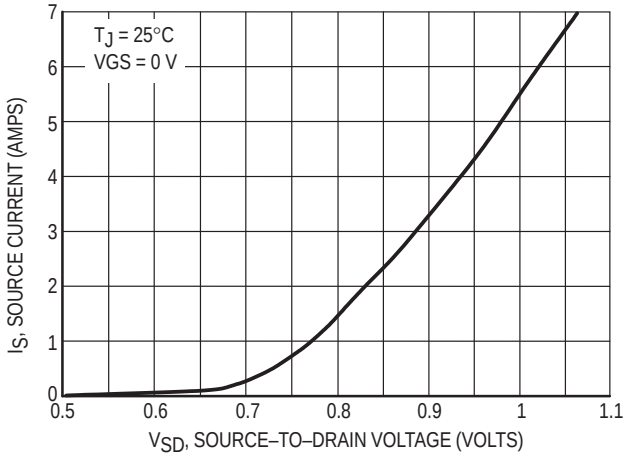


Figure 10. Diode Forward Voltage versus Current

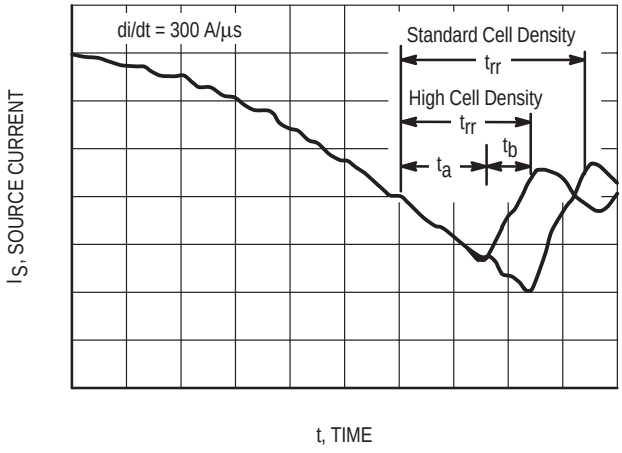


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

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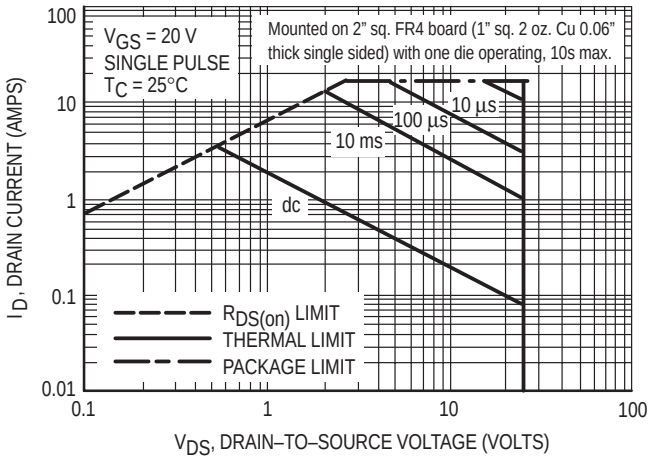

Figure 12. Maximum Rated Forward Biased Safe Operating Area

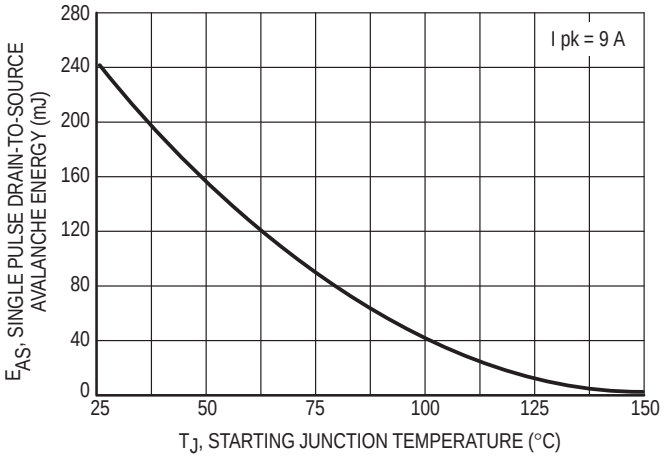

Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

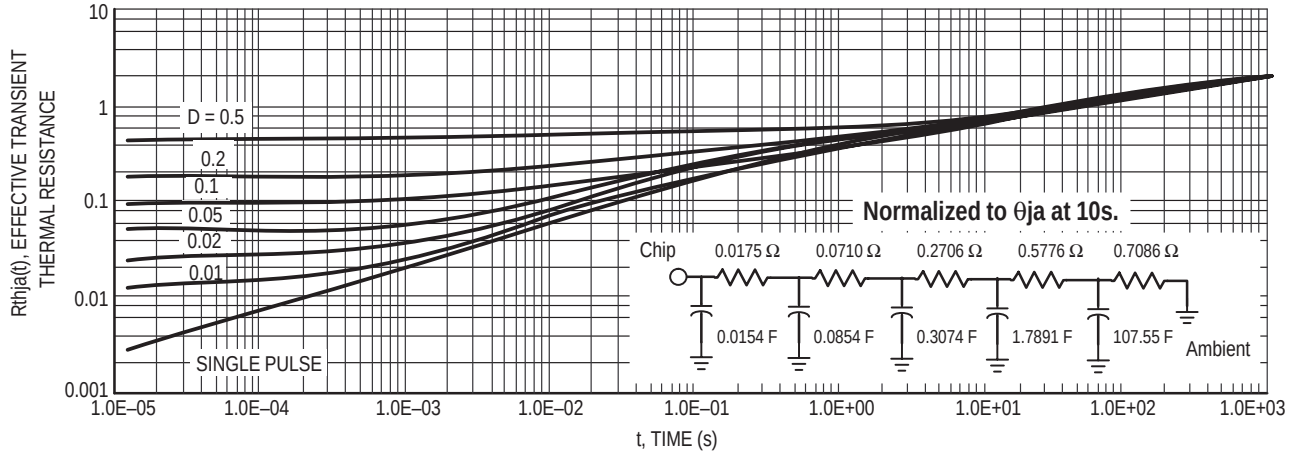

Figure 14. Thermal Response

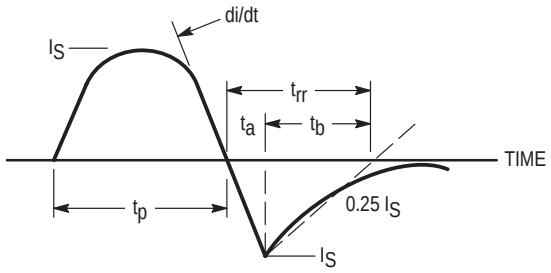

Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

TMOS P-Channel Field Effect Transistors

MMDF2P01HD

Motorola Preferred Device

DUAL TMOS POWER FET
2.0 AMPERES
12 VOLTS
$R_{DS(on)}$ = 0.18 OHM

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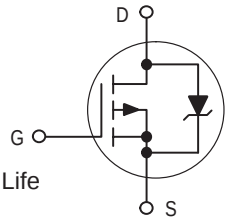
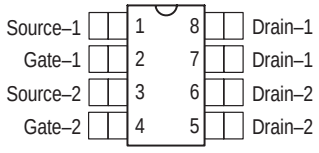


CASE 751–05, Style 11
SO–8



Top View

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	12	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	12	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 8.0	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	3.4 2.1 17	Adc Apk
Total Power Dissipation @ T_A = 25°C (2)	P_D	2.0	Watts
Operating and Storage Temperature Range		– 55 to 150	°C
Thermal Resistance — Junction to Ambient (2)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

D2P01

(1) Negative sign for P–Channel device omitted for clarity.
(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF2P01HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	12	—	—	Vdc
Temperature Coefficient (Positive)			—	17	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 12 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	1.0	μAdc
(V_{DS} = 12 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	10	
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	0.7	1.0	1.1	Vdc
Temperature Coefficient (Negative)			—	3.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 4.5 Vdc, I_D = 2.0 Adc)		$R_{DS(on)}$	—	0.16	0.180	Ohm
(VGS = 2.7 Vdc, I_D = 1.0 Adc)			—	0.2	0.220	
Forward Transconductance (V_{DS} = 2.5 Vdc, I_D = 1.0 Adc)		g_{FS}	3.0	4.75	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 10 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	530	740	pF
Output Capacitance		C_{oss}	—	410	570	
Reverse Transfer Capacitance		C_{rss}	—	177	250	
SWITCHING CHARACTERISTICS(3)						
Turn–On Delay Time	(V_{DD} = 6.0 Vdc, I_D = 2.0 Adc, V_{GS} = 2.7 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	21	45	ns
Rise Time		t_r	—	156	315	
Turn–Off Delay Time		$t_{d(off)}$	—	38	75	
Fall Time		t_f	—	68	135	
Turn–On Delay Time	(V_{DS} = 6.0 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	16	35	
Rise Time		t_r	—	44	90	
Turn–Off Delay Time		$t_{d(off)}$	—	68	135	
Fall Time		t_f	—	54	110	
Gate Charge	(V_{DS} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc)	Q_T	—	9.3	13	nC
		Q_1	—	0.8	—	
		Q_2	—	4.0	—	
		Q_3	—	3.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(2)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.69	2.0	Vdc
	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.2	—	
Reverse Recovery Time	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	48	—	ns
		t_a	—	23	—	
		t_b	—	25	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.05	—	μC

(1) Negative sign for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(3) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

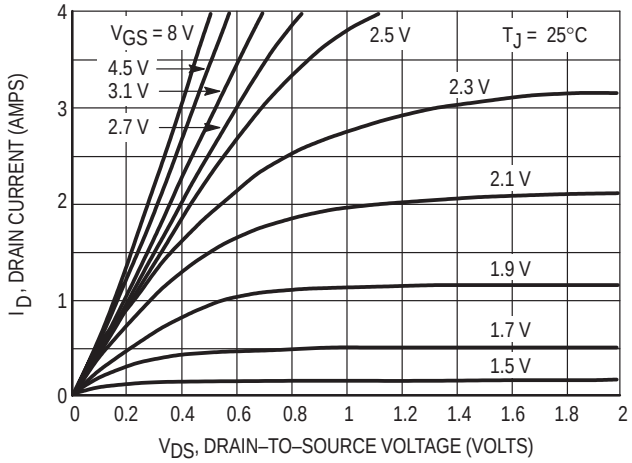


Figure 1. On–Region Characteristics

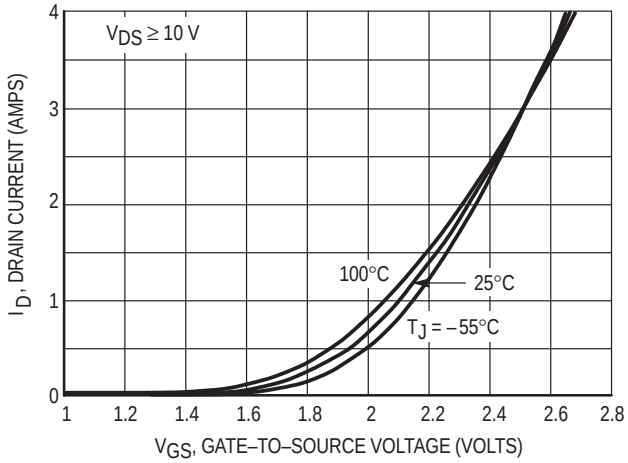


Figure 2. Transfer Characteristics

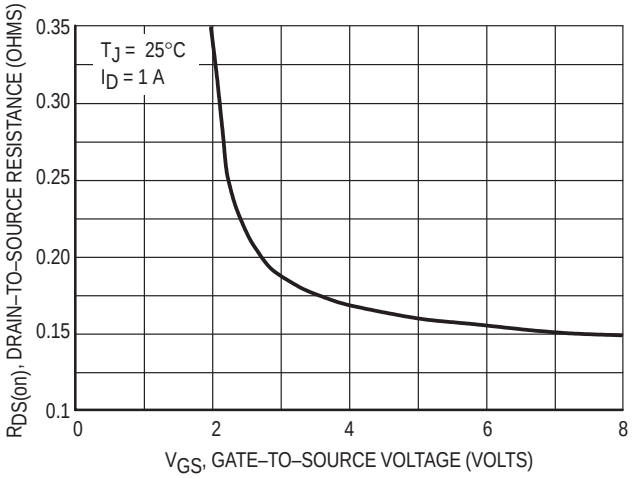


Figure 3. On–Resistance versus Gate–To–Source Voltage

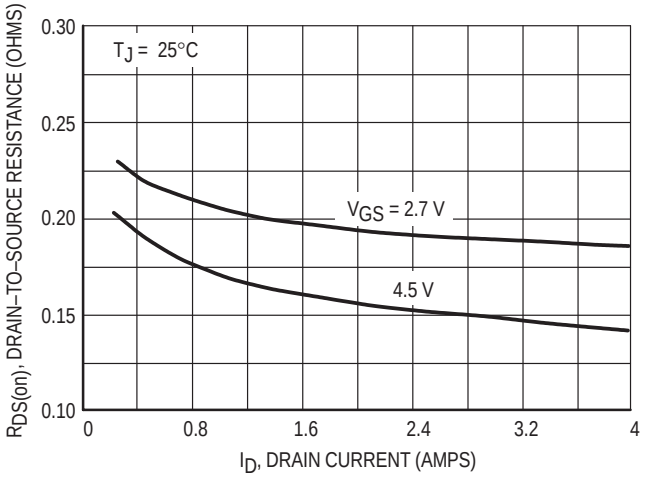


Figure 4. On–Resistance versus Drain Current and Gate Voltage

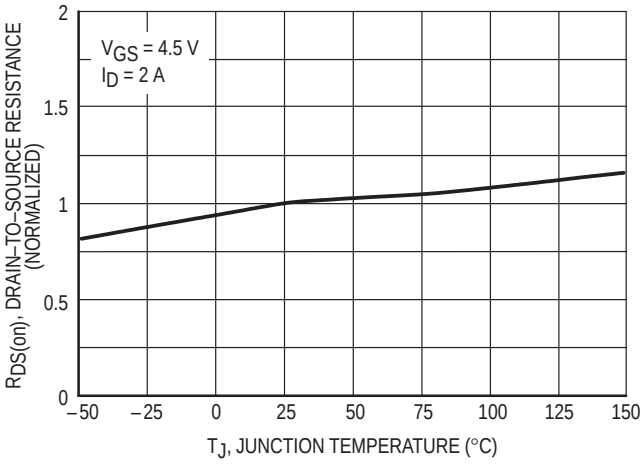


Figure 5. On–Resistance Variation with Temperature

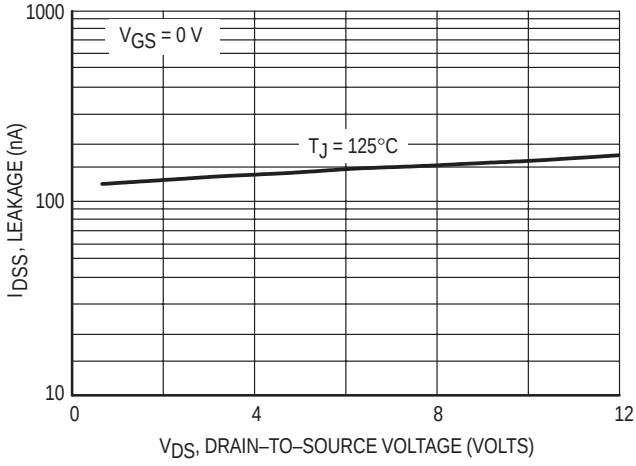


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

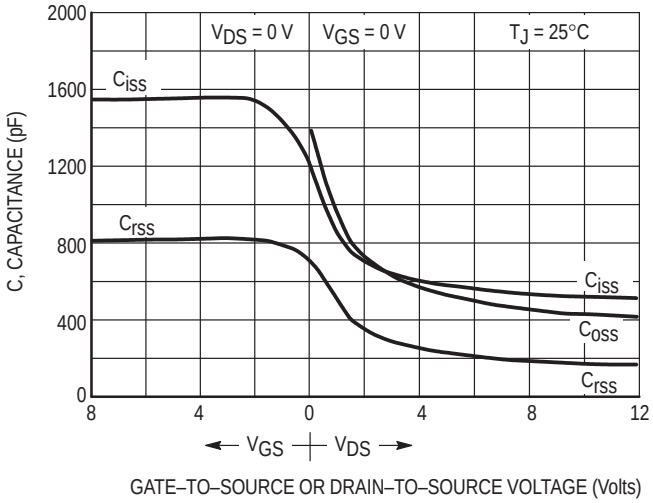


Figure 7. Capacitance Variation

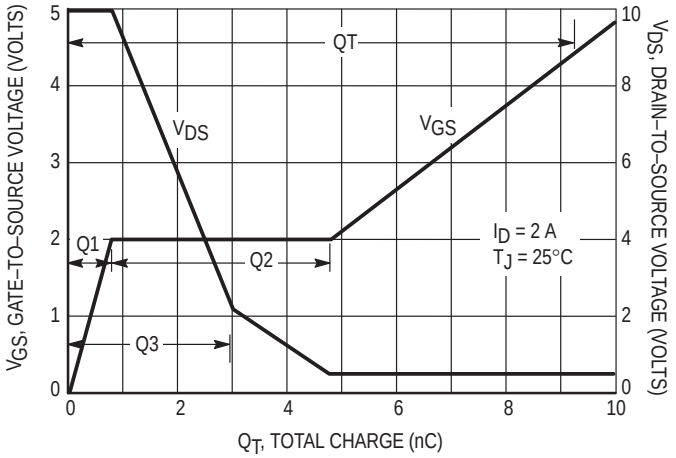


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

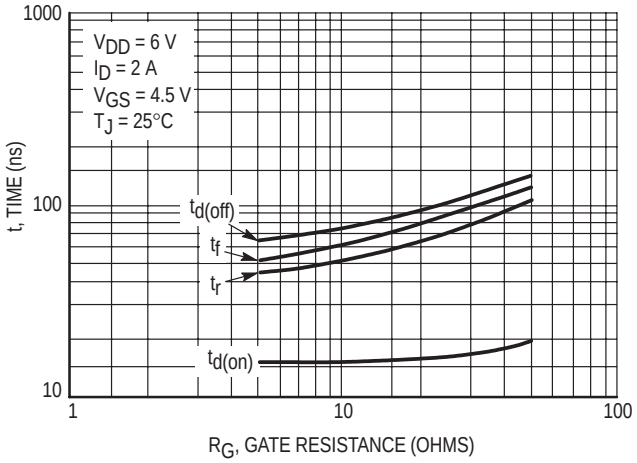


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 14. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

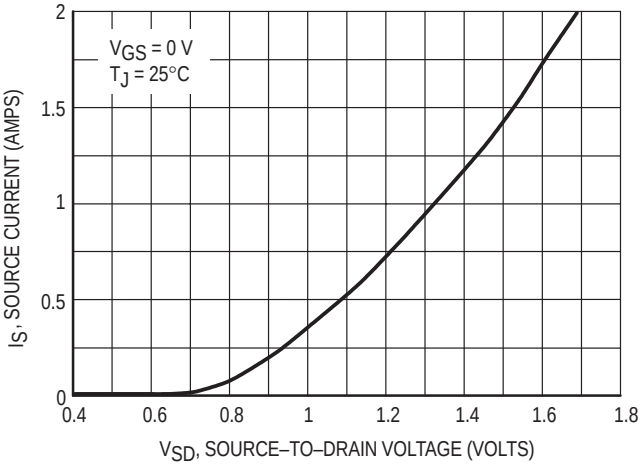


Figure 10. Diode Forward Voltage versus Current

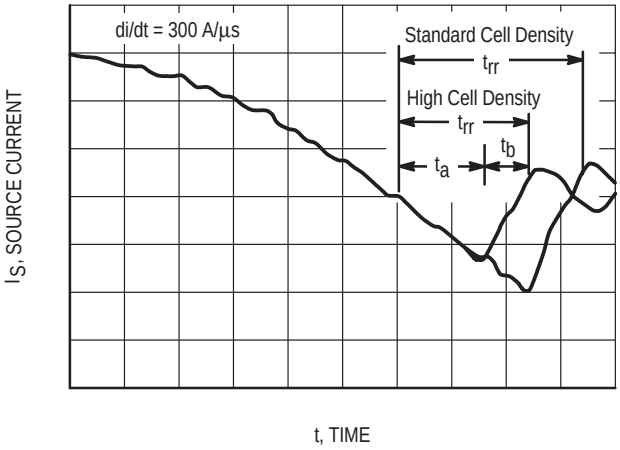


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

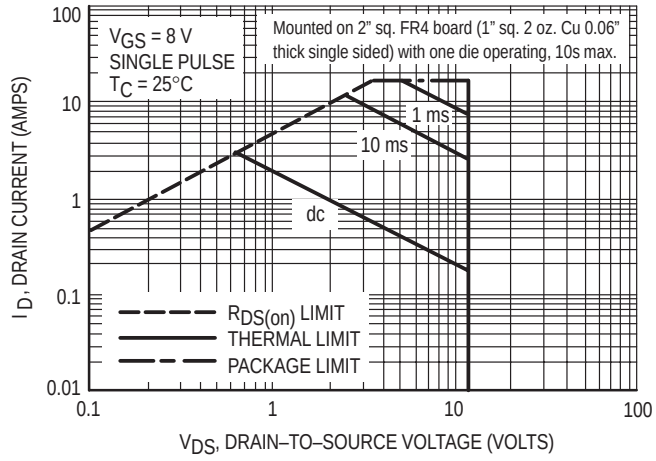


Figure 12. Maximum Rated Forward Biased Safe Operating Area

TYPICAL ELECTRICAL CHARACTERISTICS

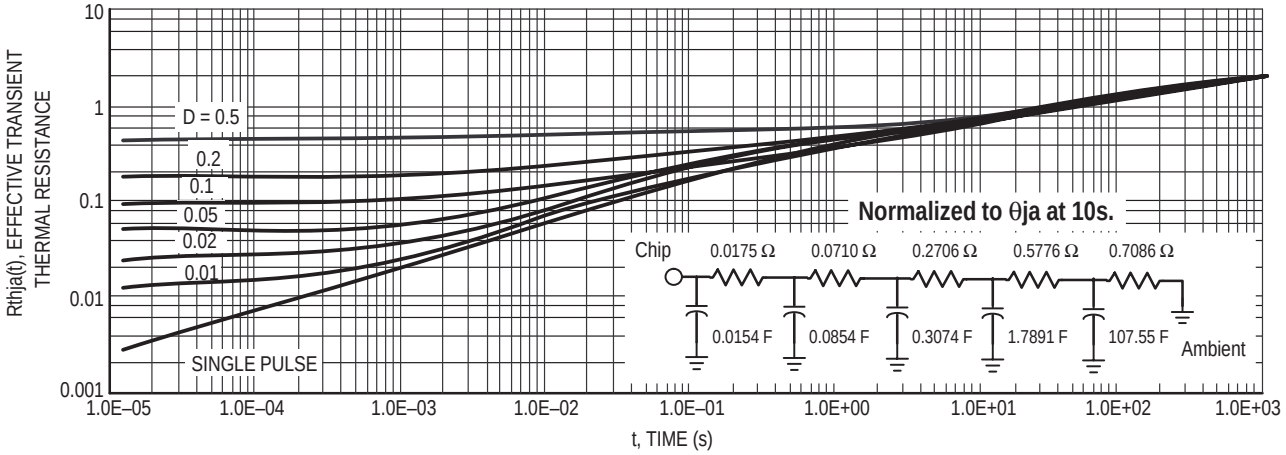


Figure 13. Thermal Response

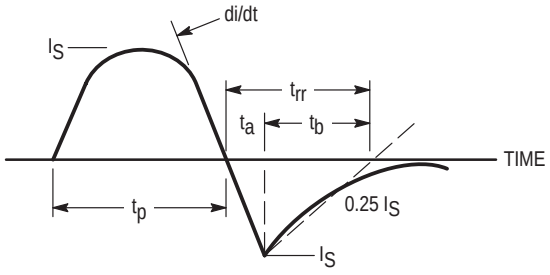


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

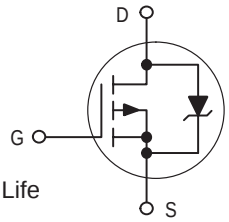
TMOS Dual P-Channel Field Effect Transistors

MMDF2P02E

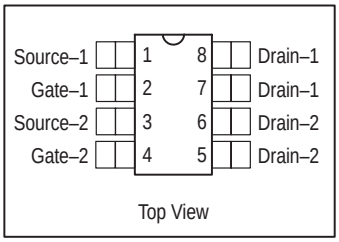
DUAL TMOS MOSFET
2.5 AMPERES
25 VOLTS
$R_{DS(on)}$ = 0.250 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's TMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- I_{DSS} Specified at Elevated Temperatures
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided



CASE 751–05, Style 11
SO–8



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	25	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	2.5 1.7 13	Adc Apk
Total Power Dissipation @ T_A = 25°C (2) Derate above 25°C	P_D	2.0 16	W mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 10 Vdc, Peak I_L = 7.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	245	mJ
Thermal Resistance, Junction to Ambient (2)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 0.0625″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

F2P02

(1) Negative sign for P–Channel device omitted for clarity.
(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF2P02ER2	13″	12 mm embossed tape	2500

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	25 —	— 2.2	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	1.0 –	2.0 3.8	3.0 –	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	— —	0.19 0.3	0.25 0.4	Ohm
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.0 Adc)		g_{FS}	1.0	2.8	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	340	475	pF
Output Capacitance		C_{oss}	—	220	300	
Transfer Capacitance		C_{rss}	—	75	150	
SWITCHING CHARACTERISTICS(3)						
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 5.0 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	20	40	ns
Rise Time		t_r	—	40	80	
Turn–Off Delay Time		$t_{d(off)}$	—	53	106	
Fall Time		t_f	—	41	82	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	13	26	
Rise Time		t_r	—	29	58	
Turn–Off Delay Time		$t_{d(off)}$	—	30	60	
Fall Time		t_f	—	28	56	
Gate Charge	(V_{DS} = 16 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	10	15	nC
		Q_1	—	1.0	—	
		Q_2	—	3.5	—	
		Q_3	—	3.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(2)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.5	2.0	Vdc
Reverse Recovery Time See Figure 11	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	32	64	ns
		t_a	—	19	—	
		t_b	—	12	—	
Reverse Recovery Storage Charge		Q_{RR}	—	0.035	—	μC

(1) Negative sign for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(3) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

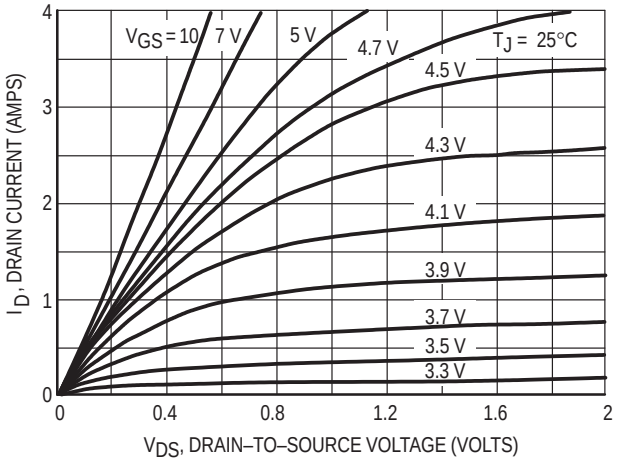


Figure 1. On–Region Characteristics

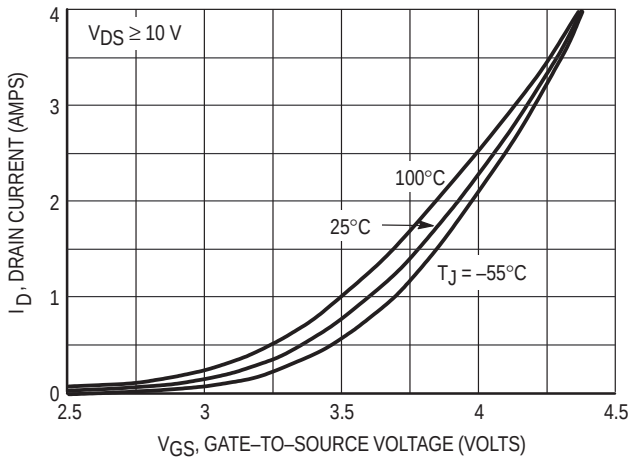


Figure 2. Transfer Characteristics

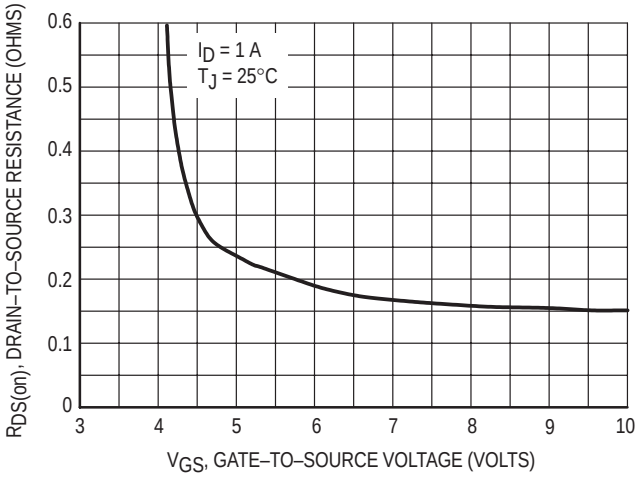


Figure 3. On–Resistance versus Gate–to–Source Voltage

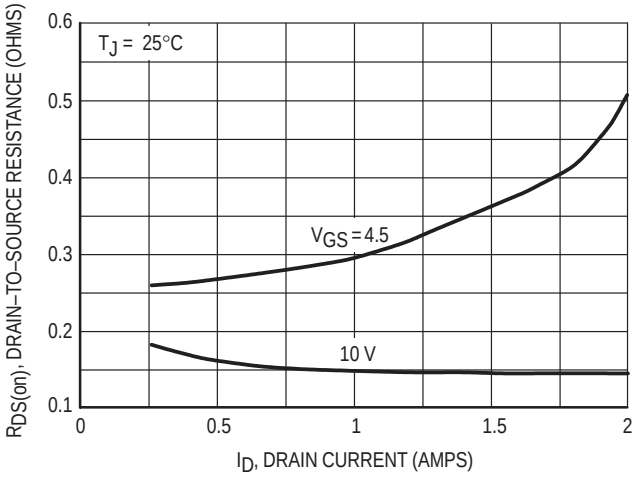


Figure 4. On–Resistance versus Drain Current and Gate Voltage

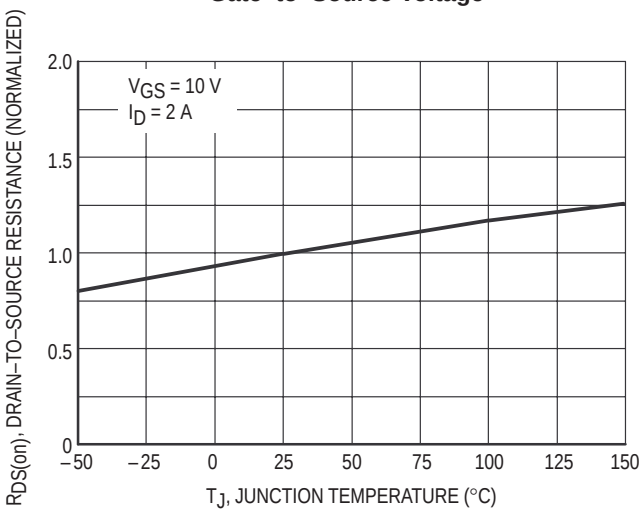


Figure 5. On–Resistance Variation with Temperature

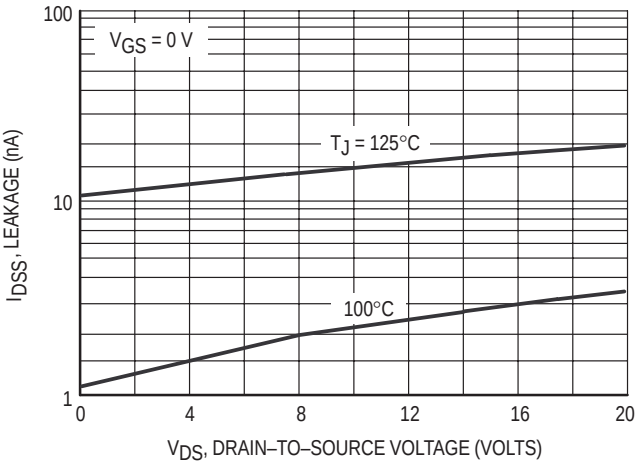


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

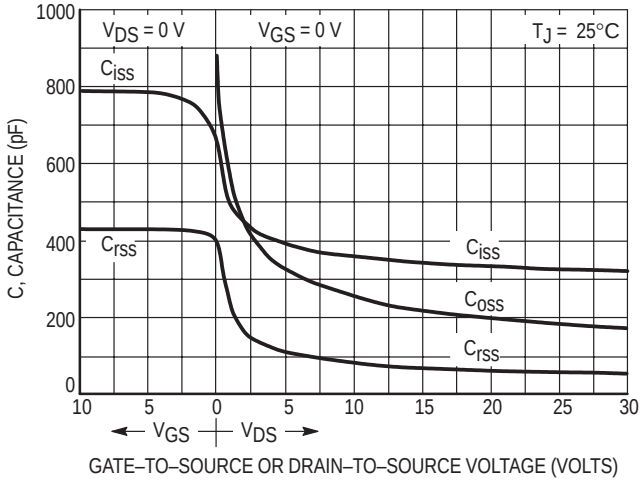


Figure 7. Capacitance Variation

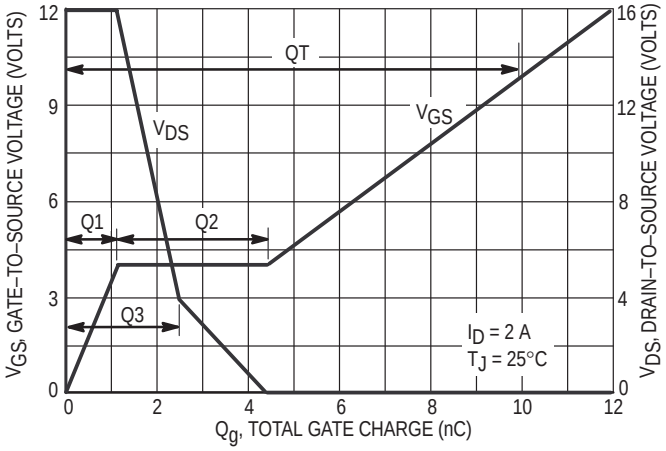


Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

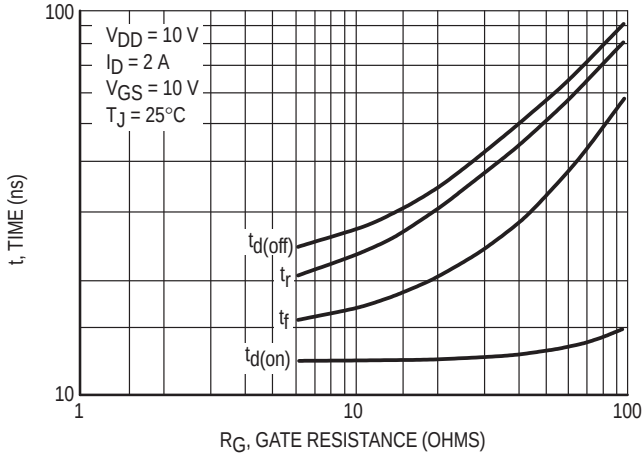


Figure 9. Resistive Switching Time Variation versus Gate Resistance

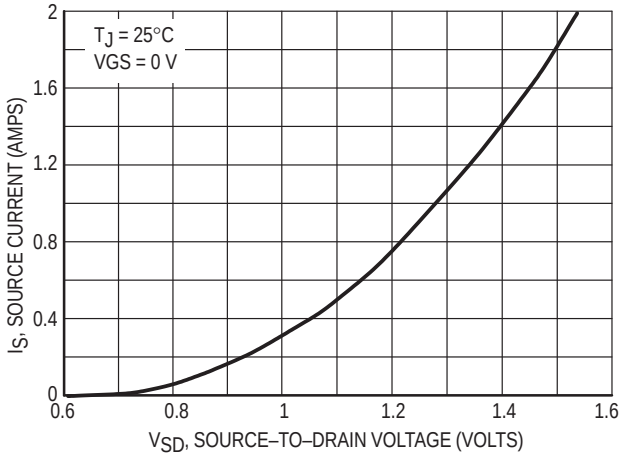


Figure 10. Diode Forward Voltage versus Current

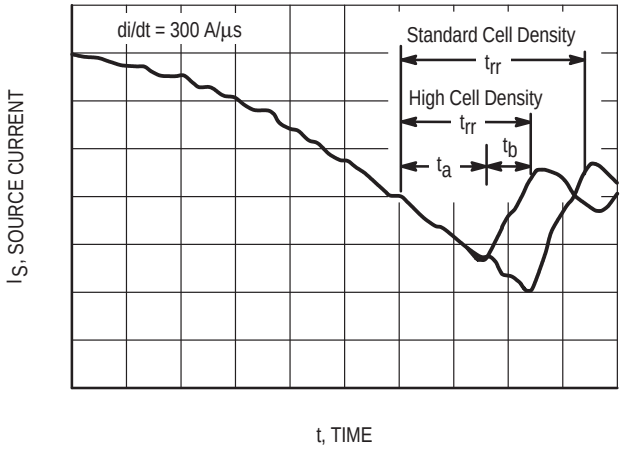


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

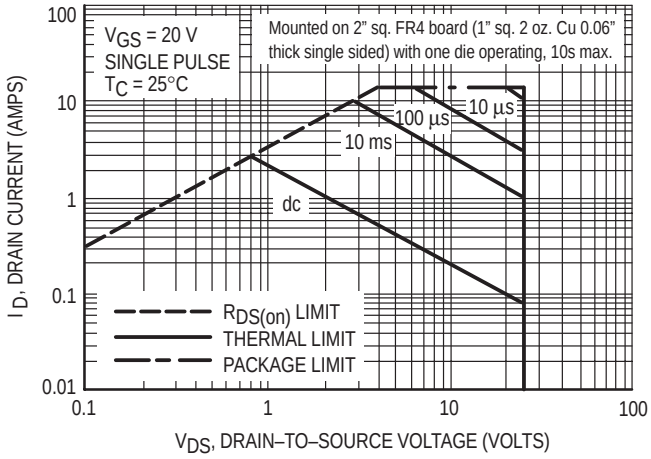


Figure 12. Maximum Rated Forward Biased Safe Operating Area

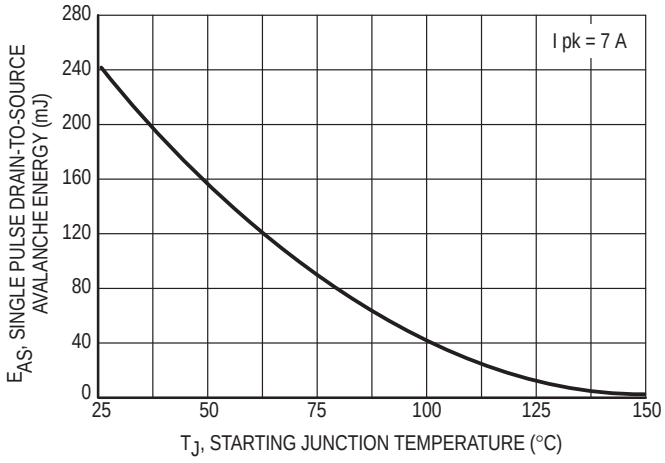


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

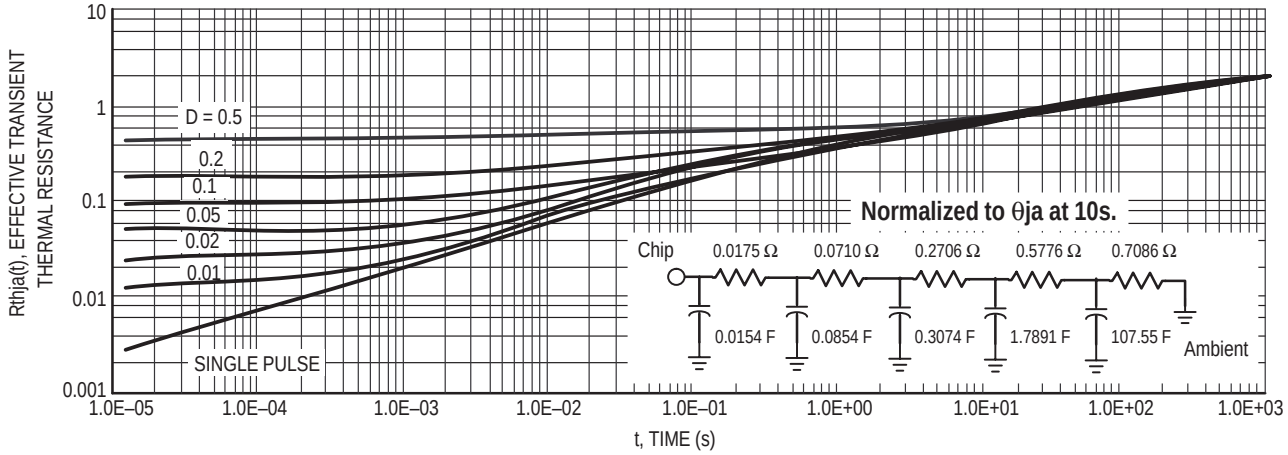


Figure 14. Thermal Response

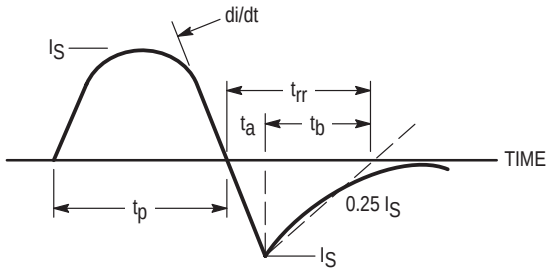


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

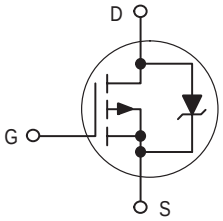
TMOS P-Channel Field Effect Transistors

MMDF2P02HD

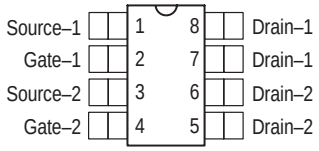
Motorola Preferred Device

DUAL TMOS POWER FET
2.0 AMPERES
20 VOLTS
$R_{DS(on)}$ = 0.160 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.



CASE 751–05, Style 11
SO–8



Top View

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	3.3 2.1 20	Adc Apk
Total Power Dissipation @ T_A = 25°C (2)	P_D	2.0	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 5.0 Vdc, I_L = 6.0 Apk, L = 18 mH, R_G = 25 Ω)	E_{AS}	324	mJ
Thermal Resistance — Junction to Ambient (2)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

D2P02

(1) Negative sign for P–Channel device omitted for clarity.
(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF2P02HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 20 —	 — 25	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 —	 1.5 4.0	 2.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc) (VGS = 4.5 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	 — —	 0.118 0.152	 0.160 0.180	Ohm
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.0 Adc)		g_{FS}	2.0	3.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	420	588	pF
Output Capacitance		C_{oss}	—	290	406	
Reverse Transfer Capacitance		C_{rss}	—	116	232	
SWITCHING CHARACTERISTICS(3)						
Turn–On Delay Time	(V_{DS} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	19	38	ns
Rise Time		t_r	—	66	132	
Turn–Off Delay Time		$t_{d(off)}$	—	25	50	
Fall Time		t_f	—	37	74	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	11	22	
Rise Time		t_r	—	21	42	
Turn–Off Delay Time		$t_{d(off)}$	—	45	90	
Fall Time		t_f	—	36	72	
Gate Charge	(V_{DS} = 16 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	15	20	nC
		Q_1	—	1.2	—	
		Q_2	—	5.0	—	
		Q_3	—	4.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(2)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 1.5 1.24	 2.1 —	Vdc
Reverse Recovery Time	(V_{DD} = 15 V, I_S = 2.0 A, dI_S/dt = 100 A/μs)	t_{rr}	—	38	—	ns
		t_a	—	17	—	
		t_b	—	21	—	
		Q_{RR}	—	0.034	—	μC

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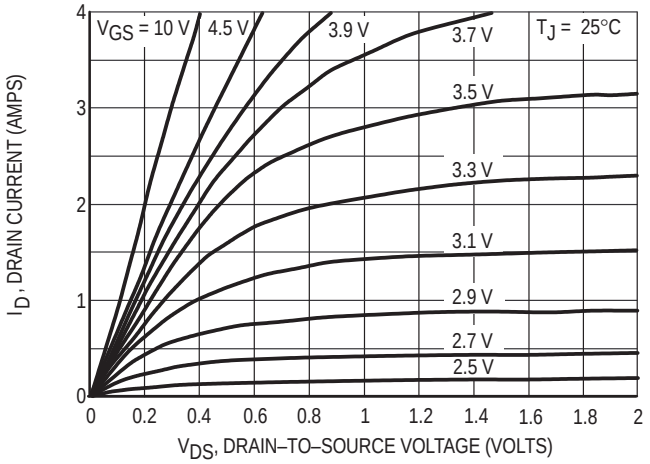

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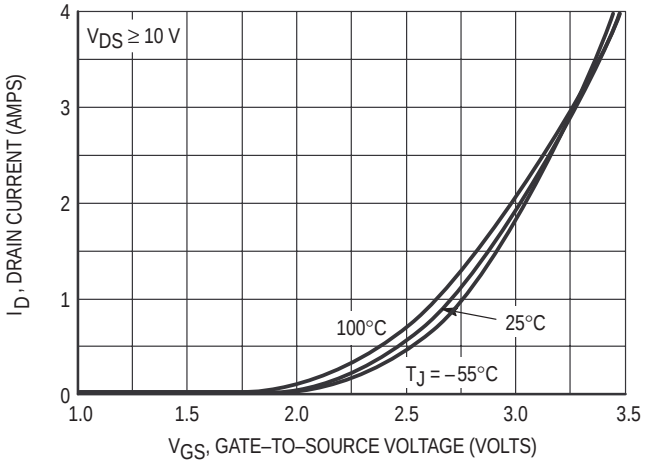

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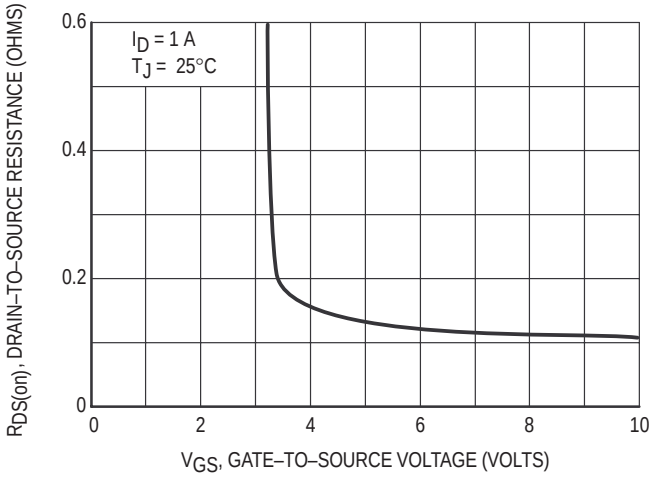

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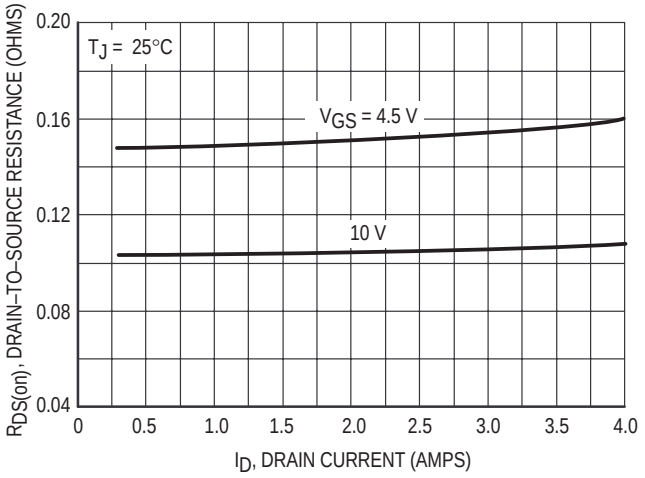

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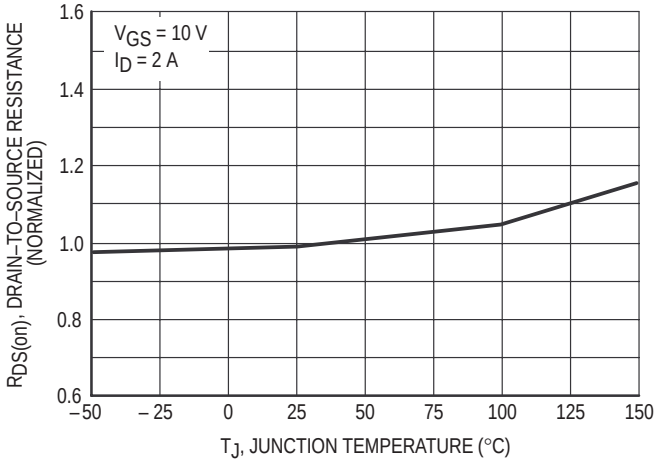

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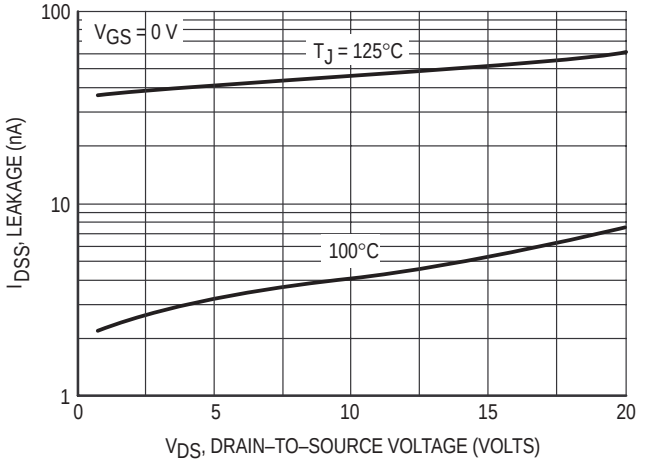

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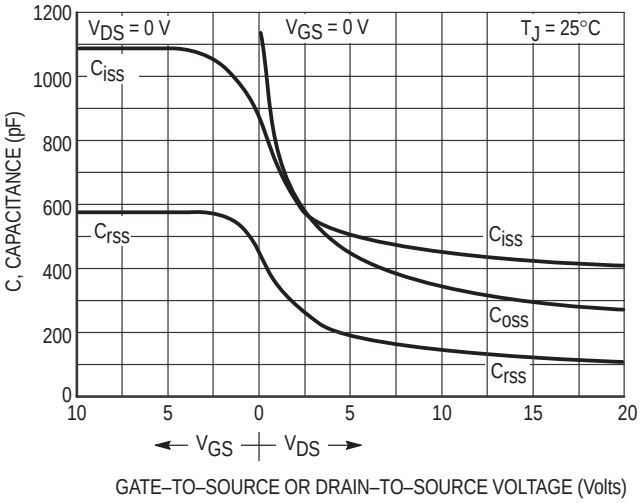
The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.



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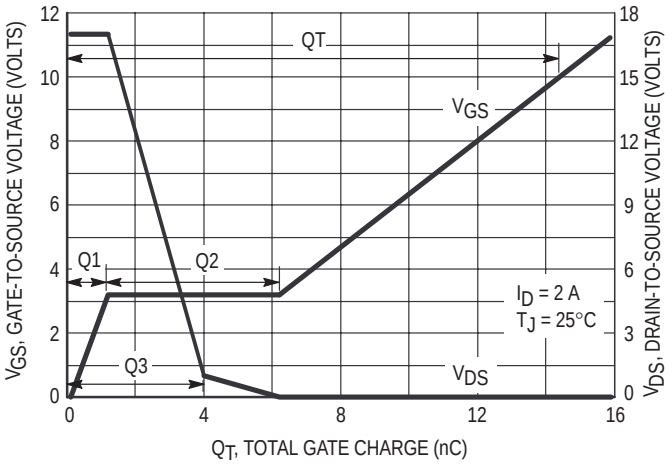


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

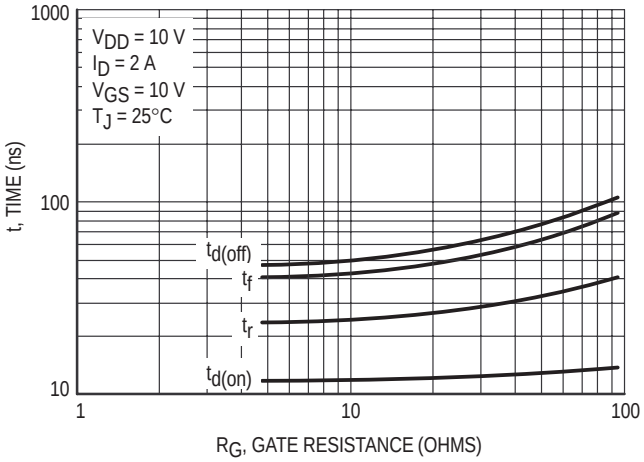


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

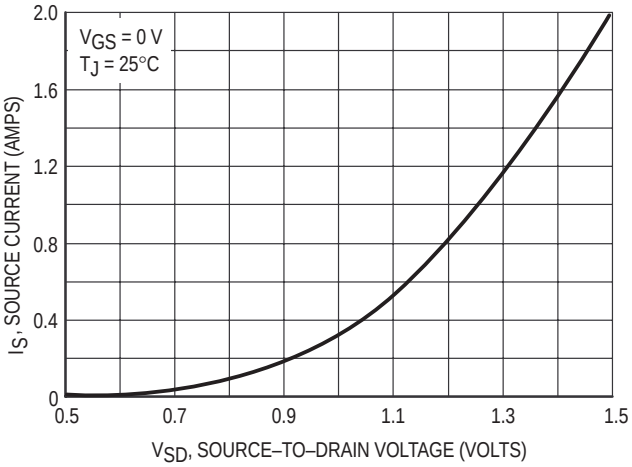


Figure 10. Diode Forward Voltage versus Current

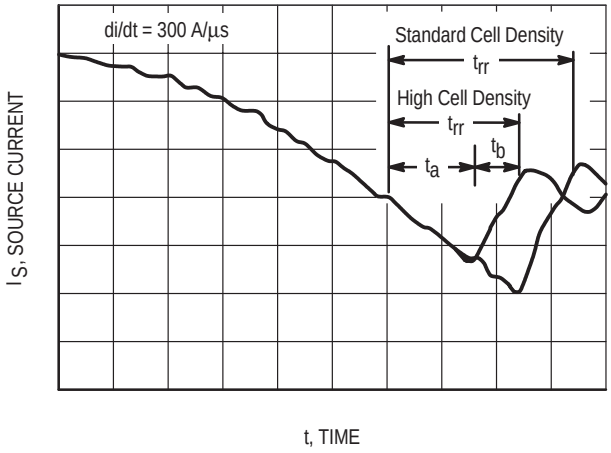


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

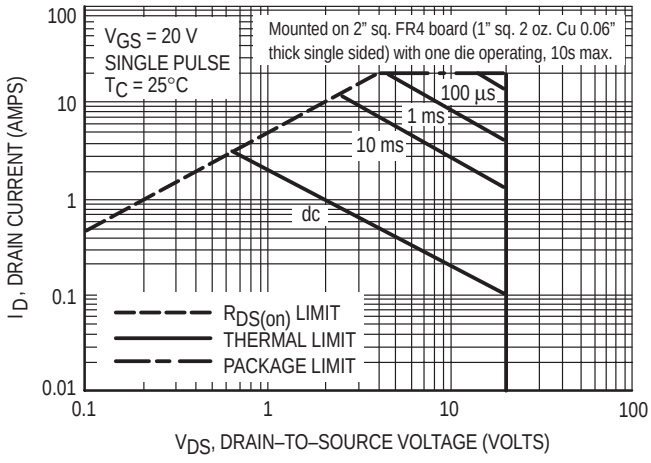


Figure 12. Maximum Rated Forward Biased Safe Operating Area

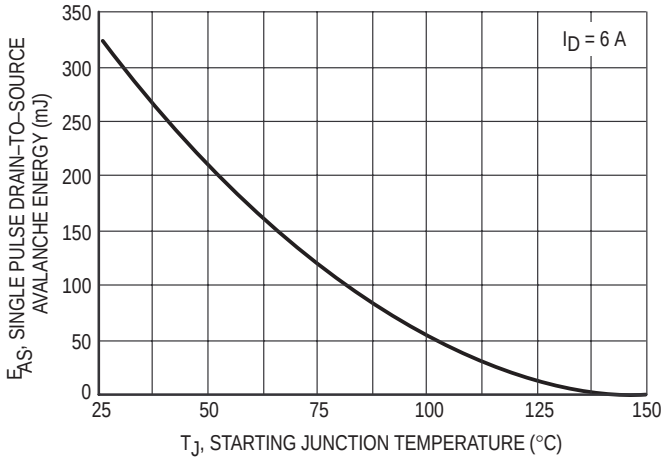


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

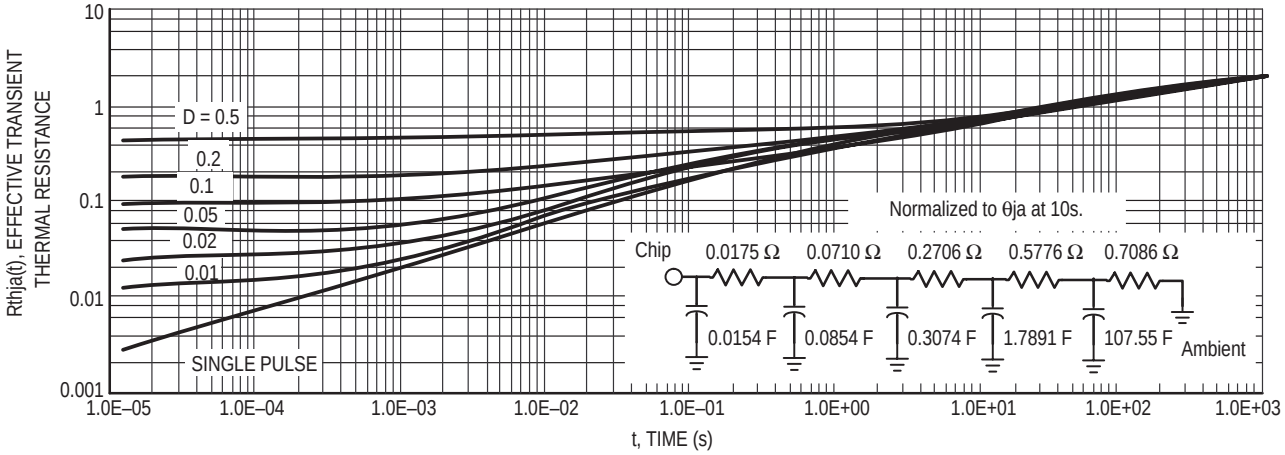


Figure 14. Thermal Response

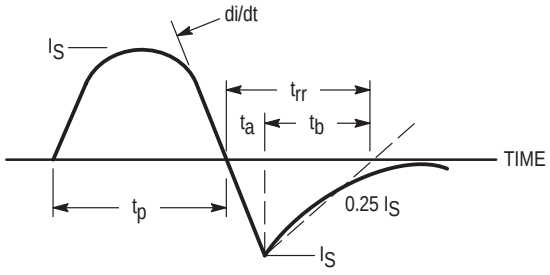


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

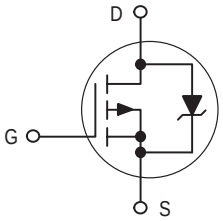
TMOS Dual P-Channel Field Effect Transistors

MMDF2P03HD

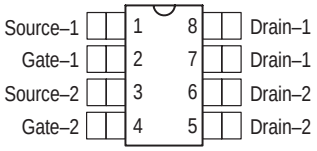
Motorola Preferred Device

DUAL TMOS
POWER MOSFET
2.0 AMPERES
30 VOLTS
$R_{DS(on)}$ = 0.200 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.



CASE 751–05, Style 11
SO–8



Top View

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	30	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	3.0 1.9 15	Adc Apk
Total Power Dissipation @ T_C = 25°C (2)	P_D	2.0	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 30 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 6.0 Apk, L = 18 mH, R_G = 25 Ω)	E_{AS}	324	mJ
Thermal Resistance — Junction to Ambient (2)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

D2P03

(1) Negative sign for P–Channel device omitted for clarity.
(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF2P03HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.
REV 5

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 30 —	 — 27	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 —	 1.5 4.0	 2.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	 — —	 0.170 0.225	 0.200 0.300	Ohm
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.0 Adc)		g_{FS}	2.0	3.4	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	397	550	pF
Output Capacitance		C_{oss}	—	189	250	
Transfer Capacitance		C_{rss}	—	64	126	
SWITCHING CHARACTERISTICS(3)						
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 2.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	16.25	33	ns
Rise Time		t_r	—	17.5	35	
Turn–Off Delay Time		$t_{d(off)}$	—	62.5	125	
Fall Time		t_f	—	194	390	
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	9.0	18	
Rise Time		t_r	—	10	20	
Turn–Off Delay Time		$t_{d(off)}$	—	81	162	
Fall Time		t_f	—	192	384	
Gate Charge See Figure 8	(V_{DS} = 24 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	14.2	19	nC
		Q_1	—	1.1	—	
		Q_2	—	4.5	—	
		Q_3	—	3.5	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(2)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	1.82 1.36	2.0 —	Vdc
Reverse Recovery Time See Figure 15	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	42.3	—	ns
		t_a	—	15.6	—	
		t_b	—	26.7	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.044	—	μC

(1) Negative sign for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(3) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

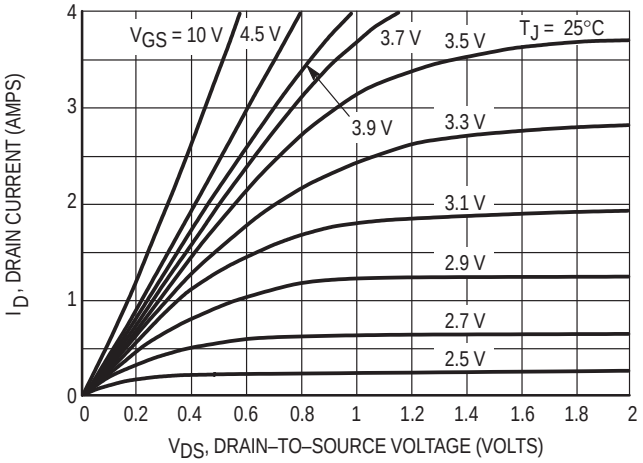


Figure 1. On–Region Characteristics

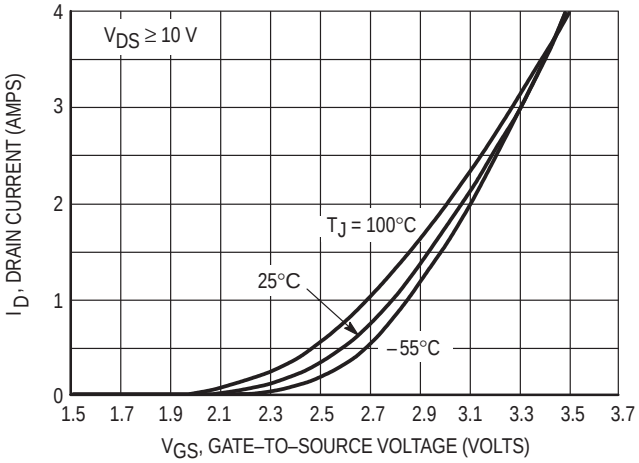


Figure 2. Transfer Characteristics

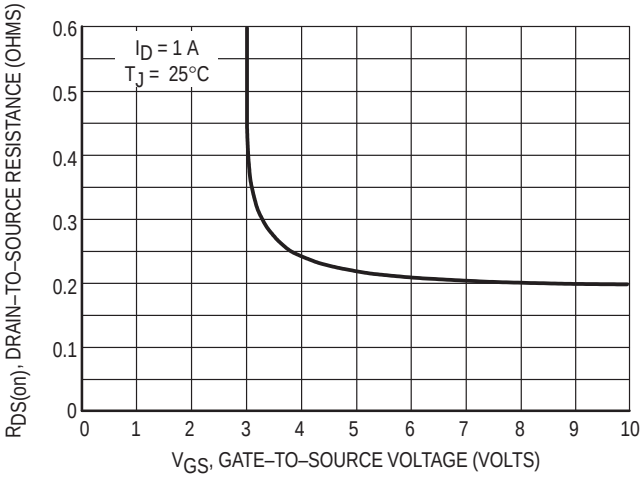


Figure 3. On–Resistance versus Gate–to–Source Voltage

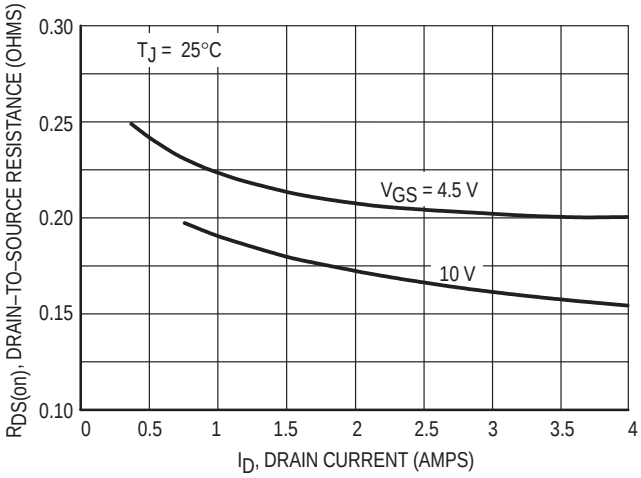


Figure 4. On–Resistance versus Drain Current and Gate Voltage

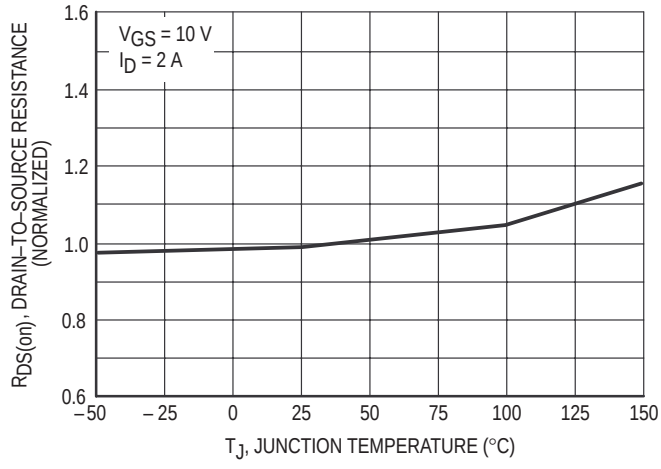


Figure 5. On–Resistance Variation with Temperature

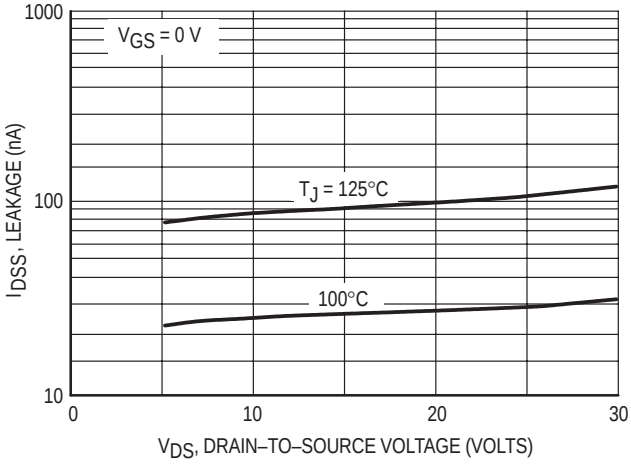


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

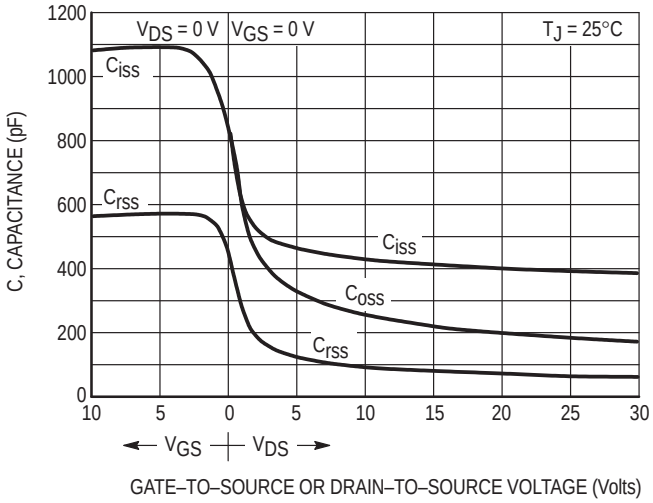


Figure 7. Capacitance Variation

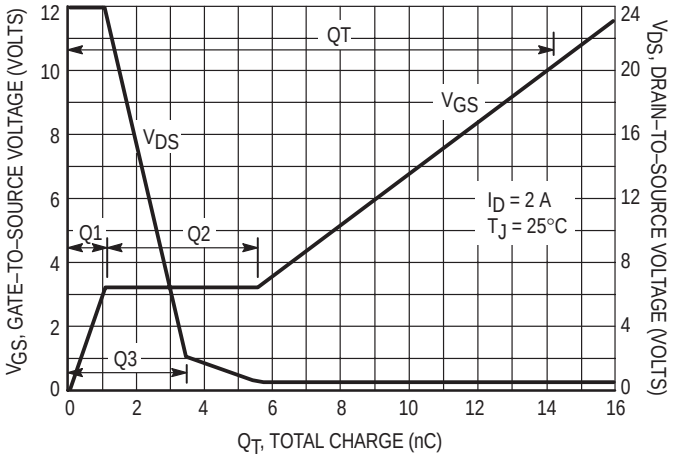


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

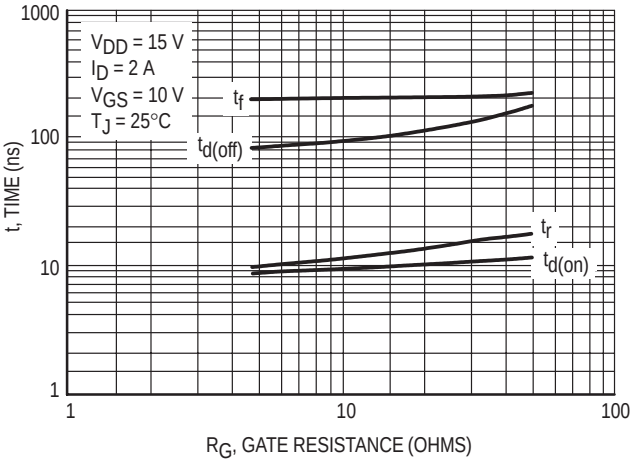


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

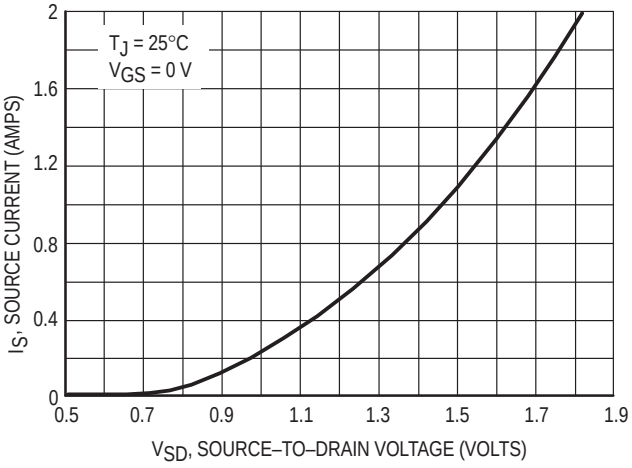


Figure 10. Diode Forward Voltage versus Current

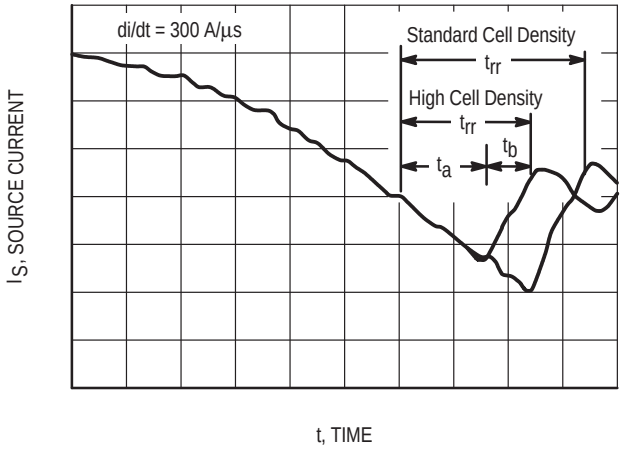


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

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A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

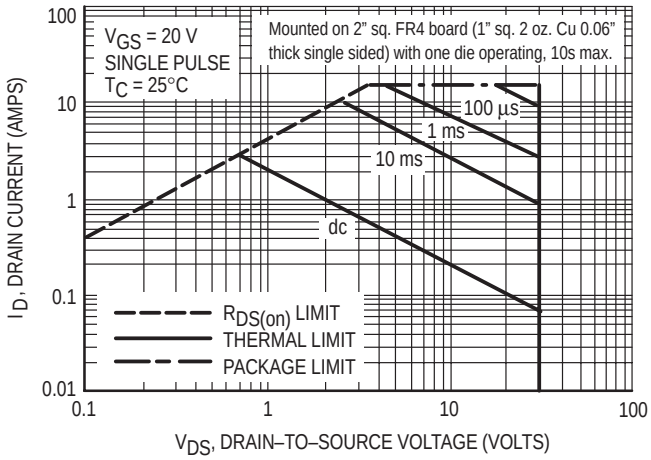


Figure 12. Maximum Rated Forward Biased Safe Operating Area

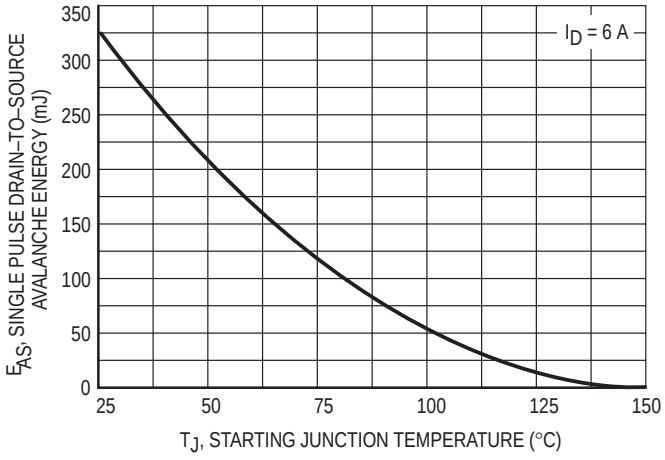


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

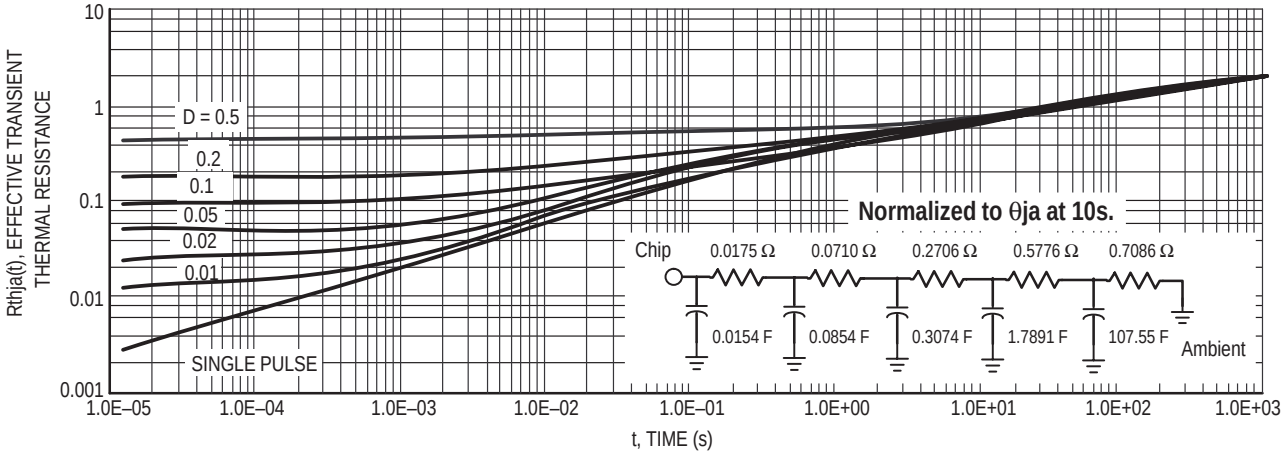


Figure 14. Thermal Response

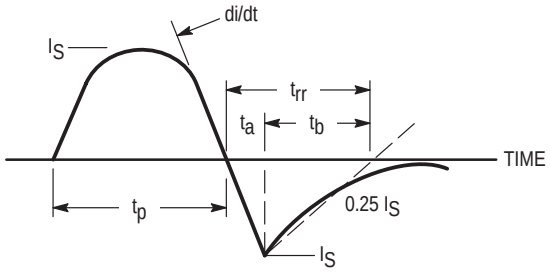


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

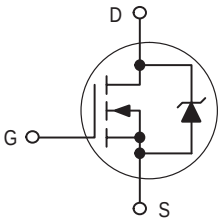
TMOS Dual N-Channel Field Effect Transistors

MMDF3N02HD

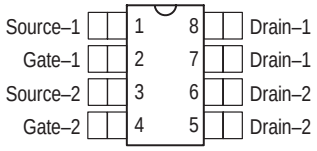
Motorola Preferred Device

DUAL TMOS
POWER MOSFET
3.0 AMPERES
20 VOLTS
$R_{DS(on)}$ = 0.090 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.



CASE 751–05, Style 11
SO–8



Top View

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	3.8 2.6 19	Adc Apk
Total Power Dissipation @ T_A = 25°C (1)	P_D	2.0	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 9.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	405	mJ
Thermal Resistance — Junction to Ambient (1)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

D3N02

(1) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF3N02HDR2	13″	12 mm embossed tape	2500

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 20 —	 — 29	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 —	 1.5 4.0	 2.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.5 Adc)		$R_{DS(on)}$	 — —	 0.058 0.074	 0.090 0.100	Ohms
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.5 Adc)		g_{FS}	2.0	3.88	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	455	630	pF
Output Capacitance		C_{oss}	—	184	250	
Transfer Capacitance		C_{rss}	—	45	90	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 3.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	11	22	ns
Rise Time		t_r	—	58	116	
Turn–Off Delay Time		$t_{d(off)}$	—	17	35	
Fall Time		t_f	—	20	40	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	7.0	21	
Rise Time		t_r	—	32	64	
Turn–Off Delay Time		$t_{d(off)}$	—	27	54	
Fall Time		t_f	—	21	42	
Gate Charge See Figure 8	(V_{DS} = 16 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	12.5	18	nC
		Q_1	—	1.3	—	
		Q_2	—	2.8	—	
		Q_3	—	2.4	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.79 0.72	1.3 —	Vdc
Reverse Recovery Time See Figure 15	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	23	—	ns
		t_a	—	18	—	
		t_b	—	5.0	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.025	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

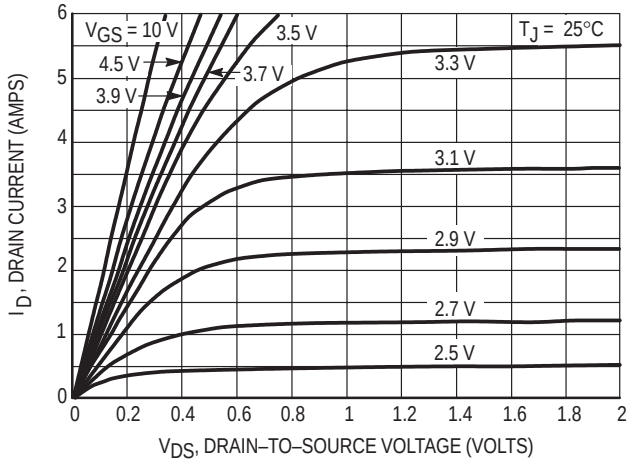


Figure 1. On–Region Characteristics

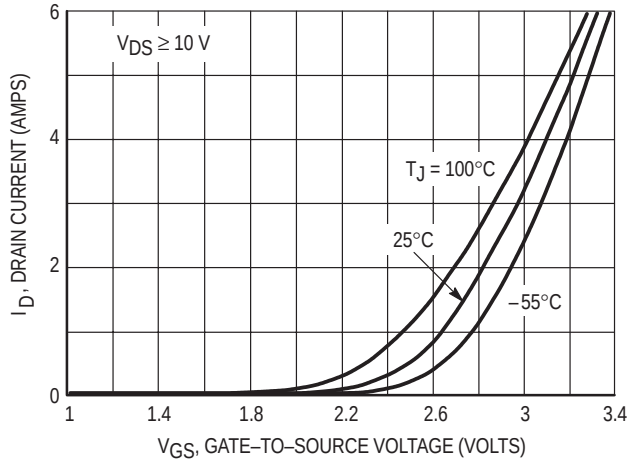


Figure 2. Transfer Characteristics

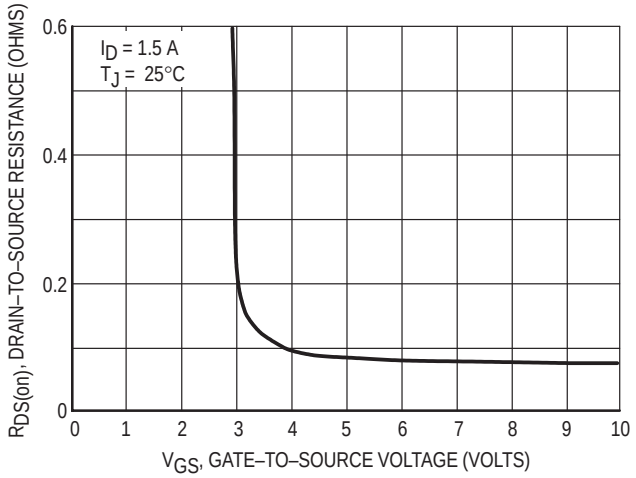


Figure 3. On–Resistance versus Gate–To–Source Voltage

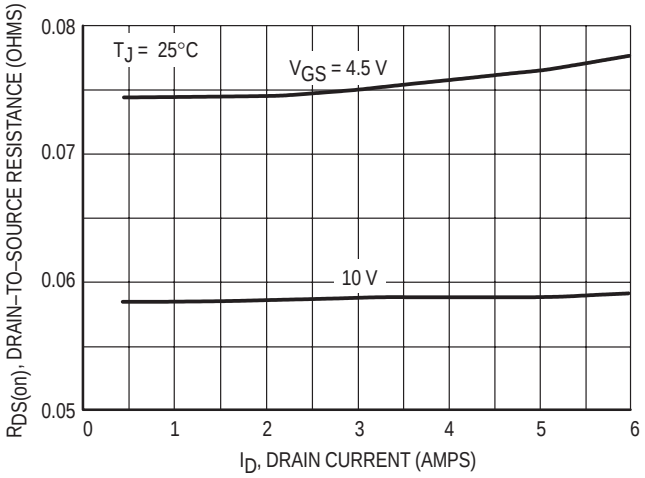


Figure 4. On–Resistance versus Drain Current and Gate Voltage

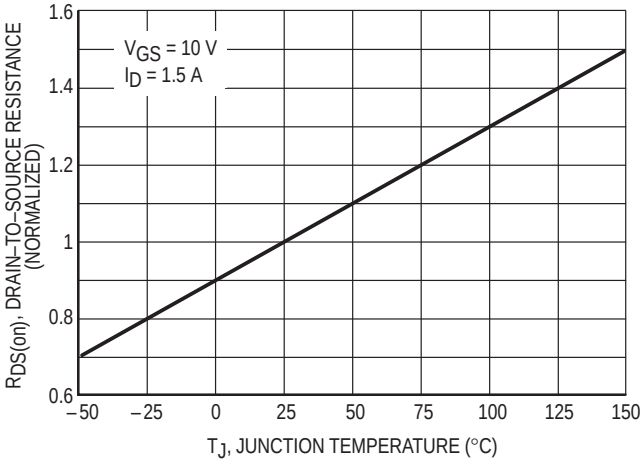


Figure 5. On–Resistance Variation with Temperature

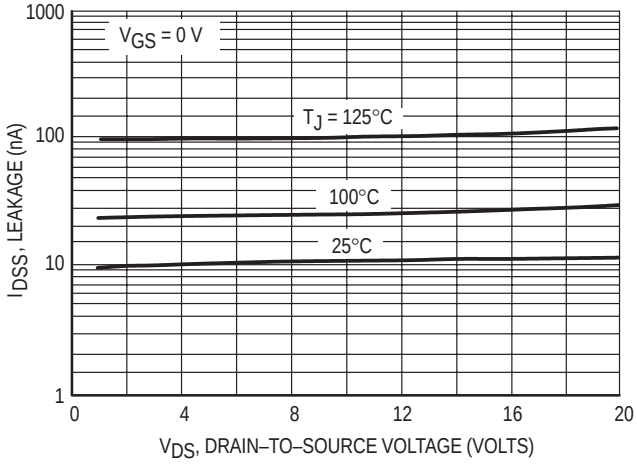


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

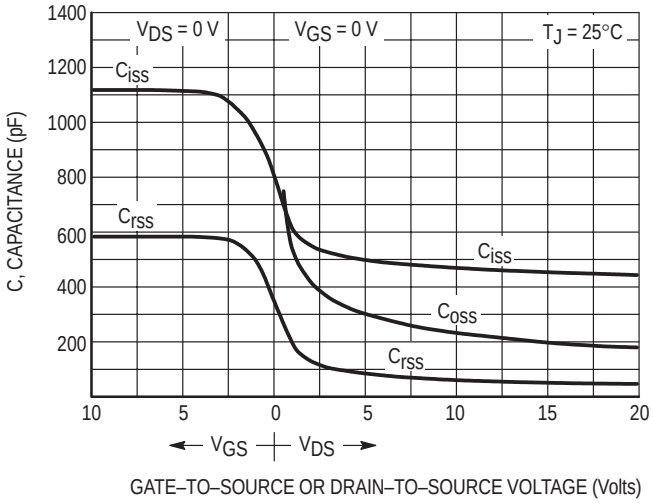


Figure 7. Capacitance Variation

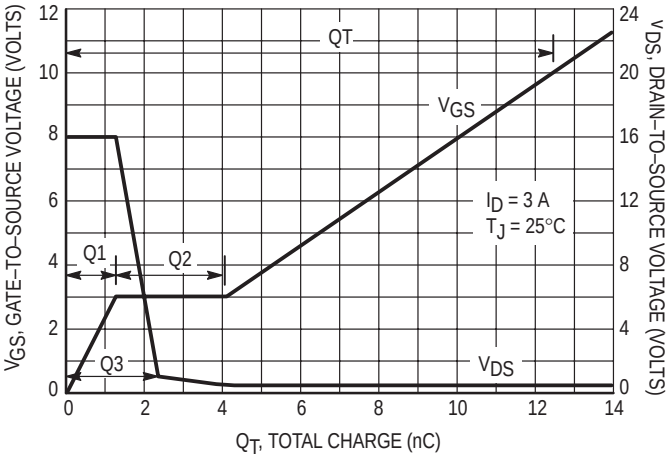


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

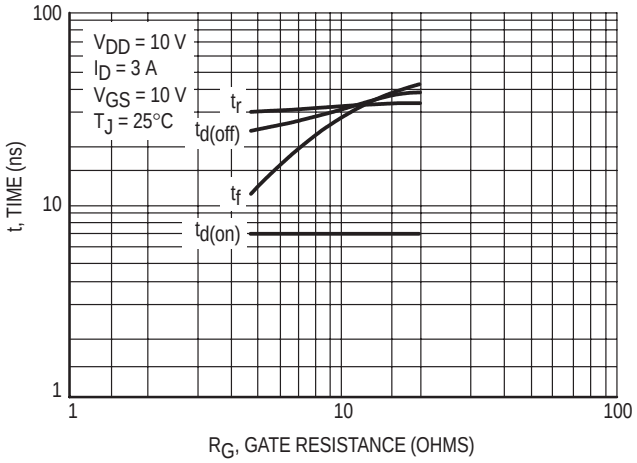


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

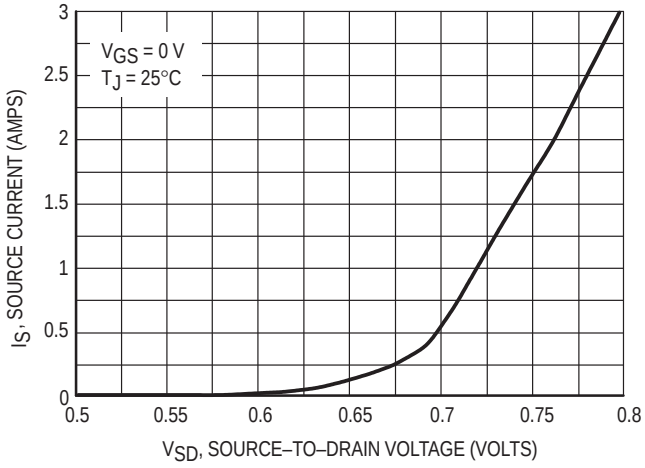


Figure 10. Diode Forward Voltage versus Current

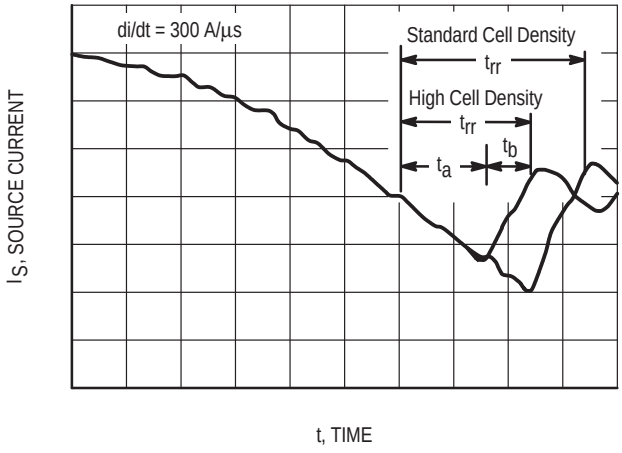


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

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Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

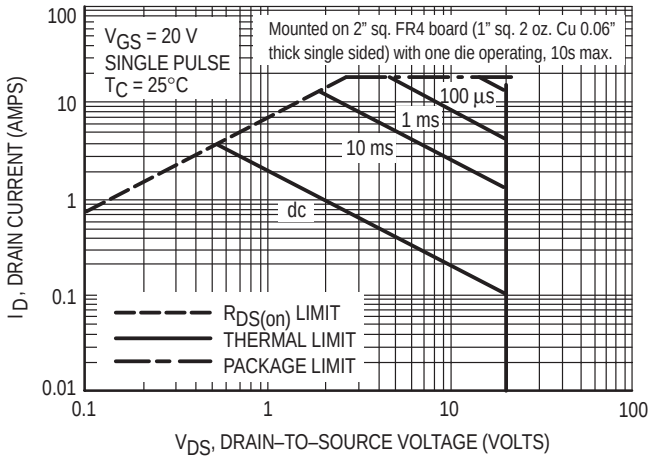
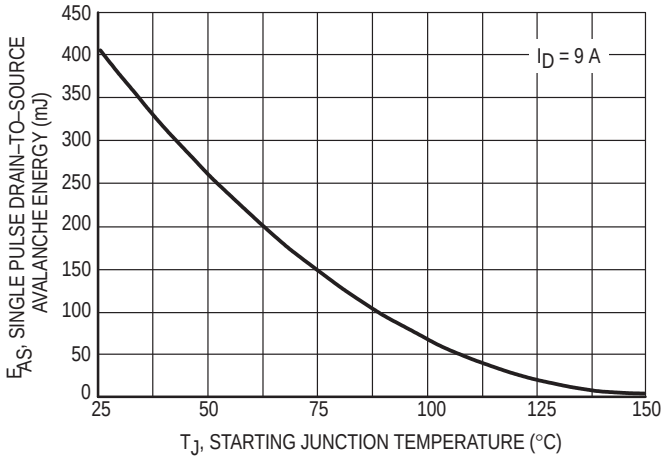


Figure 12. Maximum Rated Forward Biased Safe Operating Area



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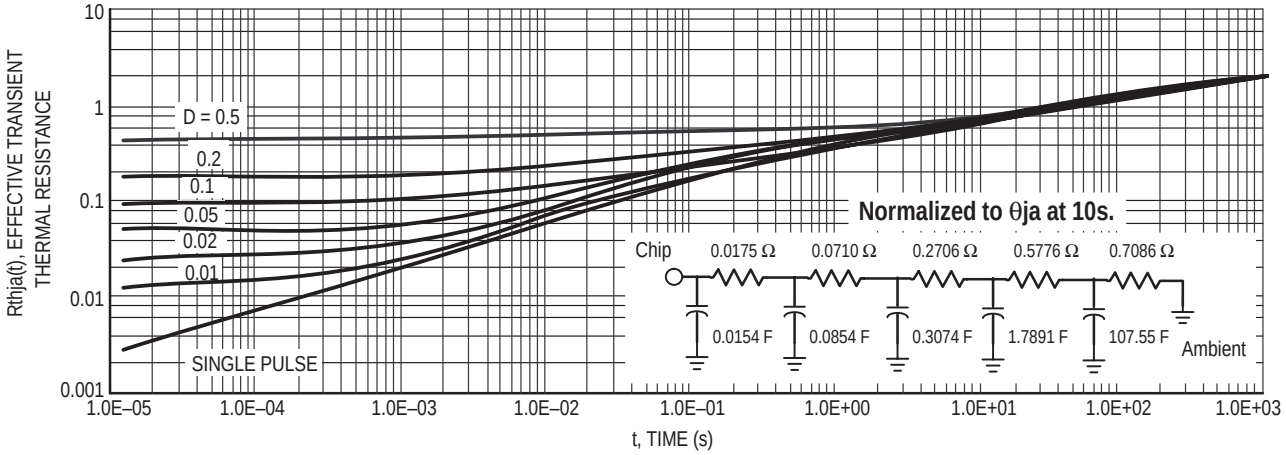
TYPICAL ELECTRICAL CHARACTERISTICS



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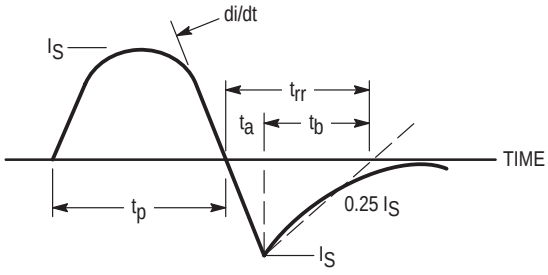

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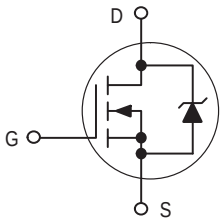

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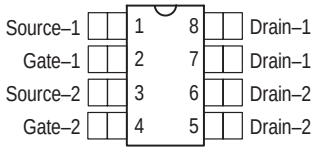
SO–8



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MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	30	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	4.1 3.0 40	Adc Apk
Total Power Dissipation @ T_A = 25°C (1)	P_D	2.0	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 30 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 9.0 Apk, L = 8.0 mH, R_G = 25 Ω)	E_{AS}	324	mJ
Thermal Resistance — Junction to Ambient (1)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

D3N03

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMDF3N03HDR2	13″	12 mm embossed tape	2500 units

(1) When mounted on 2" square FR–4 board (1" square 2 oz. Cu 0.06" thick single sided) with one die operating, 10s max.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 5

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	30	—	—	Vdc
Temperature Coefficient (Positive)			—	34.5	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	1.0	μAdc
(V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	10	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.7	3.0	Vdc
Threshold Temperature Coefficient (Negative)						mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	—	0.06	0.07	Ohms
(V_{GS} = 4.5 Vdc, I_D = 1.5 Adc)			—	0.065	0.075	
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.5 Adc)		g_{FS}	2.0	3.6	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	450	630	pF
Output Capacitance		C_{oss}	—	160	225	
Transfer Capacitance		C_{rss}	—	35	70	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 3.0 Adc, V_{GS} = 4.5 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	12	24	ns
Rise Time		t_r	—	65	130	
Turn–Off Delay Time		$t_{d(off)}$	—	16	32	
Fall Time		t_f	—	19	38	
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8	16	ns
Rise Time		t_r	—	15	30	
Turn–Off Delay Time		$t_{d(off)}$	—	30	60	
Fall Time		t_f	—	23	46	
Gate Charge	(V_{DS} = 10 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	11.5	16	nC
		Q_1	—	1.5	—	
		Q_2	—	3.5	—	
		Q_3	—	2.8	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.82	1.2	Vdc
	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.7	—	
Reverse Recovery Time See Figure 12	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	24	—	ns
		t_a	—	17	—	
		t_b	—	7	—	
Reverse Recovery Storage Charge		Q_{RR}	—	0.025	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

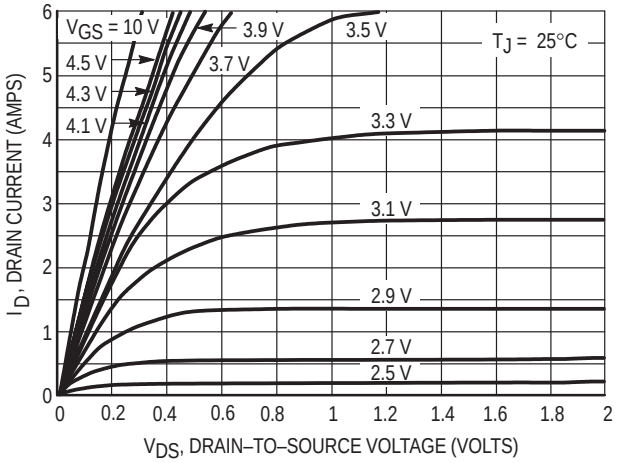


Figure 1. On–Region Characteristics

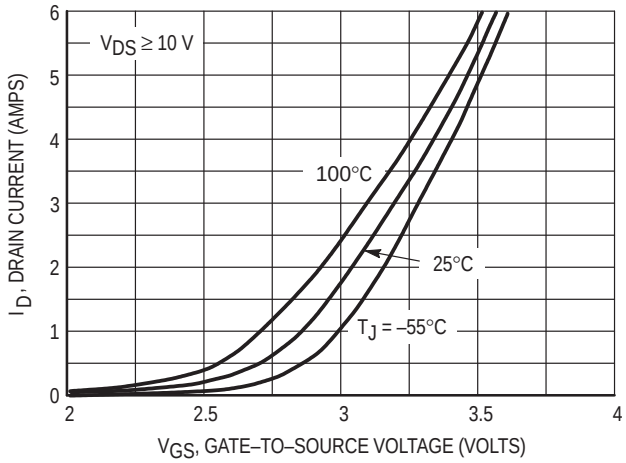


Figure 2. Transfer Characteristics

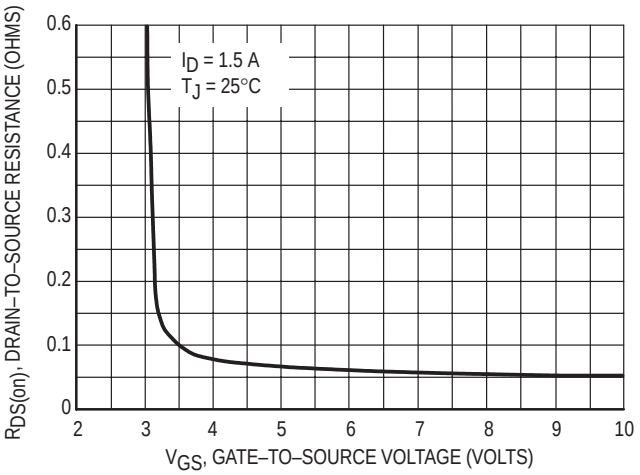


Figure 3. On–Resistance versus Gate–to–Source Voltage

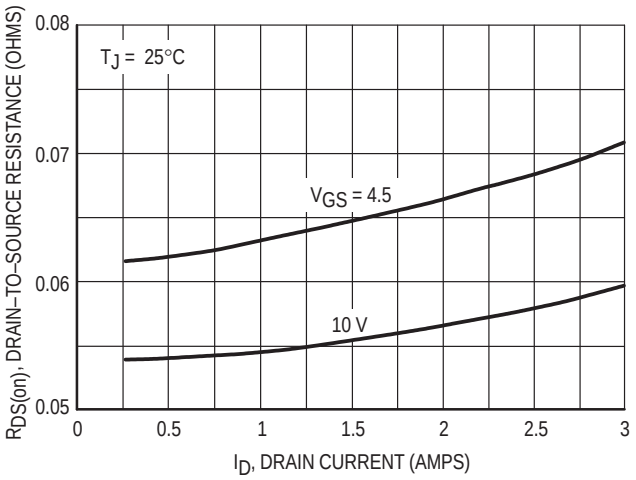


Figure 4. On–Resistance versus Drain Current and Gate Voltage

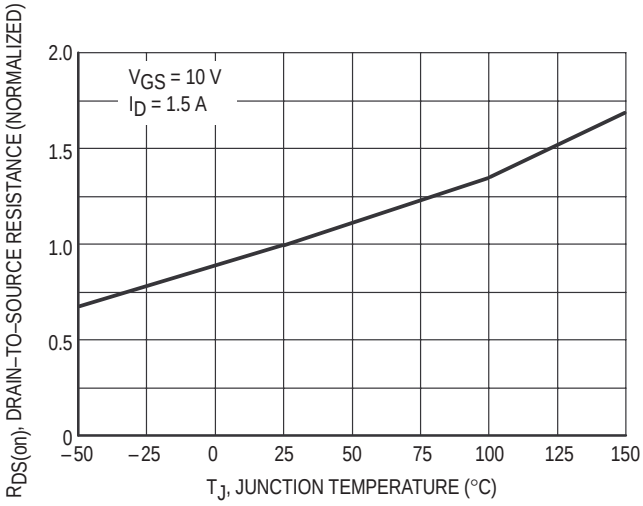


Figure 5. On–Resistance Variation with Temperature

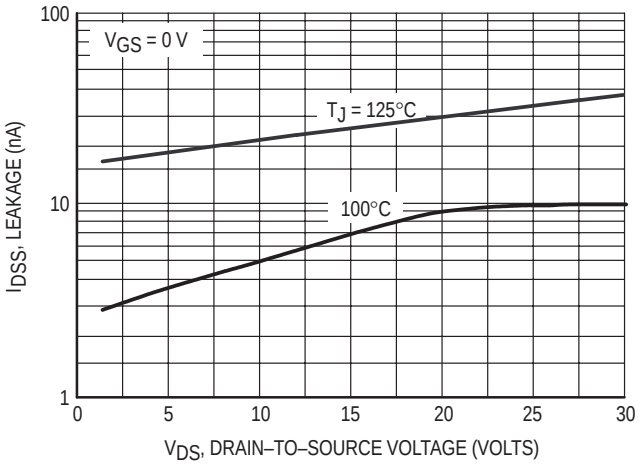


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

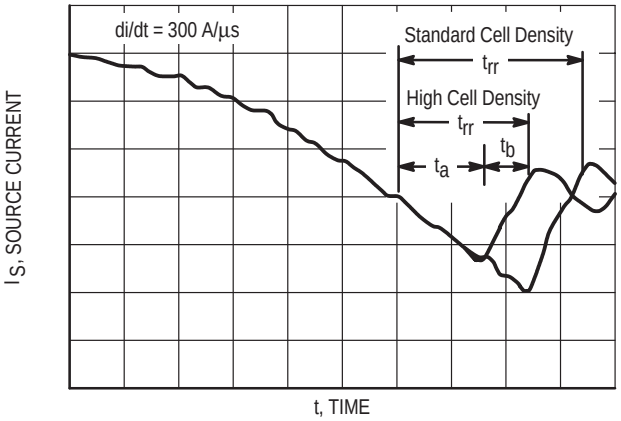


Figure 7. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 9). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

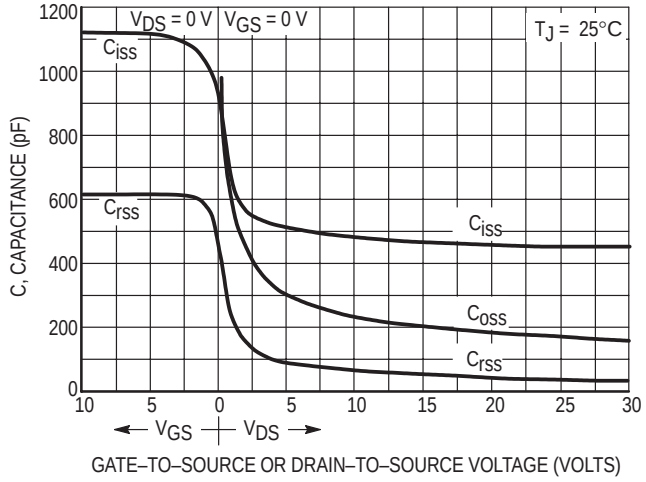


Figure 8. Capacitance Variation

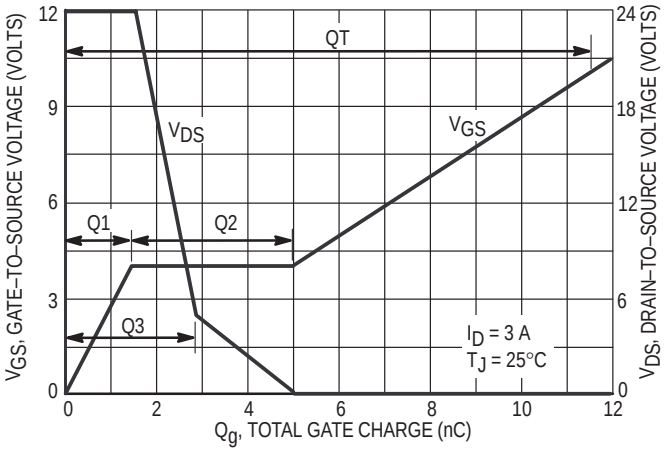


Figure 9. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

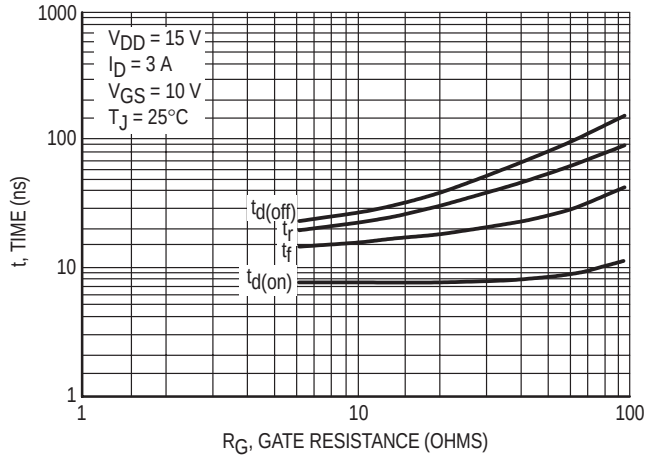


Figure 10. Resistive Switching Time Variation versus Gate Resistance

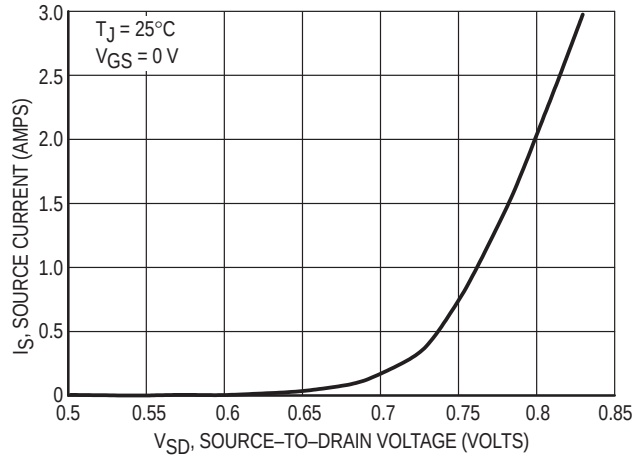


Figure 11. Diode Forward Voltage versus Current

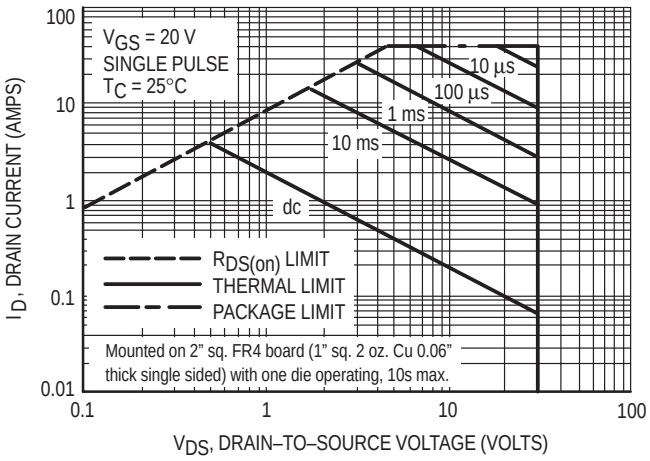


Figure 12. Maximum Rated Forward Biased Safe Operating Area

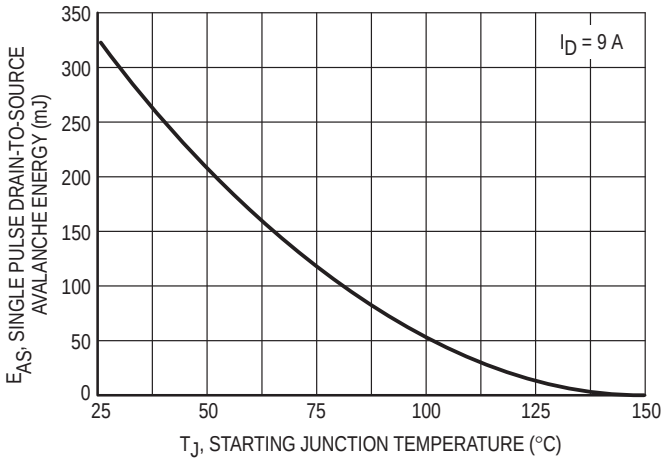


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

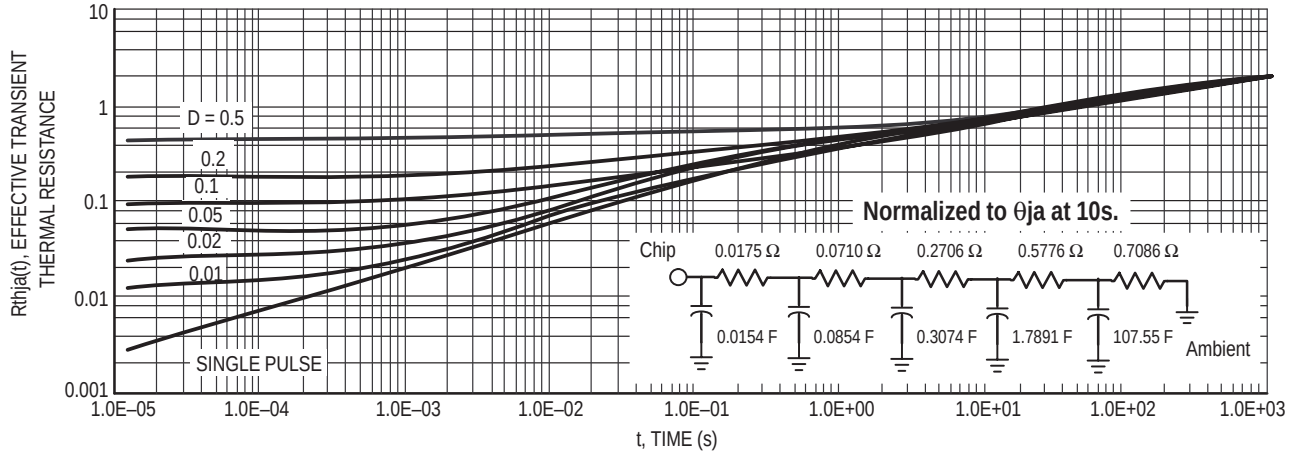


Figure 14. Thermal Response

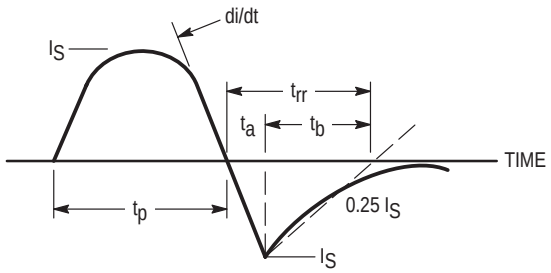


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

TMOS Dual N-Channel Field Effect Transistors

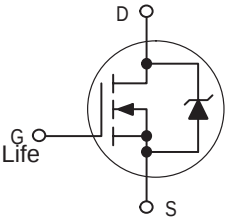
MMDF4N01HD

Motorola Preferred Device

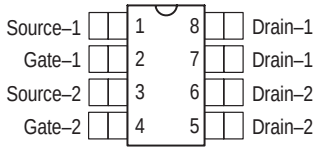
DUAL TMOS
POWER MOSFET
4.0 AMPERES
20 VOLTS
$R_{DS(on)}$ = 0.045 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided



CASE 751–05, Style 11
SO–8



Top View

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 8.0	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \leq 10$ μs)	I_D I_D I_{DM}	5.2 4.1 48	Adc Apk
Total Power Dissipation @ T_A = 25°C (1)	P_D	2.0	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Thermal Resistance — Junction to Ambient (1)	$R_{\theta JA}$	62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

D4N01

(1) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided) with one die operating, 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMSF4N01HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	20	—	—	Vdc
Temperature Coefficient (Positive)			—	2.0	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 12 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	1.0	µAdc
(V_{DS} = 12 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	10	
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mAdc)		$V_{GS(th)}$	0.6	0.8	1.1	Vdc
Temperature Coefficient (Negative)			—	2.8	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 4.5 Vdc, I_D = 4.0 Adc)		$R_{DS(on)}$	—	0.035	0.045	Ohm
(VGS = 2.7 Vdc, I_D = 2.0 Adc)			—	0.043	0.055	
Forward Transconductance (V_{DS} = 2.5 Vdc, I_D = 2.0 Adc)		g_{FS}	3.0	6.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 10 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	425	595	pF
Output Capacitance		C_{oss}	—	270	378	
Reverse Transfer Capacitance		C_{rss}	—	115	230	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 6.0 Vdc, I_D = 4.0 Adc, V_{GS} = 2.7 Vdc, R_G = 2.3 Ω)	$t_{d(on)}$	—	13	26	ns
Rise Time		t_r	—	60	120	
Turn–Off Delay Time		$t_{d(off)}$	—	20	40	
Fall Time		t_f	—	29	58	
Turn–On Delay Time	(V_{DD} = 6.0 Vdc, I_D = 4.0 Adc, V_{GS} = 4.5 Vdc, R_G = 2.3 Ω)	$t_{d(on)}$	—	10	20	
Rise Time		t_r	—	42	84	
Turn–Off Delay Time		$t_{d(off)}$	—	24	48	
Fall Time		t_f	—	28	56	
Gate Charge (See Figure 8)	(V_{DS} = 10 Vdc, I_D = 4.0 Adc, V_{GS} = 4.5 Vdc)	Q_T	—	9.2	13	nC
		Q_1	—	1.3	—	
		Q_2	—	3.5	—	
		Q_3	—	3.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.95	1.1	Vdc
	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.78	—	
Reverse Recovery Time	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/µs)	t_{rr}	—	38	—	ns
		t_a	—	17	—	
		t_b	—	22	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.028	—	µC

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

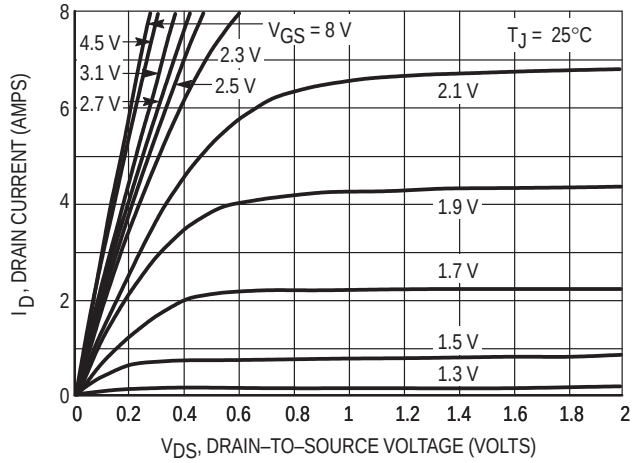


Figure 1. On–Region Characteristics

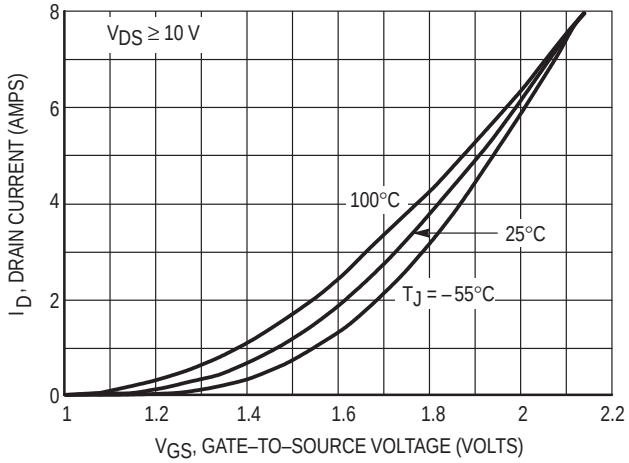


Figure 2. Transfer Characteristics

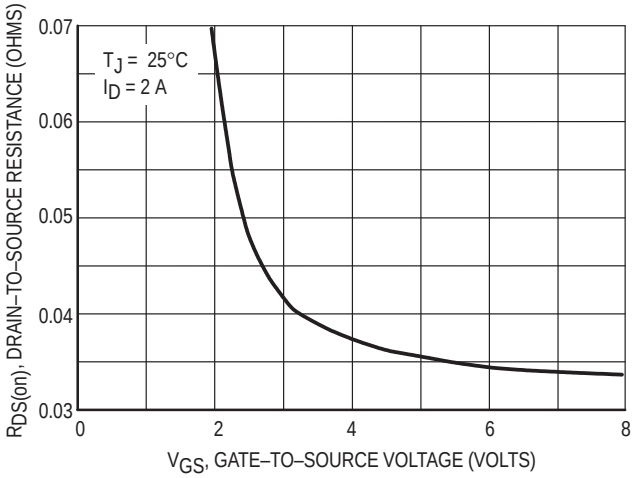


Figure 3. On–Resistance versus Gate–To–Source Voltage

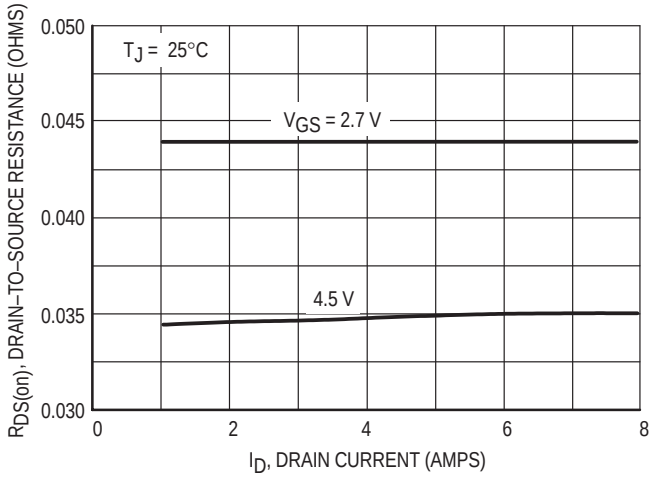


Figure 4. On–Resistance versus Drain Current and Gate Voltage

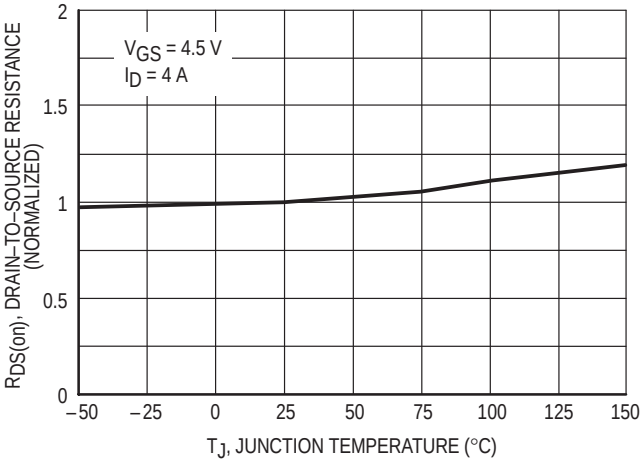


Figure 5. On–Resistance Variation with Temperature

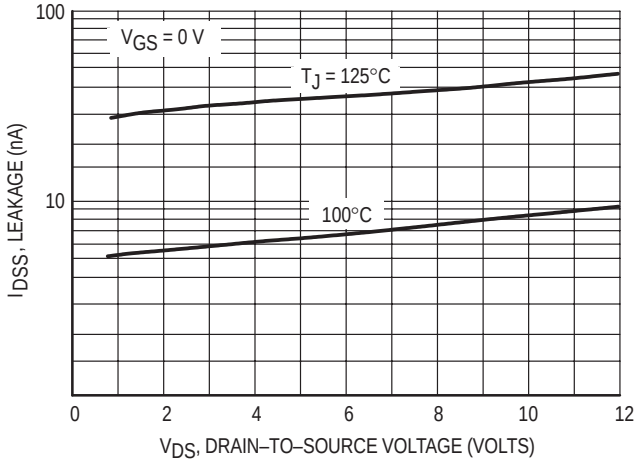


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

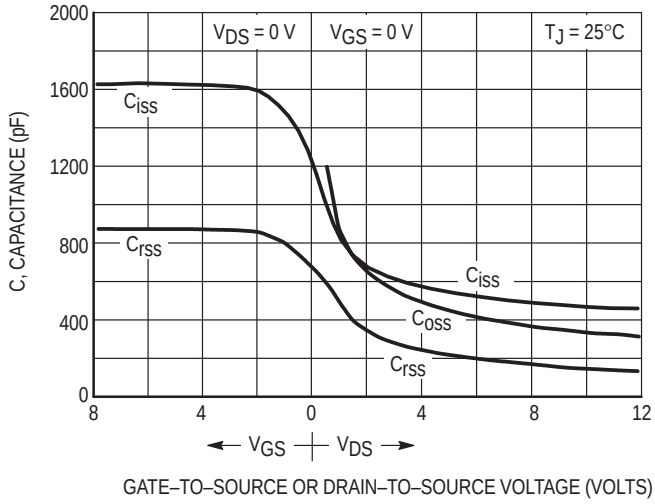


Figure 7. Capacitance Variation

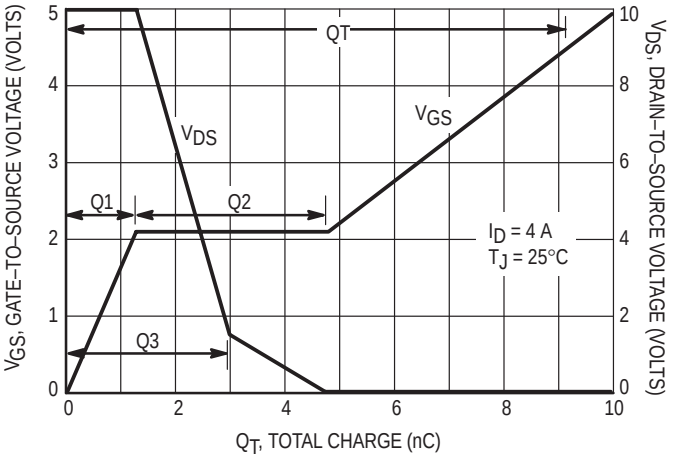


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

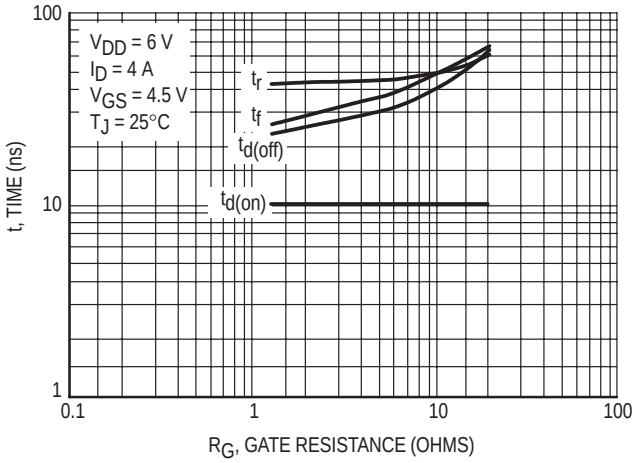


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 14. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

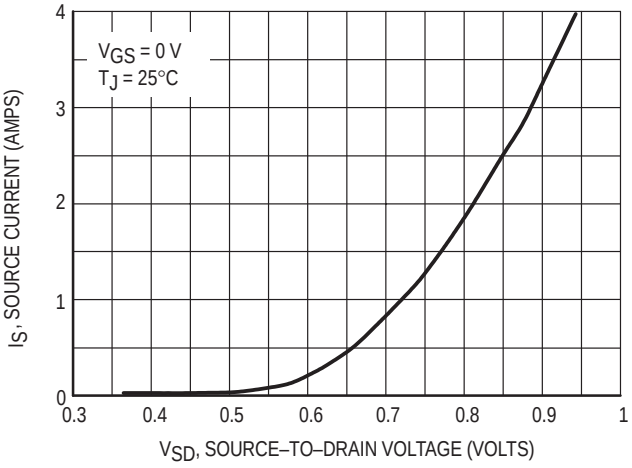


Figure 10. Diode Forward Voltage versus Current

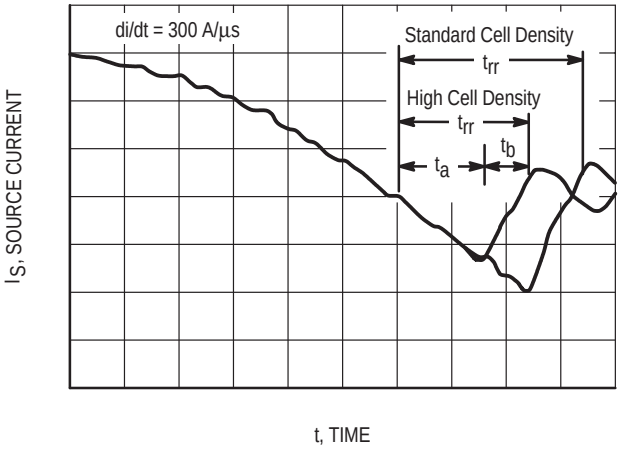


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

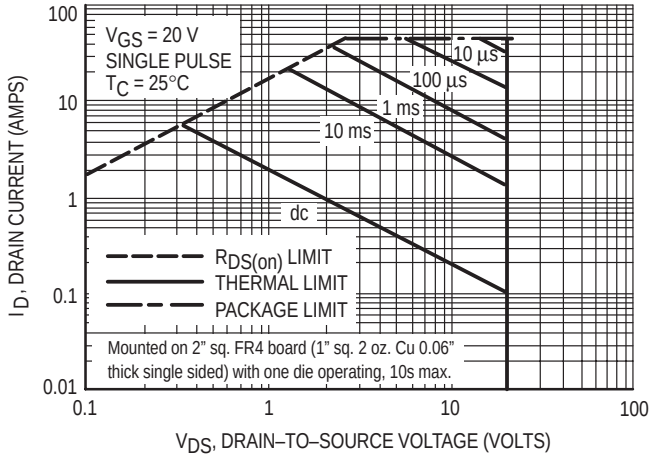


Figure 12. Maximum Rated Forward Biased Safe Operating Area

TYPICAL ELECTRICAL CHARACTERISTICS

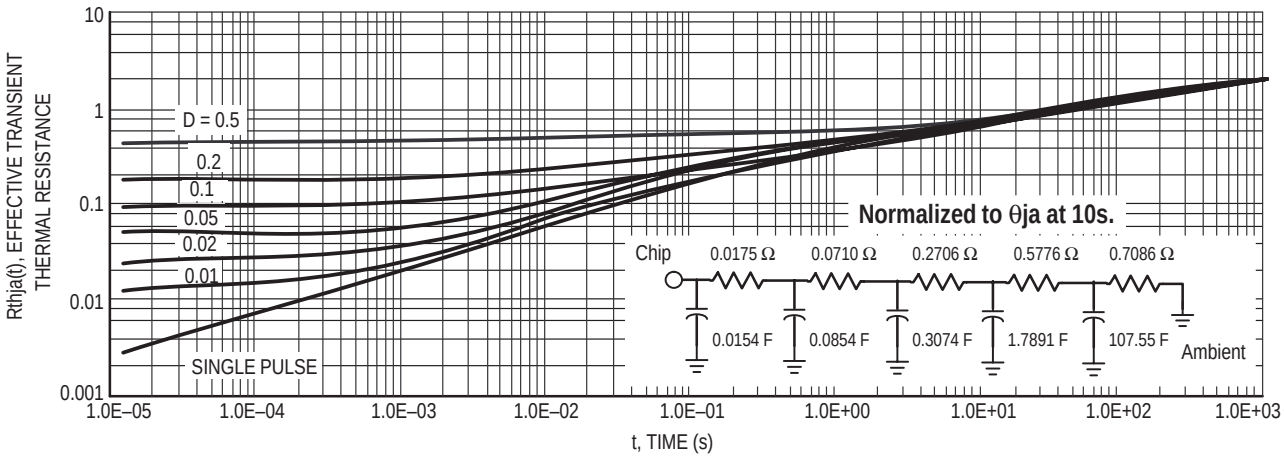


Figure 13. Thermal Response

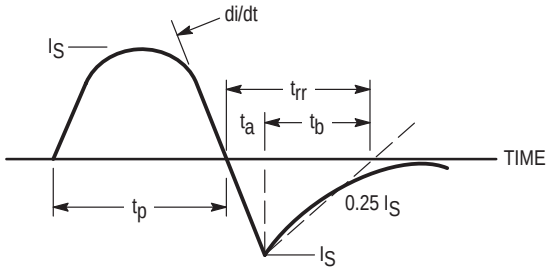


Figure 14. Diode Reverse Recovery Waveform

Product Preview

Medium Power Surface Mount Products

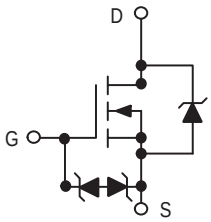
TMOS Dual N-Channel with Monolithic Zener ESD Protected Gate

MMDF4N01Z

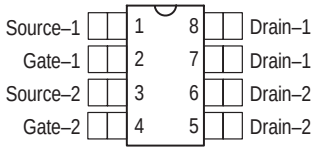
Motorola Preferred Device

DUAL TMOS
POWER MOSFET
4.0 AMPERES
20 VOLTS
$R_{DS(on)}$ = 0.045 OHM

EZFETs™ are an advanced series of power MOSFETs which utilize Motorola's High Cell Density TMOS process and contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.



CASE 751–05, Style 11
SO–8



- Zener Protected Gates Provide Electrostatic Discharge Protection
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 8.0	Vdc
Drain Current — Continuous @ T_A = 25°C (1) — Continuous @ T_A = 70°C (1) — Pulsed Drain Current (3)	I_D I_D I_{DM}	4.5 4.0 23	Adc Apk
Total Power Dissipation @ T_A = 25°C (1) Linear Derating Factor (1)	P_D	2.0 16	Watts mW/°C
Total Power Dissipation @ T_A = 25°C (2) Linear Derating Factor (2)	P_D	1.39 11.11	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C

THERMAL RESISTANCE

Rating	Symbol	Typ.	Max.	Unit
Thermal Resistance — Junction to Ambient, PCB Mount (1) — Junction to Ambient, PCB Mount (2)	$R_{\theta JA}$ $R_{\theta JA}$	— —	62.5 90	°C/W

(1) When mounted on 1 inch square FR–4 or G–10 board (V_{GS} = 4.5 V, @ 10 Seconds)
(2) When mounted on minimum recommended FR–4 or G–10 board (V_{GS} = 4.5 V, @ Steady State)
(3) Repetitive rating; pulse width limited by maximum junction temperature.

DEVICE MARKING **ORDERING INFORMATION**

D4N01Z	Device	Reel Size	Tape Width	Quantity
	MMDF4N01ZR2	13″	12 mm embossed tape	2500 units

This document contains information on a new product. Specifications and information are subject to change without notice.
Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (3) (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	 20 —	 — 15	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)	I_{DSS}	 — —	 — —	 2.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0)	I_{GSS}	—	—	5.0	
ON CHARACTERISTICS(1)					
Gate Threshold Voltage (Cpk ≥ 2.0) (3) (V_{DS} = V_{GS}, I_D = 0.25 mAdc) Threshold Temperature Coefficient (Negative)	$V_{GS(th)}$	 0.7 —	 0.83 3.0	 1.1 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (3) (V_{GS} = 4.5 Vdc, I_D = 4.0 Adc) (V_{GS} = 2.7 Vdc, I_D = 2.0 Adc)	$R_{DS(on)}$	 — —	 35 45	 45 55	mΩ
Forward Transconductance (V_{DS} = 2.5 Vdc, I_D = 2.0 Adc)	g_{FS}	 5.0	 8.5	 —	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	—	450	630	pF
Output Capacitance	C_{oss}	—	160	225	
Transfer Capacitance	C_{rss}	—	330	460	
SWITCHING CHARACTERISTICS(2)					
Turn–On Delay Time	$t_{d(on)}$	—	28	40	ns
Rise Time	t_r	—	128	180	
Turn–Off Delay Time	$t_{d(off)}$	—	194	270	
Fall Time	t_f	—	195	270	
Turn–On Delay Time	$t_{d(on)}$	—	50	70	ns
Rise Time	t_r	—	340	475	
Turn–Off Delay Time	$t_{d(off)}$	—	106	150	
Fall Time	t_f	—	197	275	
Gate Charge (see figure 8)	Q_T	—	10.5	15	nC
	Q_1	—	0.8	—	
	Q_2	—	4.4	—	
	Q_3	—	3.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage(1) (I_S = 4.0 Adc, V_{GS} = 0 Vdc) (I_S = 4.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 0.84 0.65	 1.2 —	Vdc
Reverse Recovery Time	t_{rr}	—	250	—	ns
	t_a	—	88	—	
	t_b	—	162	—	
Reverse Recovery Storage Charge	Q_{RR}	—	1.0	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

Medium Power Field Effect Transistor

N–Channel Enhancement Mode
Silicon Gate TMOS E–FET™
SOT–223 for Surface Mount

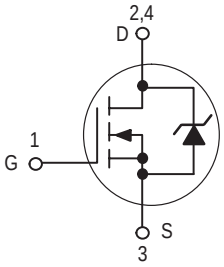
MMFT1N10E

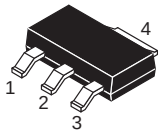
Motorola Preferred Device

MEDIUM POWER
TMOS FET
1 AMP
100 VOLTS
$R_{DS(on)}$ = 0.25 OHM

This advanced E–FET is a TMOS Medium Power MOSFET designed to withstand high energy in the avalanche and commutation modes. This new energy efficient device also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, dc–dc converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients. The device is housed in the SOT–223 package which is designed for medium power surface mount applications.

- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ — 0.25 Ω max
- The SOT–223 Package can be Soldered Using Wave or Reflow. The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die
- Available in 12 mm Tape and Reel
  Use MMFT1N10ET1 to order the 7 inch/1000 unit reel.
  Use MMFT1N10ET3 to order the 13 inch/4000 unit reel.





CASE 318E–04, STYLE 3
TO–261AA

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DS}	100	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±20	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	1 4	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D(1)	0.8 6.4	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 60 V, V_{GS} = 10 V, Peak I_L = 1 A, L = 0.2 mH, R_G = 25 Ω)	E_{AS}	168	mJ

DEVICE MARKING

1N10

THERMAL CHARACTERISTICS

Thermal Resistance — Junction–to–Ambient (surface mounted)	$R_{\theta JA}$	156	°C/W
Maximum Temperature for Soldering Purposes, Time in Solder Bath	T_L	260 10	°C Sec

(1) Power rating when mounted on FR–4 glass epoxy printed circuit board using recommended footprint.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage, (V_{GS} = 0, I_D = 250 μA)		$V_{(BR)DSS}$	100	—	—	Vdc
Zero Gate Voltage Drain Current, (V_{DS} = 100 V, V_{GS} = 0)		I_{DSS}	—	—	10	μAdc
Gate–Body Leakage Current, (V_{GS} = 20 V, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage, (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	—	4.5	Vdc
Static Drain–to–Source On–Resistance, (V_{GS} = 10 V, I_D = 0.5 A)		$R_{DS(on)}$	—	—	0.25	Ohms
Drain–to–Source On–Voltage, (V_{GS} = 10 V, I_D = 1 A)		$V_{DS(on)}$	—	—	0.33	Vdc
Forward Transconductance, (V_{DS} = 10 V, I_D = 0.5 A)		g_{FS}	—	2.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	410	—	pF
Output Capacitance		C_{oss}	—	145	—	
Reverse Transfer Capacitance		C_{rss}	—	55	—	
SWITCHING CHARACTERISTICS						
Turn–On Delay Time	(V_{DD} = 25 V, I_D = 0.5 A V_{GS} = 10 V, R_G = 50 ohms, R_{GS} = 25 ohms)	$t_{d(on)}$	—	15	—	ns
Rise Time		t_r	—	15	—	
Turn–Off Delay Time		$t_{d(off)}$	—	30	—	
Fall Time		t_f	—	32	—	
Total Gate Charge	(V_{DS} = 80 V, I_D = 1 A, V_{GS} = 10 Vdc) See Figures 15 and 16	Q_g	—	7	—	nC
Gate–Source Charge		Q_{gs}	—	1.3	—	
Gate–Drain Charge		Q_{gd}	—	3.2	—	
SOURCE DRAIN DIODE CHARACTERISTICS(1)						
Forward On–Voltage	I_S = 1 A, V_{GS} = 0	V_{SD}	—	0.8	—	Vdc
Forward Turn–On Time	I_S = 1 A, V_{GS} = 0, dI_S/dt = 400 A/μs, V_R = 50 V	t_{on}	Limited by stray inductance			
Reverse Recovery Time		t_{rr}	—	90	—	ns

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

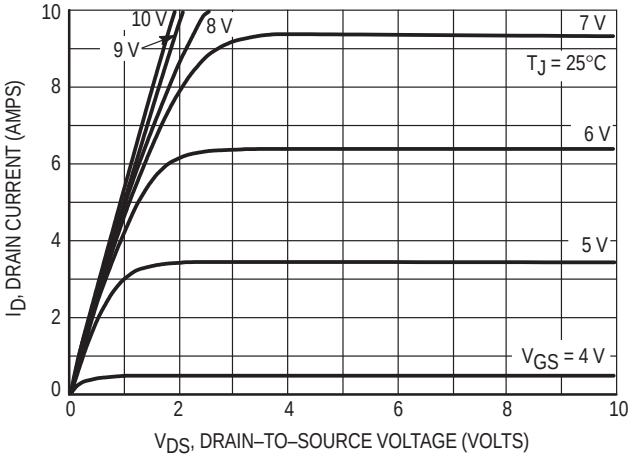
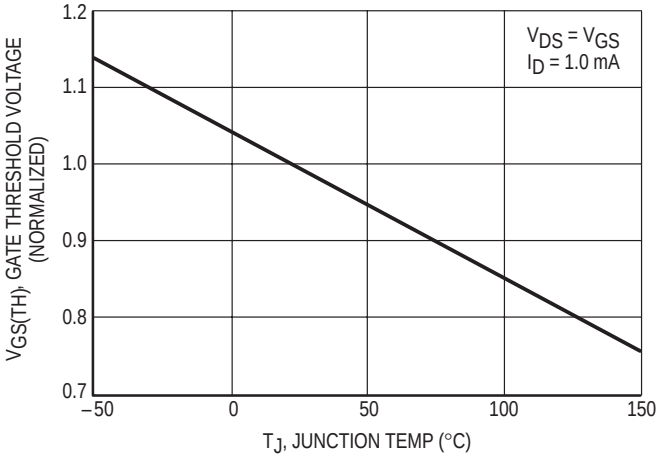


Figure 1. On Region Characteristics



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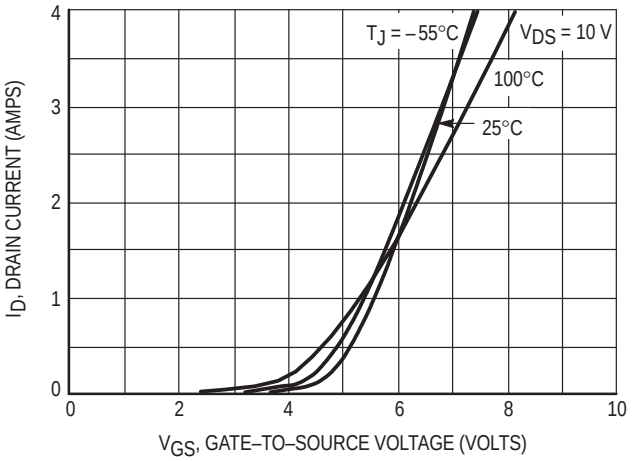

Figure 3. Transfer Characteristics

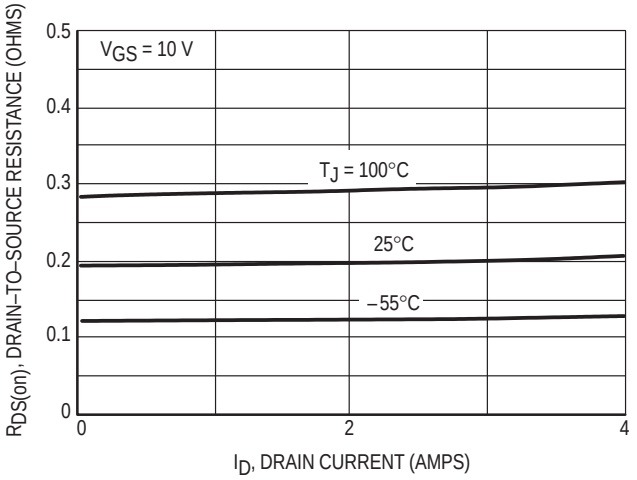

Figure 4. On–Resistance versus Drain Current

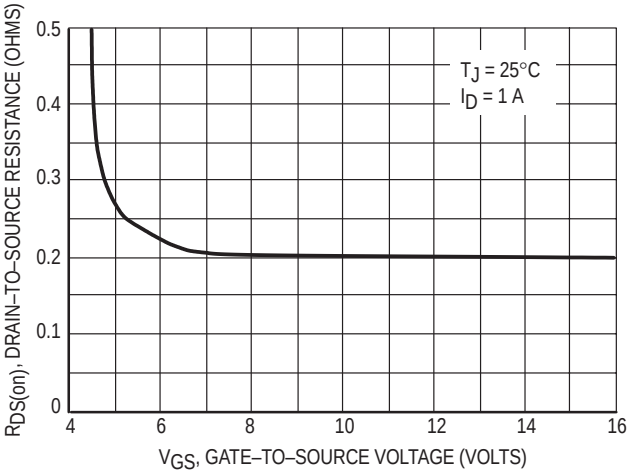

Figure 5. On–Resistance versus Gate–to–Source Voltage

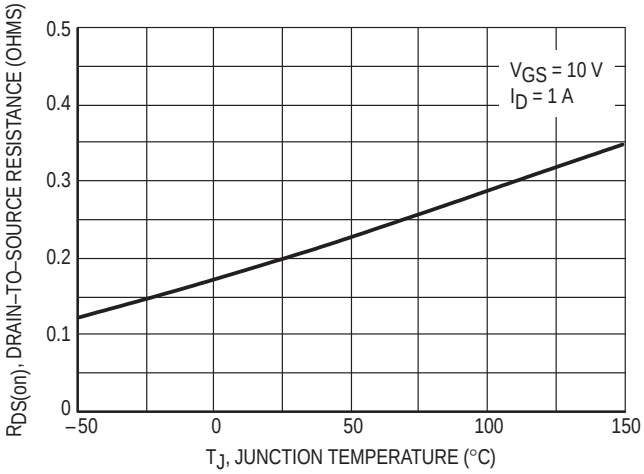

Figure 6. On–Resistance versus Junction Temperature

FORWARD BIASED SAFE OPERATING AREA

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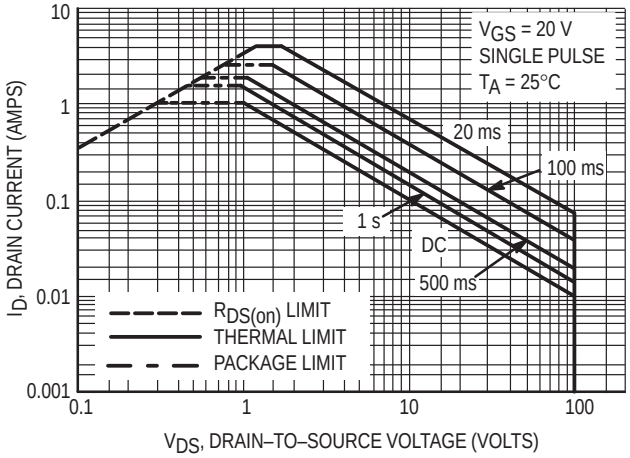

Figure 7. Maximum Rated Forward Biased Safe Operating Area

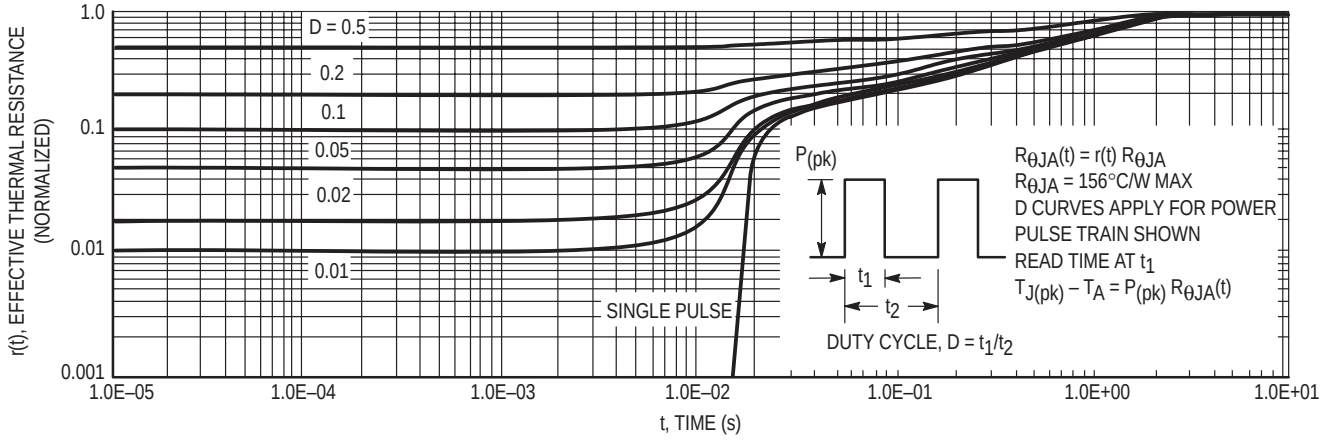

Figure 8. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

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$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source–drain diode current just prior to the onset of commutation.

V_R is specified at 80% rated BV_{DSS} to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola’s test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

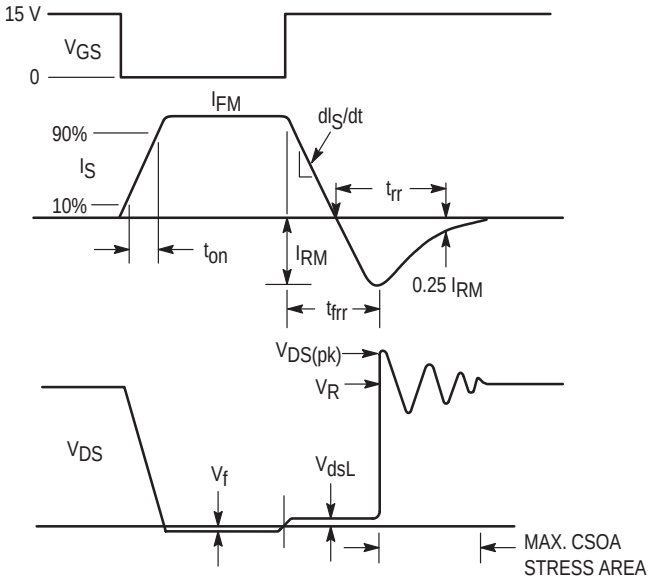


Figure 9. Commutating Waveforms

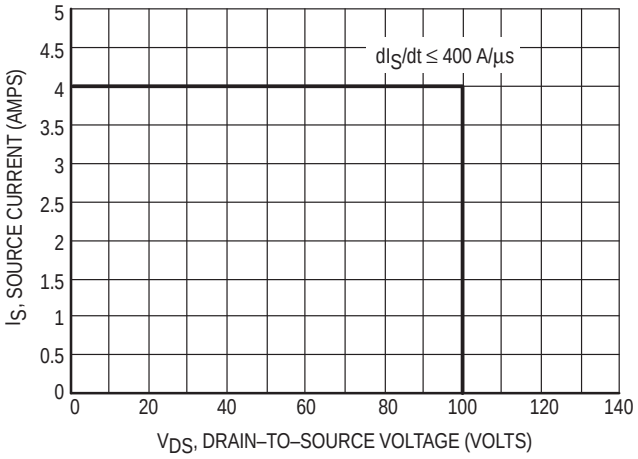


Figure 10. Commutating Safe Operating Area (CSOA)

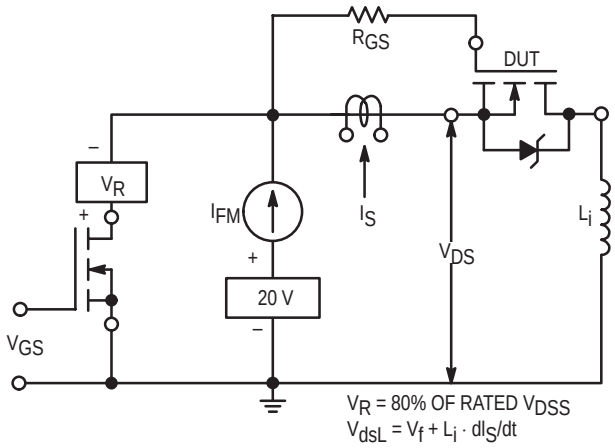


Figure 11. Commutating Safe Operating Area Test Circuit

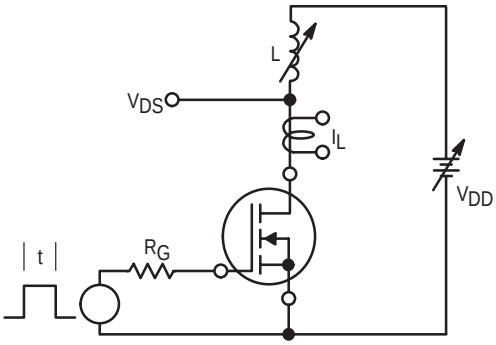


Figure 12. Unclamped Inductive Switching Test Circuit

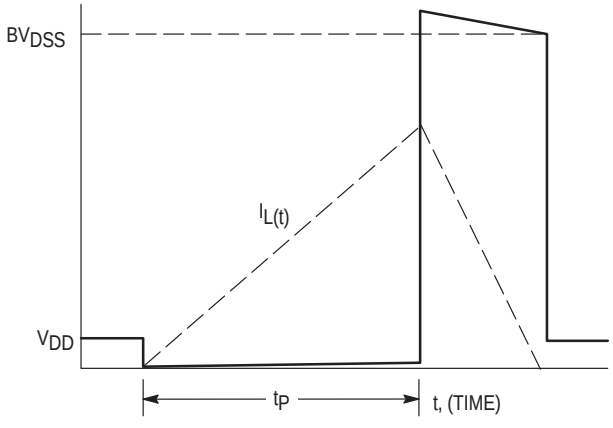


Figure 13. Unclamped Inductive Switching Waveforms

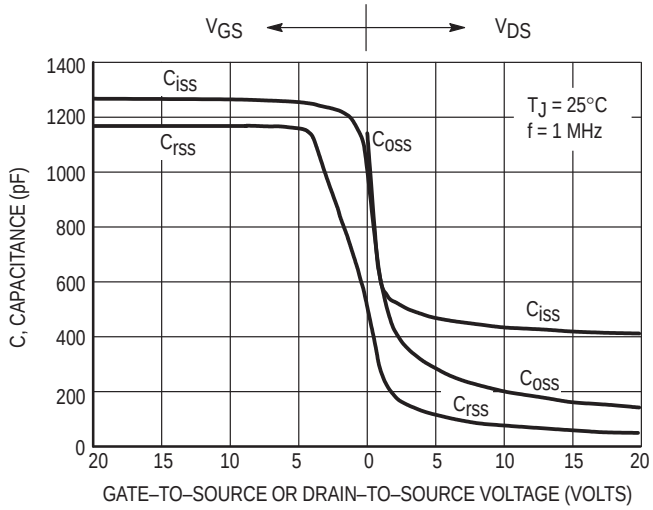


Figure 14. Capacitance Variation With Voltage

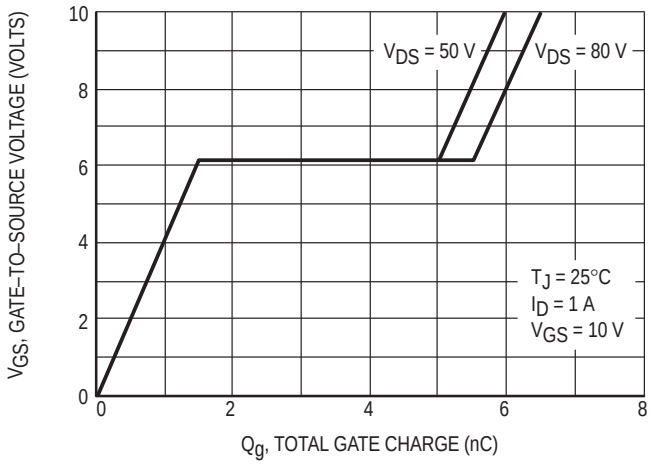
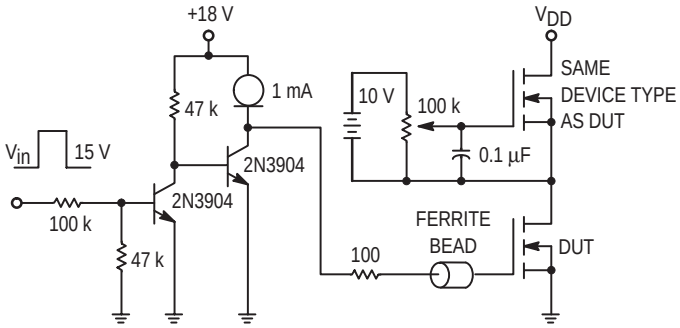


Figure 15. Gate Charge versus Gate–To–Source Voltage



Vin = 15 Vpk; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%.

Figure 16. Gate Charge Test Circuit

Medium Power Field Effect Transistor

N–Channel Enhancement Mode
Silicon Gate TMOS E–FET™
SOT–223 for Surface Mount

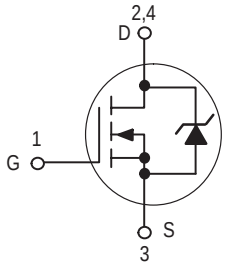
MMFT2N02EL

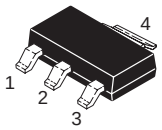
Motorola Preferred Device

MEDIUM POWER
LOGIC LEVEL TMOS FET
1.6 AMP
20 VOLTS
$R_{DS(on)}$ = 0.15 OHM

This advanced E–FET is a TMOS Medium Power MOSFET designed to withstand high energy in the avalanche and commutation modes. This device is also designed with a low threshold voltage so it is fully enhanced with 5 Volts. This new energy efficient device also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, dc–dc converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients. The device is housed in the SOT–223 package which is designed for medium power surface mount applications.

- Silicon Gate for Fast Switching Speeds
- Low Drive Requirement to Interface Power Loads to Logic Level ICs, $V_{GS(th)}$ = 2 Volts Max
- Low $R_{DS(on)}$ — 0.15 Ω max
- The SOT–223 Package can be Soldered Using Wave or Reflow. The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die
- Available in 12 mm Tape and Reel
  Use MMFT2N02ELT1 to order the 7 inch/1000 unit reel.
  Use MMFT2N02ELT3 to order the 13 inch/4000 unit reel.





CASE 318E–04, STYLE 3
TO–261AA

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DS}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±15	
Drain Current — Continuous — Pulsed	I_D I_{DM}	1.6 6.4	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D(1)	0.8 6.4	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 10 V, V_{GS} = 5 V, Peak I_L = 2 A, L = 0.2 mH, R_G = 25 Ω)	E_{AS}	66	mJ

DEVICE MARKING

2N02L

THERMAL CHARACTERISTICS

Thermal Resistance — Junction–to–Ambient (surface mounted)	$R_{\theta JA}$	156	°C/W
Maximum Temperature for Soldering Purposes, Time in Solder Bath	T_L	260 10	°C Sec

(1) Power rating when mounted on FR–4 glass epoxy printed circuit board using recommended footprint.

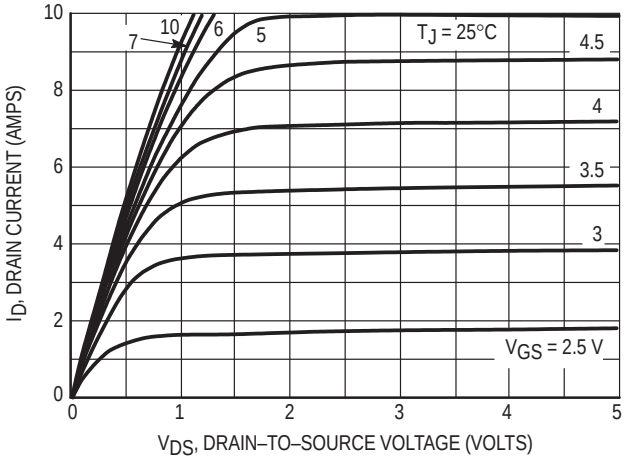
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage, (V_{GS} = 0, I_D = 250 μA)		$V_{(BR)DSS}$	20	—	—	Vdc
Zero Gate Voltage Drain Current, (V_{DS} = 20 V, V_{GS} = 0)		I_{DSS}	—	—	10	μAdc
Gate–Body Leakage Current, (V_{GS} = 15 V, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage, (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	1	—	2	Vdc
Static Drain–to–Source On–Resistance, (V_{GS} = 5 V, I_D = 0.8 A)		$R_{DS(on)}$	—	—	0.15	Ohms
Drain–to–Source On–Voltage, (V_{GS} = 5 V, I_D = 1.6 A)		$V_{DS(on)}$	—	—	0.32	Vdc
Forward Transconductance, (V_{DS} = 10 V, I_D = 0.8 A)		g_{FS}	—	2.6	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 15 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	580	—	pF
Output Capacitance		C_{oss}	—	430	—	
Reverse Transfer Capacitance		C_{rss}	—	250	—	
SWITCHING CHARACTERISTICS						
Turn–On Delay Time	(V_{DD} = 15 V, I_D = 1.6 A V_{GS} = 5 V, R_G = 50 ohms, R_{GS} = 25 ohms)	$t_{d(on)}$	—	16	—	ns
Rise Time		t_r	—	73	—	
Turn–Off Delay Time		$t_{d(off)}$	—	77	—	
Fall Time		t_f	—	107	—	
Total Gate Charge	(V_{DS} = 16 V, I_D = 1.6 A, V_{GS} = 5 Vdc) See Figures 15 and 16	Q_g	—	20	—	nC
Gate–Source Charge		Q_{gs}	—	1.7	—	
Gate–Drain Charge		Q_{gd}	—	6	—	
SOURCE DRAIN DIODE CHARACTERISTICS(1)						
Forward On–Voltage	I_S = 1.6 A, V_{GS} = 0	V_{SD}	—	0.9	—	Vdc
Forward Turn–On Time	I_S = 1.6 A, V_{GS} = 0, dI_S/dt = 400 A/μs, V_R = 16 V	t_{on}	Limited by stray inductance			
Reverse Recovery Time		t_{rr}	—	55	—	ns

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%



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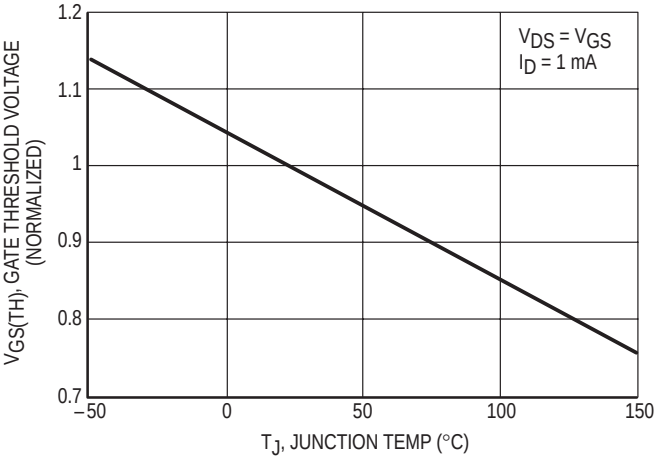

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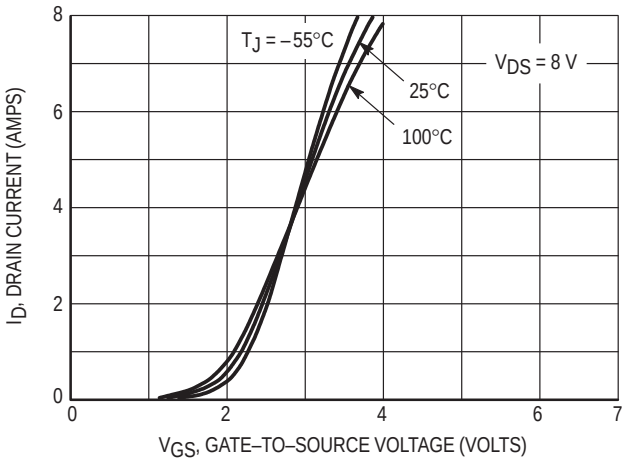

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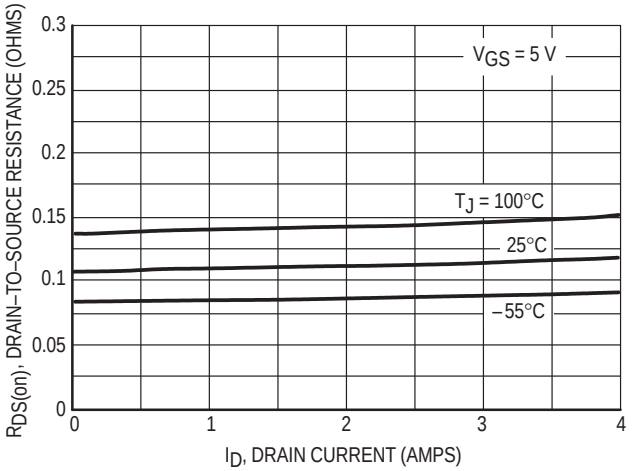

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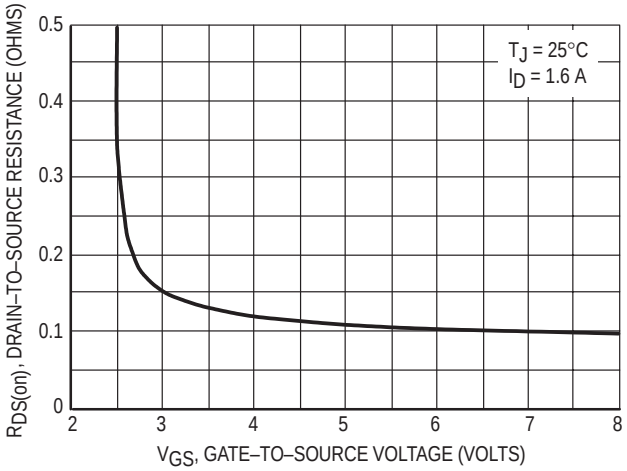

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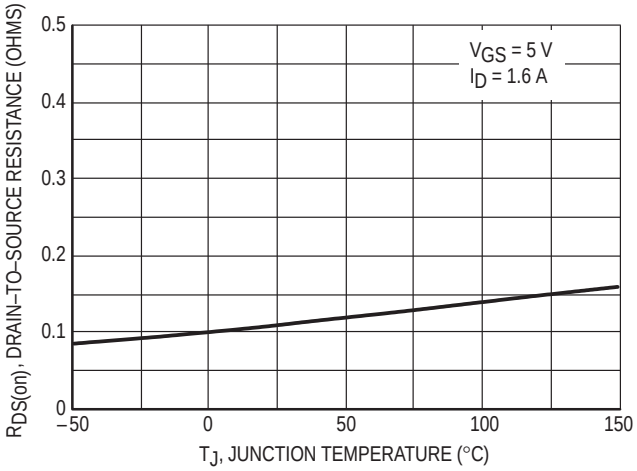

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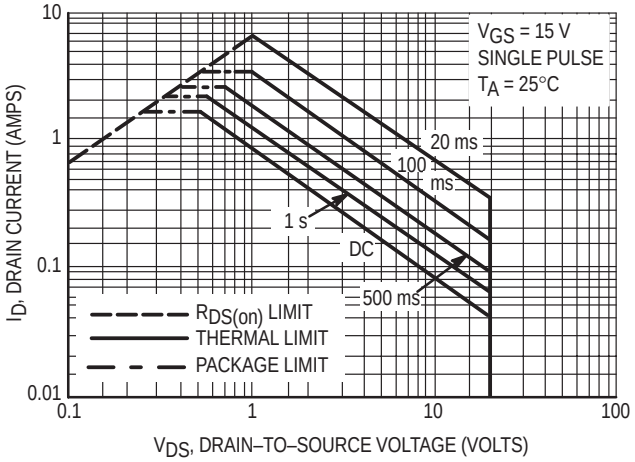
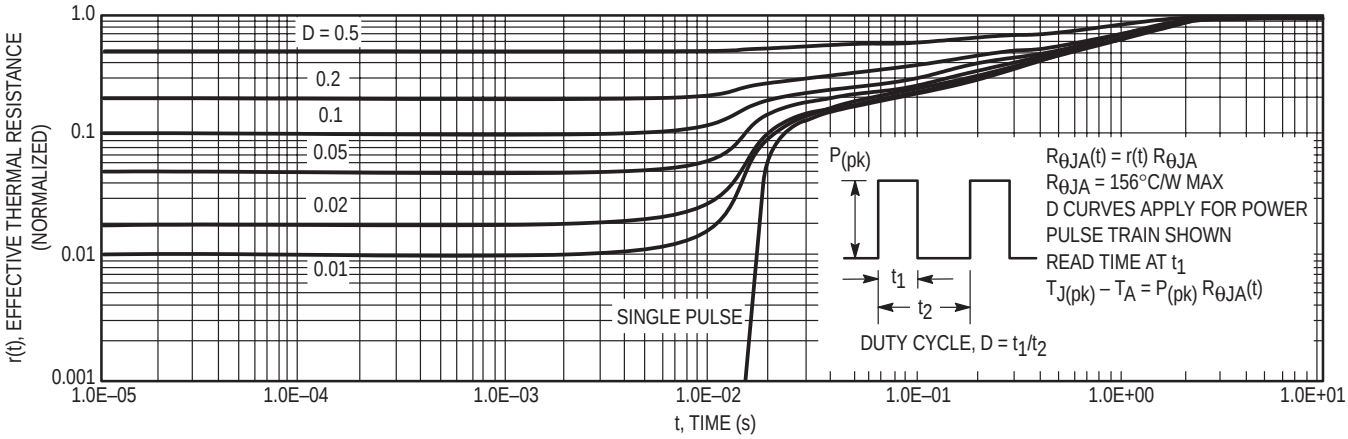


Figure 7. Maximum Rated Forward Biased Safe Operating Area



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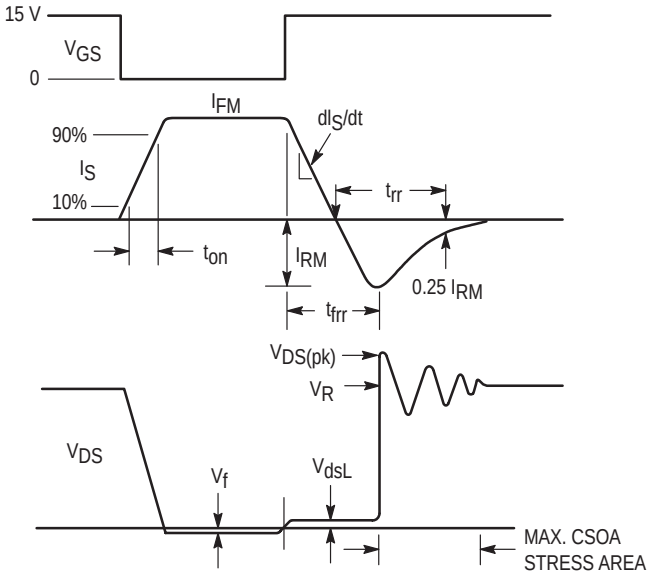

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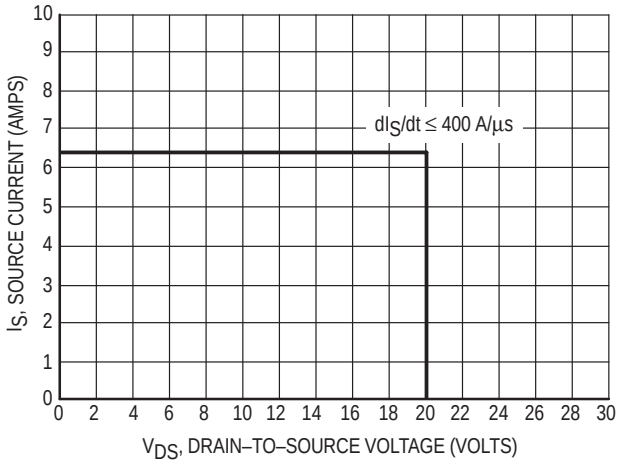

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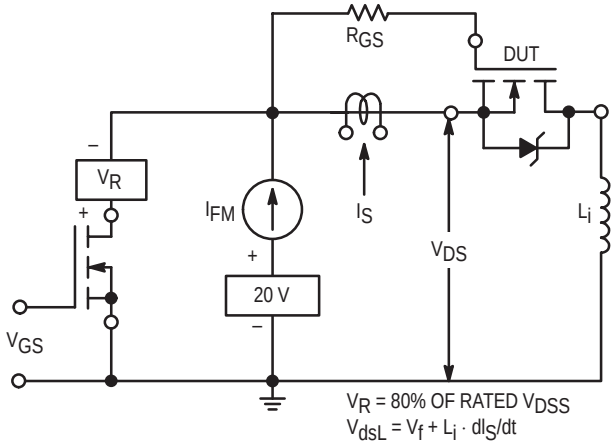

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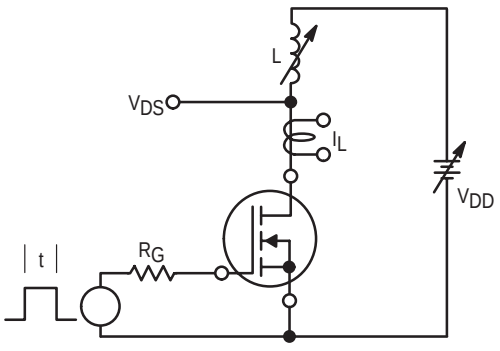


Figure 12. Unclamped Inductive Switching Test Circuit

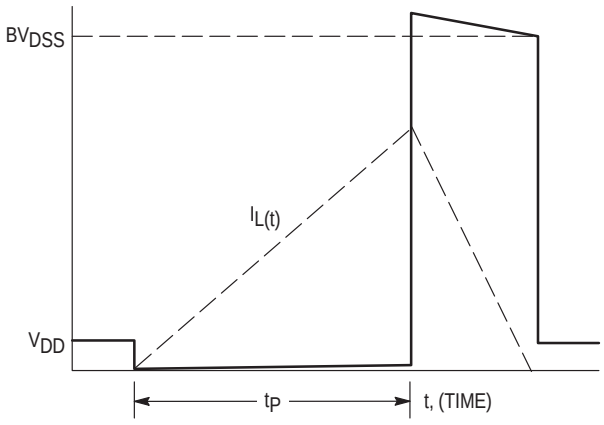


Figure 13. Unclamped Inductive Switching Waveforms

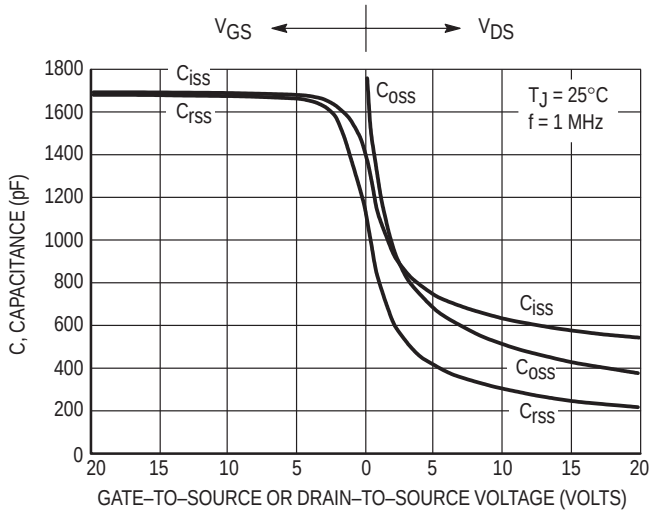


Figure 14. Capacitance Variation With Voltage

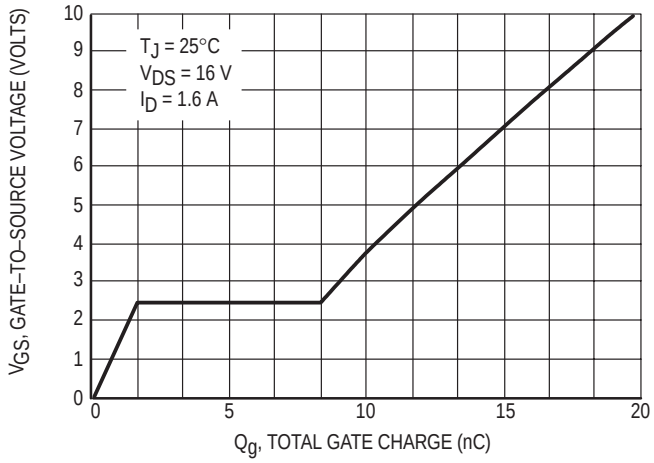
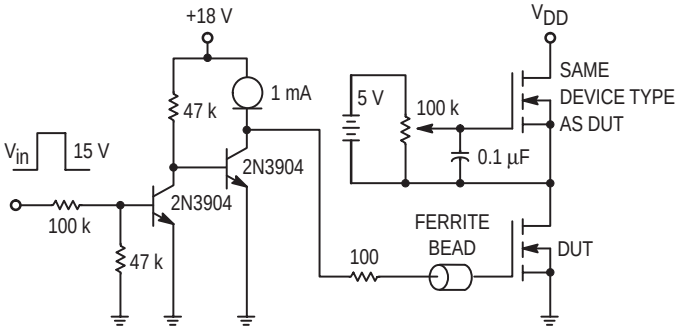


Figure 15. Gate Charge versus Gate–To–Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%.

Figure 16. Gate Charge Test Circuit

Medium Power Field Effect Transistor

P–Channel Enhancement Mode
Silicon Gate TMOS E–FET™
SOT–223 for Surface Mount

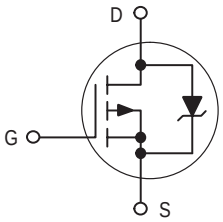
MMFT2955E

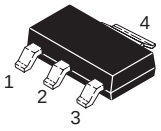
Motorola Preferred Device

TMOS MEDIUM POWER FET
1.2 AMP
60 VOLTS
$R_{DS(on)}$ = 0.3 OHM

This advanced E–FET is a TMOS medium power MOSFET designed to withstand high energy in the avalanche and commutation modes. This new energy efficient device also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients. The device is housed in the SOT–223 package which is designed for medium power surface mount applications.

- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ — 0.3 Ω max
- The SOT–223 Package can be Soldered Using Wave or Reflow. The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die
- Available in 12 mm Tape and Reel
  Use MMFT2955ET1 to order the 7 inch/1000 unit reel.
  Use MMFT2955ET3 to order the 13 inch/4000 unit reel.





CASE 318E–04, STYLE 3
TO–261AA

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DS}	60	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±15	
Drain Current — Continuous — Pulsed	I_D I_{DM}	1.2 4.8	Adc
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D(1)	0.8 6.4	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 V, V_{GS} = 10 V, Peak I_L = 1.2 A, L = 0.2 mH, R_G = 25 Ω)	E_{AS}	108	mJ

DEVICE MARKING

2955

THERMAL CHARACTERISTICS

Thermal Resistance — Junction–to–Ambient (surface mounted)	$R_{\theta JA}$	156	°C/W
Maximum Temperature for Soldering Purposes, Time in Solder Bath	T_L	260 10	°C Sec

(1) Power rating when mounted on FR–4 glass epoxy printed circuit board using recommended footprint.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage, (V_{GS} = 0, I_D = 250 μA)		$V_{(BR)DSS}$	60	—	—	Vdc
Zero Gate Voltage Drain Current, (V_{DS} = 60 V, V_{GS} = 0)		I_{DSS}	—	—	10	μAdc
Gate–Body Leakage Current, (V_{GS} = 15 V, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS						
Gate Threshold Voltage, (V_{DS} = V_{GS}, I_D = 1 mA)		$V_{GS(th)}$	2	—	4.5	Vdc
Static Drain–to–Source On–Resistance, (V_{GS} = 10 V, I_D = 0.6 A)		$R_{DS(on)}$	—	—	0.3	Ohms
Drain–to–Source On–Voltage, (V_{GS} = 10 V, I_D = 1.2 A)		$V_{DS(on)}$	—	—	0.48	Vdc
Forward Transconductance, (V_{DS} = 15 V, I_D = 0.6 A)		g_{FS}	—	7.5	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz)	C_{iss}	—	460	—	pF
Output Capacitance		C_{oss}	—	210	—	
Reverse Transfer Capacitance		C_{rss}	—	84	—	
SWITCHING CHARACTERISTICS						
Turn–On Delay Time	(V_{DD} = 25 V, I_D = 1.6 A V_{GS} = 10 V, R_G = 50 ohms, R_{GS} = 25 ohms)	$t_{d(on)}$	—	18	—	ns
Rise Time		t_r	—	29	—	
Turn–Off Delay Time		$t_{d(off)}$	—	44	—	
Fall Time		t_f	—	32	—	
Total Gate Charge	(V_{DS} = 48 V, I_D = 1.2 A, V_{GS} = 10 Vdc) See Figures 15 and 16	Q_g	—	18	—	nC
Gate–Source Charge		Q_{gs}	—	2.8	—	
Gate–Drain Charge		Q_{gd}	—	7.5	—	
SOURCE DRAIN DIODE CHARACTERISTICS(1)						
Forward On–Voltage	I_S = 1.2 A, V_{GS} = 0	V_{SD}	—	1	—	Vdc
Forward Turn–On Time	I_S = 1.2 A, V_{GS} = 0, dI_S/dt = 400 A/μs, V_R = 30 V	t_{on}	Limited by stray inductance			
Reverse Recovery Time		t_{rr}	—	90	—	ns

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

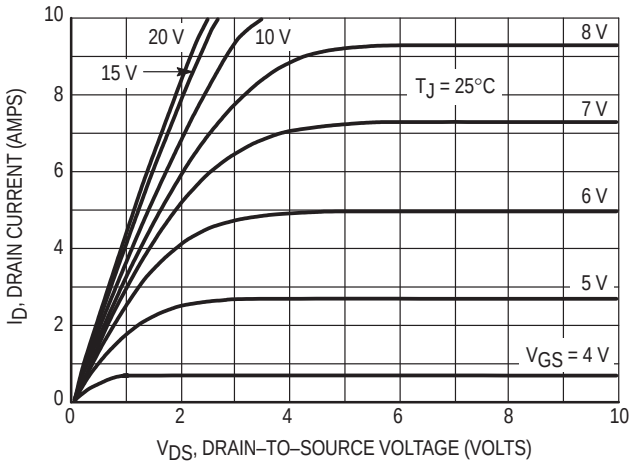


Figure 1. On Region Characteristics

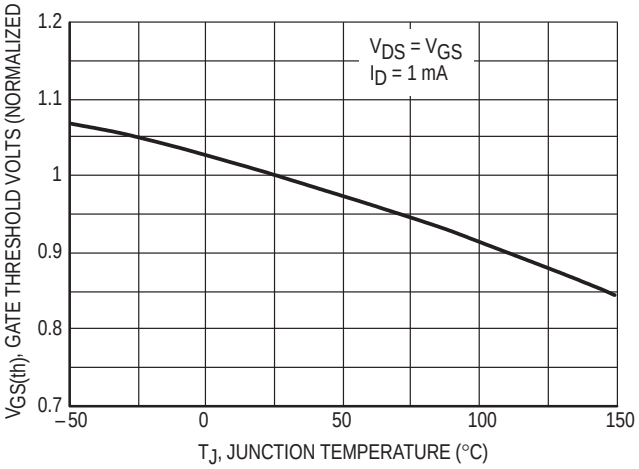


Figure 2. Gate–Threshold Voltage Variation With Temperature

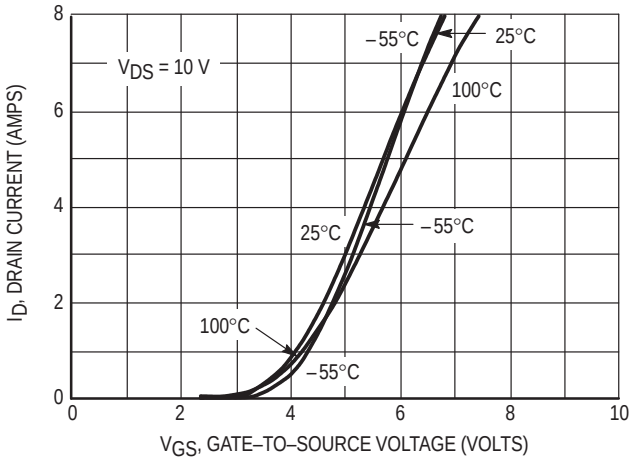


Figure 3. Transfer Characteristics

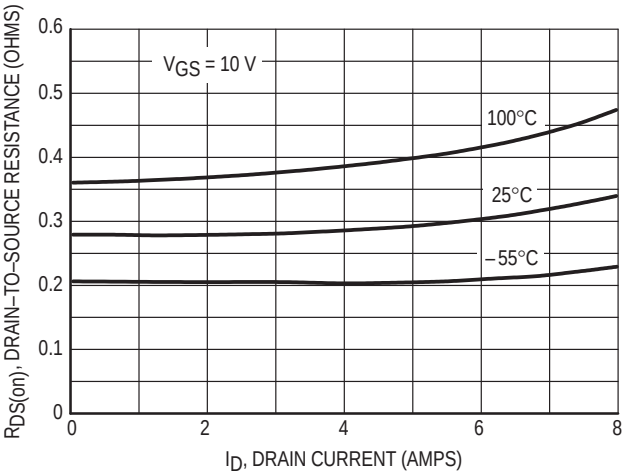


Figure 4. On–Resistance versus Drain Current

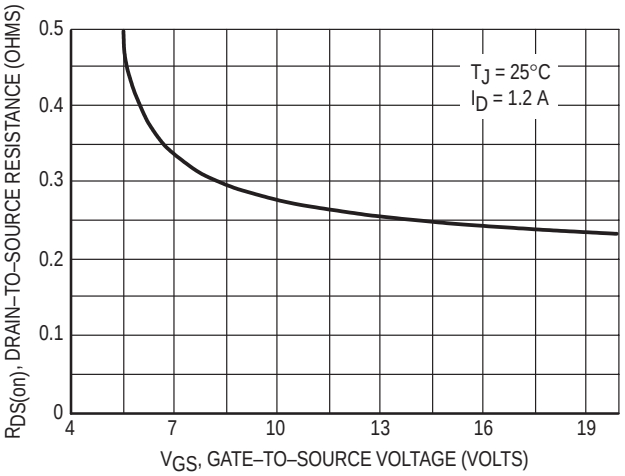


Figure 5. On–Resistance versus Gate–to–Source Voltage

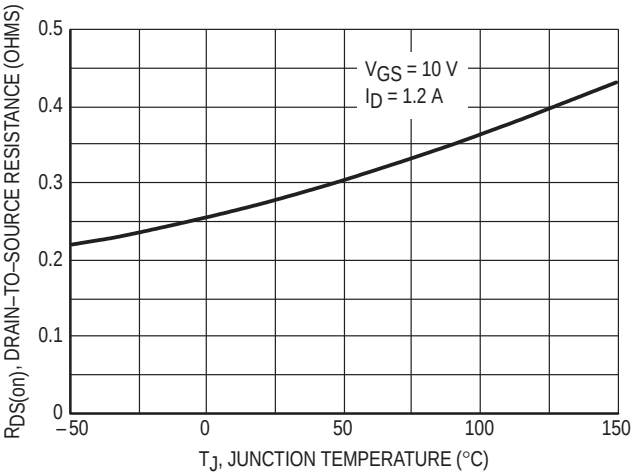


Figure 6. On–Resistance versus Junction Temperature

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a ambient temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various ambient temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, BVDSS. The switching SOA is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

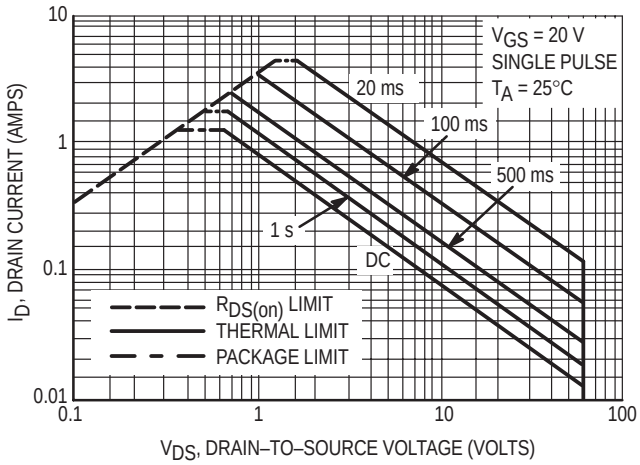


Figure 7. Maximum Rated Forward Biased Safe Operating Area

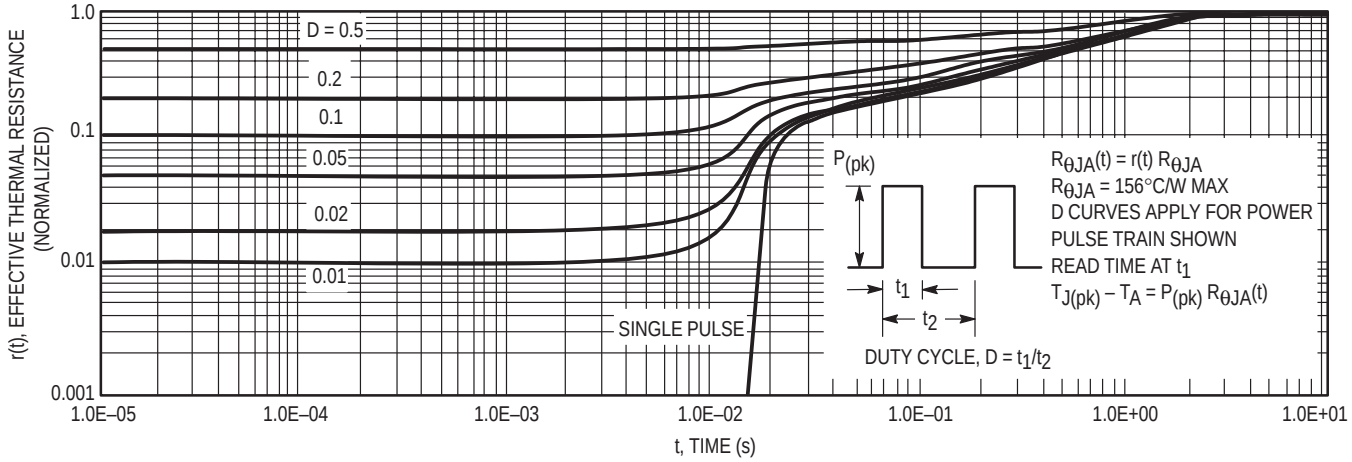


Figure 8. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 10 defines the limits of safe operation for commutated source–drain current versus re–applied drain voltage when the source–drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 9 are present. Full or half–bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source–drain diode current just prior to the onset of commutation.

V_R is specified at 80% rated BV_{DSS} to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola’s test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

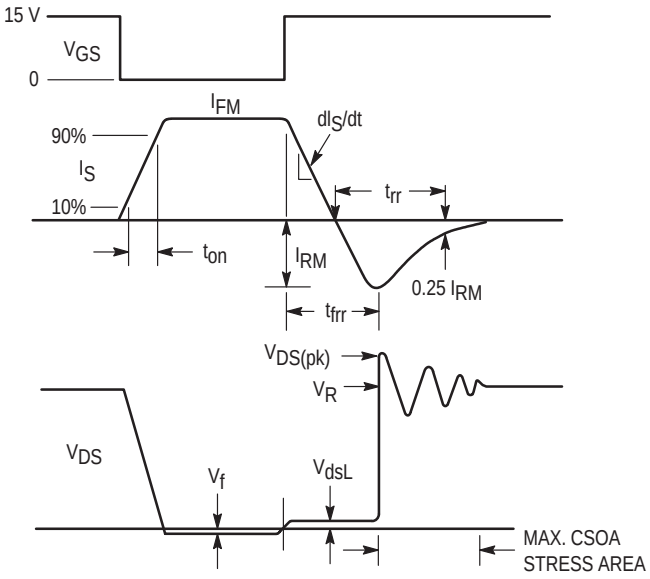


Figure 9. Commutating Waveforms

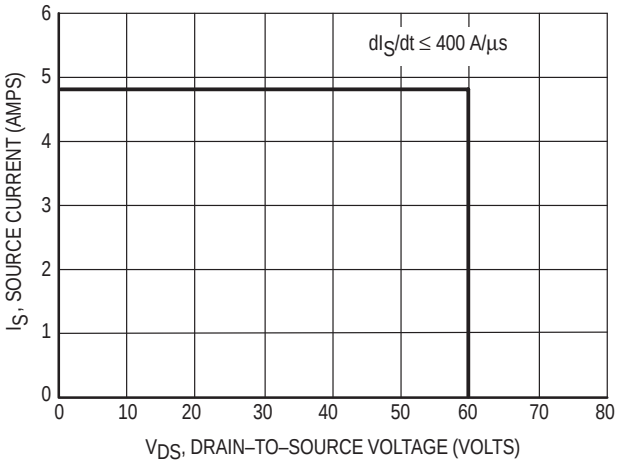


Figure 10. Commutating Safe Operating Area (CSOA)

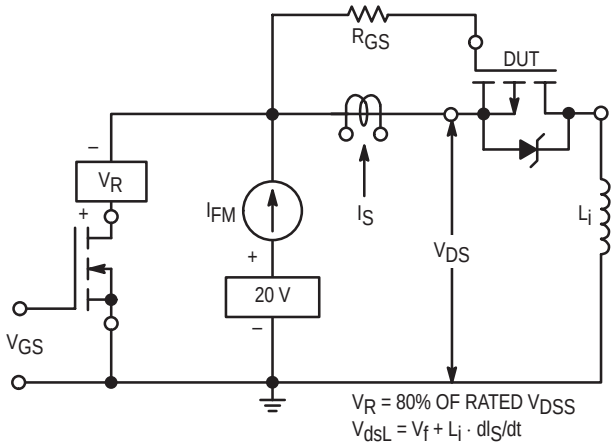


Figure 11. Commutating Safe Operating Area Test Circuit

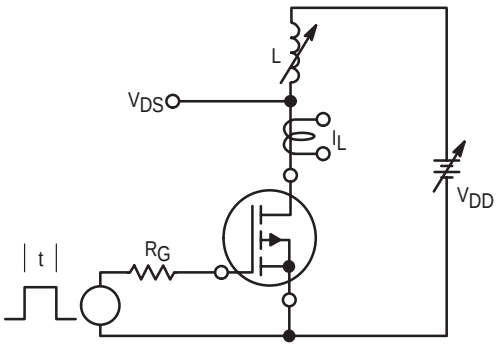


Figure 12. Unclamped Inductive Switching Test Circuit

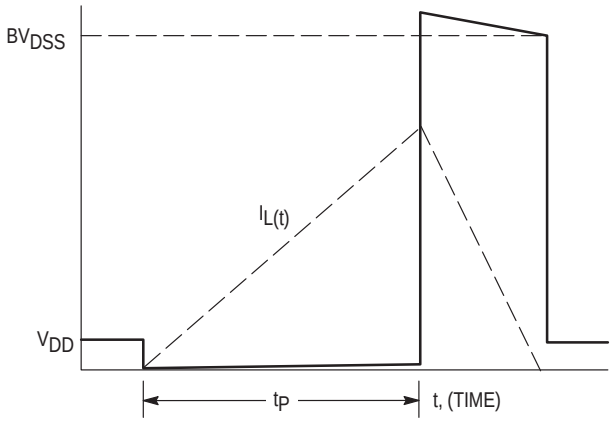


Figure 13. Unclamped Inductive Switching Waveforms

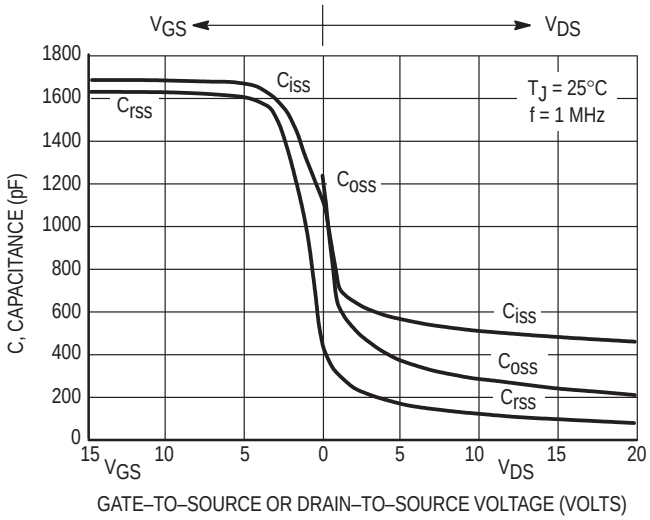


Figure 14. Capacitance Variation with Voltage

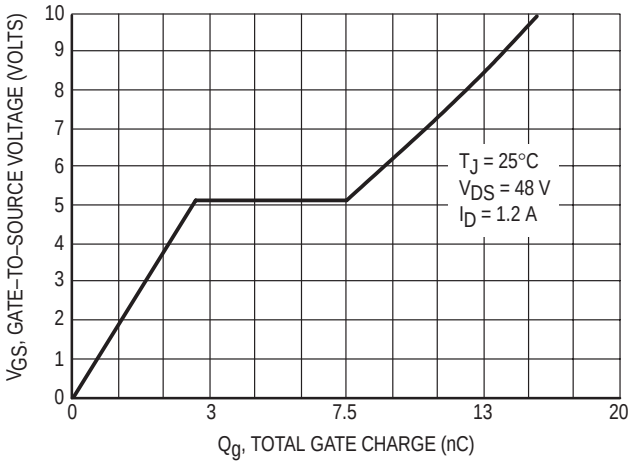
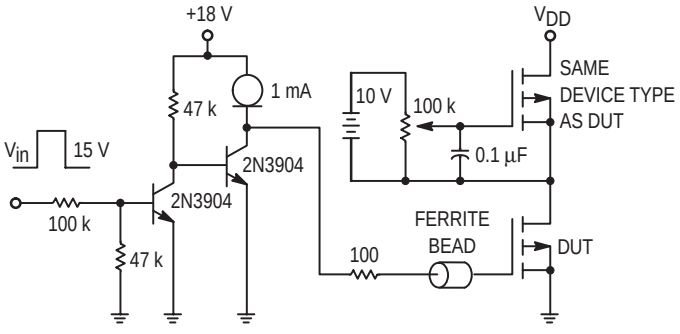


Figure 15. Gate Charge versus Gate–To–Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%.

Figure 16. Gate Charge Test Circuit

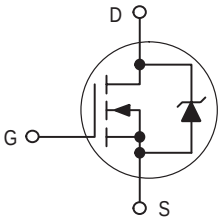
Product Preview

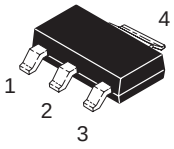
TMOS V™
SOT-223 for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

MMFT3055V

TMOS POWER FET
1.7 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.130 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 318E–04, Style 3
TO–261AA

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Available in 12 mm Tape & Reel
  Use MMFT3055VT1 to order the 7 inch/1000 unit reel
  Use MMFT3055VT3 to order the 13 inch/4000 unit reel

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage – Continuous – Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current – Continuous – Continuous @ 100°C – Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	1.7 1.4 6.0	Adc Apk
Total PD @ T_A = 25°C mounted on 1” sq. Drain pad on FR–4 bd material Total PD @ T_A = 25°C mounted on 0.70” sq. Drain pad on FR–4 bd material Total PD @ T_A = 25°C mounted on min. Drain pad on FR–4 bd material Derate above 25°C	P_D	2.0 1.7 0.9 6.3	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 3.4 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	 58	mJ
Thermal Resistance – Junction to Ambient on 1” sq. Drain pad on FR–4 bd material – Junction to Ambient on 0.70” sq. Drain pad on FR–4 bd material – Junction to Ambient on min. Drain pad on FR–4 bd material	 $R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JA}$	 70 88 159	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.
E–FET and TMOS V are trademarks of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	63	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.8	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	5.6	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.85 Adc)		$R_{DS(on)}$	—	0.115	0.13	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.7 Adc)		$V_{DS(on)}$	—	—	0.27	Vdc
(V_{GS} = 10 Vdc, I_D = 0.85 Adc, T_J = 150°C)			—	—	0.25	
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 1.7 Adc)		g_{FS}	1.0	2.7	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	360	500	pF
Output Capacitance		C_{oss}	—	110	150	
Transfer Capacitance		C_{rss}	—	25	50	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 1.7 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.0	20	ns
Rise Time		t_r	—	9.0	20	
Turn–Off Delay Time		$t_{d(off)}$	—	32	60	
Fall Time		t_f	—	18	40	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 1.7 Adc, V_{GS} = 10 Vdc)	Q_T	—	13	20	nC
		Q_1	—	2.0	—	
		Q_2	—	5.0	—	
		Q_3	—	4.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 1.7 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.85	1.6	Vdc
	(I_S = 1.7 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.7	—	
Reverse Recovery Time	(I_S = 1.7 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	40	—	ns
		t_a	—	34	—	
		t_b	—	6.0	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.089	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

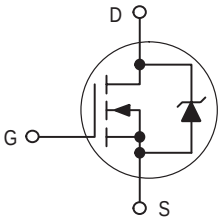
Product Preview

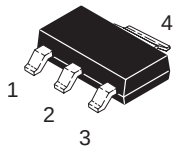
TMOS V™
SOT-223 for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

MMFT3055VL

TMOS POWER FET
1.5 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.140 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 318E–04, Style 3
TO–261AA

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Available in 12 mm Tape & Reel
  Use MMFT3055VLT1 to order the 7 inch/1000 unit reel
  Use MMFT3055VLT3 to order the 13 inch/4000 unit reel

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage – Continuous – Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 20	Vdc Vpk
Drain Current – Continuous – Continuous @ 100°C – Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	1.5 1.2 5.0	Adc Apk
Total PD @ T_A = 25°C mounted on 1” sq. Drain pad on FR–4 bd material Total PD @ T_A = 25°C mounted on 0.70” sq. Drain pad on FR–4 bd material Total PD @ T_A = 25°C mounted on min. Drain pad on FR–4 bd material Derate above 25°C	P_D	2.0 1.7 0.9 6.3	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	 45	mJ
Thermal Resistance – Junction to Ambient on 1” sq. Drain pad on FR–4 bd material – Junction to Ambient on 0.70” sq. Drain pad on FR–4 bd material – Junction to Ambient on min. Drain pad on FR–4 bd material	 $R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JA}$	 70 88 159	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.
E–FET and TMOS V are trademarks of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	60 —	— 65	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	1.0 —	1.5 3.7	2.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 0.75 Adc)		$R_{DS(on)}$	—	0.125	0.14	Ohm
Drain–to–Source On–Voltage (V_{GS} = 5.0 Vdc, I_D = 1.5 Adc) (V_{GS} = 5.0 Vdc, I_D = 0.75 Adc, T_J = 150°C)		$V_{DS(on)}$	— —	— —	0.25 0.24	Vdc
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 1.5 Adc)		g_{FS}	1.0	3.5	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	350	490	pF
Output Capacitance		C_{oss}	—	110	150	
Transfer Capacitance		C_{rss}	—	29	60	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 1.5 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	9.5	20	ns
Rise Time		t_r	—	18	40	
Turn–Off Delay Time		$t_{d(off)}$	—	35	70	
Fall Time		t_f	—	22	40	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 1.5 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	9.0	10	nC
		Q_1	—	1.0	—	
		Q_2	—	4.0	—	
		Q_3	—	4.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 1.5 Adc, V_{GS} = 0 Vdc) (I_S = 1.5 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	— —	0.82 0.68	1.2 —	Vdc
Reverse Recovery Time	(I_S = 1.5 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	41	—	ns
		t_a	—	29	—	
		t_b	—	12	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.066	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

Designer's™ Data Sheet

Medium Power Surface Mount Products

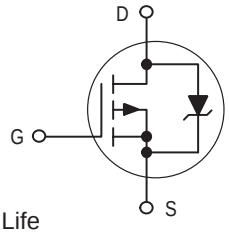
TMOS Single P-Channel Field Effect Transistors

MMSF2P02E

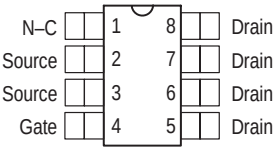
Motorola Preferred Device

SINGLE TMOS POWER MOSFET 2.5 AMPERES 20 VOLTS $R_{DS(on)}$ = 0.250 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's TMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.



CASE 751–05, Style 13
SO–8



Top View

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided
- I_{DSS} Specified at Elevated Temperature

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C (2) — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	2.5 1.7 13	Adc Apk
Total Power Dissipation @ T_A = 25°C(2)	P_D	2.5	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 5.0 Vdc, I_L = 6.0 Apk, L = 12 mH, R_G = 25 Ω)	E_{AS}	216	mJ
Thermal Resistance — Junction to Ambient(2)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

S2P02

(1) Negative sign for P–Channel device omitted for clarity.
(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided), 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMSF2P02ER2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 20 —	 — 24.7	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0	 2.0 4.7	 3.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	 — —	 0.19 0.3	 0.25 0.4	Ohm
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.0 Adc)		g_{FS}	1.0	2.8	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	340	475	pF
Output Capacitance		C_{oss}	—	220	300	
Transfer Capacitance		C_{rss}	—	75	150	
SWITCHING CHARACTERISTICS(3)						
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 5.0 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	20	40	ns
Rise Time		t_r	—	40	80	
Turn–Off Delay Time		$t_{d(off)}$	—	53	106	
Fall Time		t_f	—	41	82	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	13	26	ns
Rise Time		t_r	—	29	58	
Turn–Off Delay Time		$t_{d(off)}$	—	30	60	
Fall Time		t_f	—	28	56	
Gate Charge	(V_{DS} = 16 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	10	15	nC
		Q_1	—	1.1	—	
		Q_2	—	3.3	—	
		Q_3	—	2.5	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(2)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.5	2.0	Vdc
Reverse Recovery Time	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	34	64	ns
		t_a	—	18	—	
		t_b	—	16	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.035	—	μC

(1) Negative sign for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(3) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

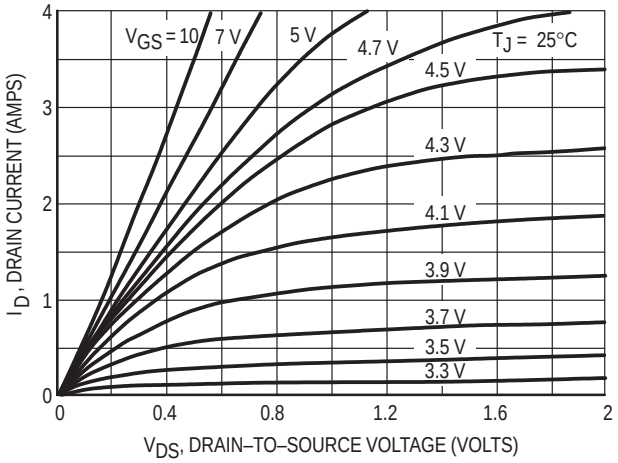


Figure 1. On–Region Characteristics

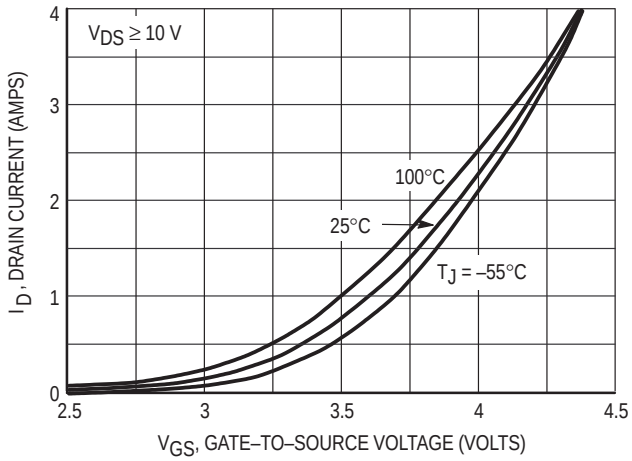


Figure 2. Transfer Characteristics

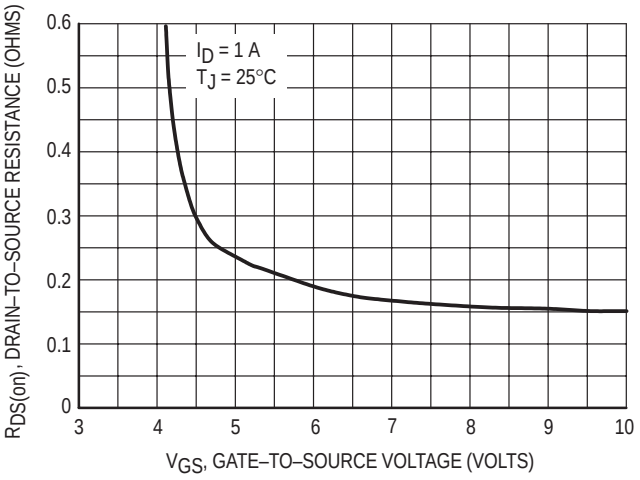


Figure 3. On–Resistance versus Gate–to–Source Voltage

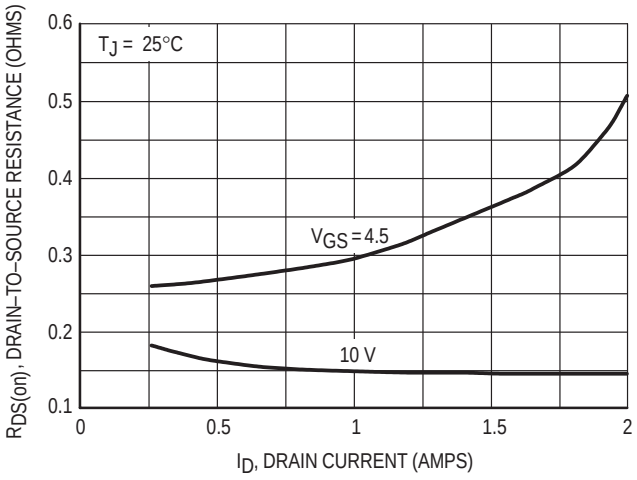


Figure 4. On–Resistance versus Drain Current and Gate Voltage

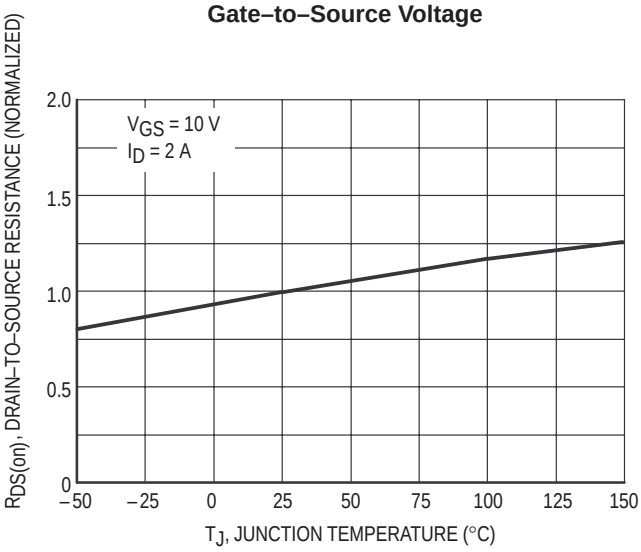


Figure 5. On–Resistance Variation with Temperature

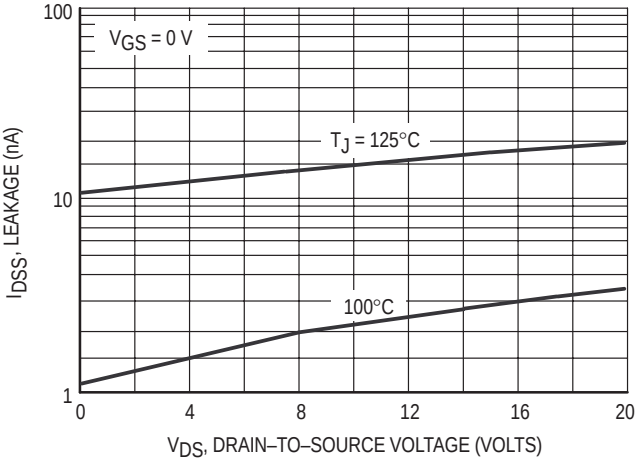


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

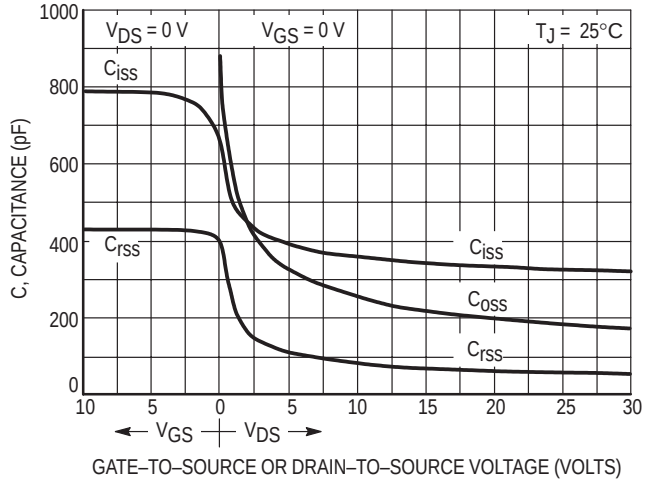


Figure 7. Capacitance Variation

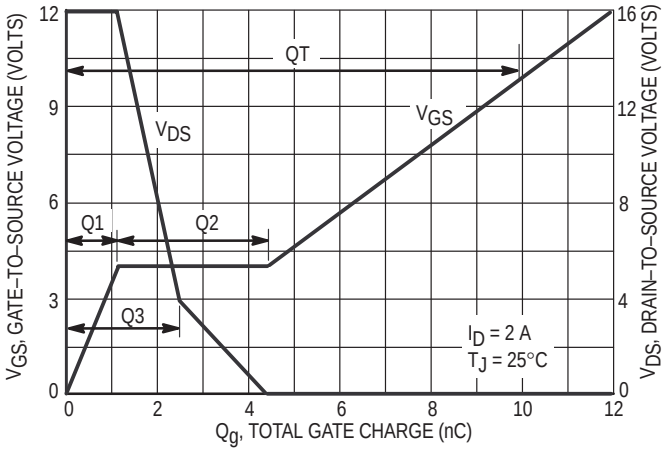


Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

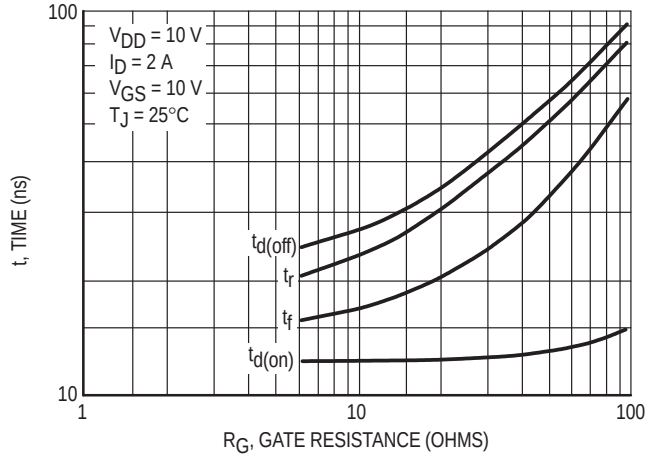


Figure 9. Resistive Switching Time Variation versus Gate Resistance

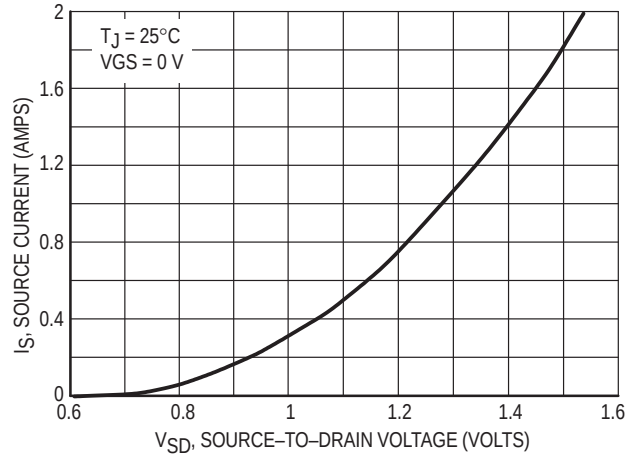


Figure 10. Diode Forward Voltage versus Current

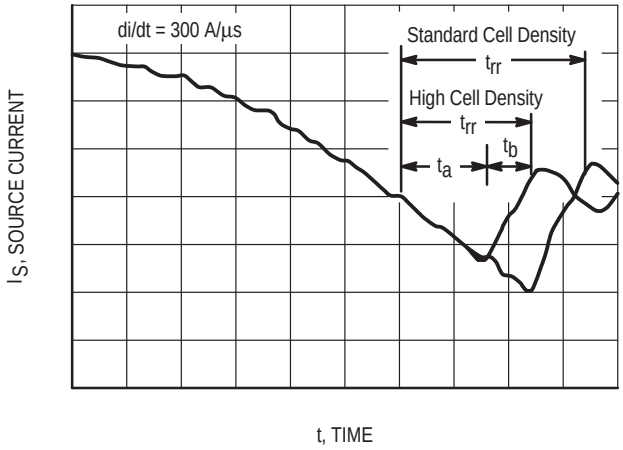


Figure 11. Reverse Recovery Time (t_{rr})

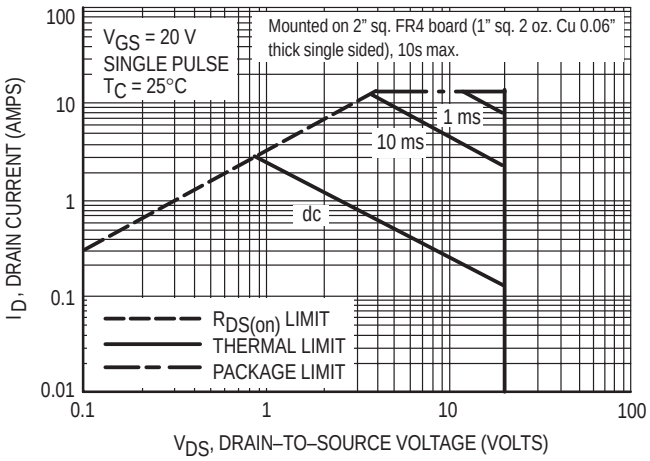


Figure 12. Maximum Rated Forward Biased Safe Operating Area

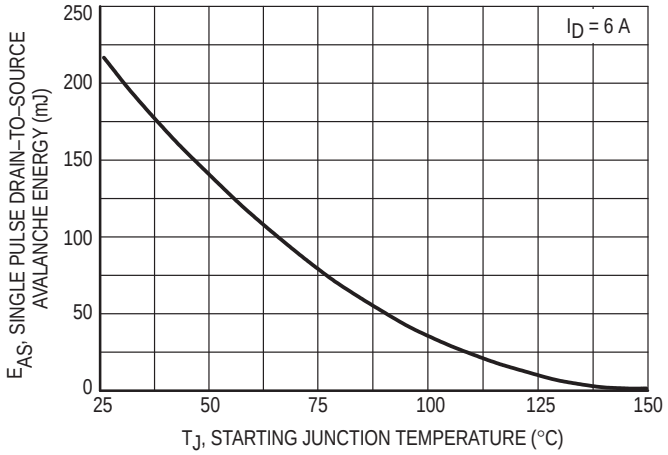


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

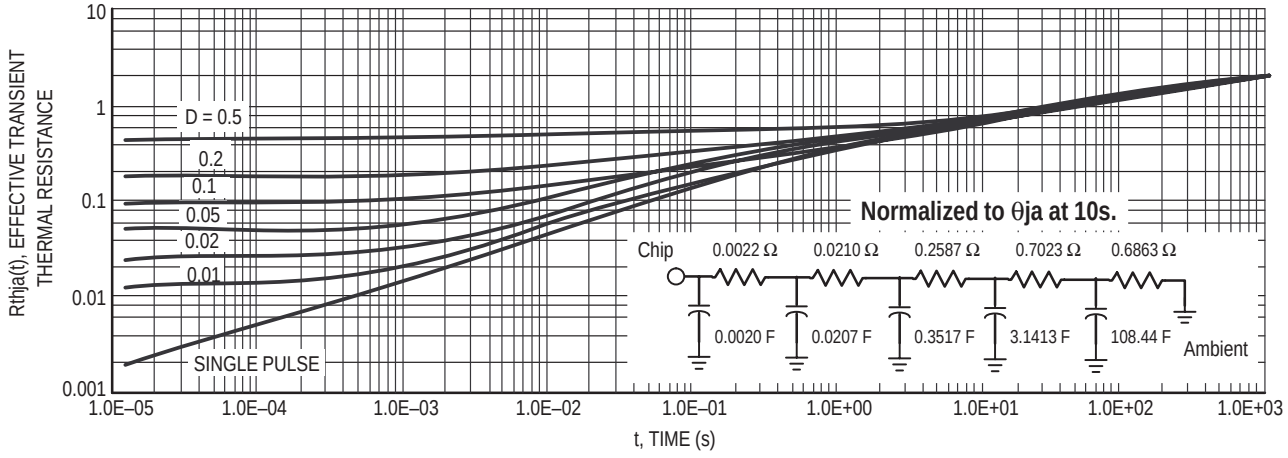


Figure 14. Thermal Response

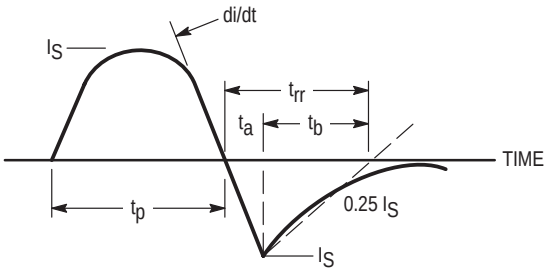


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

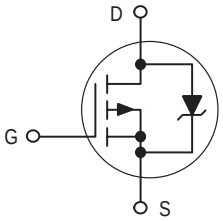
TMOS Single P-Channel Field Effect Transistors

MMSF3P02HD

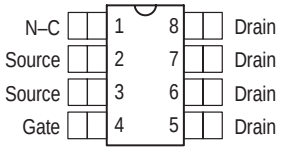
Motorola Preferred Device

SINGLE TMOS POWER MOSFET 3.0 AMPERES 20 VOLTS $R_{DS(on)}$ = 0.075 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.



CASE 751–05, Style 13
SO–8



- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	5.6 3.6 30	Adc Apk
Total Power Dissipation @ T_A = 25°C (2)	P_D	2.5	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 9.0 Apk, L = 14 mH, R_G = 25 Ω)	E_{AS}	567	mJ
Thermal Resistance — Junction to Ambient (2)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

S3P02

(1) Negative sign for P–Channel device omitted for clarity.
(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided), 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMSF3P02HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.
REV 4

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 20 —	 — 24	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 —	 1.5 4.0	 2.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc) (V_{GS} = 4.5 Vdc, I_D = 1.5 Adc)		$R_{DS(on)}$	 — —	 0.06 0.08	 0.075 0.095	Ohm
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.5 Adc)		g_{FS}	3.0	7.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1010	1400	pF
Output Capacitance		C_{oss}	—	740	920	
Transfer Capacitance		C_{rss}	—	260	490	
SWITCHING CHARACTERISTICS(3)						
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 3.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	25	50	ns
Rise Time		t_r	—	135	270	
Turn–Off Delay Time		$t_{d(off)}$	—	54	108	
Fall Time		t_f	—	84	168	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	16	32	
Rise Time		t_r	—	40	80	
Turn–Off Delay Time		$t_{d(off)}$	—	110	220	
Fall Time		t_f	—	97	194	
Gate Charge See Figure 8	(V_{DS} = 16 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	33	46	nC
		Q_1	—	3.0	—	
		Q_2	—	11	—	
		Q_3	—	10	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(2)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 1.35 0.96	 1.75 —	Vdc
Reverse Recovery Time See Figure 15	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	76	—	ns
		t_a	—	32	—	
		t_b	—	44	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.133	—	μC

(1) Negative sign for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(3) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

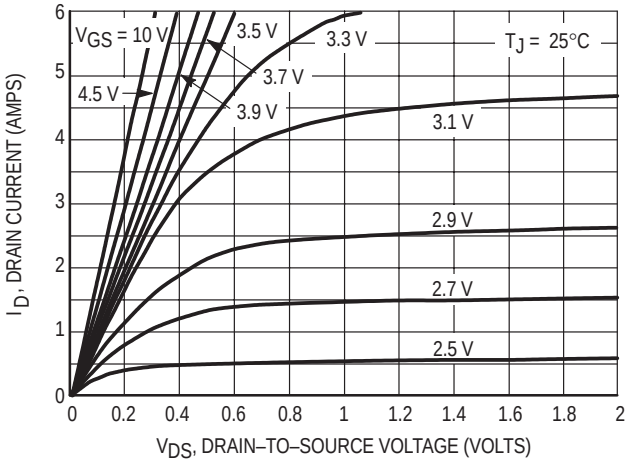


Figure 1. On–Region Characteristics

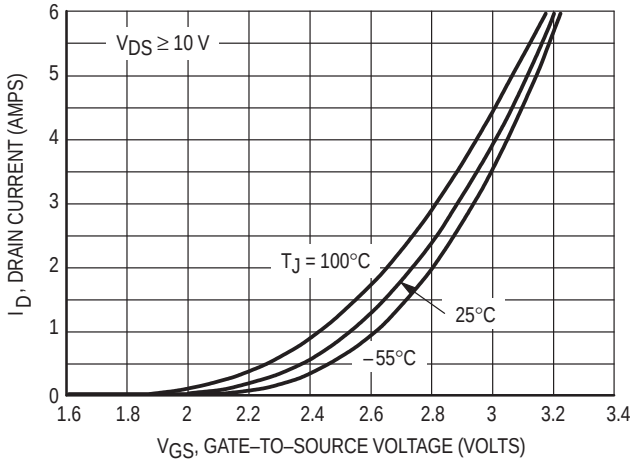


Figure 2. Transfer Characteristics

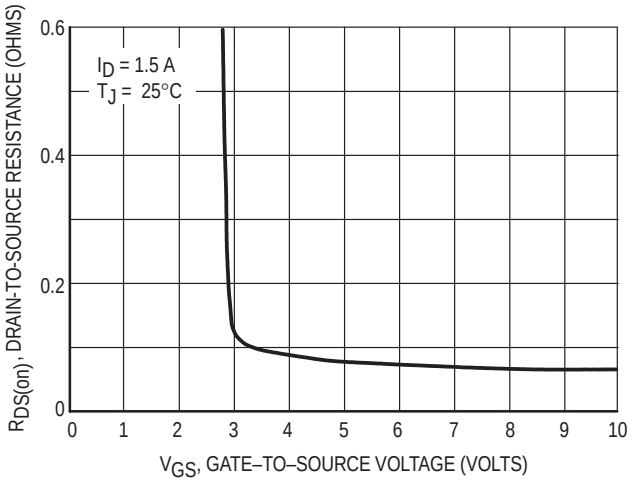


Figure 3. On–Resistance versus Gate–To–Source Voltage

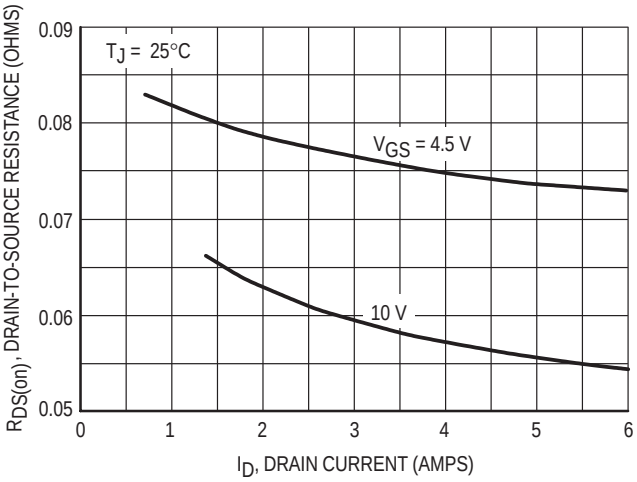


Figure 4. On–Resistance versus Drain Current and Gate Voltage

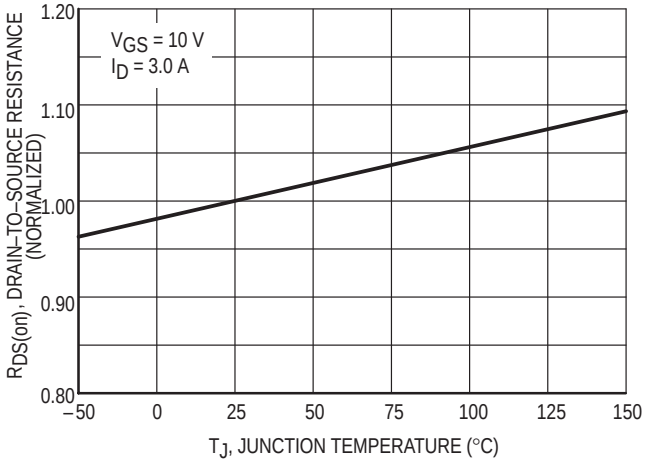


Figure 5. On–Resistance Variation with Temperature

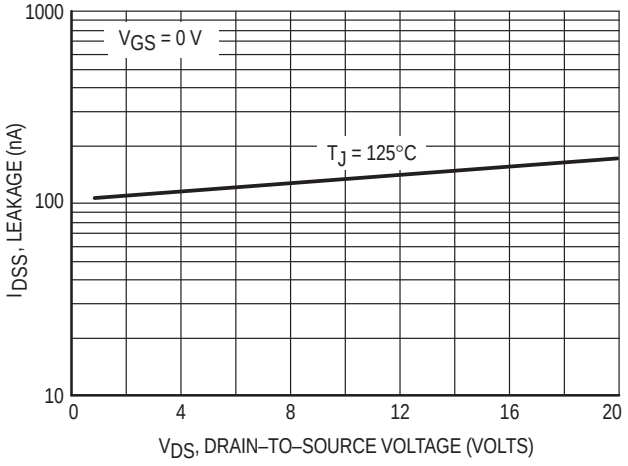


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

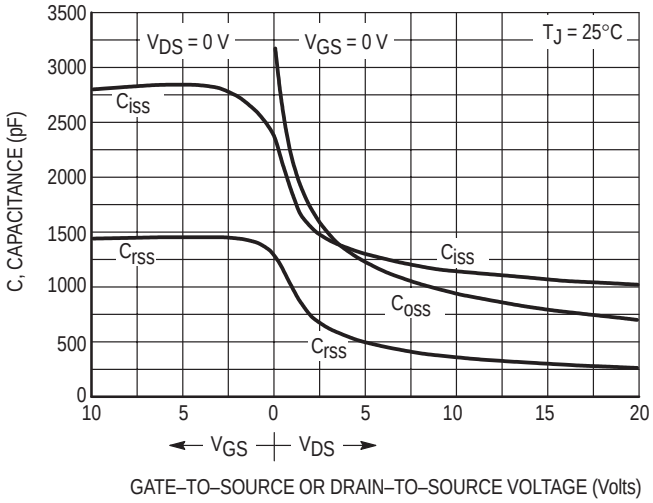


Figure 7. Capacitance Variation

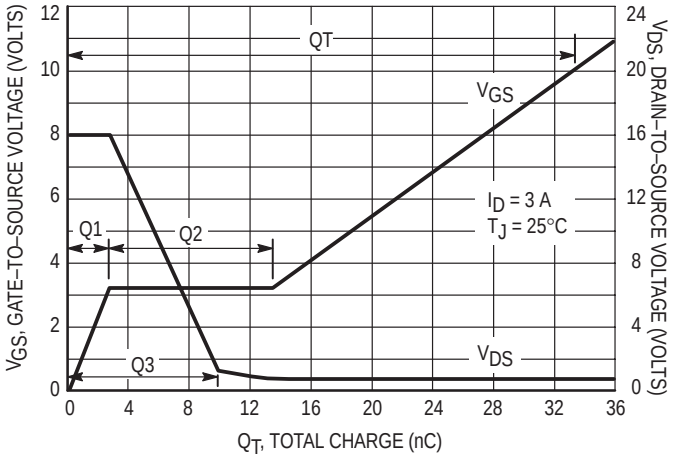


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

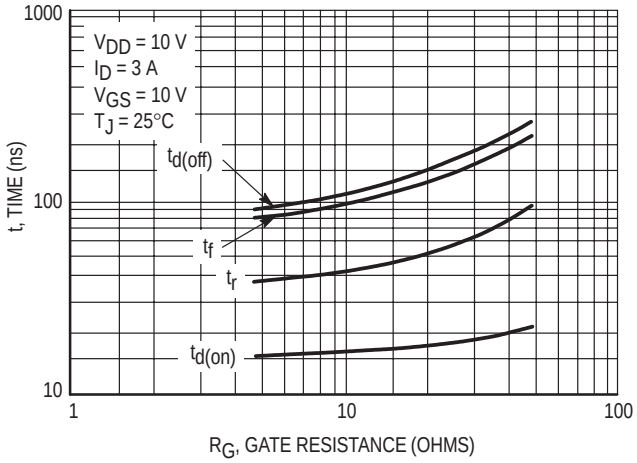


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

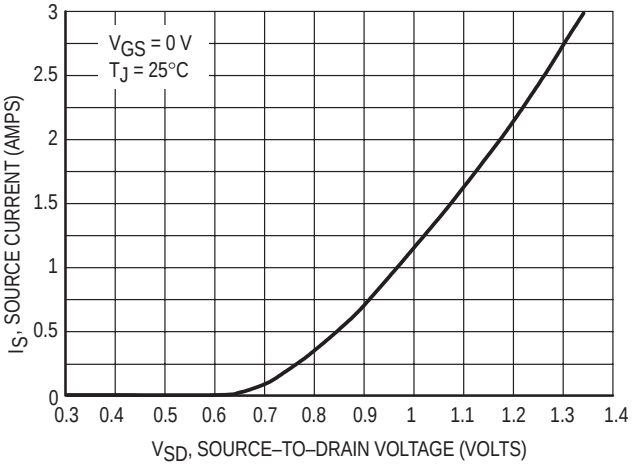


Figure 10. Diode Forward Voltage versus Current

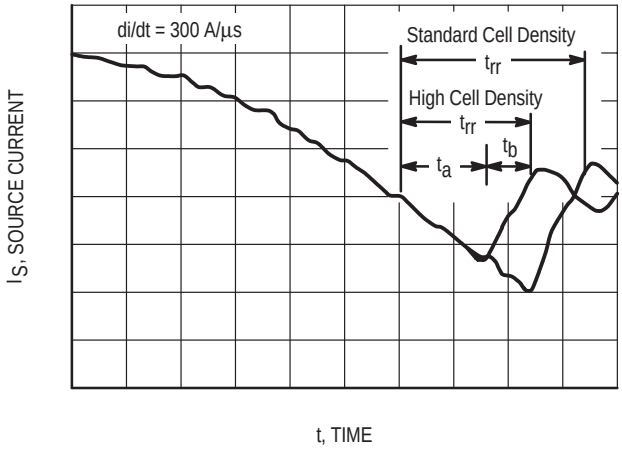


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

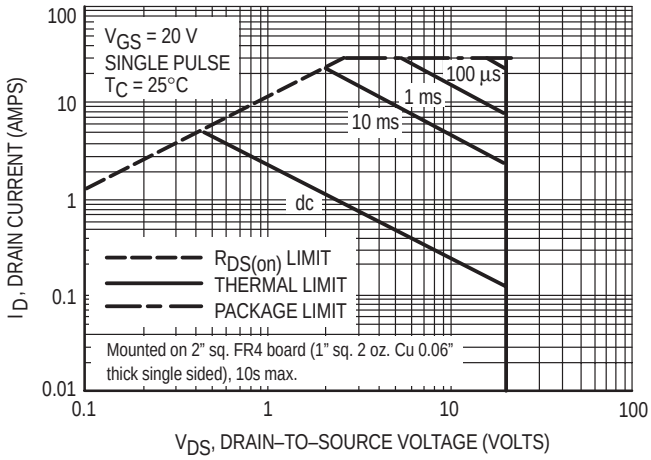


Figure 12. Maximum Rated Forward Biased Safe Operating Area

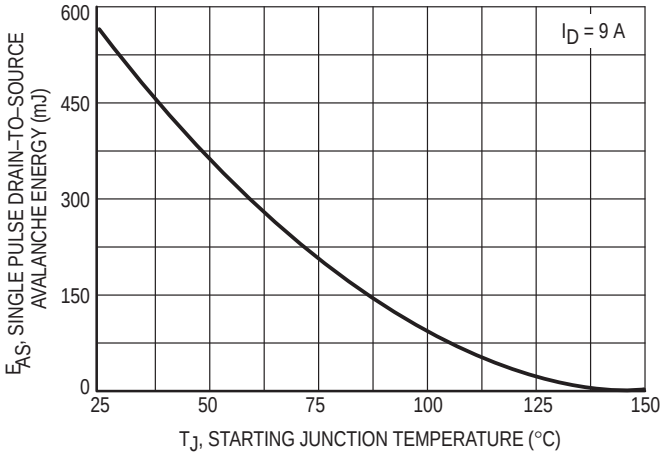


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

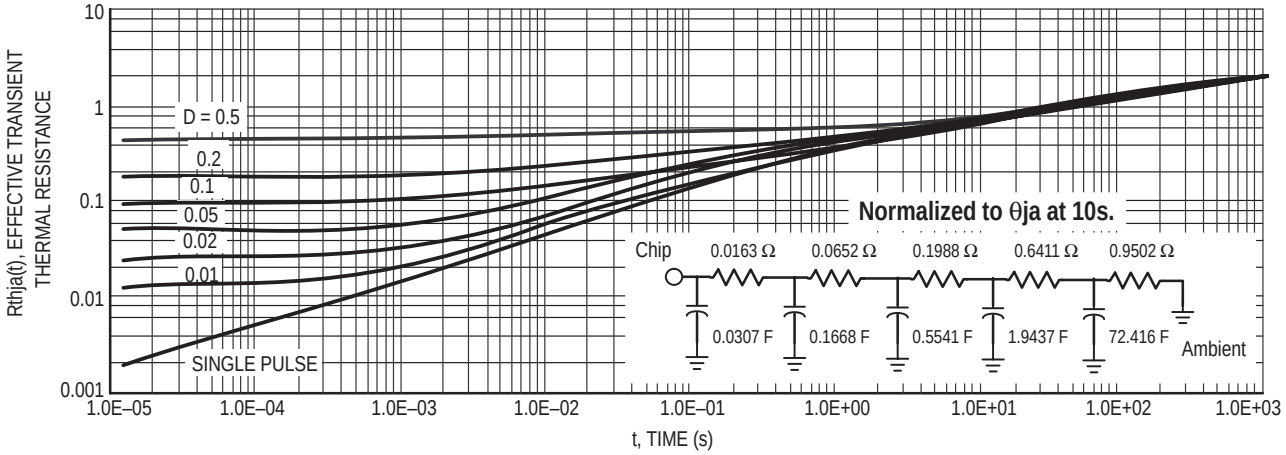


Figure 14. Thermal Response

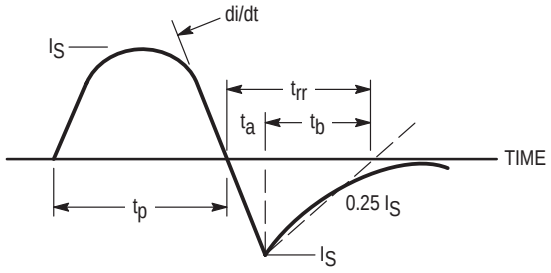


Figure 15. Diode Reverse Recovery Waveform

Advance Information

Medium Power Surface Mount Products

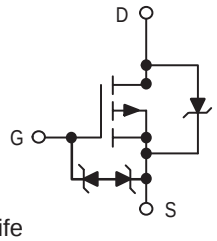
TMOS Single P-Channel with Monolithic Zener ESD Protected Gate

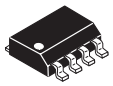
MMSF3P02Z

Motorola Preferred Device

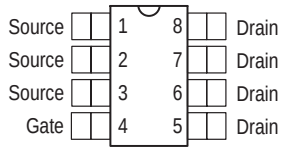
SINGLE TMOS POWER MOSFET 3.0 AMPERES 20 VOLTS $R_{DS(on)}$ = 0.060 OHM

EZFETs™ are an advanced series of power MOSFETs which utilize Motorola's High Cell Density TMOS process and contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ amd true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.





CASE 751–05, Style 12
SO–8



Top View

- Zener Protected Gates Provide Electrostatic Discharge Protection
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Designed to withstand 200V Machine Model and 2000V Human Body Model
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) *

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 15	Vdc
Drain Current — Continuous @ T_A = 25°C (1) — Continuous @ T_A = 70°C (1) — Pulsed Drain Current (3)	I_D I_D I_{DM}	6.5 3.0 52	Adc Apk
Total Power Dissipation @ T_A = 25°C (1) Linear Derating Factor (1)	P_D	2.5 20	Watts mW/°C
Total Power Dissipation @ T_A = 25°C (2) Linear Derating Factor (2)	P_D	1.6 12	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 9 Apk, L = 14 mH, R_G = 25 Ω)	E_{AS}	567	mJ
Thermal Resistance — Junction to Ambient (1) — Junction to Ambient (2)	$R_{\theta JA}$	50 80	°C/W

* Negative sign for P–Channel omitted for clarity.
(1) When mounted on 1 inch square FR–4 or G–10 board (V_{GS} = 10 V, @ 10 Seconds)
(2) When mounted on minimum recommended FR–4 or G–10 board (V_{GS} = 10 V, @ Steady State)
(3) Repetitive rating; pulse width limited by maximum junction temperature.

DEVICE MARKING **ORDERING INFORMATION**

S3P02Z	Device	Reel Size	Tape Width	Quantity
	MMSF3P02ZR2	13″	12 mm embossed tape	2500 units

This document contains information on a new product. Specifications and information are subject to change without notice.
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (1) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			20	—	—	
Temperature Coefficient (Positive)			—	23	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc)			—	0.05	2.0	
(V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	0.2	10	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0)		I_{GSS}	—	0.85	5.0	μAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (1) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			1.0	1.8	3.0	
Threshold Temperature Coefficient (Negative)			—	3.7	—	mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (1) (3)		$R_{DS(on)}$				mΩ
(V_{GS} = 10 Vdc, I_D = 3.0 Adc)			—	45	60	
(V_{GS} = 4.5 Vdc, I_D = 1.5 Adc)			—	65	80	
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.5 Adc) (1)		g_{FS}	4.0	5.6	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1100	2200	pF
Output Capacitance		C_{oss}	—	720	1440	
Transfer Capacitance		C_{rss}	—	320	640	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω) (1)	$t_{d(on)}$	—	90	180	ns
Rise Time		t_r	—	350	700	
Turn–Off Delay Time		$t_{d(off)}$	—	810	1620	
Fall Time		t_f	—	1030	2060	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 3.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω) (1)	$t_{d(on)}$	—	230	460	ns
Rise Time		t_r	—	1300	2600	
Turn–Off Delay Time		$t_{d(off)}$	—	510	1020	
Fall Time		t_f	—	1040	2080	
Gate Charge	(V_{DS} = 16 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc) (1)	Q_T	—	39	55	nC
		Q_1	—	2.7	—	
		Q_2	—	14.3	—	
		Q_3	—	10.2	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (1)	V_{SD}				Vdc
	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.2	1.6	
			—	0.76	—	
Reverse Recovery Time	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (1)	t_{rr}	—	677	—	ns
		t_a	—	256	—	
		t_b	—	420	—	
Reverse Recovery Storage Charge		Q_{RR}	—	5.0	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

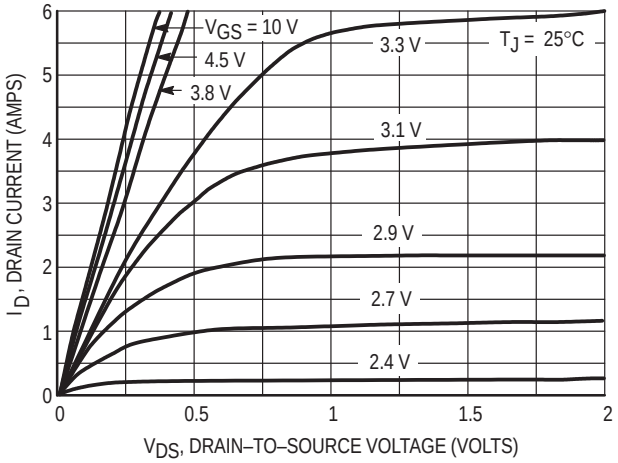


Figure 1. On–Region Characteristics

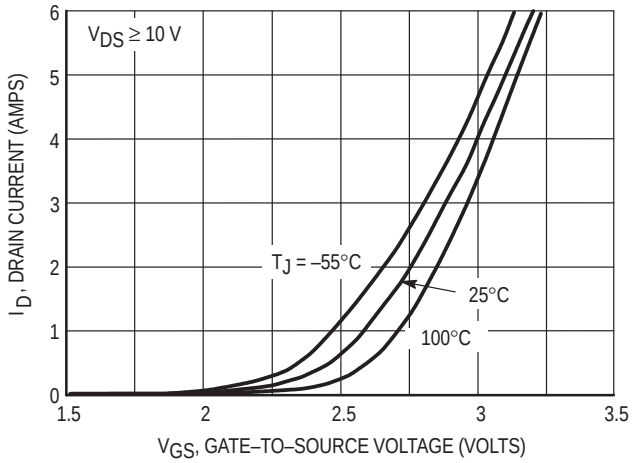


Figure 2. Transfer Characteristics

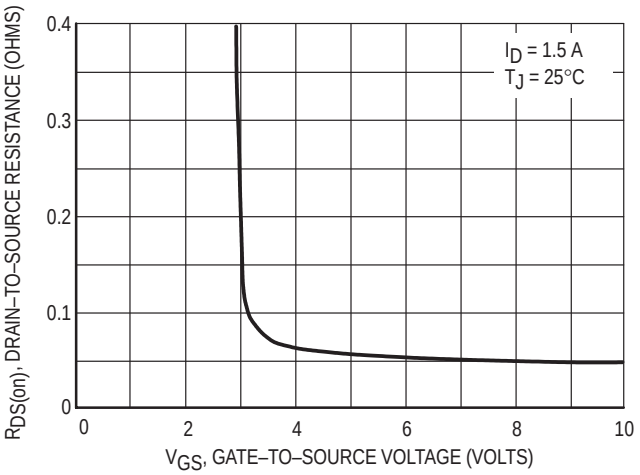


Figure 3. On–Resistance versus Gate–to–Source Voltage

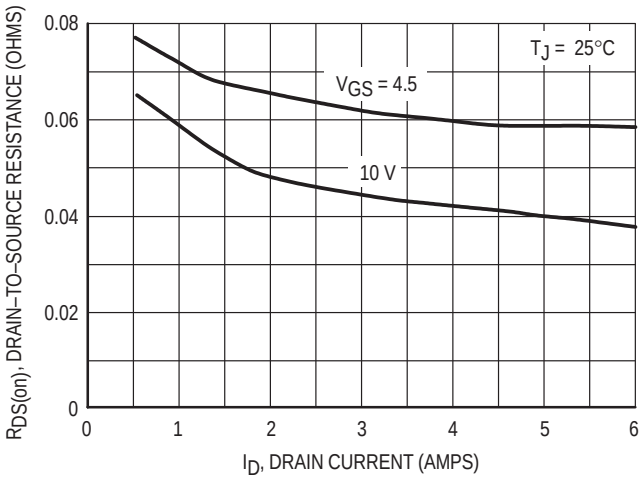


Figure 4. On–Resistance versus Drain Current and Gate Voltage

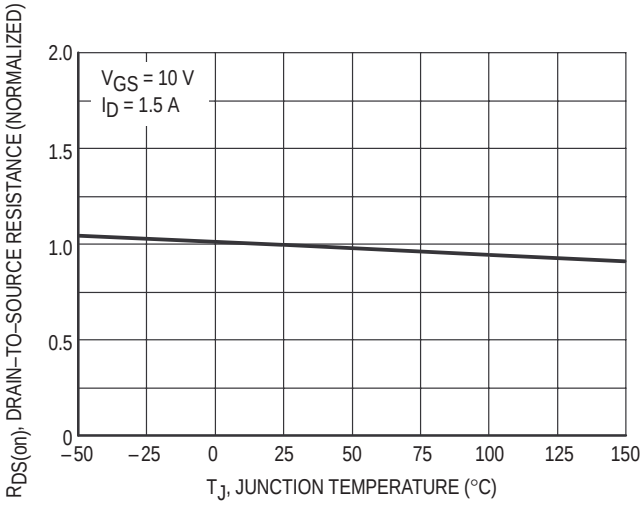


Figure 5. On–Resistance Variation with Temperature

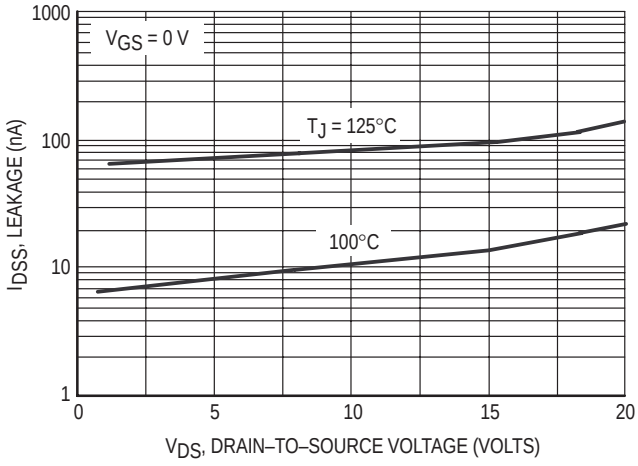


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

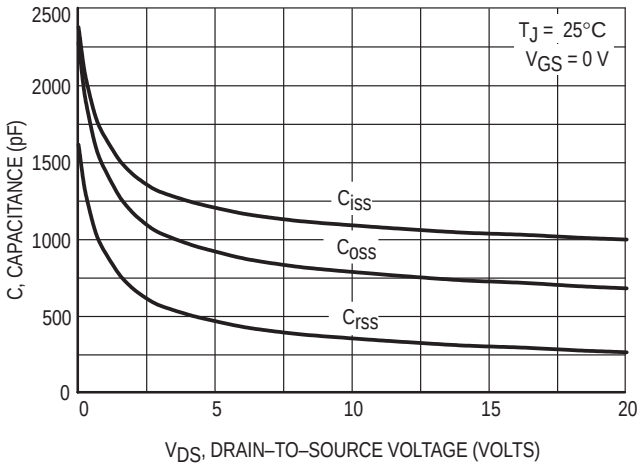


Figure 7. Capacitance Variation

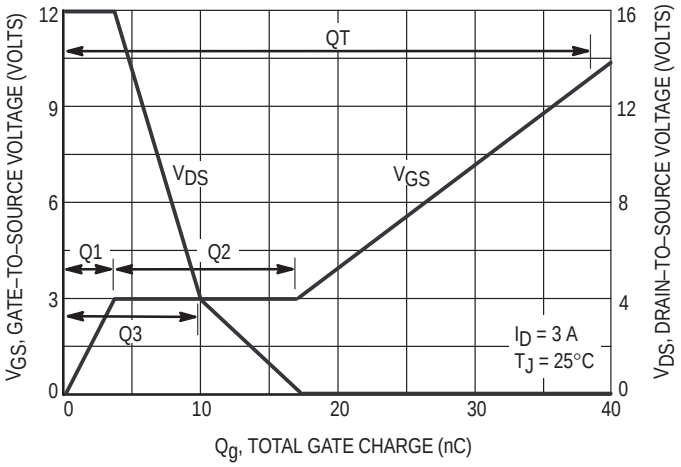


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

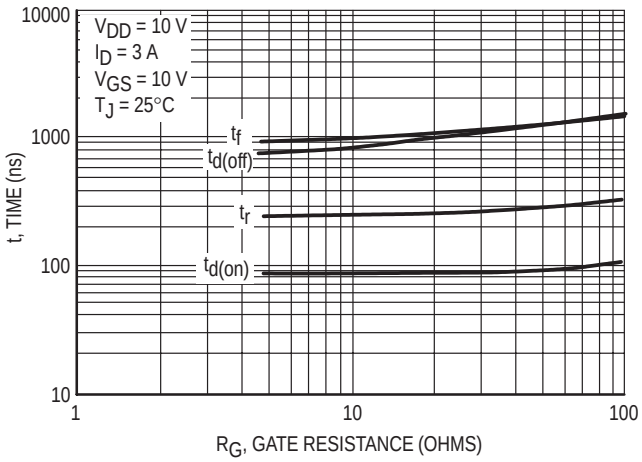


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

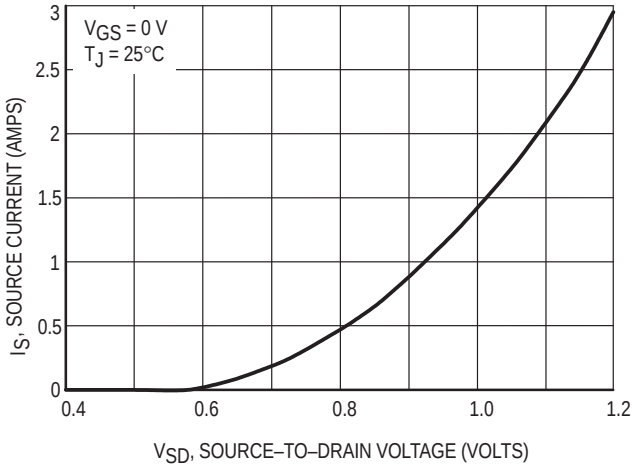


Figure 10. Diode Forward Voltage versus Current

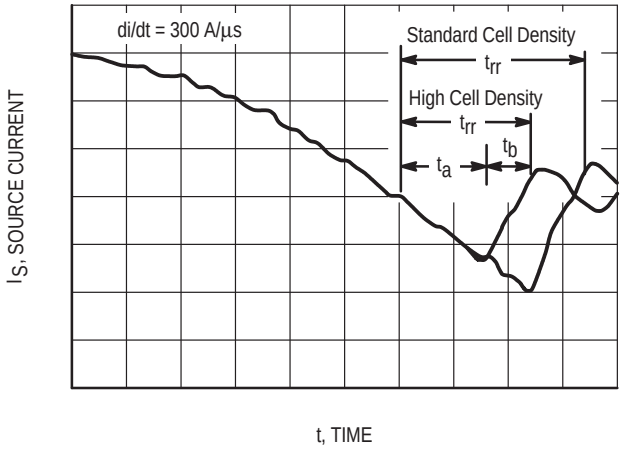


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

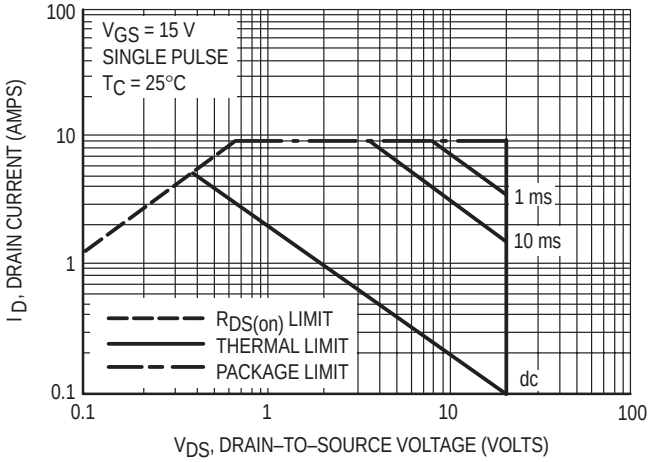


Figure 12. Maximum Rated Forward Biased Safe Operating Area

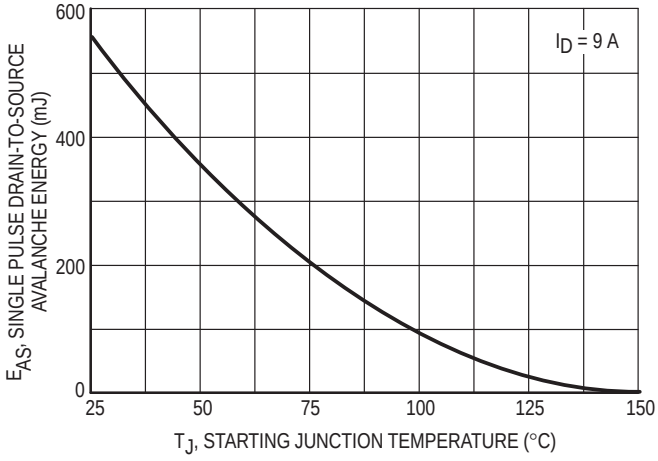


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

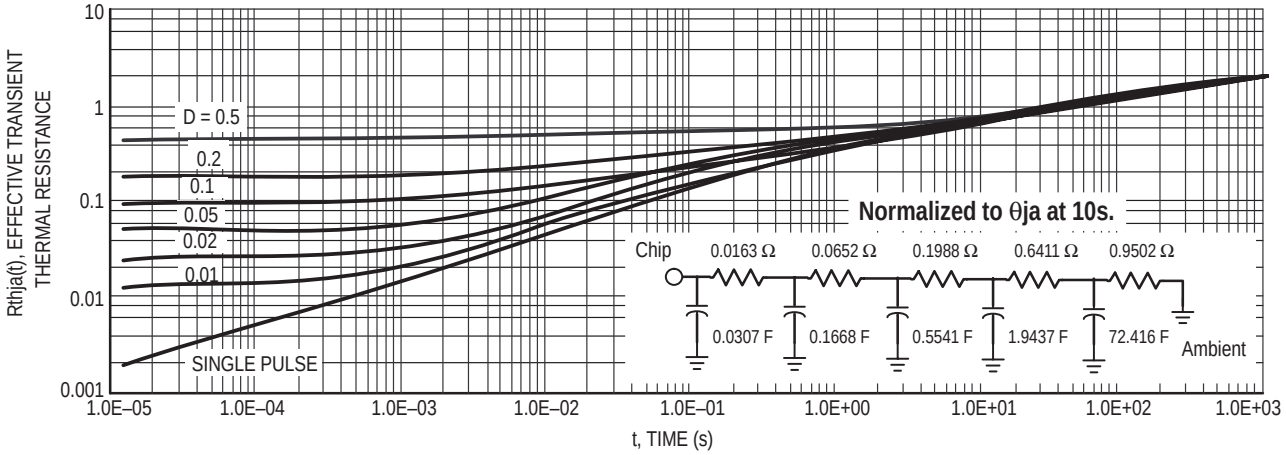


Figure 14. Thermal Response

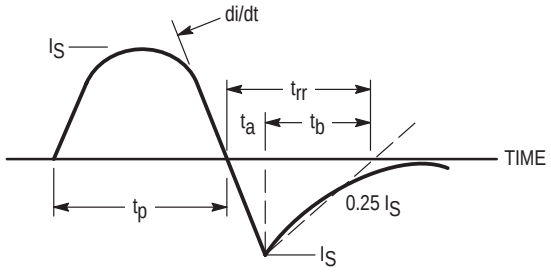


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

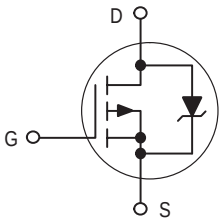
TMOS P-Channel Field Effect Transistors

MMSF3P03HD

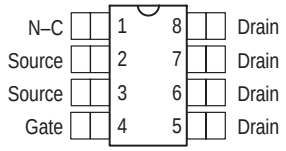
Motorola Preferred Device

SINGLE TMOS POWER FET
3.0 AMPERES
30 VOLTS
$R_{DS(on)}$ = 0.1 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.



CASE 751–05, Style 13
SO–8



Top View

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	30	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	4.6 3.0 50	Adc Apk
Total Power Dissipation @ T_A = 25°C (2)	P_D	2.5	Watts
Operating and Storage Temperature Range	– 55 to 150		°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 5.0 Vdc, I_L = 9.0 Apk, L = 14 mH, R_G = 25 Ω)	E_{AS}	567	mJ
Thermal Resistance — Junction to Ambient (2)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

S3P03

(1) Negative signs for P–Channel device omitted for clarity.
(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided), 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMSF3P03HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.
REV 4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	30	—	—	Vdc
Temperature Coefficient (Positive)			—	30	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	1.0	μAdc
(V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	10	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	5.0	100	nAdc
ON CHARACTERISTICS(2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Temperature Coefficient (Negative)			—	3.9	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	—	0.80	0.100	Ohm
(V_{GS} = 4.5 Vdc, I_D = 1.5 Adc)			—	0.90	0.110	
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 1.5 Adc)		g_{FS}	3.0	5.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1015	1420	pF
Output Capacitance		C_{oss}	—	470	660	
Transfer Capacitance		C_{rss}	—	135	190	
SWITCHING CHARACTERISTICS(3)						
Turn–On Delay Time	(V_{DS} = 15 Vdc, I_D = 3.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	26	52	ns
Rise Time		t_r	—	102	204	
Turn–Off Delay Time		$t_{d(off)}$	—	67	134	
Fall Time		t_f	—	69	138	
Turn–On Delay Time	(V_{DS} = 15 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	14	28	
Rise Time		t_r	—	32	64	
Turn–Off Delay Time		$t_{d(off)}$	—	104	208	
Fall Time		t_f	—	66	132	
Gate Charge	(V_{DS} = 24 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	32.4	45	nC
		Q_1	—	2.7	—	
		Q_2	—	9.0	—	
		Q_3	—	6.9	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.3	2.0	Vdc
	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.85	—	
Reverse Recovery Time	(I_S = 3.0 Adc, dI_S/dt = 100 A/μs)	t_{rr}	—	31	—	ns
		t_a	—	22	—	
		t_b	—	9.0	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.034	—	μC

(1) Negative sign for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(3) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

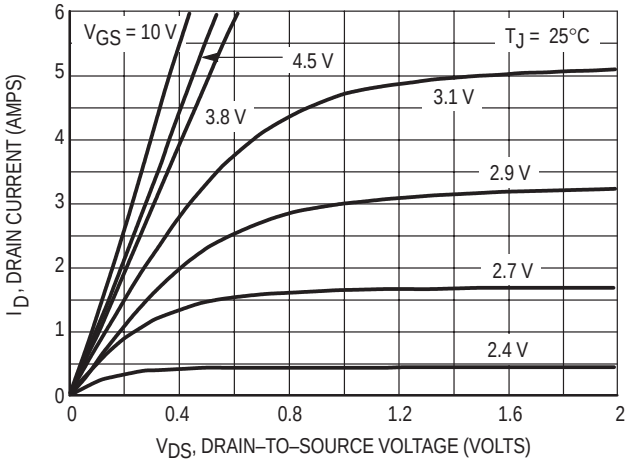


Figure 1. On–Region Characteristics

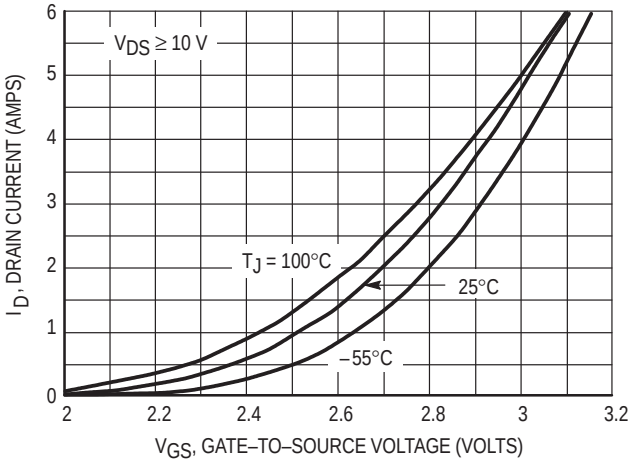


Figure 2. Transfer Characteristics

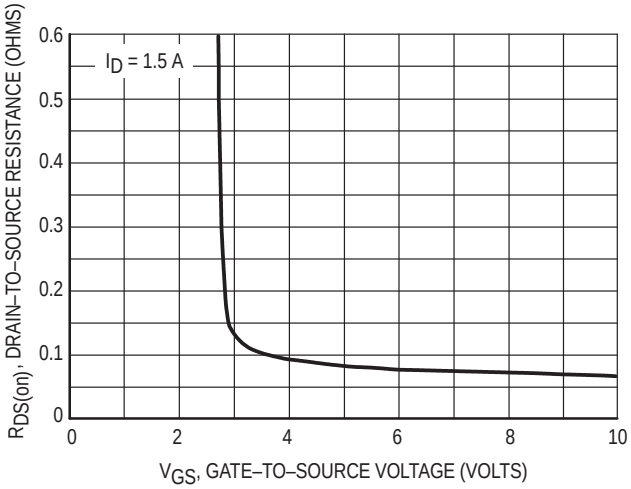


Figure 3. On–Resistance versus Gate–To–Source Voltage

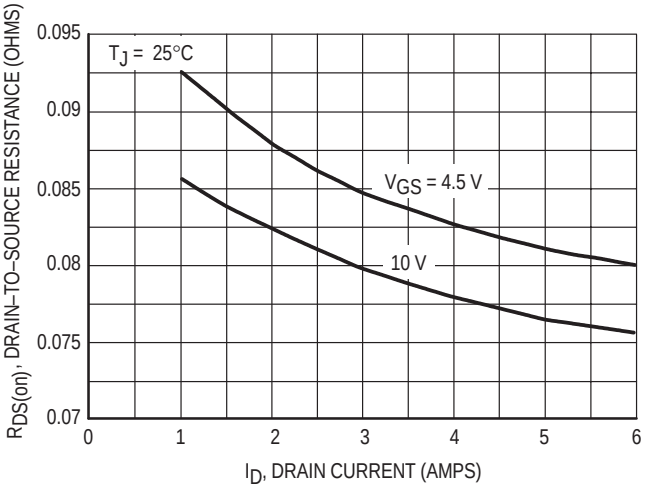


Figure 4. On–Resistance versus Drain Current and Gate Voltage

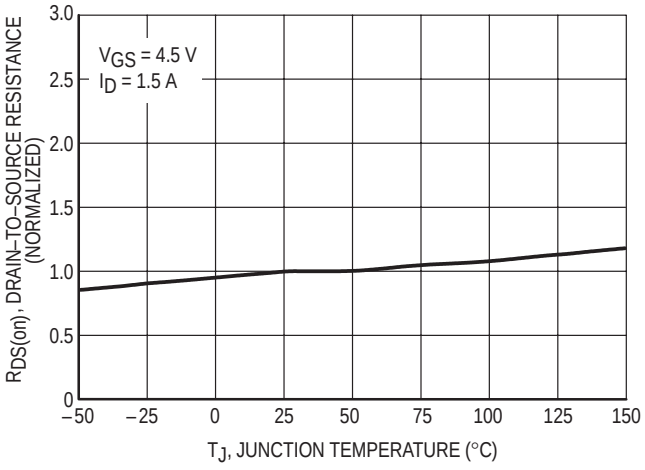


Figure 5. On–Resistance Variation with Temperature

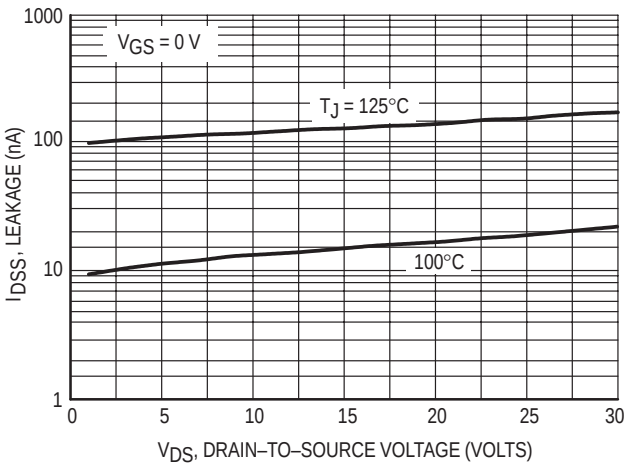


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

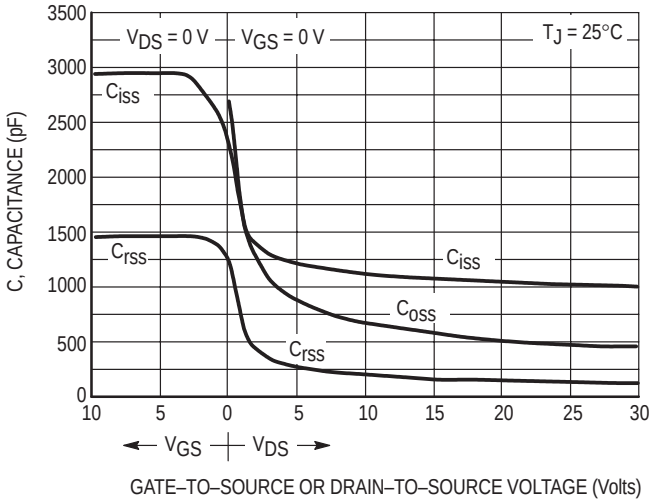


Figure 7. Capacitance Variation

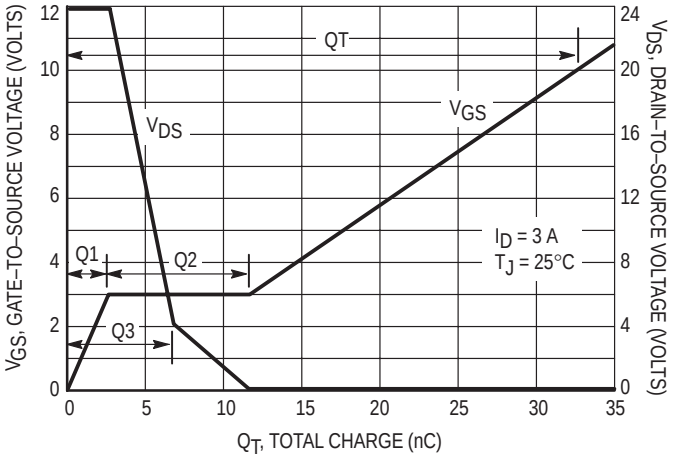


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

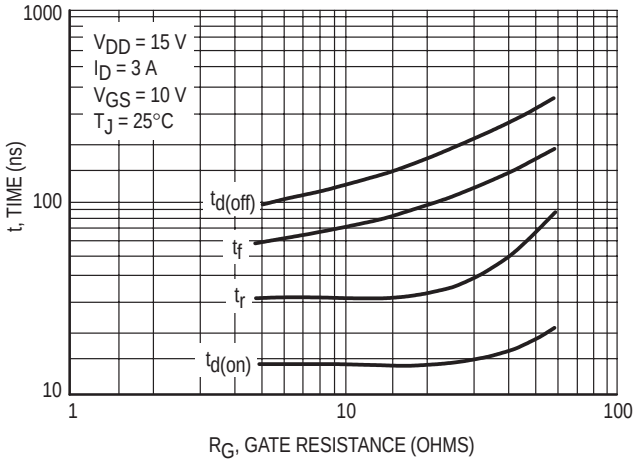


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

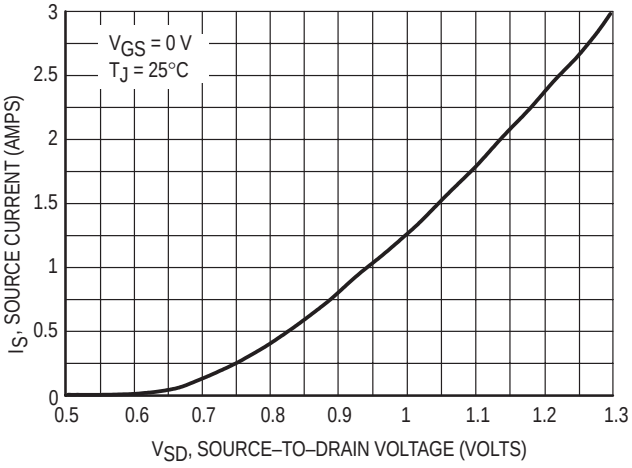


Figure 10. Diode Forward Voltage versus Current

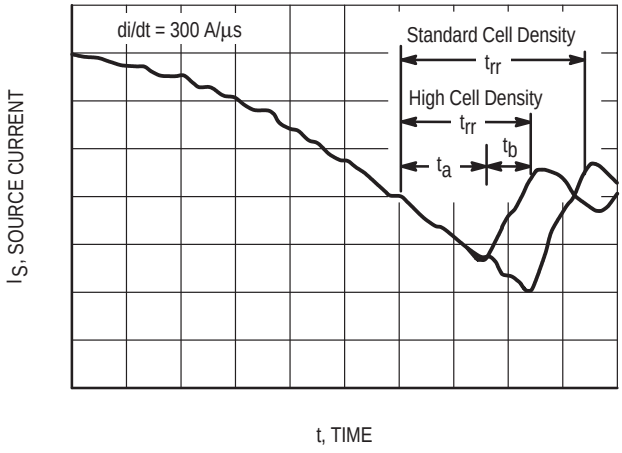


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

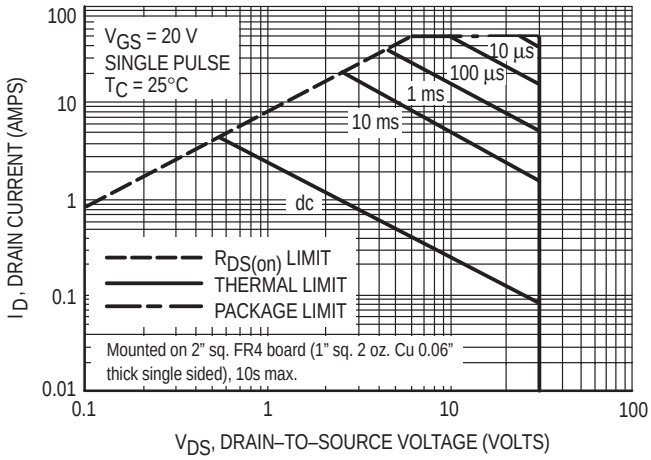


Figure 12. Maximum Rated Forward Biased Safe Operating Area

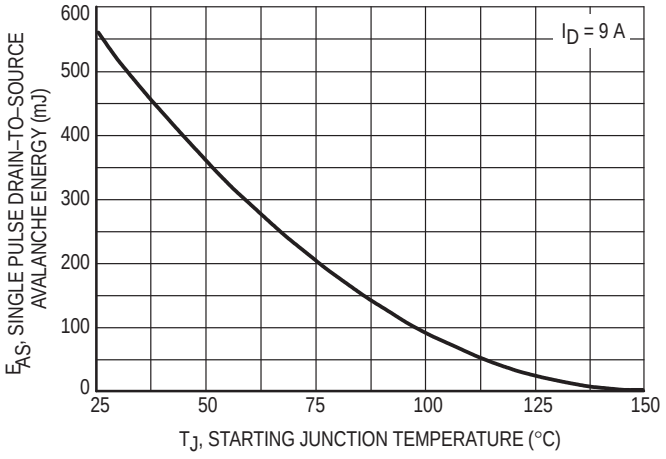


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

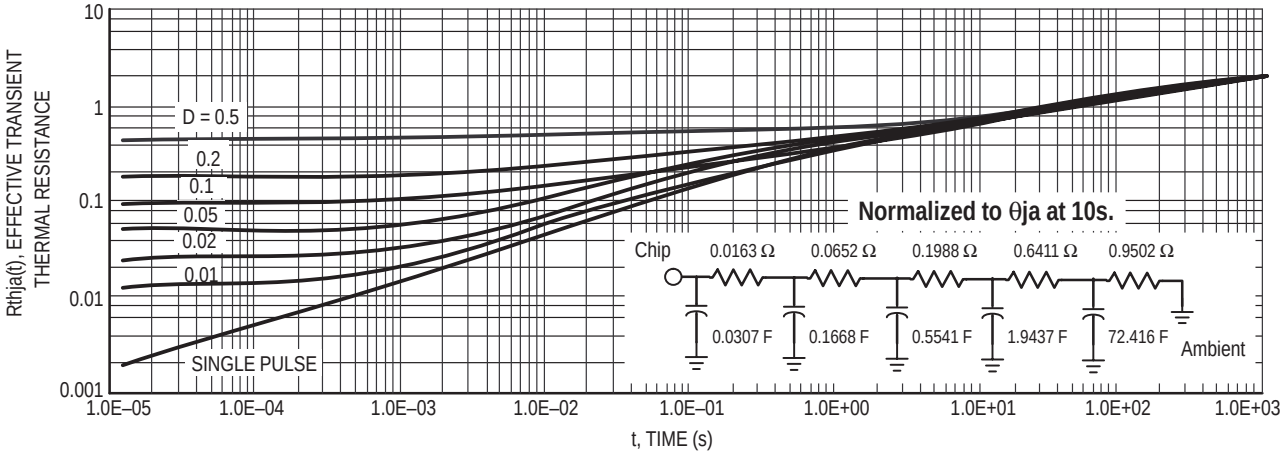


Figure 14. Thermal Response

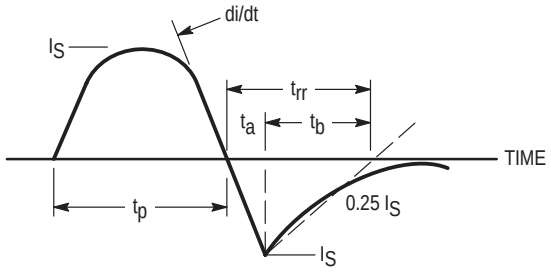


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

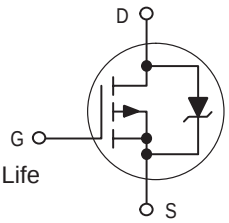
TMOS P-Channel Field Effect Transistors

MMSF4P01HD

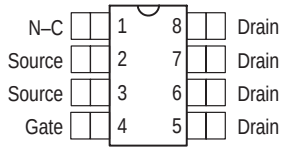
Motorola Preferred Device

SINGLE TMOS POWER FET
4.0 AMPERES
12 VOLTS
$R_{DS(on)}$ = 0.08 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.



CASE 751–05, Style 13
SO–8



Top View

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)(1)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	12	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	12	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 8.0	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	5.1 3.3 26	Adc Apk
Total Power Dissipation @ T_A = 25°C (2)	P_D	2.5	Watts
Operating and Storage Temperature Range	– 55 to 150		°C
Thermal Resistance — Junction to Ambient (2)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

S4P01

(1) Negative sign for P–Channel device omitted for clarity.
(2) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided), 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMSF4P01HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			12	—	—	
Temperature Coefficient (Positive)			—	22	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 12 Vdc, V_{GS} = 0 Vdc)			—	—	1.0	
(V_{DS} = 12 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	10	
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(2)						
Gate Threshold Voltage		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			0.7	0.95	1.1	
Temperature Coefficient (Negative)			—	2.7	—	mV/°C
Static Drain–to–Source On–Resistance		$R_{DS(on)}$				Ohm
(VGS = 4.5 Vdc, I_D = 4.0 Adc)			—	0.073	0.08	
(V_{GS} = 2.7 Vdc, I_D = 2.0 Adc)			—	0.08	0.09	
Forward Transconductance (V_{DS} = 2.5 Vdc, I_D = 2.0 Adc)		g_{FS}	3.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 10 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1270	1700	pF
Output Capacitance		C_{oss}	—	935	1300	
Reverse Transfer Capacitance		C_{rss}	—	420	600	
SWITCHING CHARACTERISTICS(3)						
Turn–On Delay Time	(V_{DS} = 6.0 Vdc, I_D = 4.0 Adc, V_{GS} = 2.7 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	25	35	ns
Rise Time		t_r	—	250	350	
Turn–Off Delay Time		$t_{d(off)}$	—	58	80	
Fall Time		t_f	—	106	150	
Turn–On Delay Time	(V_{DD} = 6.0 Vdc, I_D = 4.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	17	25	
Rise Time		t_r	—	71	100	
Turn–Off Delay Time		$t_{d(off)}$	—	95	140	
Fall Time		t_f	—	106	150	
Gate Charge	(V_{DS} = 10 Vdc, I_D = 4.0 Adc, V_{GS} = 4.5 Vdc)	Q_T	—	24	34	nC
		Q_1	—	2.4	—	
		Q_2	—	11.4	—	
		Q_3	—	8.4	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(2)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc)	V_{SD}				Vdc
	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.3	1.8	
			—	1.1	—	
Reverse Recovery Time	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	134	—	ns
		t_a	—	66	—	
		t_b	—	68	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.33	—	μC

(1) Negative sign for P–Channel device omitted for clarity.
(2) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(3) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

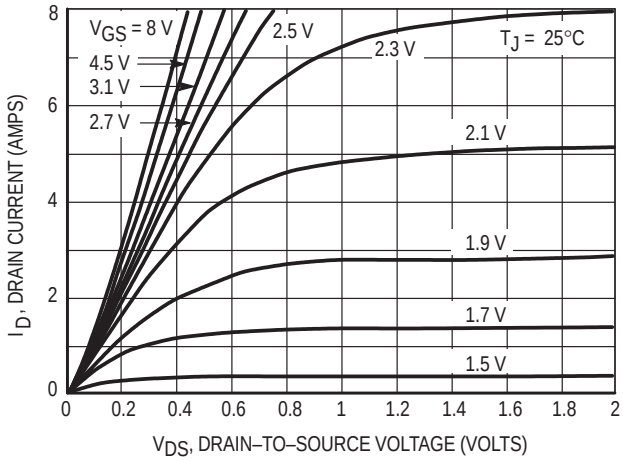
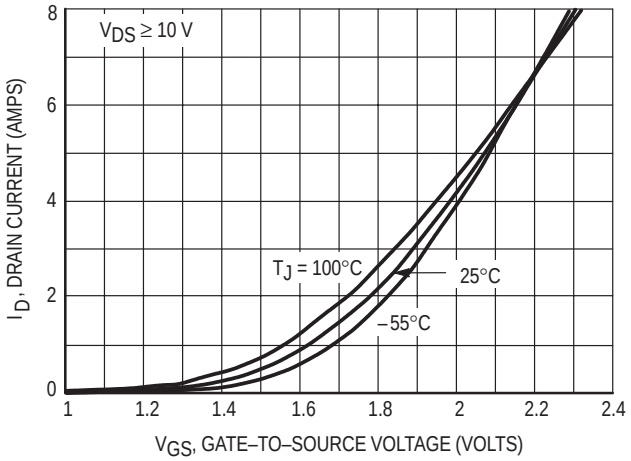


Figure 1. On–Region Characteristics



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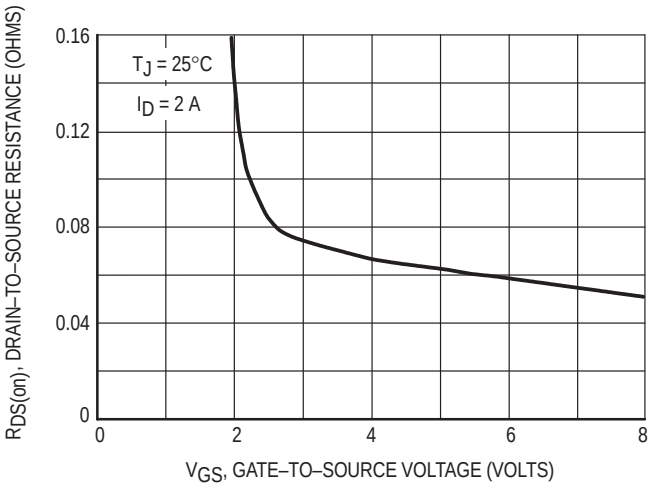

Figure 3. On–Resistance versus Gate–To–Source Voltage

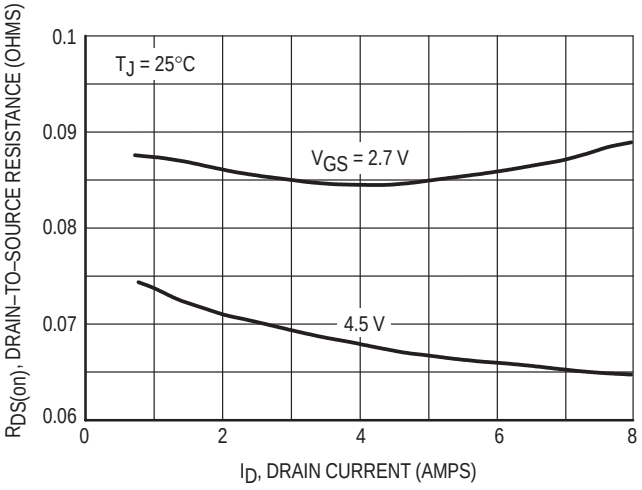

Figure 4. On–Resistance versus Drain Current and Gate Voltage

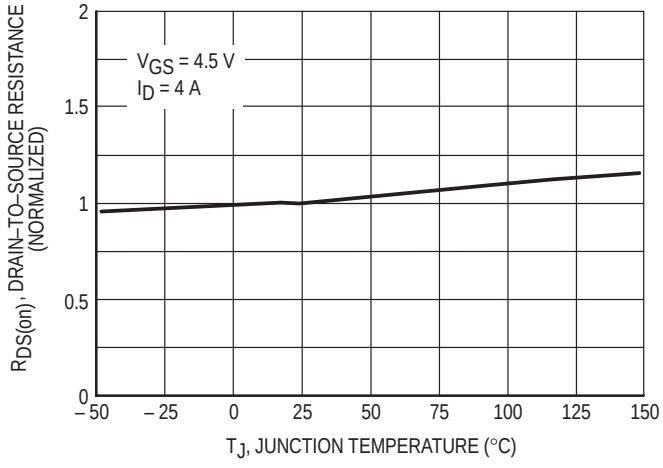

Figure 5. On–Resistance Variation with Temperature

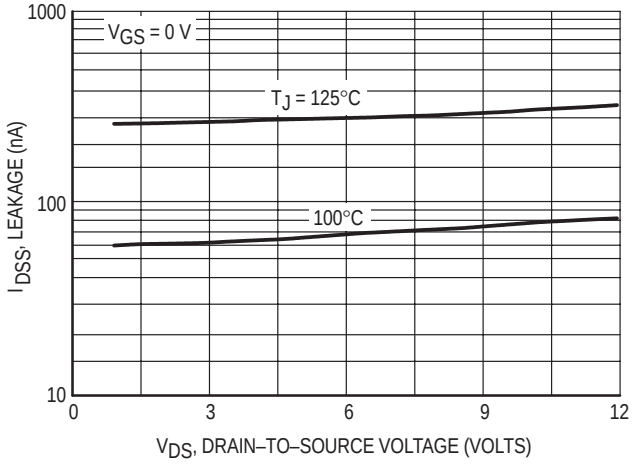

Figure 6. Drain–To–Source Leakage Current versus Voltage

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During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

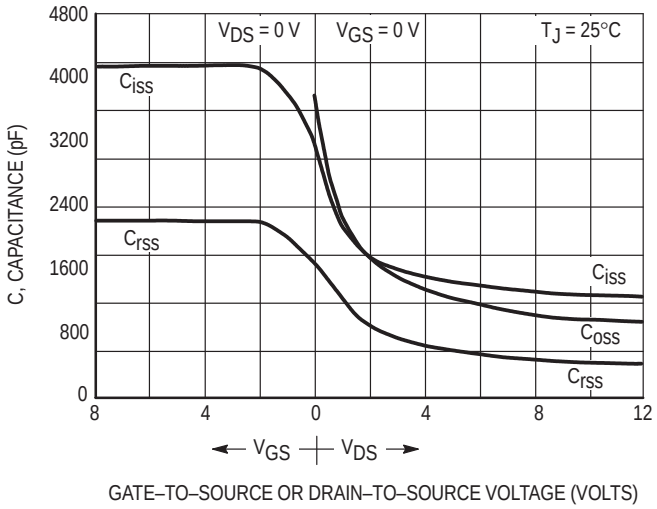


Figure 7. Capacitance Variation

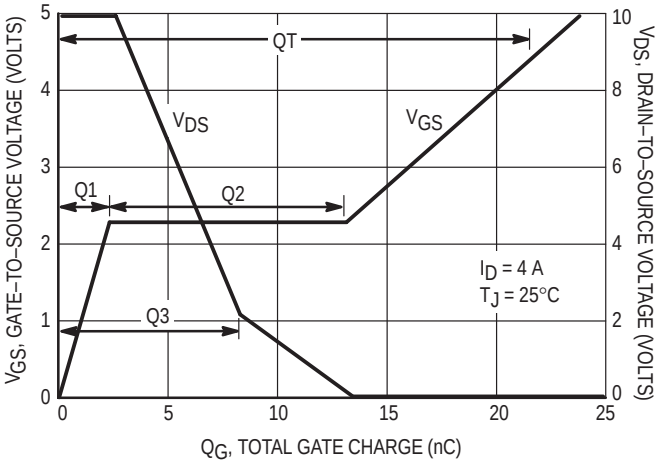


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

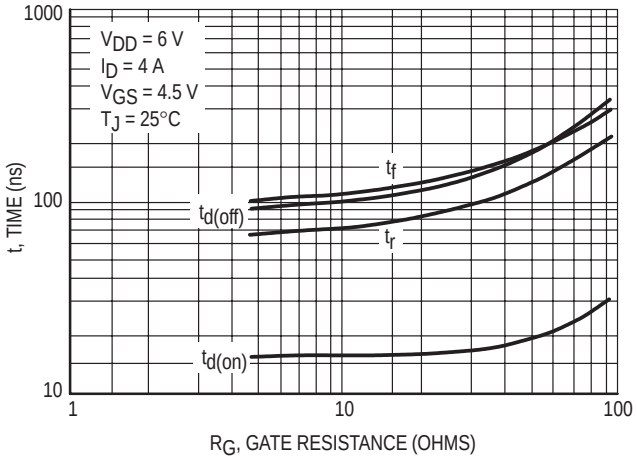


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 14. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

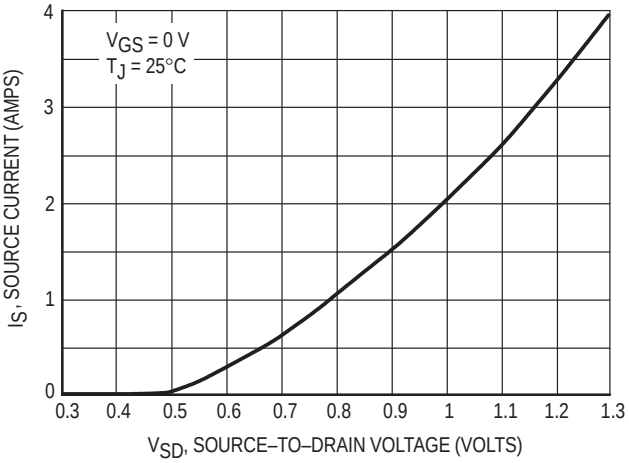


Figure 10. Diode Forward Voltage versus Current

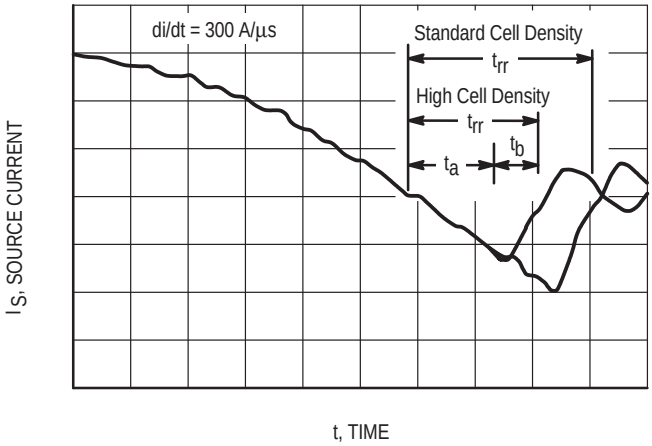


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

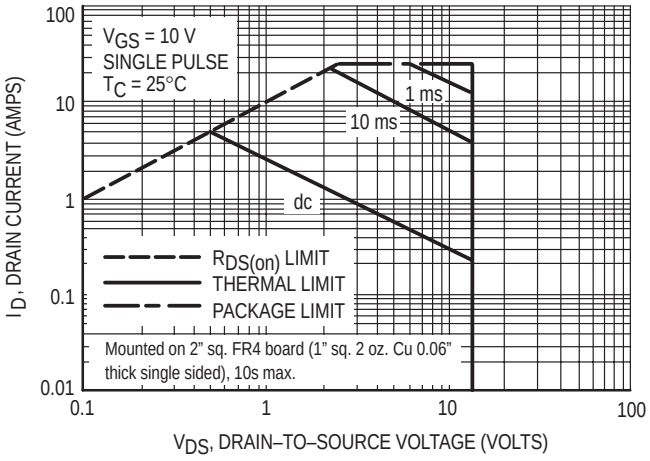


Figure 12. Maximum Rated Forward Biased Safe Operating Area

TYPICAL ELECTRICAL CHARACTERISTICS

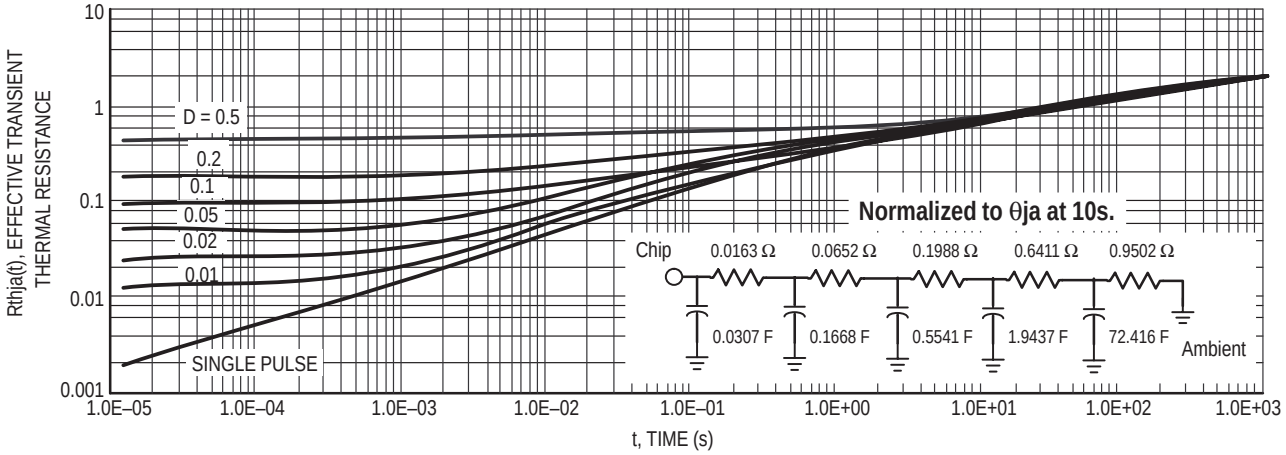


Figure 13. Thermal Response

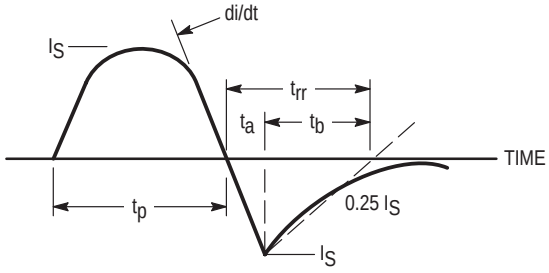


Figure 14. Diode Reverse Recovery Waveform

Advance Information

Medium Power Surface Mount Products

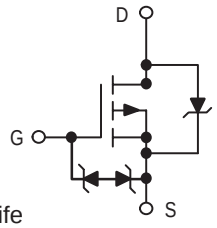
TMOS Single P-Channel with Monolithic Zener ESD Protected Gate

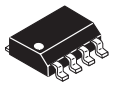
MMSF4P01Z

Motorola Preferred Device

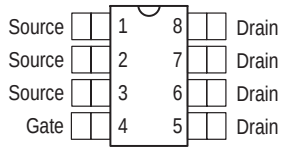
SINGLE TMOS POWER MOSFET 4.0 AMPERES 20 VOLTS $R_{DS(on)}$ = 0.070 OHM

EZFETs™ are an advanced series of power MOSFETs which utilize Motorola's High Cell Density TMOS process and contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ amd true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.





CASE 751–05, Style 12
SO–8



Top View

- Zener Protected Gates Provide Electrostatic Discharge Protection
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Designed to withstand 200V Machine Model and 2000V Human Body Model
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) *

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 8.0	Vdc
Drain Current — Continuous @ T_A = 25°C (1) — Continuous @ T_A = 70°C (1) — Pulsed Drain Current (3)	I_D I_D I_{DM}	5.7 4.0 46	Adc Apk
Total Power Dissipation @ T_A = 25°C (1) Linear Derating Factor (1)	P_D	2.5 20	Watts mW/°C
Total Power Dissipation @ T_A = 25°C (2) Linear Derating Factor (2)	P_D	1.6 12	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Thermal Resistance — Junction to Ambient (1) — Junction to Ambient (2)	$R_{\theta JA}$	50 80	°C/W

* Negative sign for P–Channel omitted for clarity.

(1) When mounted on 1 inch square FR–4 or G–10 board (V_{GS} = 4.5 V, @ 10 Seconds)
(2) When mounted on minimum recommended FR–4 or G–10 board (V_{GS} = 4.5 V, @ Steady State)
(3) Repetitive rating; pulse width limited by maximum junction temperature.

DEVICE MARKING

S4P01Z

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMSF4P01ZR2	13″	12 mm embossed tape	2500 units

This document contains information on a new product. Specifications and information are subject to change without notice.
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (1) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			20	—	—	
Temperature Coefficient (Positive)			—	16.6	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 12 Vdc, V_{GS} = 0 Vdc)			—	0.05	2.0	
(V_{DS} = 12 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	0.55	10	
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0)		I_{GSS}	—	0.15	5.0	μAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (1) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			0.7	0.85	1.1	
Threshold Temperature Coefficient (Negative)			—	2.5	—	mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (1) (3)		$R_{DS(on)}$				mΩ
(V_{GS} = 4.5 Vdc, I_D = 4.0 Adc)			—	50	70	
(V_{GS} = 2.7 Vdc, I_D = 2.0 Adc)			—	70	90	
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 2.0 Adc) (1)		g_{FS}	4.0	7.5	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 10 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	270	540	pF
Output Capacitance		C_{oss}	—	825	1650	
Transfer Capacitance		C_{rss}	—	100	200	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 6.0 Vdc, I_D = 4.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω) (1)	$t_{d(on)}$	—	150	300	ns
Rise Time		t_r	—	800	1600	
Turn–Off Delay Time		$t_{d(off)}$	—	1420	2840	
Fall Time		t_f	—	1830	3660	
Turn–On Delay Time	(V_{DD} = 6.0 Vdc, I_D = 4.0 Adc, V_{GS} = 2.7 Vdc, R_G = 6.0 Ω) (1)	$t_{d(on)}$	—	260	520	ns
Rise Time		t_r	—	1950	3900	
Turn–Off Delay Time		$t_{d(off)}$	—	600	1200	
Fall Time		t_f	—	1390	2780	
Gate Charge	(V_{DS} = 10 Vdc, I_D = 4.0 Adc, V_{GS} = 4.5 Vdc) (1)	Q_T	—	24	34	nC
		Q_1	—	3.0	—	
		Q_2	—	11	—	
		Q_3	—	8.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc) (1)	V_{SD}				Vdc
	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.1	1.8	
			—	0.75	—	
Reverse Recovery Time	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (1)	t_{rr}	—	373	—	ns
		t_a	—	750	—	
		t_b	—	1120	—	
Reverse Recovery Storage Charge		Q_{RR}	—	9.0	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

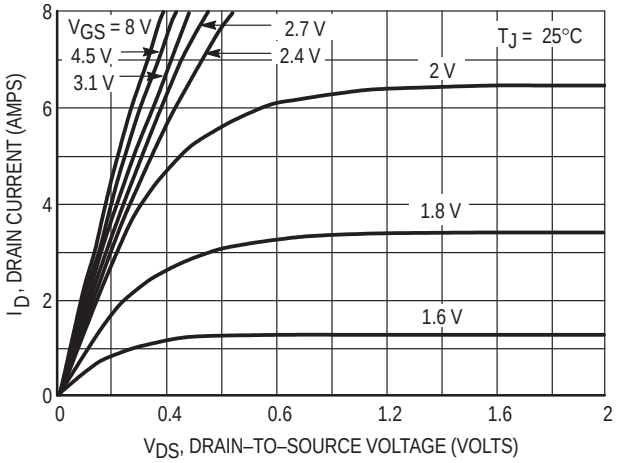


Figure 1. On–Region Characteristics

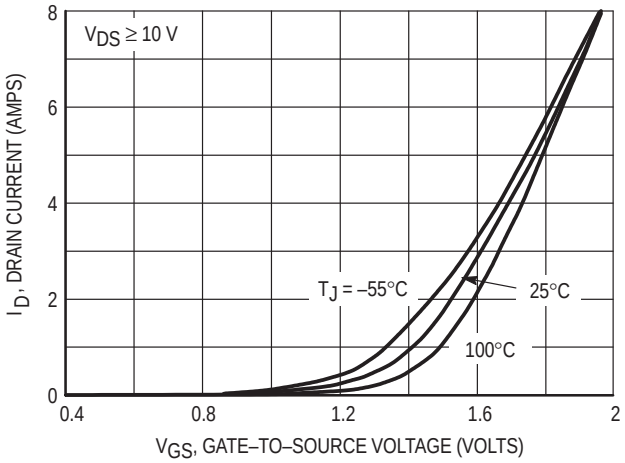


Figure 2. Transfer Characteristics

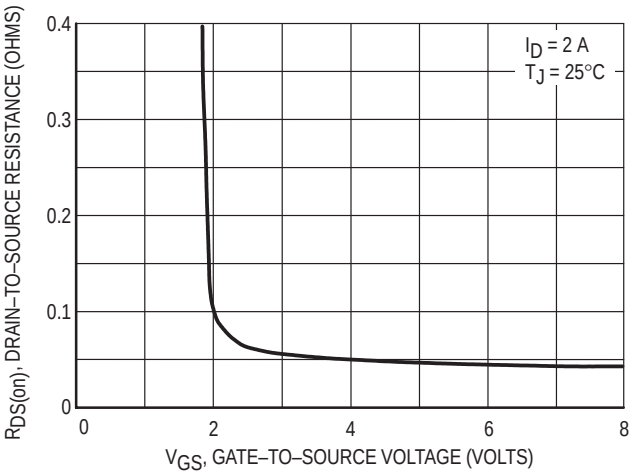


Figure 3. On–Resistance versus Gate–to–Source Voltage

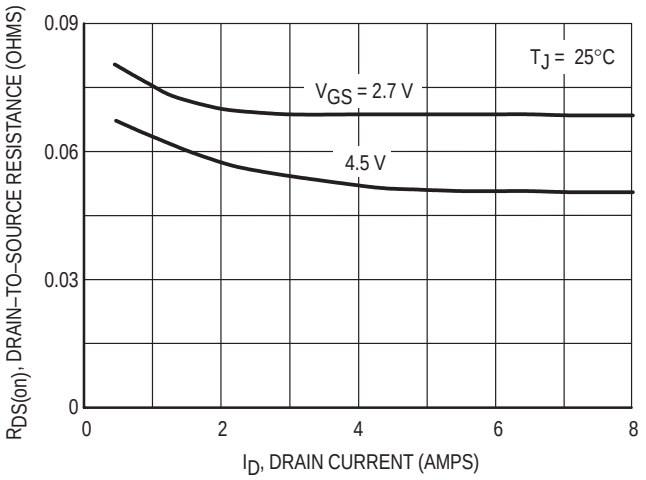


Figure 4. On–Resistance versus Drain Current and Gate Voltage

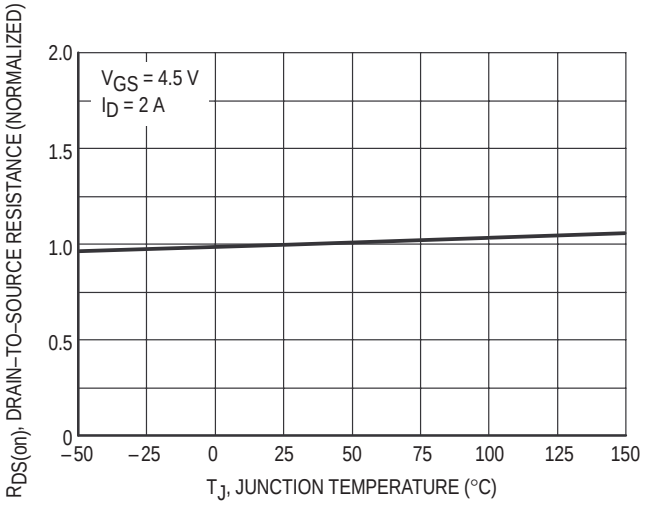


Figure 5. On–Resistance Variation with Temperature

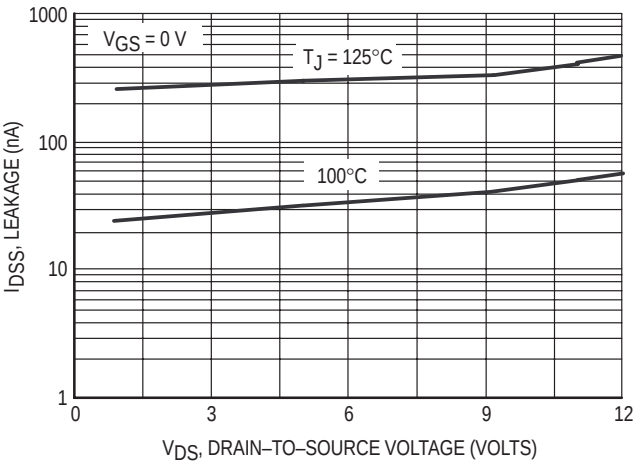


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

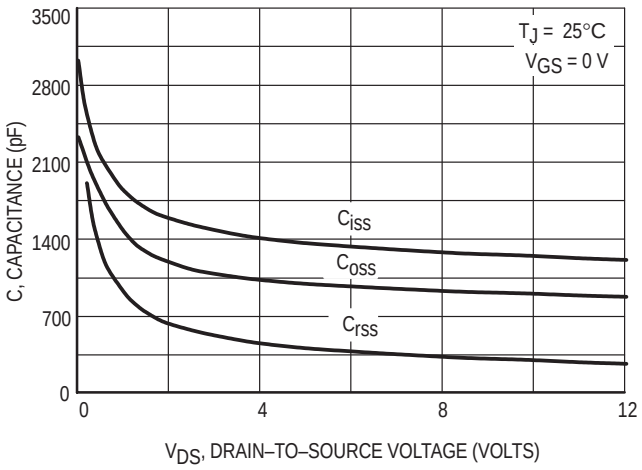


Figure 7. Capacitance Variation

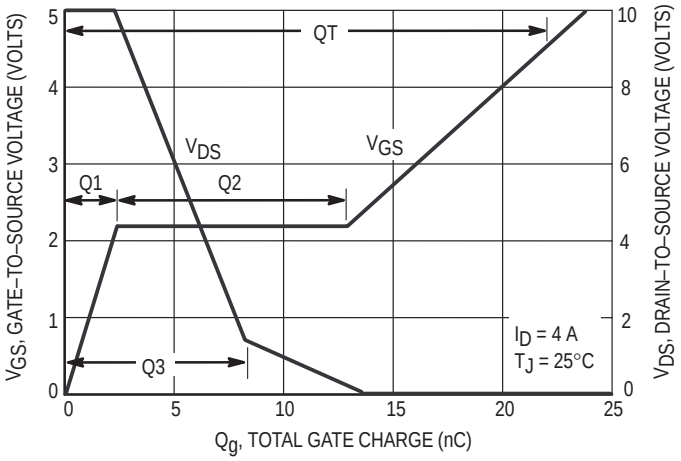


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

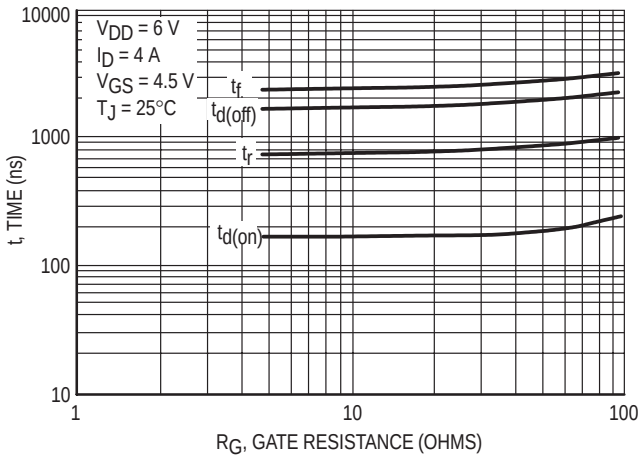


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

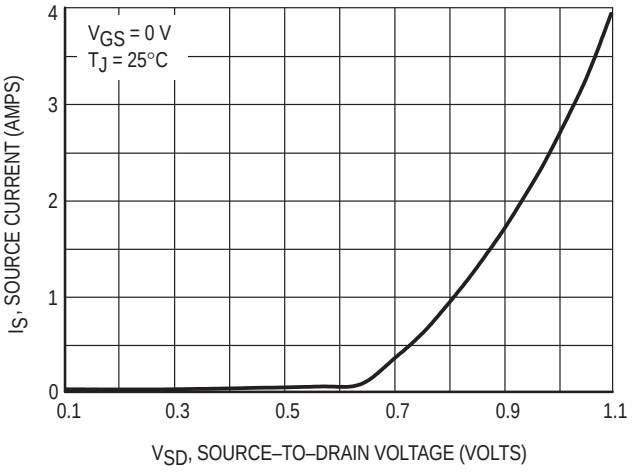


Figure 10. Diode Forward Voltage versus Current

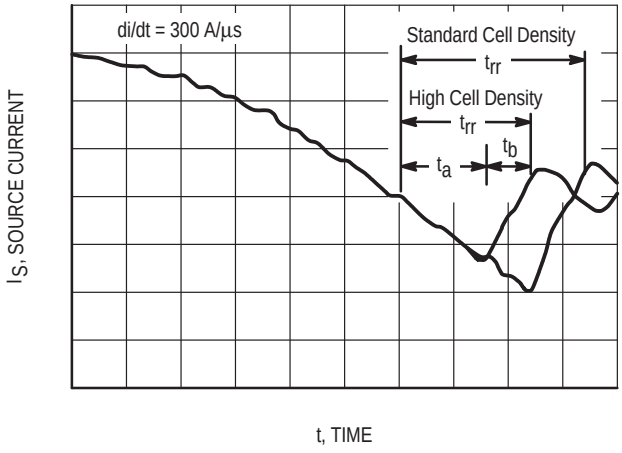


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature. Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

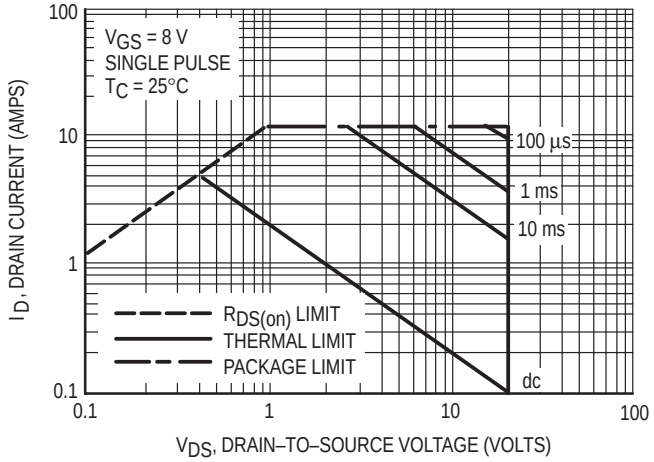


Figure 12. Maximum Rated Forward Biased Safe Operating Area

TYPICAL ELECTRICAL CHARACTERISTICS

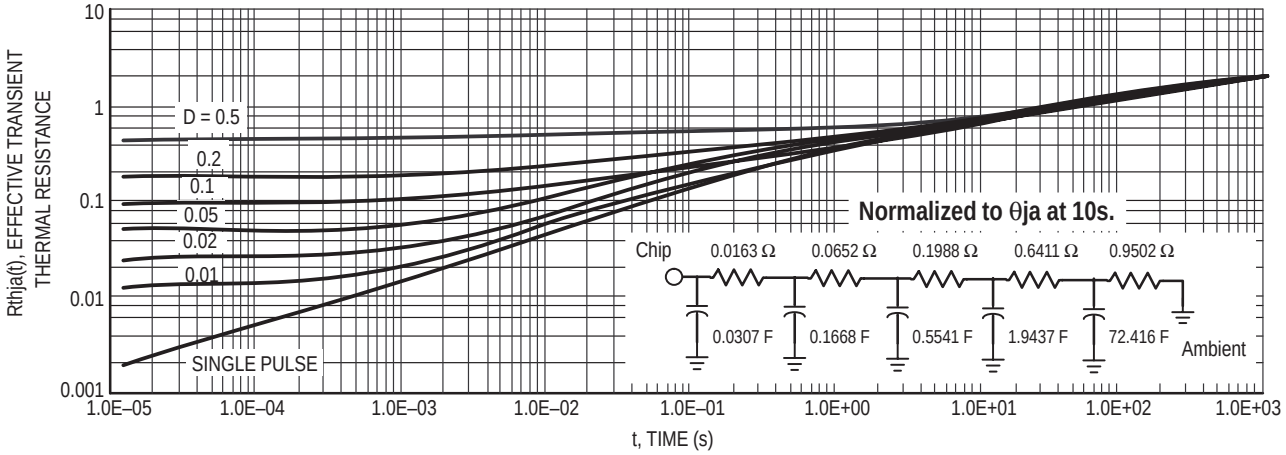


Figure 13. Thermal Response

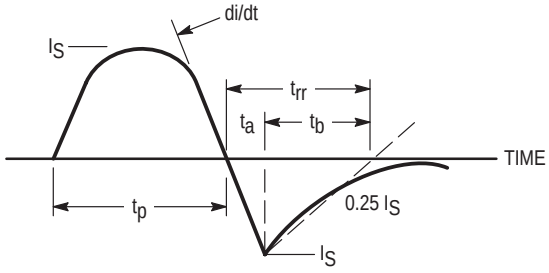


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

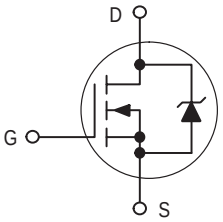
TMOS Single N-Channel Field Effect Transistors

MMSF5N02HD

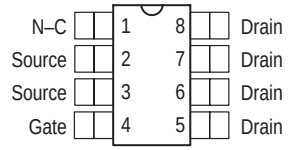
Motorola Preferred Device

SINGLE TMOS POWER MOSFET 5.0 AMPERES 20 VOLTS $R_{DS(on)}$ = 0.025 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.



CASE 751–05, Style 13
SO–8



Top View

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	8.2 5.6 41	Adc Apk
Total Power Dissipation @ T_A = 25°C (1)	P_D	2.5	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 20 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 15 Apk, L = 6.0 mH, R_G = 25 Ω)	E_{AS}	675	mJ
Thermal Resistance — Junction to Ambient (1)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

S5N02

(1) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided), 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMSF5N02HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 20 —	 — 41	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 20 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 0.02 —	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 —	 1.5 4.0	 2.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc) (V_{GS} = 4.5 Vdc, I_D = 2.5 Adc)		$R_{DS(on)}$	 — —	 0.0185 0.0219	 0.025 0.040	Ohm
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.5 Adc)		g_{FS}	3.0	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1130	1582	pF
Output Capacitance		C_{oss}	—	464	650	
Transfer Capacitance		C_{rss}	—	117	235	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 5.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	15	30	ns
Rise Time		t_r	—	93	185	
Turn–Off Delay Time		$t_{d(off)}$	—	35	70	
Fall Time		t_f	—	40	80	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 5.0 Adc, V_{GS} = 10 Vdc, R_G = 6.0 Ω)	$t_{d(on)}$	—	9.0	—	
Rise Time		t_r	—	53	—	
Turn–Off Delay Time		$t_{d(off)}$	—	56	—	
Fall Time		t_f	—	39	—	
Gate Charge See Figure 8	(V_{DS} = 16 Vdc, I_D = 5.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	30.3	43	nC
		Q_1	—	3.0	—	
		Q_2	—	7.5	—	
		Q_3	—	6.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 5.0 Adc, V_{GS} = 0 Vdc) (I_S = 5.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 0.82 0.69	 1.0 —	Vdc
Reverse Recovery Time See Figure 15	(I_S = 5.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	32	—	ns
		t_a	—	24	—	
		t_b	—	8.0	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.045	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

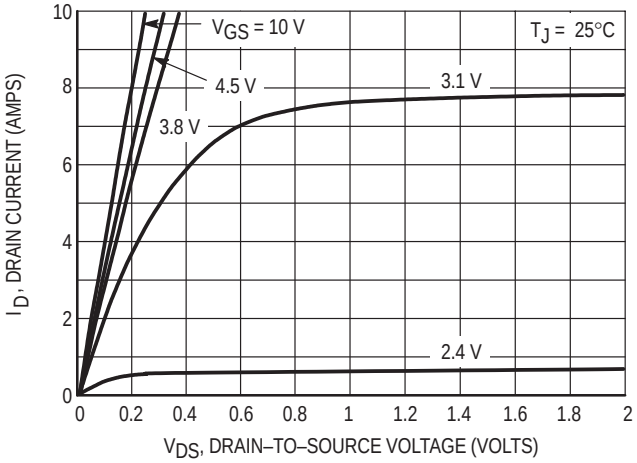


Figure 1. On–Region Characteristics

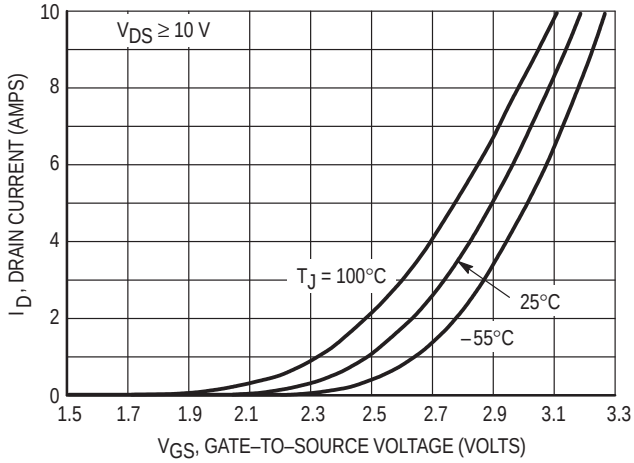


Figure 2. Transfer Characteristics

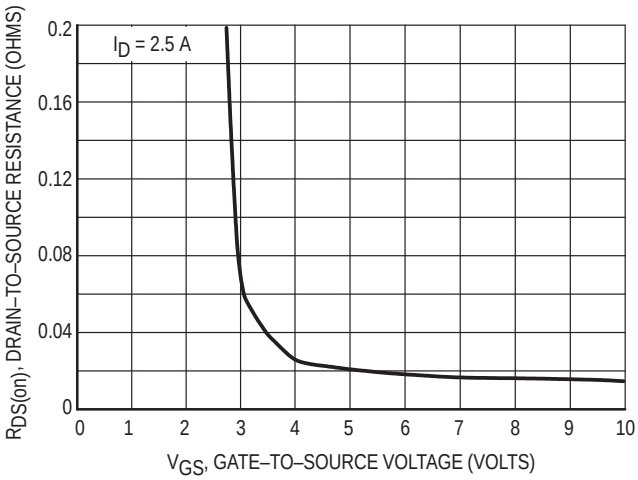


Figure 3. On–Resistance versus Gate–to–Source Voltage

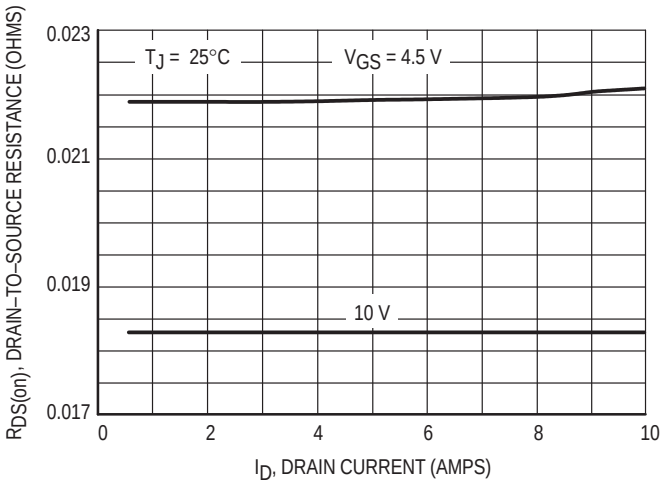


Figure 4. On–Resistance versus Drain Current and Gate Voltage

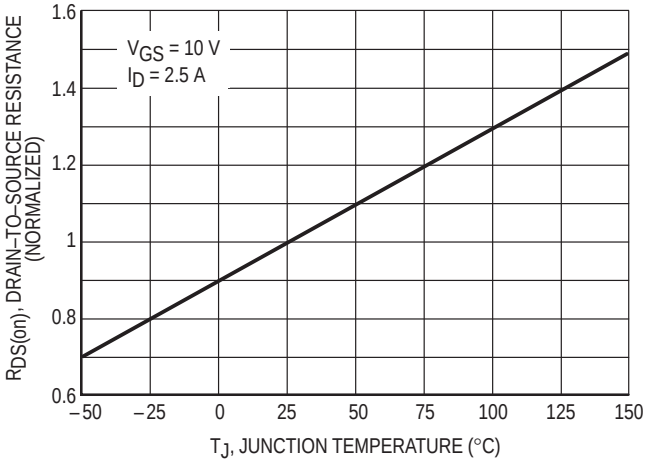


Figure 5. On–Resistance Variation with Temperature

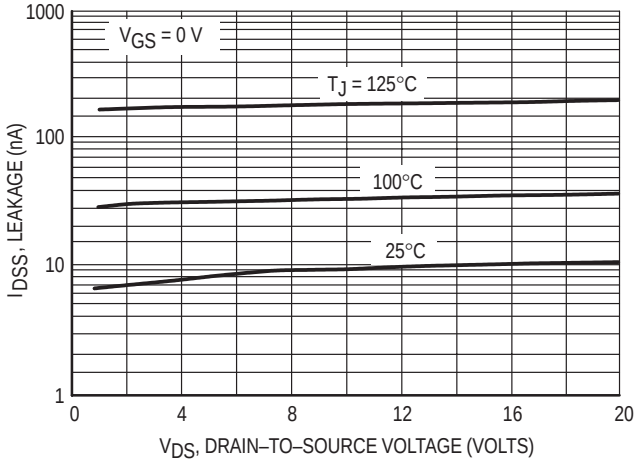


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

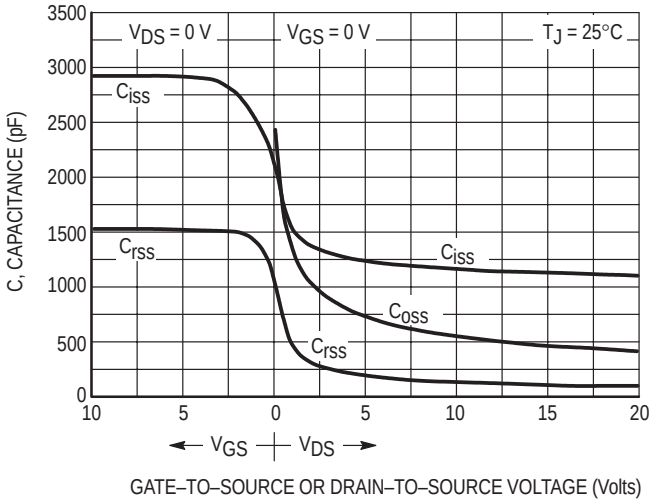


Figure 7. Capacitance Variation

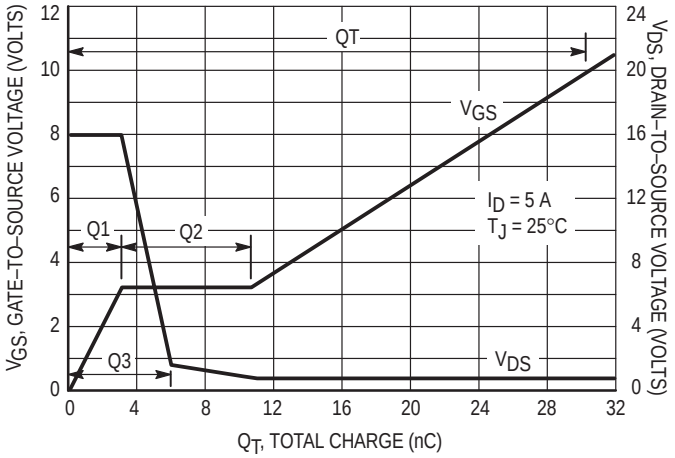


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

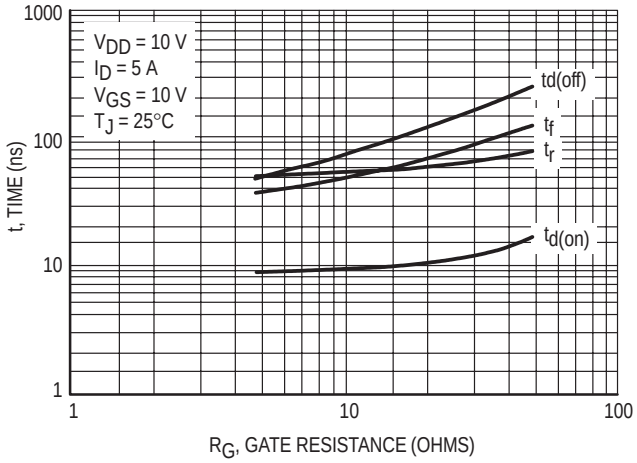


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

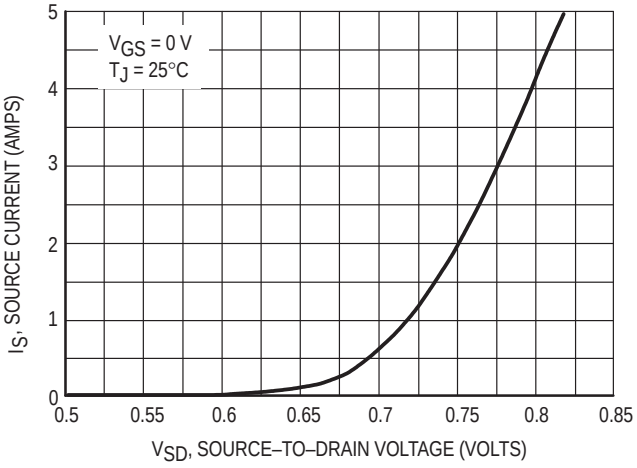


Figure 10. Diode Forward Voltage versus Current

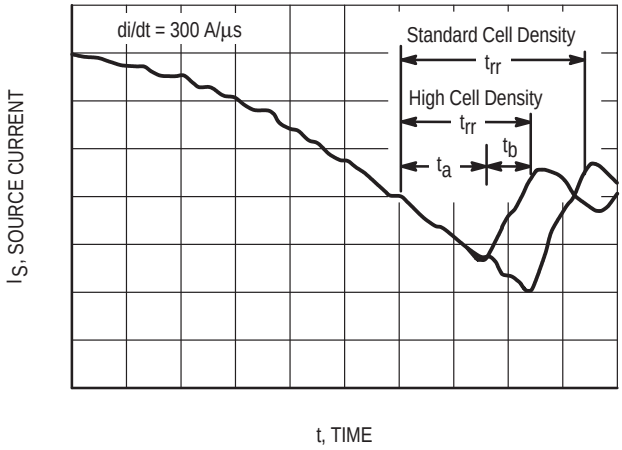


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

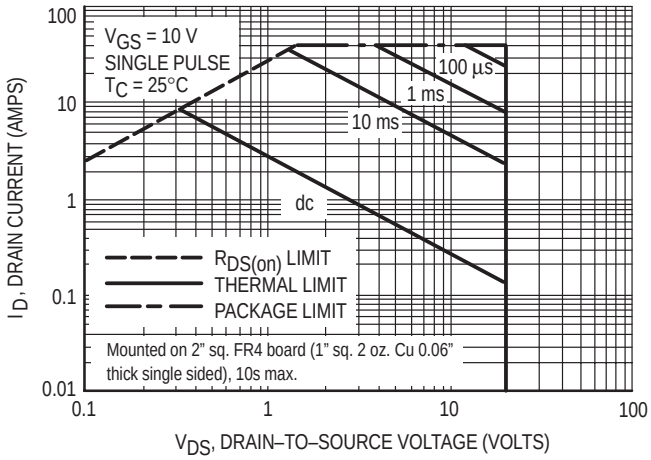


Figure 12. Maximum Rated Forward Biased Safe Operating Area

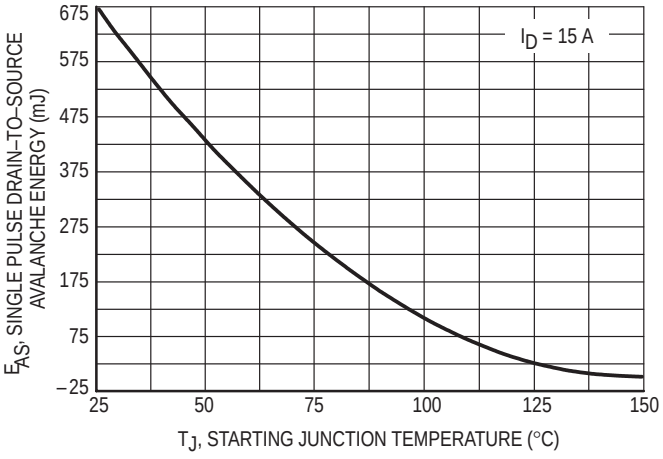


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

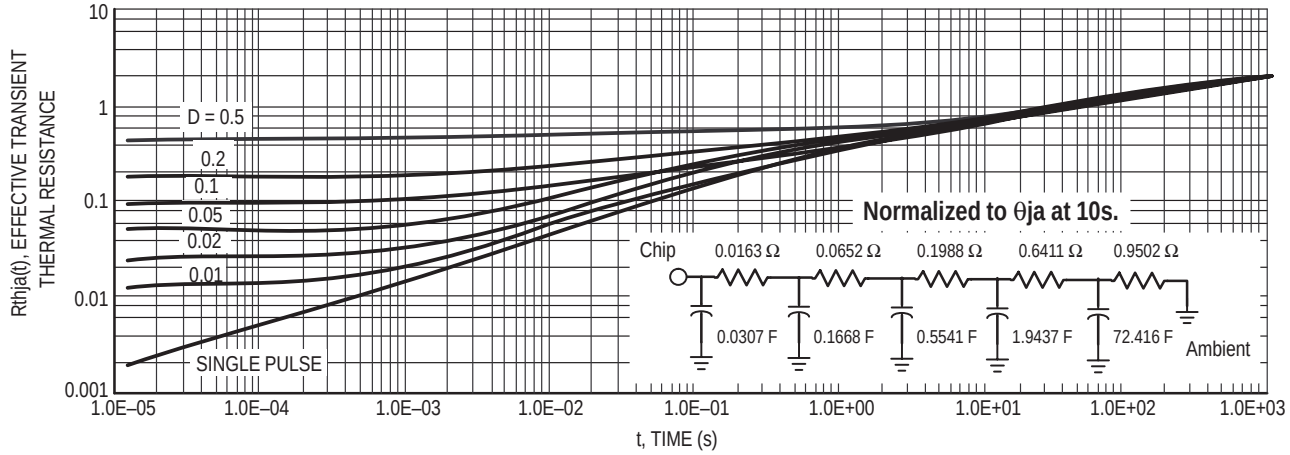


Figure 14. Thermal Response

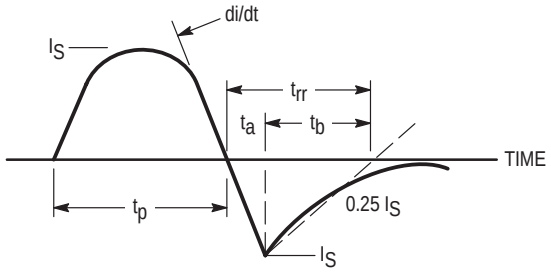


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

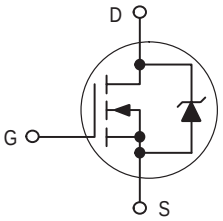
TMOS Single N-Channel Field Effect Transistors

MMSF5N03HD

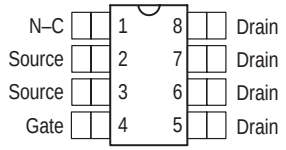
Motorola Preferred Device

SINGLE TMOS
POWER MOSFET
5.0 AMPERES
30 VOLTS
$R_{DS(on)}$ = 0.040 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.



CASE 751–05, Style 13
SO–8



Top View

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	30	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	6.5 4.4 33	Adc Apk
Total Power Dissipation @ T_A = 25°C (1)	P_D	2.5	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 30 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 15 Apk, L = 4.0 mH, R_G = 25 Ω)	E_{AS}	450	mJ
Thermal Resistance — Junction to Ambient (1)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

S5N03

(1) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided), 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMSF5N03HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 4

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 30 —	 — 34	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 —	 2.0 5.0	 3.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc) (V_{GS} = 4.5 Vdc, I_D = 2.5 Adc)		$R_{DS(on)}$	 — —	 0.033 0.04	 0.040 0.050	Ohms
Forward Transconductance (V_{DS} = 3 Vdc, I_D = 2.5 Adc)		g_{FS}	3.0	8.0	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1207	1680	pF
Output Capacitance		C_{oss}	—	354	490	
Transfer Capacitance		C_{rss}	—	62	120	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 5.0 Adc, V_{GS} = 4.5 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	20	40	ns
Rise Time		t_r	—	108	216	
Turn–Off Delay Time		$t_{d(off)}$	—	36	72	
Fall Time		t_f	—	37	74	
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 5.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	11	22	
Rise Time		t_r	—	36	72	
Turn–Off Delay Time		$t_{d(off)}$	—	68	136	
Fall Time		t_f	—	38	76	
Gate Charge See Figure 8	(V_{DS} = 24 Vdc, I_D = 5.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	15.2	21	nC
		Q_1	—	3.4	—	
		Q_2	—	6.6	—	
		Q_3	—	5.6	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 5 Adc, V_{GS} = 0 Vdc) (I_S = 5 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 0.88 0.77	 1.3 —	Vdc
Reverse Recovery Time See Figure 15	(I_S = 5.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	33	—	ns
		t_a	—	21	—	
		t_b	—	12	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.037	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

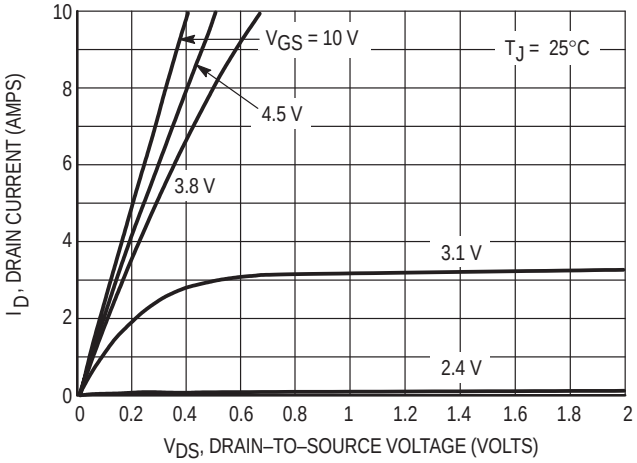


Figure 1. On–Region Characteristics

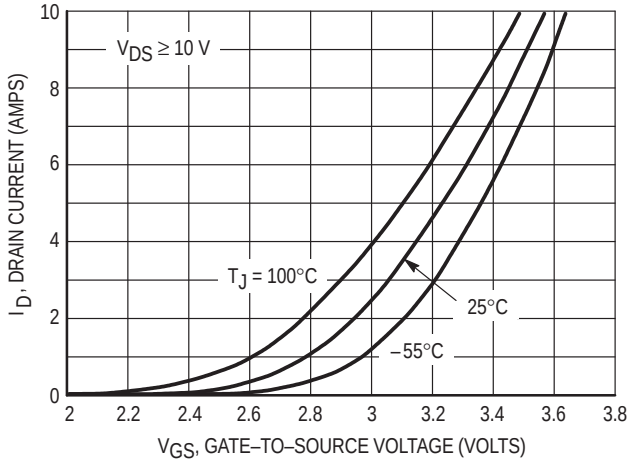


Figure 2. Transfer Characteristics

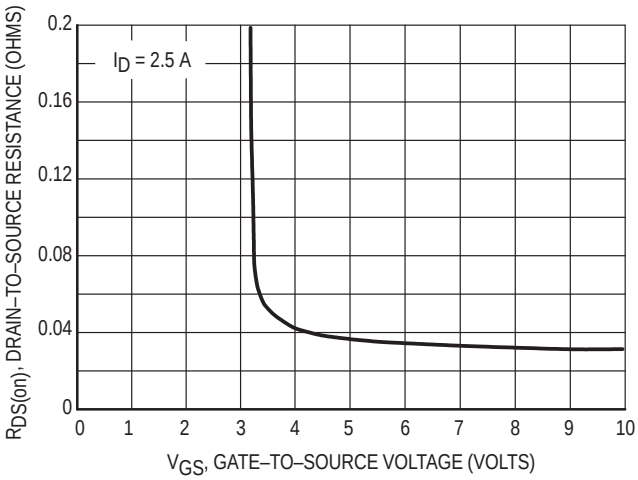


Figure 3. On–Resistance versus Gate–To–Source Voltage

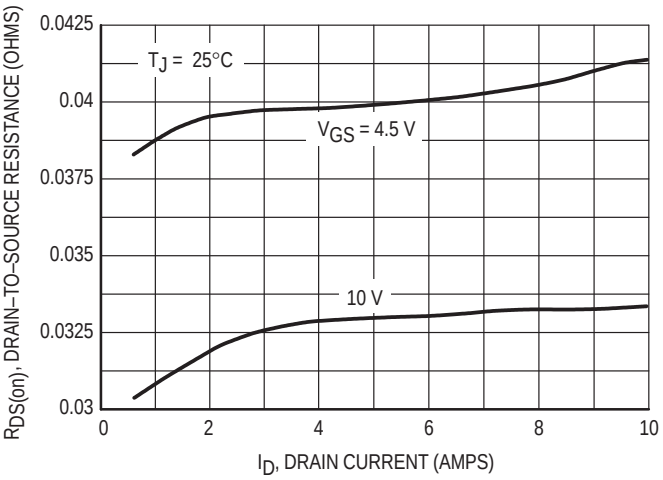


Figure 4. On–Resistance versus Drain Current and Gate Voltage

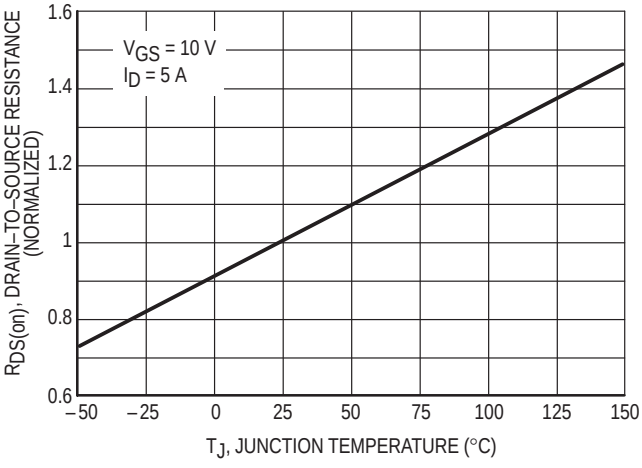


Figure 5. On–Resistance Variation with Temperature

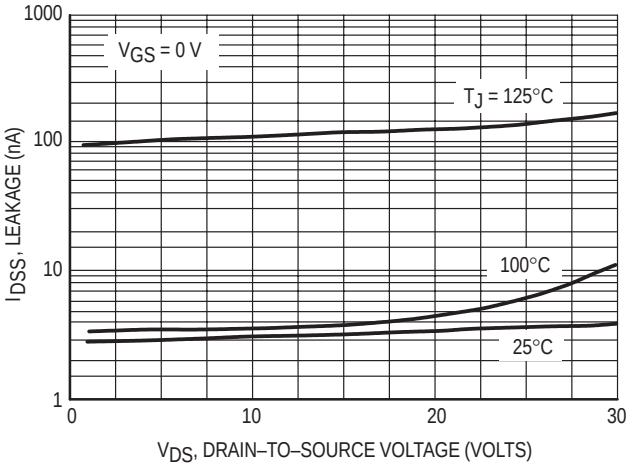


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

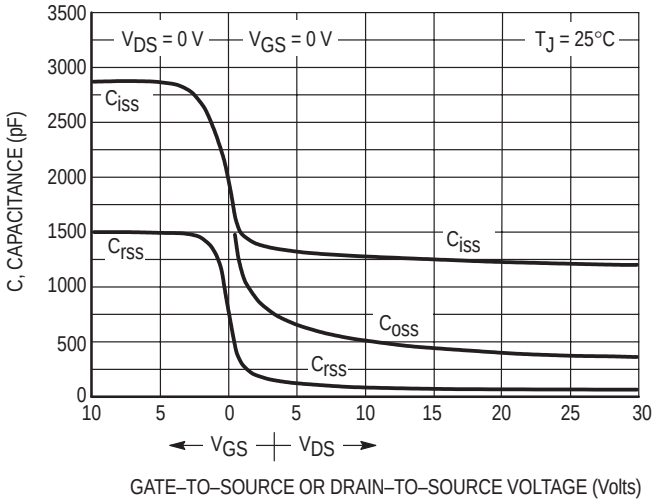


Figure 7. Capacitance Variation

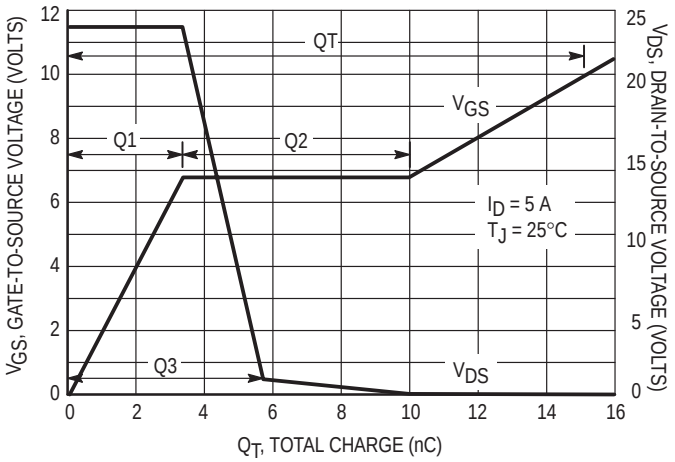


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

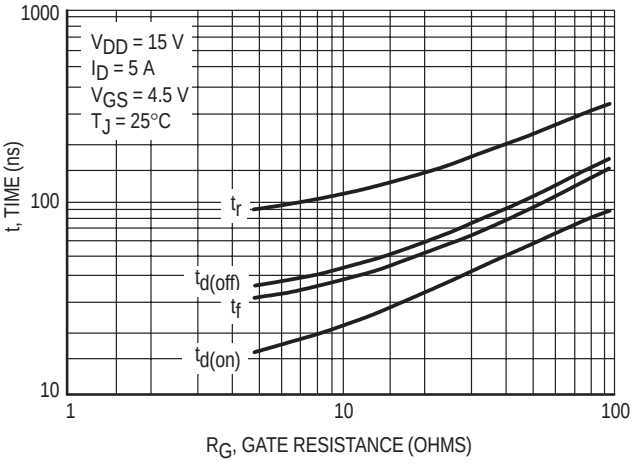


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

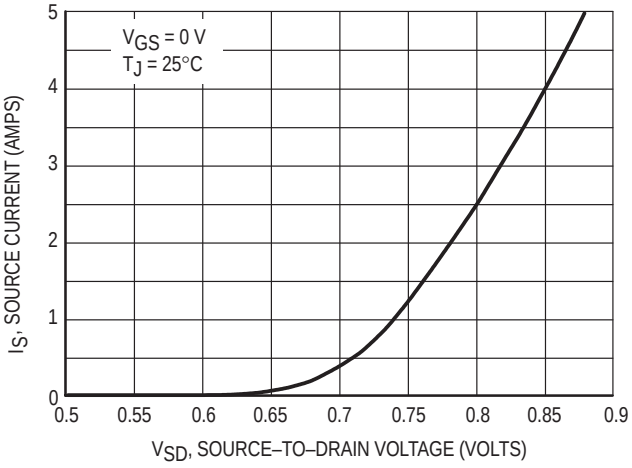


Figure 10. Diode Forward Voltage versus Current

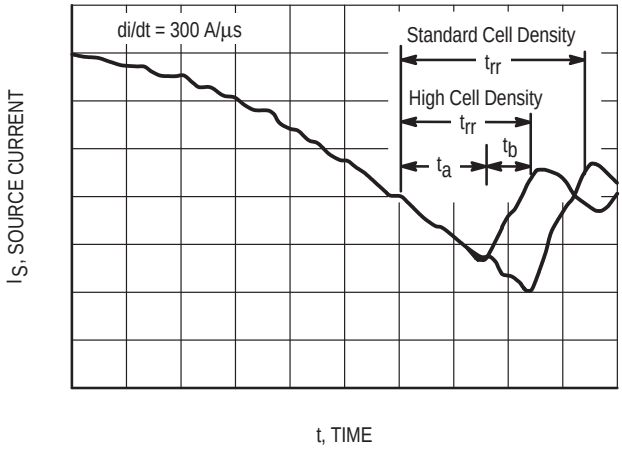


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

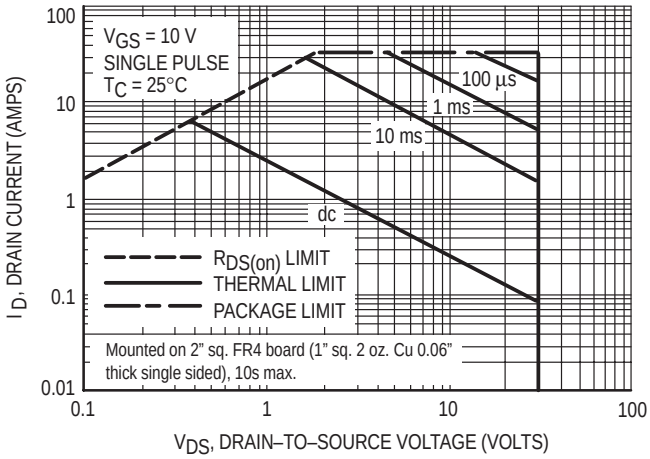


Figure 12. Maximum Rated Forward Biased Safe Operating Area

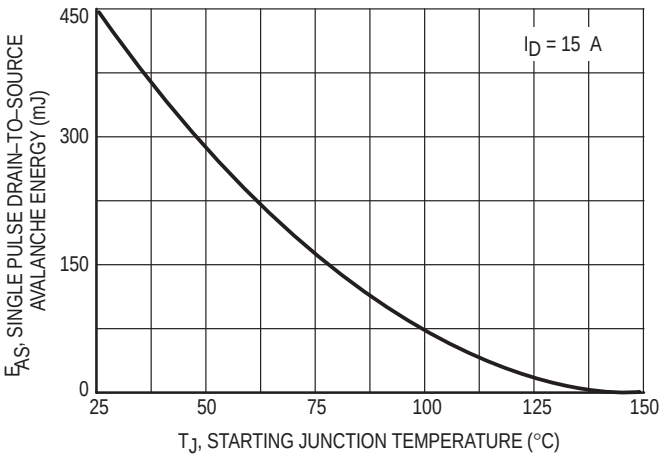


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

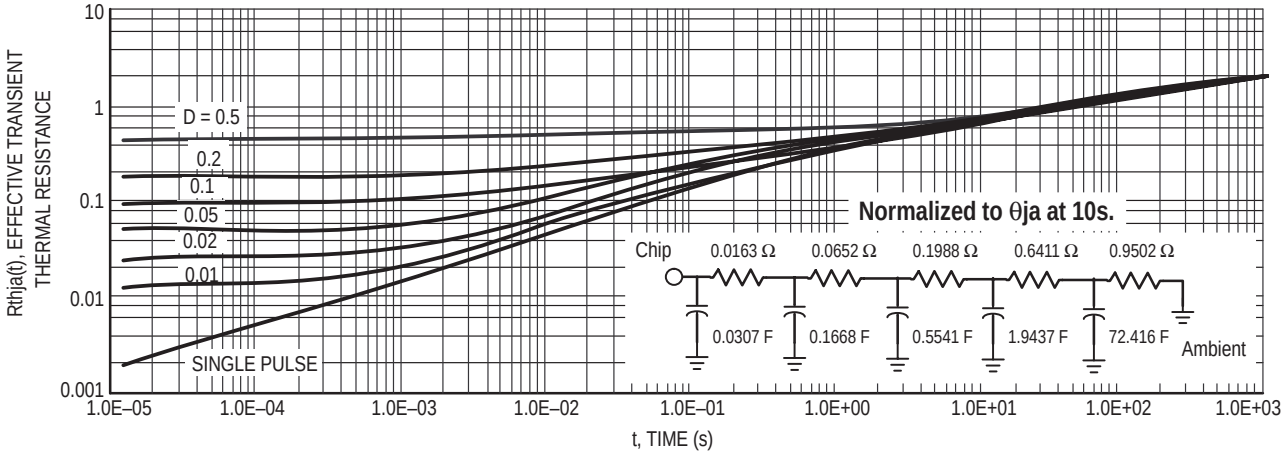


Figure 14. Thermal Response

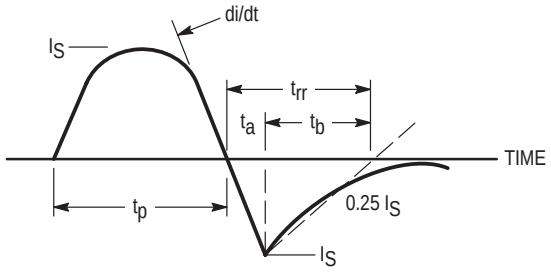


Figure 15. Diode Reverse Recovery Waveform

Advance Information

Medium Power Surface Mount Products

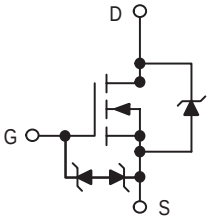
TMOS Single N-Channel with Monolithic Zener ESD Protected Gate

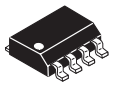
MMSF5N03Z

Motorola Preferred Device

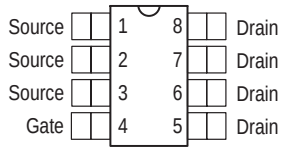
SINGLE TMOS POWER MOSFET 5.0 AMPERES 30 VOLTS $R_{DS(on)}$ = 0.030 OHM

EZFETs™ are an advanced series of power MOSFETs which utilize Motorola's High Cell Density TMOS process and contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ amd true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.





CASE 751–05, Style 12
SO–8



Top View

- Zener Protected Gates Provide Electrostatic Discharge Protection
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Designed to withstand 200V Machine Model and 2000V Human Body Model
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	30	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 15	Vdc
Drain Current — Continuous @ T_A = 25°C (1) — Continuous @ T_A = 70°C (1) — Pulsed Drain Current (3)	I_D I_D I_{DM}	7.5 5.6 60	Adc Apk
Total Power Dissipation @ T_A = 25°C (1) Linear Derating Factor (1)	P_D	2.5 20	Watts mW/°C
Total Power Dissipation @ T_A = 25°C (2) Linear Derating Factor (2)	P_D	1.6 12	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 30 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 15 Apk, L = 4.0 mH, R_G = 25 Ω)	E_{AS}	450	mJ
Thermal Resistance — Junction to Ambient (1) — Junction to Ambient (2)	$R_{\theta JA}$	50 80	°C/W

(1) When mounted on 1 inch square FR–4 or G–10 board (V_{GS} = 10 V, @ Steady State)
(2) When mounted on minimum recommended FR–4 or G–10 board (V_{GS} = 10 V, @ Steady State)
(3) Repetitive rating; pulse width limited by maximum junction temperature.

DEVICE MARKING

S5N03Z

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMSF5N03ZR2	13″	12 mm embossed tape	2500 units

This document contains information on a new product. Specifications and information are subject to change without notice.
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (1) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			30	—	—	
Temperature Coefficient (Positive)			—	35	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 30 Vdc, V_{GS} = 0 Vdc)			—	0.03	2.0	
(V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	0.15	10	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0)		I_{GSS}	—	1.3	5.0	μAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (1) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			1.0	2.0	3.0	
Threshold Temperature Coefficient (Negative)			—	5.5	—	mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (1) (3)		$R_{DS(on)}$				mΩ
(V_{GS} = 10 Vdc, I_D = 5.0 Adc)			—	22	30	
(V_{GS} = 4.5 Vdc, I_D = 2.5 Adc)			—	30	40	
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 2.5 Adc) (1)		g_{FS}	4.0	9.5	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	750	1500	pF
Output Capacitance		C_{oss}	—	340	680	
Transfer Capacitance		C_{rss}	—	45	90	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DS} = 15 Vdc, I_D = 5.0 Adc, V_{GS} = 10 Vdc, R_G = 6 Ω) (1)	$t_{d(on)}$	—	40	80	ns
Rise Time		t_r	—	90	180	
Turn–Off Delay Time		$t_{d(off)}$	—	470	940	
Fall Time		t_f	—	170	340	
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 5.0 Adc, V_{GS} = 4.5 Vdc, R_G = 6 Ω) (1)	$t_{d(on)}$	—	120	240	ns
Rise Time		t_r	—	350	700	
Turn–Off Delay Time		$t_{d(off)}$	—	430	860	
Fall Time		t_f	—	140	280	
Gate Charge	(V_{DS} = 24 Vdc, I_D = 5.0 Adc, V_{GS} = 10 Vdc) (1)	Q_T	—	34	48	nC
		Q_1	—	3.5	—	
		Q_2	—	9.5	—	
		Q_3	—	6.5	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 5.0 Adc, V_{GS} = 0 Vdc) (1)	V_{SD}				Vdc
	(I_S = 5.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.83	1.6	
			—	0.67	—	
Reverse Recovery Time	(I_S = 5.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (1)	t_{rr}	—	110	—	ns
		t_a	—	22	—	
		t_b	—	90	—	
Reverse Recovery Storage Charge		Q_{RR}	—	0.17	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

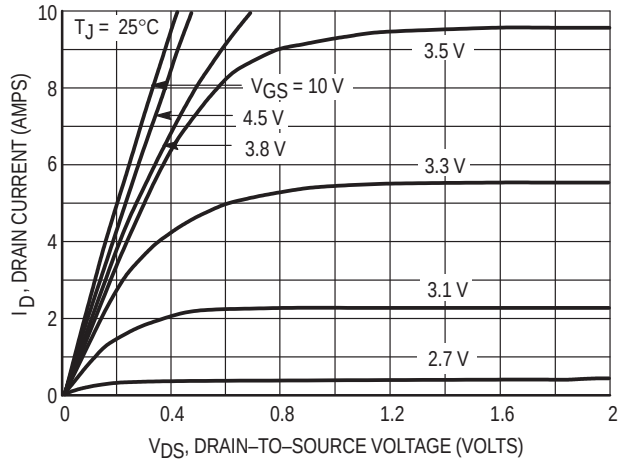


Figure 1. On–Region Characteristics

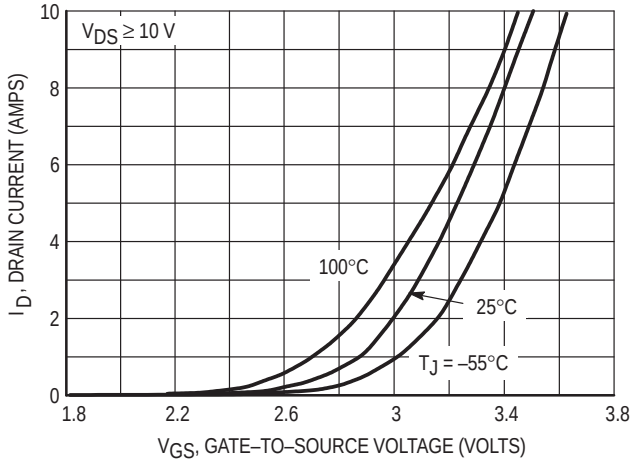


Figure 2. Transfer Characteristics

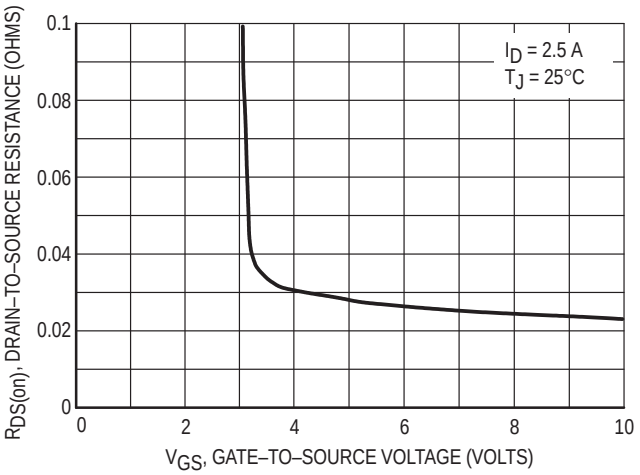


Figure 3. On–Resistance versus Gate–to–Source Voltage

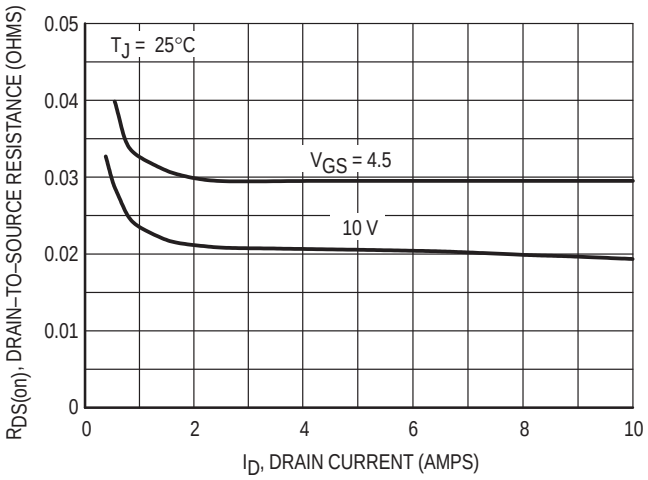


Figure 4. On–Resistance versus Drain Current and Gate Voltage

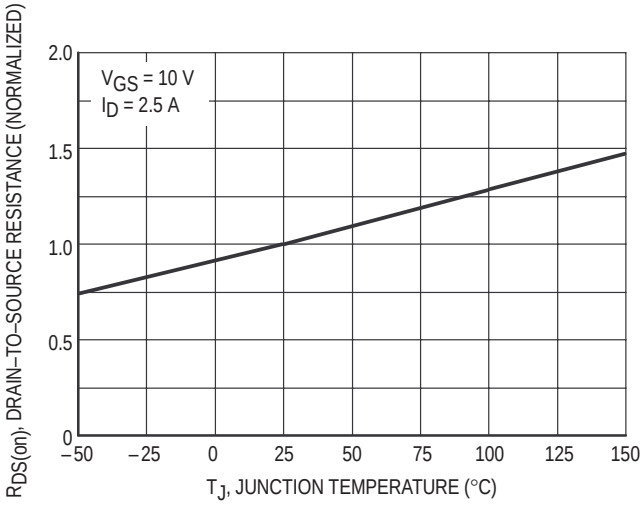


Figure 5. On–Resistance Variation with Temperature

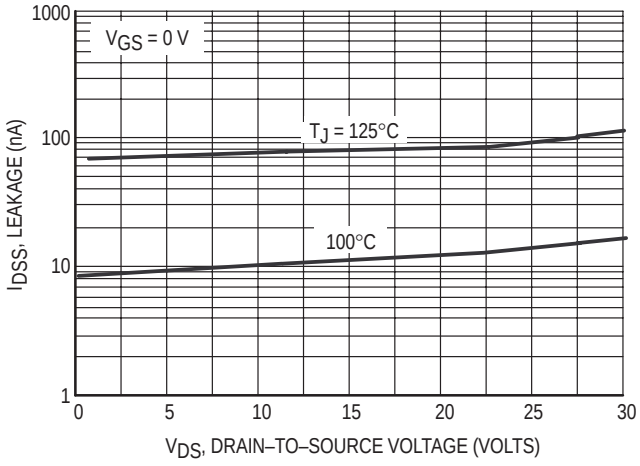


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

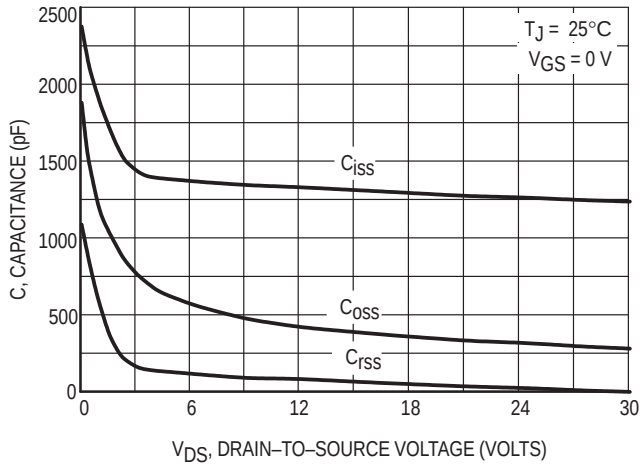


Figure 7. Capacitance Variation

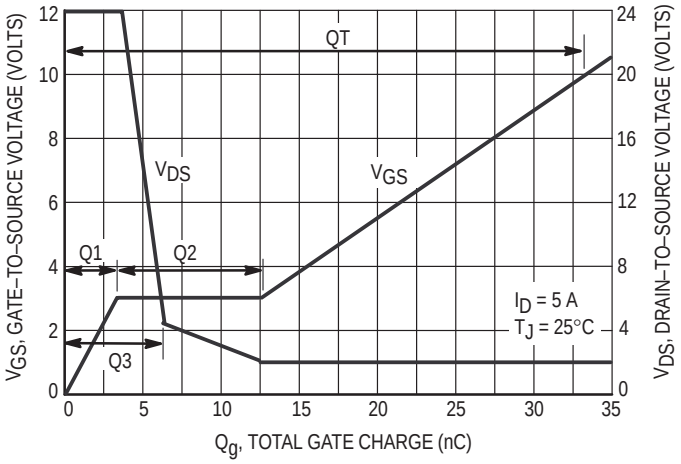


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

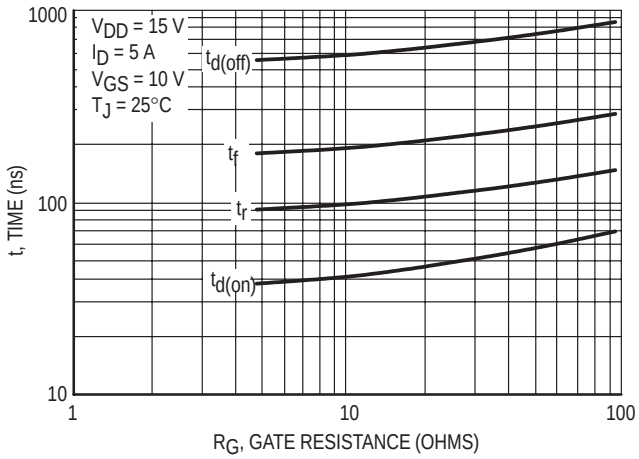


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

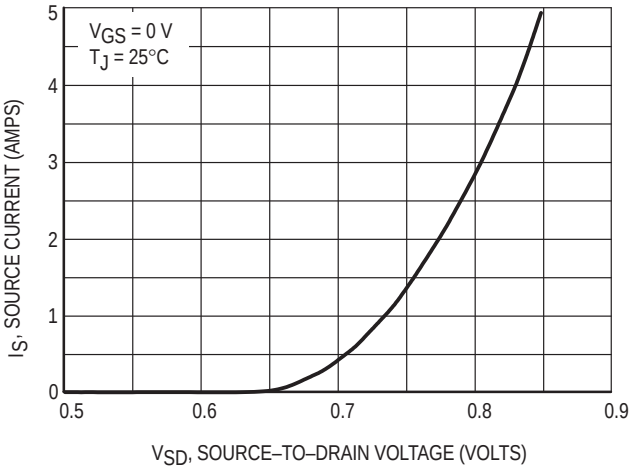


Figure 10. Diode Forward Voltage versus Current

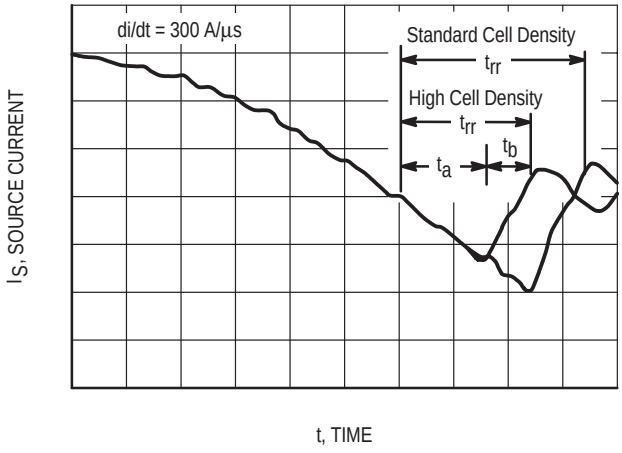


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

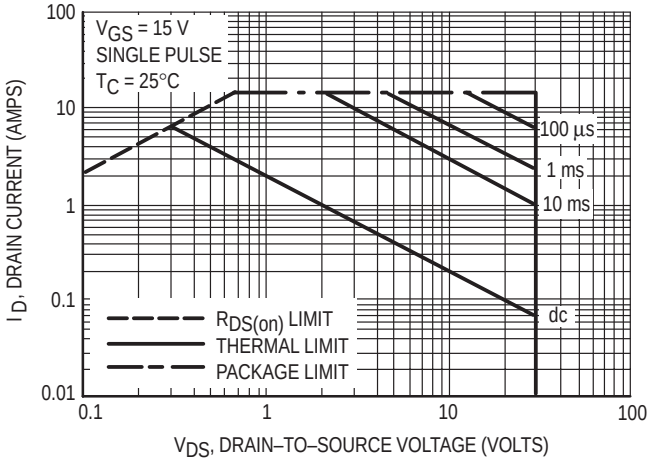


Figure 12. Maximum Rated Forward Biased Safe Operating Area

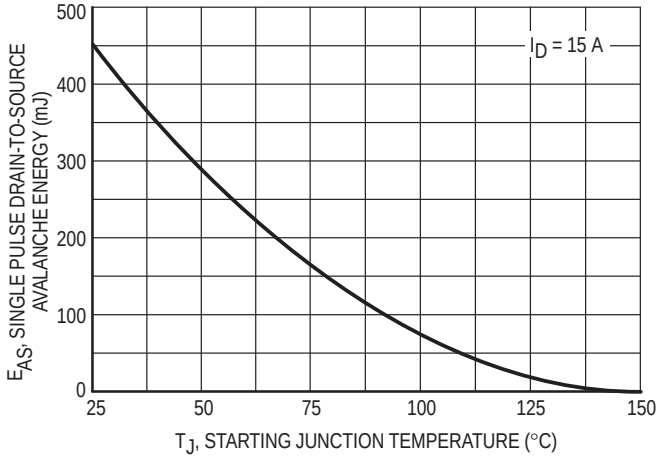


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

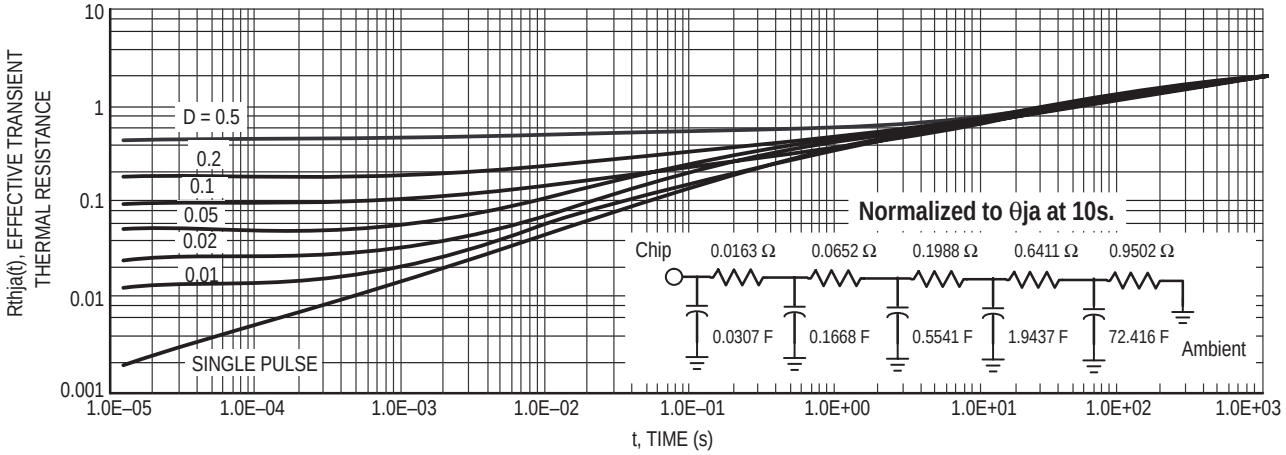


Figure 14. Thermal Response

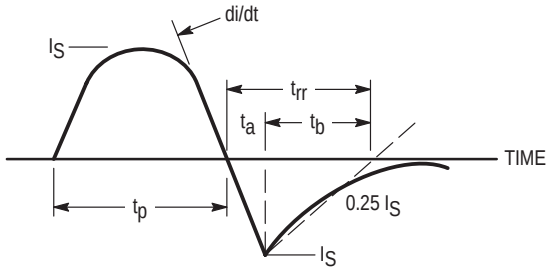


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Medium Power Surface Mount Products

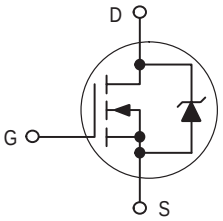
TMOS Single N-Channel Field Effect Transistors

MMSF7N03HD

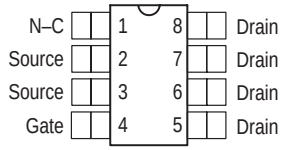
Motorola Preferred Device

SINGLE TMOS POWER MOSFET 8.0 AMPERES 30 VOLTS $R_{DS(on)}$ = 0.028 OHM

MiniMOS™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.



CASE 751–05, Style 13
SO–8



Top View

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package — Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	30	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C — Continuous @ T_A = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	8.2 5.6 50	Adc Apk
Total Power Dissipation @ T_A = 25°C (1)	P_D	2.5	Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 30 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 15 Apk, L = 4.0 mH, R_G = 25 Ω)	E_{AS}	450	mJ
Thermal Resistance — Junction to Ambient (1)	$R_{\theta JA}$	50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

DEVICE MARKING

S7N03

(1) Mounted on 2" square FR4 board (1" sq. 2 oz. Cu 0.06" thick single sided), 10 sec. max.

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MMSF7N03HDR2	13″	12 mm embossed tape	2500 units

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 30 —	 — 41	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 0.02 —	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 —	 1.5 4.0	 2.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 7.0 Adc) (V_{GS} = 4.5 Vdc, I_D = 3.5 Adc)		$R_{DS(on)}$	 — —	 0.023 0.029	 0.028 0.040	Ohms
Forward Transconductance (V_{DS} = 3 Vdc, I_D = 2.5 Adc)		g_{FS}	3.0	12	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	931	1190	pF
Output Capacitance		C_{oss}	—	371	490	
Transfer Capacitance		C_{rss}	—	89	120	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 5.0 Adc, V_{GS} = 4.5 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	15	30	ns
Rise Time		t_r	—	93	185	
Turn–Off Delay Time		$t_{d(off)}$	—	35	70	
Fall Time		t_f	—	40	80	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 5.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	9.0	—	
Rise Time		t_r	—	53	—	
Turn–Off Delay Time		$t_{d(off)}$	—	56	—	
Fall Time		t_f	—	39		
Gate Charge See Figure 8	(V_{DS} = 16 Vdc, I_D = 5.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	30	43	nC
		Q_1	—	3.0	—	
		Q_2	—	7.5	—	
		Q_3	—	6.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage(1)	(I_S = 7.0 Adc, V_{GS} = 0 Vdc) (I_S = 7.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 0.82 0.69	 1.0 —	Vdc
Reverse Recovery Time See Figure 15	(I_S = 7.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	32	—	ns
		t_a	—	24	—	
		t_b	—	8.0	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.045	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

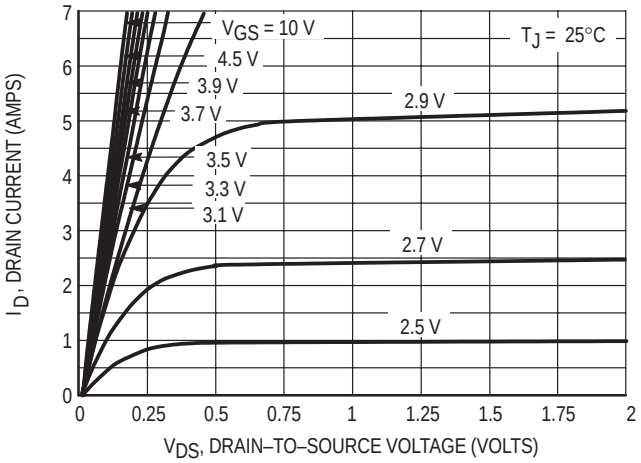


Figure 1. On–Region Characteristics

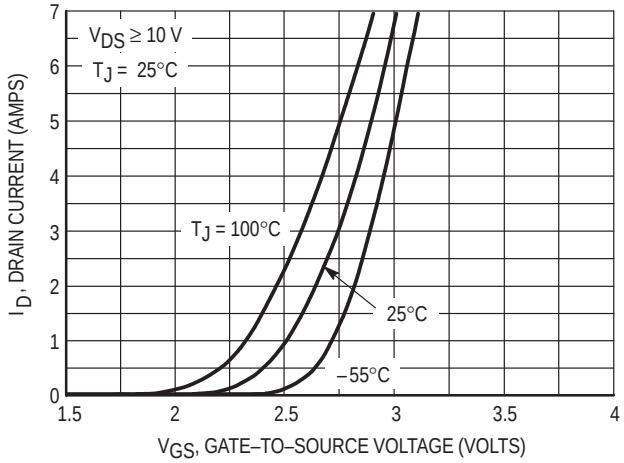


Figure 2. Transfer Characteristics

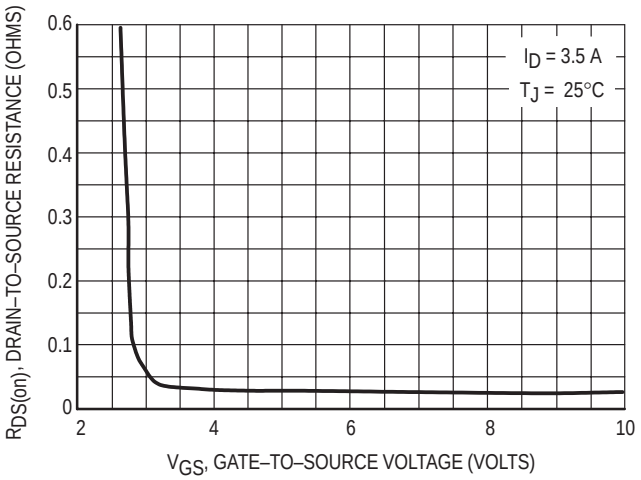


Figure 3. On–Resistance versus Gate–To–Source Voltage

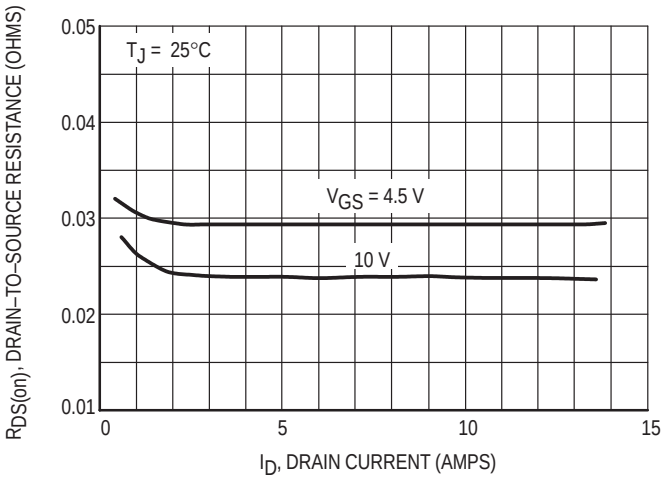


Figure 4. On–Resistance versus Drain Current and Gate Voltage

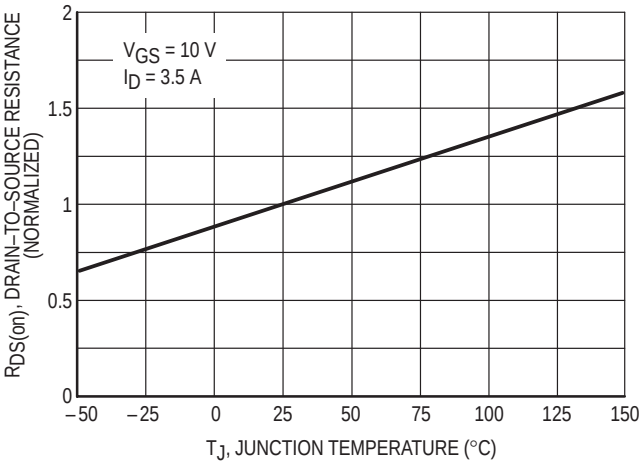


Figure 5. On–Resistance Variation with Temperature

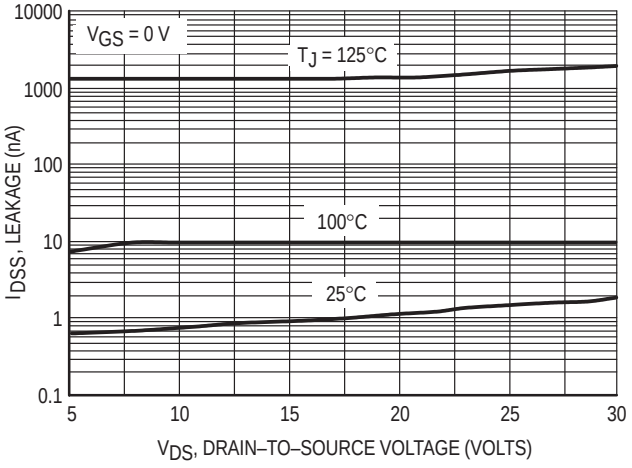


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

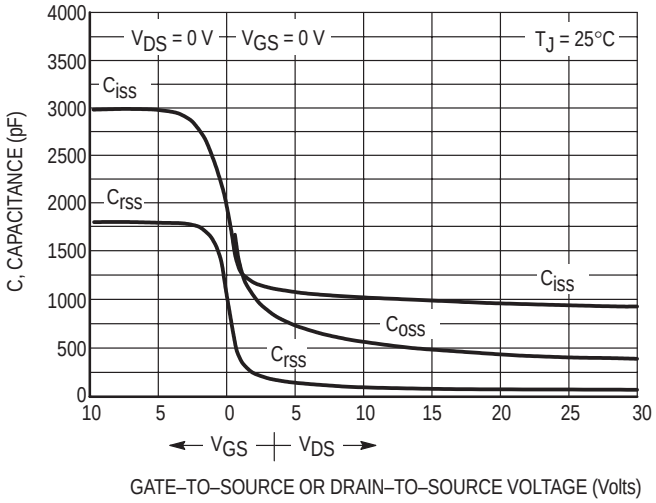


Figure 7. Capacitance Variation

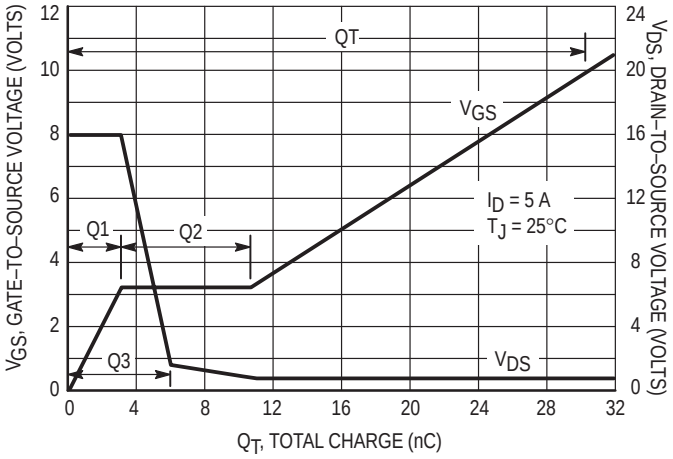


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

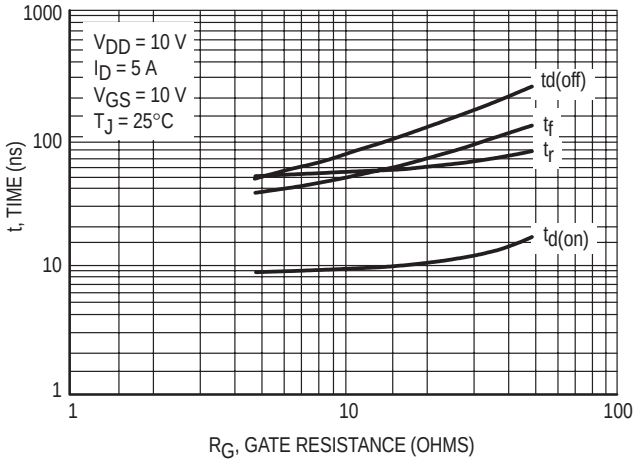


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

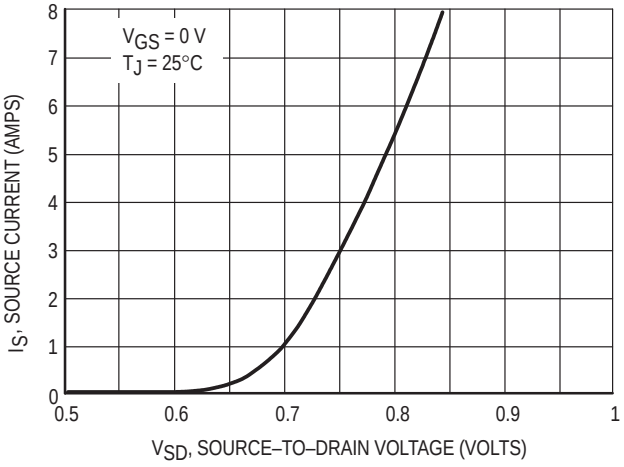


Figure 10. Diode Forward Voltage versus Current

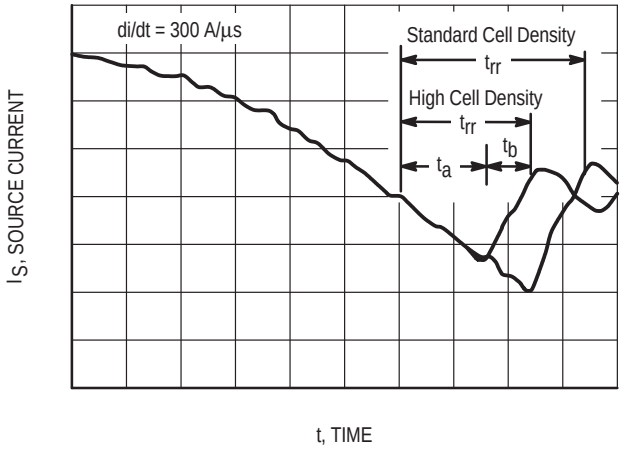


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

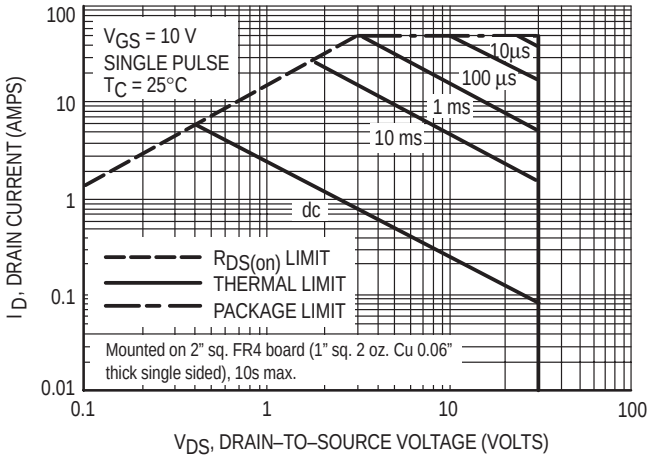


Figure 12. Maximum Rated Forward Biased Safe Operating Area

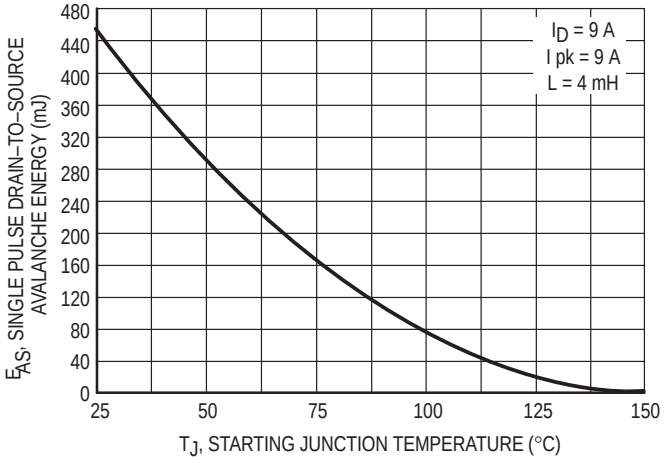


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

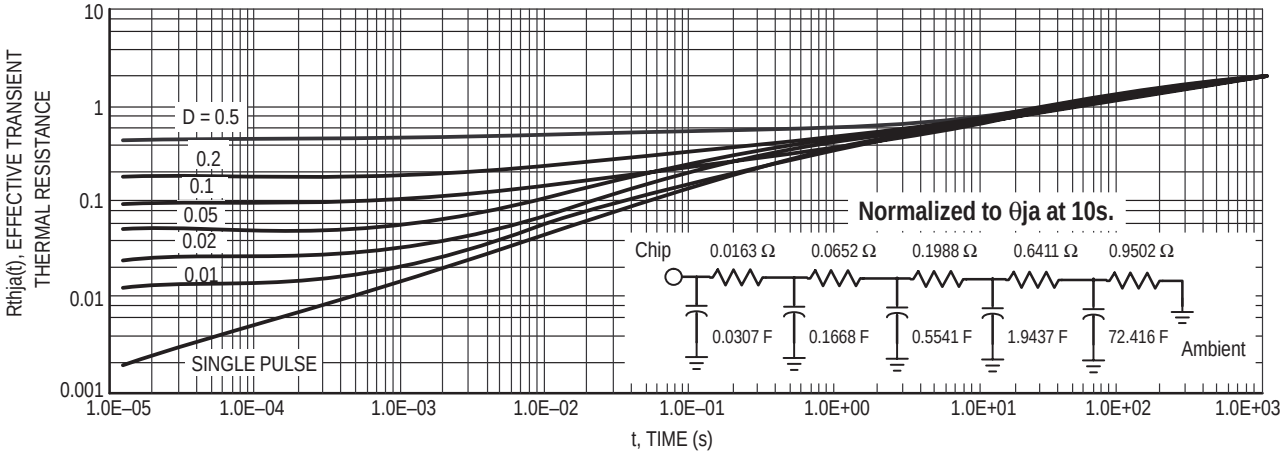


Figure 14. Thermal Response

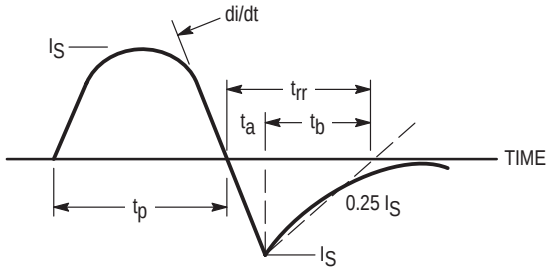


Figure 15. Diode Reverse Recovery Waveform

Power Products Division

Advance Information

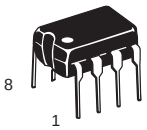
HALF-BRIDGE DRIVER

MPIC2111

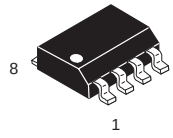
HALF–BRIDGE DRIVER

The MPIC2111 is a high voltage, high speed, power MOSFET and IGBT driver with dependent high and low side referenced output channels designed for half–bridge applications. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross–conduction. Internal deadtime is provided to avoid shoot–through in the output half–bridge. The floating channel can be used to drive an N–channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for Both Channels
- CMOS Schmitt–triggered Inputs with Pull–down
- Matched Propagation Delay for Both Channels
- Internally Set Deadtime
- High Side Output in Phase with Input



P SUFFIX
PLASTIC PACKAGE
CASE 626–05



D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)

PRODUCT SUMMARY

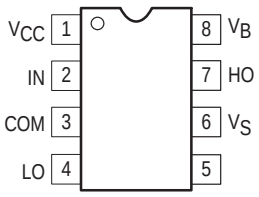
V_{OFFSET}	600 V MAX
$I_{O+/-}$	200 mA/420 mA
V_{OUT}	10 – 20 V
$t_{on/off}$ (typical)	130 & 90 ns
Deadtime (typical)	700 ns

ORDERING INFORMATION

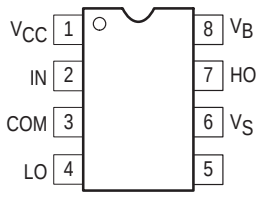
Device	Package
MPIC2111D	SOIC
MPIC2111P	PDIP

PIN CONNECTIONS

(TOP VIEW)



8 LEADS DIP
MPIC2111P

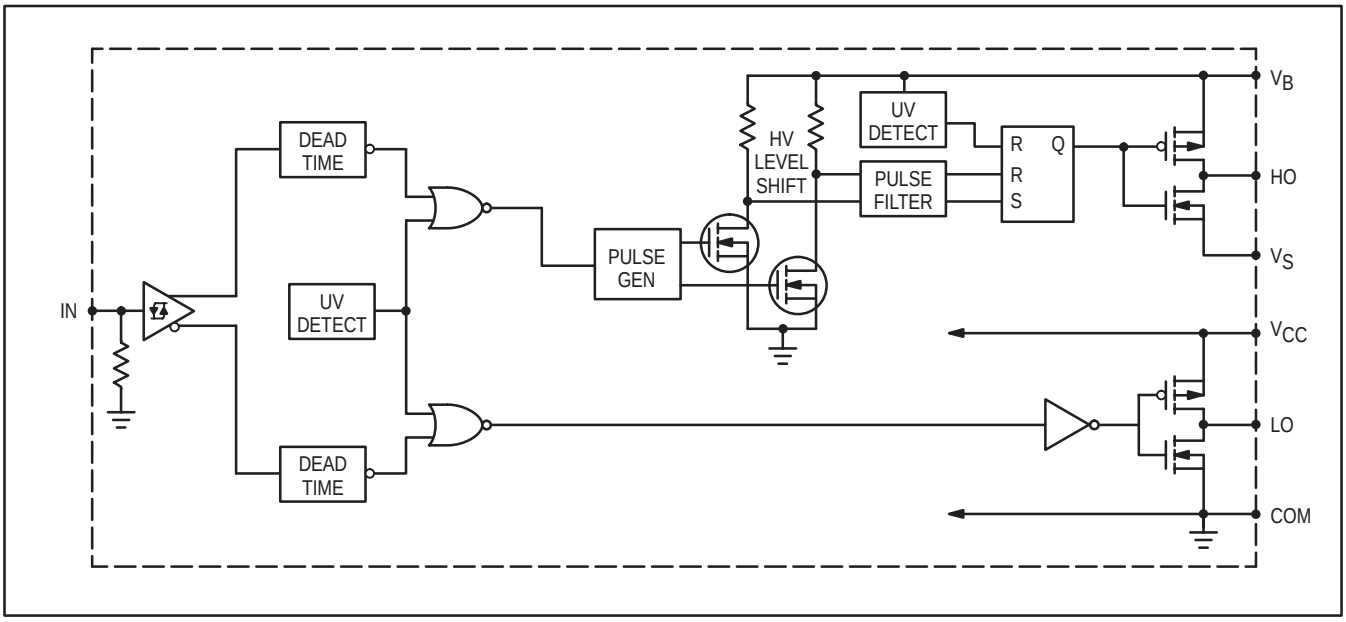


8 LEAD SOIC
MPIC2111D

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating		Symbol	Min	Max	Unit
High Side Floating Supply Absolute Voltage High Side Floating Supply Offset Voltage High Side Floating Output Voltage Low Side Fixed Supply Voltage Low Side Output Voltage Logic Input Voltage		V_B V_S V_{HO} V_{CC} V_{LO} V_{IN}	–0.3 V_B–25 V_S–0.3 –0.3 –0.3 –0.3	625 V_B+0.3 V_B+0.3 25 V_{CC}+0.3 V_{CC}+0.3	V_{DC}
Allowable Offset Supply Voltage Transient		dV_S/dt	–	50	V/ns
*Package Power Dissipation @ $T_C \le +25°C$	(8 Lead DIP) (8 Lead SOIC)	P_D –	– –	1.0 0.625	Watt
Thermal Resistance, Junction to Ambient	(8 Lead DIP) (8 Lead SOIC)	$R_{\theta JA}$	– –	125 200	°C/W
Operating and Storage Temperature		T_j, T_{stg}	–55	150	°C
Lead Temperature for Soldering Purposes, 10 seconds		T_L	–	260	°C

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differential.

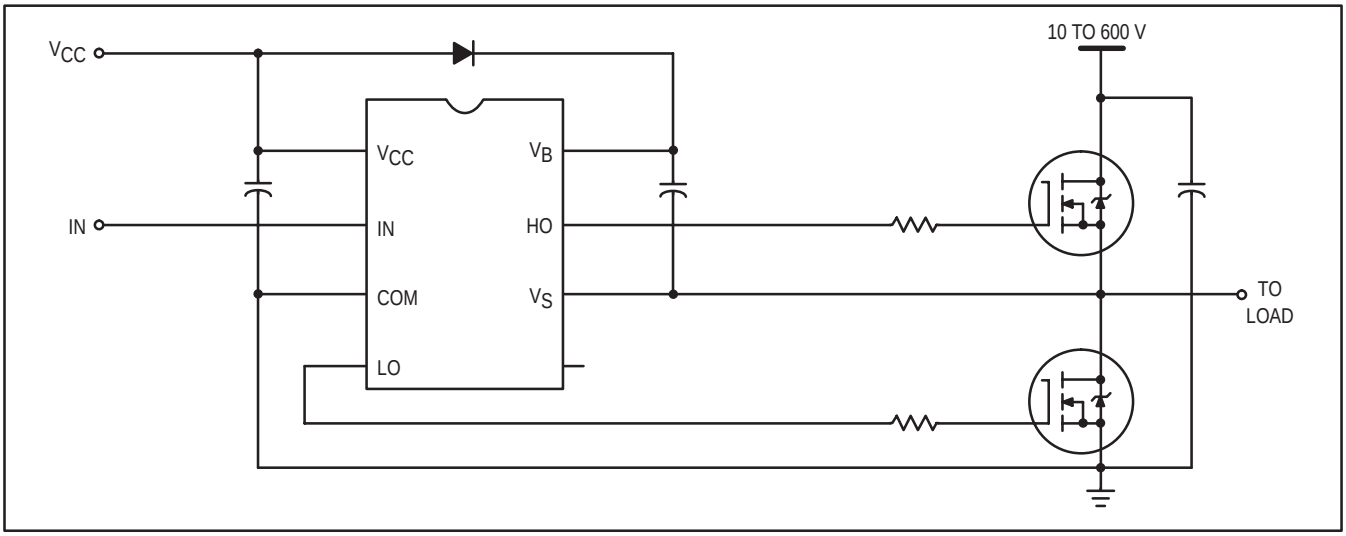
High Side Floating Supply Absolute Voltage	V_B	V_S+10	V_S+20	V
High Side Floating Supply Offset Voltage	V_S	Note 1	600	
High Side Floating Output Voltage	V_{HO}	V_S	V_B	
Low Side Fixed Supply Voltage	V_{CC}	10	20	
Low Side Output Voltage	V_{LO}	0	V_{CC}	mA
Logic Input Voltage	V_{IN}	0	V_{CC}	
Ambient Temperature	T_A	–40	125	°C

Note 1: Logic operational for V_S of –5 to +600 V. Logic state held for V_S of –5 V to $–V_{BS}$.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS V_{BIAS} (V_{CC}, V_{BS}) = 15 V unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The VO and IO parameters are referenced to COM and are applicable to the respective output leads: HO or LO.					
Logic “1” Input Voltage for HO & Logic “0” Input Voltage for LO @ V_{CC} = 10 V	V_{IH}	6.4	–	–	V_{DC}
Logic “1” Input Voltage for HO & Logic “0” Input Voltage for LO @ V_{CC} = 15 V	V_{IH}	9.5	–	–	
Logic “1” Input Voltage for HO & Logic “0” Input Voltage for LO @ V_{CC} = 20 V	V_{IH}	12.6	–	–	
Logic “0” Input Voltage for HO & Logic “1” Input Voltage for LO @ V_{CC} = 10 V	V_{IL}	–	–	3.8	
Logic “0” Input Voltage for HO & Logic “1” Input Voltage for LO @ V_{CC} = 15 V	V_{IL}	–	–	6.0	
Logic “0” Input Voltage for HO & Logic “1” Input Voltage for LO @ V_{CC} = 20 V	V_{IL}	–	–	8.3	
High Level Output Voltage, V_{BIAS}–V_O @ I_O = 0 A	V_{OH}	–	–	100	mV
Low Level Output Voltage, V_O @ I_O = 0 A	V_{OL}	–	–	100	
Offset Supply Leakage Current @ V_B = V_S = 600 V	I_{LK}	–	–	50	μA
Quiescent V_{BS} Supply Current @ V_{IN} = 0 V or V_{CC}	I_{QBS}	–	50	–	
Quiescent V_{CC} Supply Current @ V_{IN} = 0 V or V_{CC}	I_{QCC}	–	70	–	
Logic “1” Input Bias Current @ V_{IN} = 15 V	I_{IN+}	–	20	40	
Logic “0” Input Bias Current @ V_{IN} = 0 V	$I_{IN–}$	–	–	1.0	
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	–	8.5	–	V
V_{BS} Supply Undervoltage Negative Going Threshold	$V_{BSUV–}$	–	8.2	–	
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	–	8.6	–	
V_{CC} Supply Undervoltage Negative Going Threshold	$V_{CCUV–}$	–	8.2	–	
Output High Short Circuit Pulsed Current @ V_{OUT} = 0 V, PW ≤ 10 μs	I_{O+}	200	250	–	mA
Output Low Short Circuit Pulsed Current @ V_{OUT} = 15 V, PW ≤ 10 μs	$I_{O–}$	420	500	–	
DYNAMIC ELECTRICAL CHARACTERISTICS V_{BIAS} (V_{CC}, V_{BS}) = 15 V unless otherwise specified					
Turn–On Propagation Delay @ V_S = 0 V	t_{on}	–	850	–	ns
Turn–Off Propagation Delay @ V_S = 600 V	t_{off}	–	150	–	
Turn–On Rise Time @ C_L = 1000 pF	t_r	–	80	–	
Turn–Off Fall Time @ C_L = 1000 pF	t_f	–	40	–	
Deadtime, LS Turn–Off to HS Turn–On & HS Turn–Off to LS Turn–On	DT	–	700	–	
Delay Matching, HS & LS Turn–On/Off	MT	–	30	–	

TYPICAL CONNECTION



LEAD DEFINITIONS

Symbol	Lead Description
IN	Logic Input for High Side and Low Side Gate Driver Outputs (HO & LO), In Phase with HO
V_B	High Side Floating Supply
HO	High Side Gate Drive Output
V_S	High Side Floating Supply Return
V_{CC}	Low Side Supply
L_O	Low Side Gate Drive Output
COM	Logic and Low Side Return

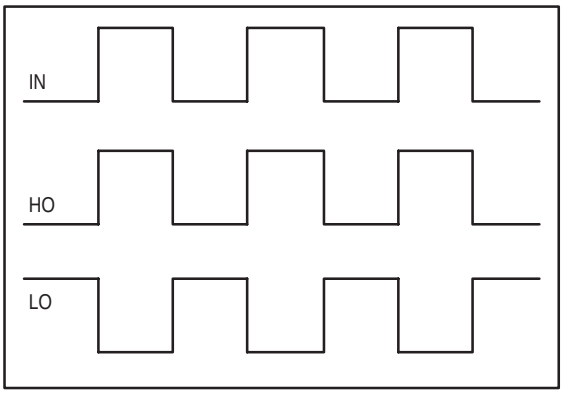


Figure 1. Input / Output Timing Diagram

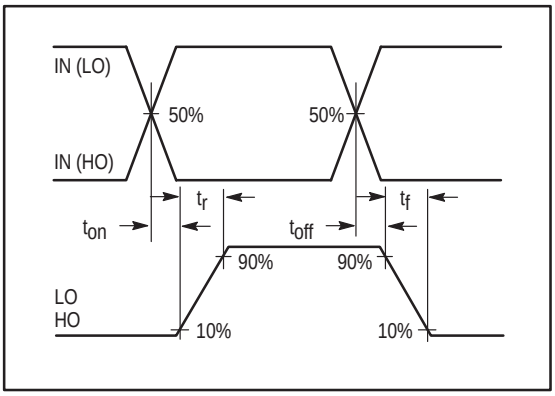


Figure 2. Switching Time Waveform Definitions

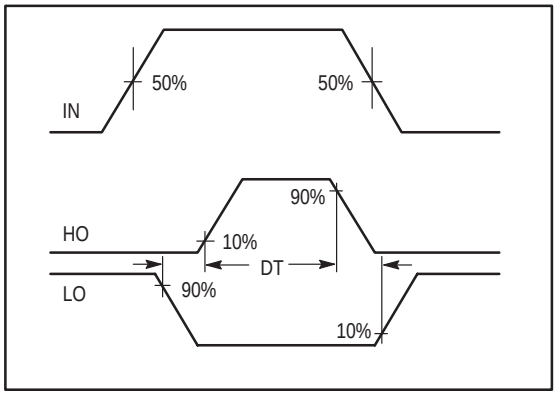


Figure 3. Deadtime Waveform Definitions

Power Products Division

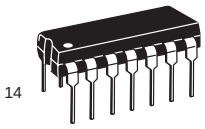
HIGH AND LOW SIDE DRIVER

MPIC2112

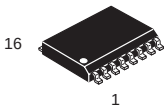
HIGH AND LOW SIDE DRIVER

The MPIC2112 is a high voltage, high speed, power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross–conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N–channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for Both Channels
- Separate Logic Supply
- Operating Supply Range from 5 to 20 V
- Logic and Power Ground Operating Offset Range from –5 to +5 V
- CMOS Schmitt–triggered Inputs with Pull–down
- Cycle by Cycle Edge–triggered Shutdown Logic
- Matched Propagation Delay for Both Channels
- Outputs in Phase with Inputs



P SUFFIX
PLASTIC PACKAGE
CASE 646–06



DW SUFFIX
PLASTIC PACKAGE
CASE 751G–02
SOIC – WIDE

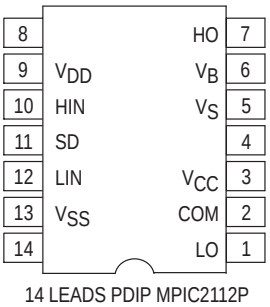
ORDERING INFORMATION

Device	Package
MPIC2112DW	SOIC WIDE
MPIC2112P	PDIP

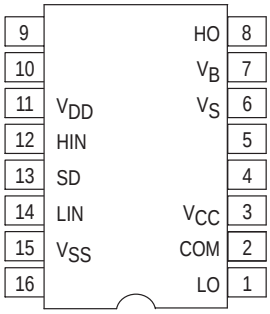
PRODUCT SUMMARY

V_{OFFSET}	**600 V MAX**
$I_{O+/-}$	**200 mA/400 mA**
V_{OUT}	**10 – 20 V**
$t_{on/off}$ **(typical)**	**125 & 105 ns**
Delay Matching	**30 ns**

PIN CONNECTIONS
(TOP VIEW)

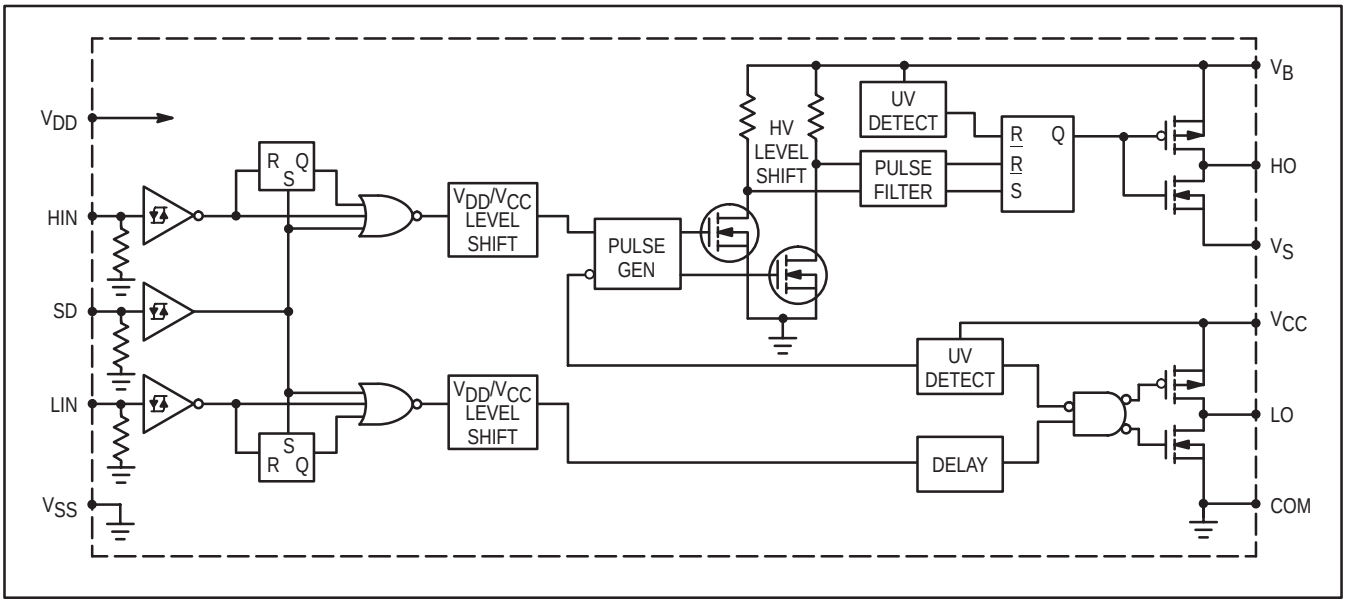


14 LEADS PDIP MPIC2112P



16 LEADS SOIC (WIDE BODY)
MPIC2112DW

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating		Symbol	Min	Max	Unit
High Side Floating Absolute Voltage High Side Floating Supply Offset Voltage High Side Floating Output Voltage Low Side Fixed Supply Voltage Low Side Output Voltage Logic Supply Voltage Logic Supply Offset Voltage Logic Input Voltage (HIN, LIN & SD)		V_B V_S V_{HO} V_{CC} V_{LO} V_{DD} V_{SS} V_{IN}	–0.3 V_B–25 V_S–0.3 –0.3 –0.3 –0.3 V_{CC}–25 V_{SS}–0.3	625 V_B+0.3 V_B+0.3 25 V_{CC}+0.3 V_{SS}+25 V_{CC}+0.3 V_{DD}+0.3	V_{DC}
Allowable Offset Supply Voltage Transient		dV_S/dt	–	50	V/ns
*Package Power Dissipation @ $T_A \le +25°C$	(14 Lead DIP) (16 SOIC–WIDE)	P_D –	– –	1.6 1.25	Watt
Thermal Resistance, Junction to Ambient	(14 Lead DIP) (16 SOIC–WIDE)	$R_{\theta JA}$	– –	75 100	°C/W
Operating and Storage Temperature		T_j, T_{stg}	–55	150	°C
Lead Temperature for Soldering Purposes, 10 seconds		T_L	–	260	°C

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15 V differential.

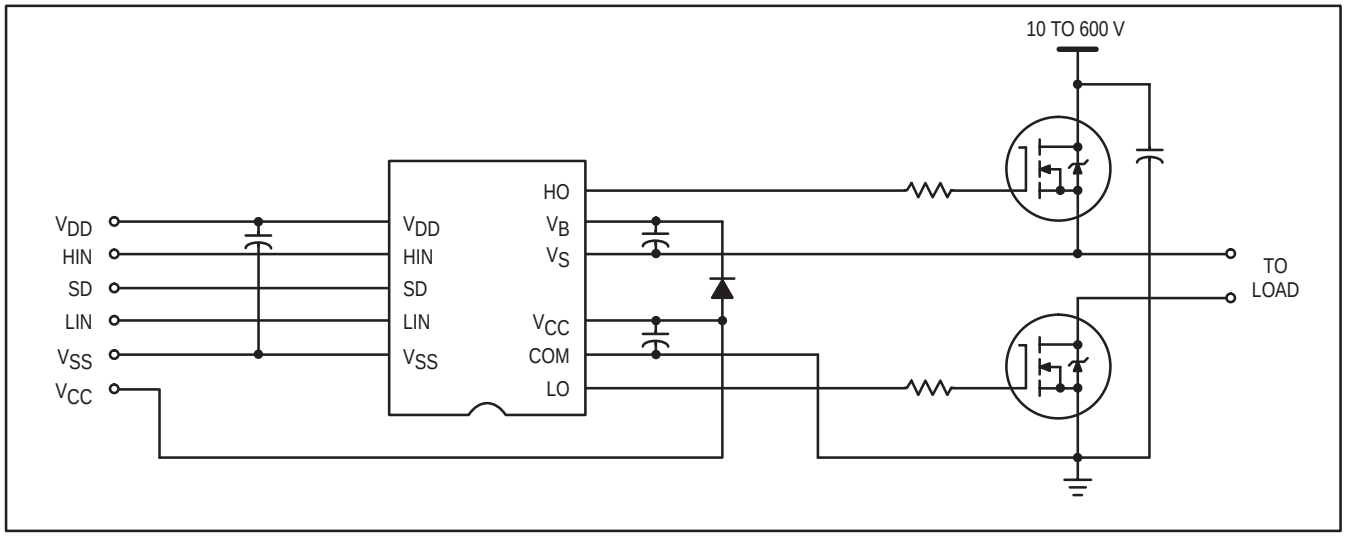
High Side Floating Supply Absolute Voltage	V_B	V_S+10	V_S+20	V
High Side Floating Supply Offset Voltage	V_S	Note 1	600	
High Side Floating Output Voltage	V_{HO}	V_S	V_B	
Low Side Fixed Supply Voltage	V_{CC}	10	20	
Low Side Output Voltage	V_{LO}	0	V_{CC}	
Logic Supply Voltage	V_{DD}	V_{SS}+5	V_{SS}+20	
Logic Supply Offset Voltage	V_{SS}	–5	5	
Logic Input Voltage (HIN, LIN & SD)	V_{IN}	V_{SS}	V_{DD}	
Ambient Temperature	T_A	–40	125	°C

Note 1: Logic operational for V_S of –5 to +600 V. Logic state held for V_S of –5 V to $–V_{BS}$.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS – SUPPLY CHARACTERISTICS V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The VO and IO parameters are referenced to COM or V_{SS} and are applicable to the respective output leads: HO or LO.					
Logic “1” Input Voltage	V_{IH}	9.5	–	–	V
Logic “0” Input Voltage	V_{IL}	–	–	6.0	
High Level Output Voltage, V_{BIAS}–V_O @ V_{IN} = V_{IH}, I_O = 0 A	V_{OH}	–	–	100	mV
Low Level Output Voltage, V_O @ V_{IN} = V_{IL}, I_O = 0 A	V_{OL}	–	–	100	
Offset Supply Leakage Current @ V_B = V_S = 600 V	I_{LK}	–	–	50	μA
Quiescent V_{BS} Supply Current @ V_{IN} = 0 V or V_{DD}	I_{QBS}	–	25	60	
Quiescent V_{CC} Supply Current @ V_{IN} = 0 V or V_{DD}	I_{QCC}	–	80	180	
Quiescent V_{DD} Supply Current @ V_{IN} = 0 V or V_{DD}	I_{QDD}	–	2.0	5.0	
Logic “1” Input Bias Current @ V_{IN} = 15 V	I_{IN+}	–	20	40	
Logic “0” Input Bias Current @ V_{IN} = 0 V	$I_{IN–}$	–	–	1.0	
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	7.4	–	9.6	V
V_{BS} Supply Undervoltage Negative Going Threshold	$V_{BSUV–}$	7.0	–	9.2	
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	7.6	–	9.6	
V_{CC} Supply Undervoltage Negative Going Threshold	$V_{CCUV–}$	7.2	–	9.2	
Output High Short Circuit Pulsed Current @ V_{OUT} = 0 V, V_{IN} = 15 V, PW ≤10 μs	I_{O+}	200	250	–	mA
Output Low Short Circuit Pulsed Current @ V_{OUT} = 15 V, V_{IN} = 0 V, PW ≤ 10 μs	$I_{O–}$	420	500	–	
DYNAMIC ELECTRICAL CHARACTERISTICS V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V and V_{SS} = COM unless otherwise specified. T_A = 25°C.					
Turn–On Propagation Delay @ V_S = 0 V	t_{on}	–	125	180	ns
Turn–Off Propagation Delay @ V_S = 600 V	t_{off}	–	105	160	
Shutdown Propagation Delay @ V_S = 600 V	t_{sd}	–	105	160	
Turn–On Rise Time @ C_L = 1000 pF	t_r	–	80	130	
Turn–Off Fall Time @ C_L = 1000 pF	t_f	–	40	65	
Delay Matching, HS & LS Turn–On/Off	MT	–	–	30	

TYPICAL CONNECTION



LEAD DEFINITIONS

Symbol	Lead Description
V_{DD}	Logic Supply
HIN	Logic Input for High Side Gate Driver Output (HO), In Phase
SD	Logic Input for Shutdown
LIN	Logic Input for Low Side Gate Driver Output (LO), In Phase
V_{SS}	Logic Ground
V_B	High Side Floating Supply
HO	High Side Gate Drive Output
V_S	High Side Floating Supply Return
V_{CC}	Low Side Supply
LO	Low Side Gate Drive Output
COM	Low Side Return

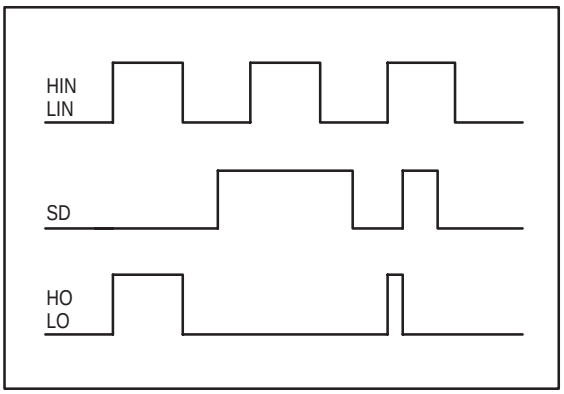


Figure 1. Input / Output Timing Diagram

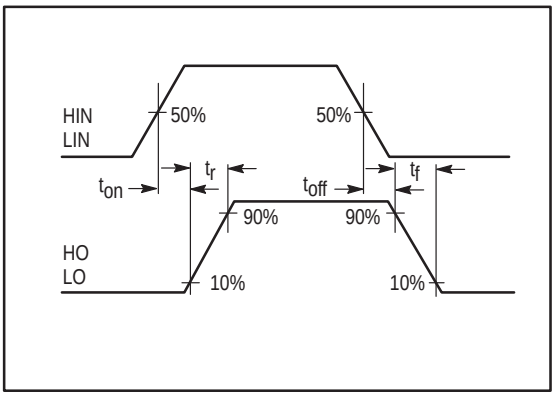


Figure 2. Switching Time Waveform Definitions

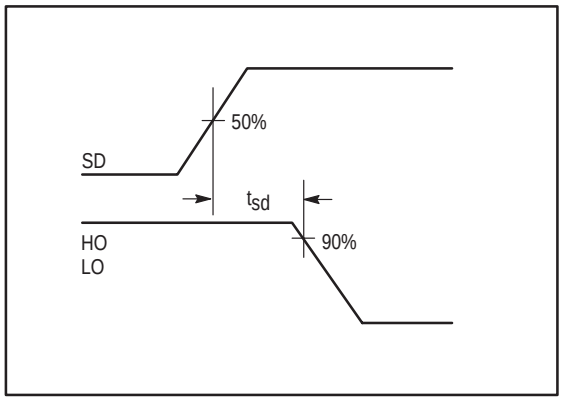


Figure 3. Deadtime Waveform Definitions

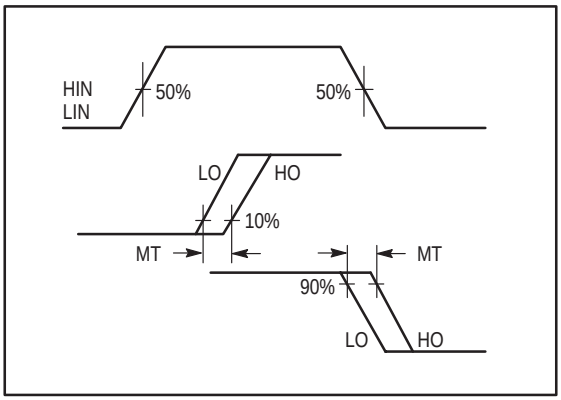


Figure 4. Delay Matching Waveform Definitions

Power Products Division

MPIC2113

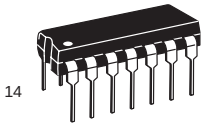
Advance Information

HIGH AND LOW SIDE DRIVER

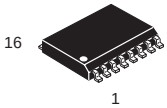
HIGH AND LOW SIDE DRIVER

The MPIC2113 is a high voltage, high speed, power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross–conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N–channel power MOSFET or IGBT in the high side configuration which operates from 10 to 600 volts.

- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for Both Channels
- Separate Logic Supply
- Operating Supply Range from 5 to 20 V
- Logic and Power Ground Operating Offset Range from –5 to +5 V
- CMOS Schmitt–triggered Inputs with Pull–down
- Cycle by Cycle Edge–triggered Shutdown Logic
- Matched Propagation Delay for Both Channels
- Outputs In Phase with Inputs



P SUFFIX
PLASTIC PACKAGE
CASE 646–06



DW SUFFIX
PLASTIC PACKAGE
CASE 751G–02
SOIC – WIDE

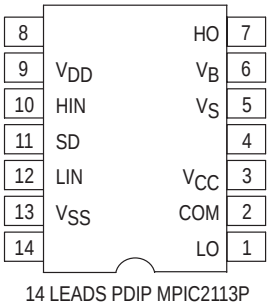
ORDERING INFORMATION

Device	Package
MPIC2113DW	SOIC WIDE
MPIC2113P	PDIP

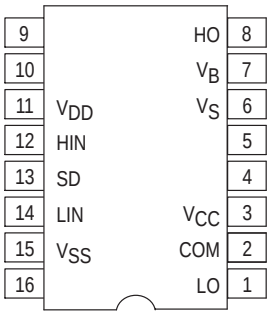
PRODUCT SUMMARY

V_{OFFSET}	**600 V MAX**
$I_{O+/-}$	**2 A/2 A**
V_{OUT}	**10 – 20 V**
$t_{on/off}$ **(typical)**	**120 & 94 ns**
Delay Matching	**10 ns**

PIN CONNECTIONS
(TOP VIEW)



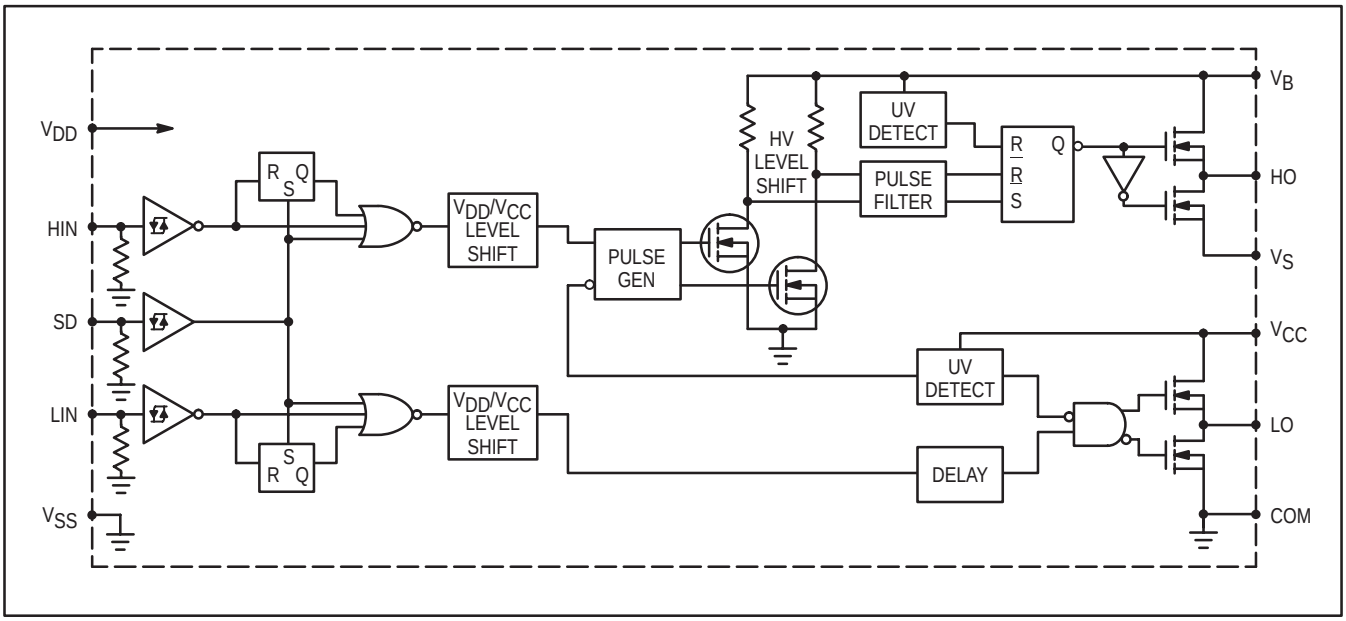
14 LEADS PDIP MPIC2113P



16 LEADS SOIC (WIDE BODY)
MPIC2113DW

This document contains information on a new product. Specifications and information herein are subject to change without notice.

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating		Symbol	Min	Max	Unit
High Side Floating Absolute Voltage High Side Floating Supply Offset Voltage High Side Floating Output Voltage Low Side Fixed Supply Voltage Low Side Output Voltage Logic Supply Voltage Logic Supply Offset Voltage Logic Input Voltage (HIN, LIN & SD)		V_B V_S V_{HO} V_{CC} V_{LO} V_{DD} V_{SS} V_{IN}	–0.3 V_B–25 V_S–0.3 –0.3 –0.3 –0.3 V_{CC}–25 V_{SS}–0.3	625 V_B+0.3 V_B+0.3 25 V_{CC}+0.3 V_{SS}+25 V_{CC}+0.3 V_{DD}+0.3	V_{DC}
Allowable Offset Supply Voltage Transient		dV_S/dt	–	50	V/ns
*Package Power Dissipation @ $T_A \le +25°C$	(14 Lead DIP) (16 SOIC–WIDE)	P_D –	– –	1.6 1.25	Watt
Thermal Resistance, Junction to Ambient	(14 Lead DIP) (16 SOIC–WIDE)	$R_{\theta JA}$	– –	75 100	°C/W
Operating and Storage Temperature		T_j, T_{stg}	–55	150	°C
Lead Temperature for Soldering Purposes, 10 seconds		T_L	–	260	°C

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15 V differential.

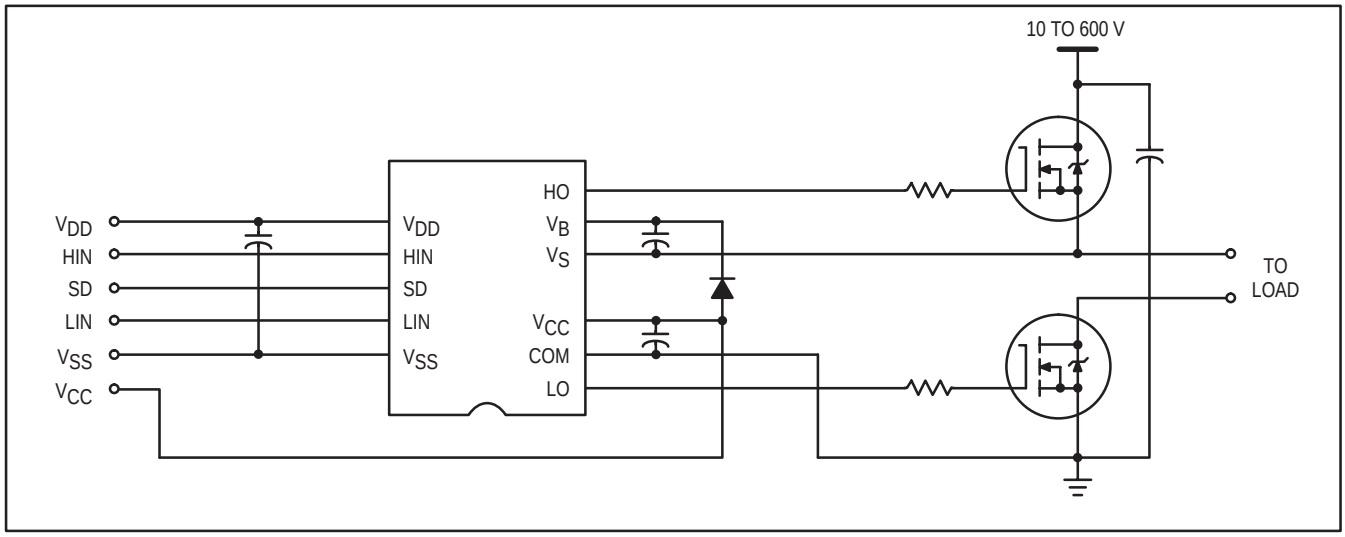
High Side Floating Supply Absolute Voltage	V_B	V_S+10	V_S+20	V
High Side Floating Supply Offset Voltage	V_S	Note 1	600	
High Side Floating Output Voltage	V_{HO}	V_S	V_B	
Low Side Fixed Supply Voltage	V_{CC}	10	20	
Low Side Output Voltage	V_{LO}	0	V_{CC}	
Logic Supply Voltage	V_{DD}	V_{SS}+5	V_{SS}+20	
Logic Supply Offset Voltage	V_{SS}	–5	5	
Logic Input Voltage (HIN, LIN & SD)	V_{IN}	V_{SS}	V_{DD}	
Ambient Temperature	T_A	–40	125	°C

Note 1: Logic operational for V_S of –5 to +600 V. Logic state held for V_S of –5 V to $–V_{BS}$.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS – SUPPLY CHARACTERISTICS V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The VO and IO parameters are referenced to COM or V_{SS} and are applicable to the respective output leads: HO or LO.					
Logic “1” Input Voltage	V_{IH}	9.5	–	–	V
Logic “0” Input Voltage	V_{IL}	–	–	6.0	
High Level Output Voltage, V_{BIAS}–V_O @ V_{IN} = V_{IH}, I_O = 0 A	V_{OH}	–	–	1.2	
Low Level Output Voltage, V_O @ V_{IN} = V_{IL}, I_O = 0 A	V_{OL}	–	–	0.1	
Offset Supply Leakage Current @ V_B = V_S = 600 V	I_{LK}	–	–	50	μA
Quiescent V_{BS} Supply Current @ V_{IN} = 0 V or V_{DD}	I_{QBS}	–	125	230	
Quiescent V_{CC} Supply Current @ V_{IN} = 0 V or V_{DD}	I_{QCC}	–	180	340	
Quiescent V_{DD} Supply Current @ V_{IN} = 0 V or V_{DD}	I_{QDD}	–	15	30	
Logic “1” Input Bias Current @ V_{IN} = 15 V	I_{IN+}	–	20	40	
Logic “0” Input Bias Current @ V_{IN} = 0 V	$I_{IN–}$	–	–	1.0	
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	7.5	–	9.7	V
V_{BS} Supply Undervoltage Negative Going Threshold	$V_{BSUV–}$	7.0	–	9.4	
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	7.4	–	9.6	
V_{CC} Supply Undervoltage Negative Going Threshold	$V_{CCUV–}$	7.0	–	9.4	
Output High Short Circuit Pulsed Current @ V_{OUT} = 0 V, V_{IN} = 15 V, PW ≤10 μs	I_{O+}	2.0	2.5	–	A
Output Low Short Circuit Pulsed Current @ V_{OUT} = 15 V, V_{IN} = 0 V, PW ≤ 10 μs	$I_{O–}$	2.0	2.5	–	
DYNAMIC ELECTRICAL CHARACTERISTICS V_{BIAS} (V_{CC}, V_{BS}, V_{DD}) = 15 V and V_{SS} = COM unless otherwise specified. T_A = 25°C.					
Turn–On Propagation Delay @ V_S = 0 V	t_{on}	–	120	150	ns
Turn–Off Propagation Delay @ V_S = 600 V	t_{off}	–	94	125	
Shutdown Propagation Delay @ V_S = 600 V	t_{sd}	–	110	140	
Turn–On Rise Time @ C_L = 1000 pF	t_r	–	25	35	
Turn–Off Fall Time @ C_L = 1000 pF	t_f	–	17	25	
Delay Matching, HS & LS Turn–On/Off	MT	–	–	10	

TYPICAL CONNECTION



LEAD DEFINITIONS

Symbol	Lead Description
V_{DD}	Logic Supply
HIN	Logic Input for High Side Gate Driver Output (HO), In Phase
SD	Logic Input for Shutdown
LIN	Logic Input for Low Side Gate Driver Output (LO), In Phase
V_{SS}	Logic Ground
V_B	High Side Floating Supply
HO	High Side Gate Drive Output
V_S	High Side Floating Supply Return
V_{CC}	Low Side Supply
LO	Low Side Gate Drive Output
COM	Low Side Return

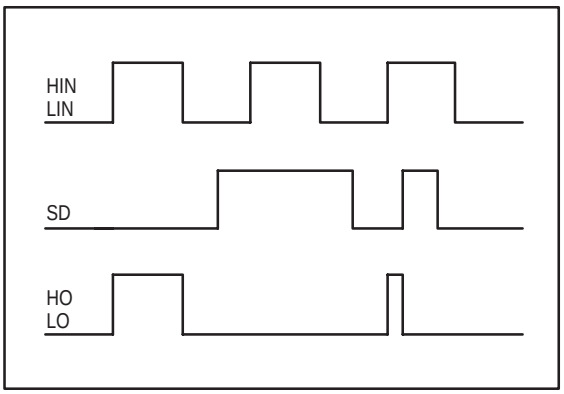


Figure 1. Input / Output Timing Diagram

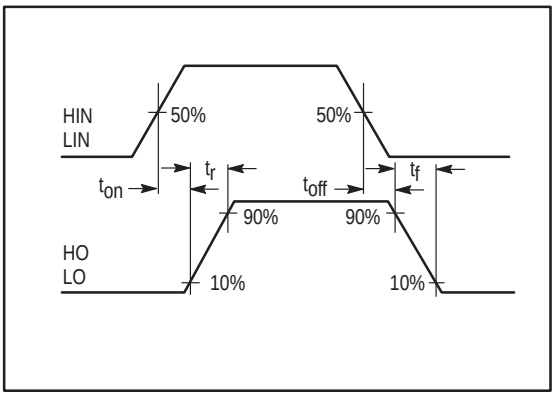


Figure 2. Switching Time Waveform Definitions

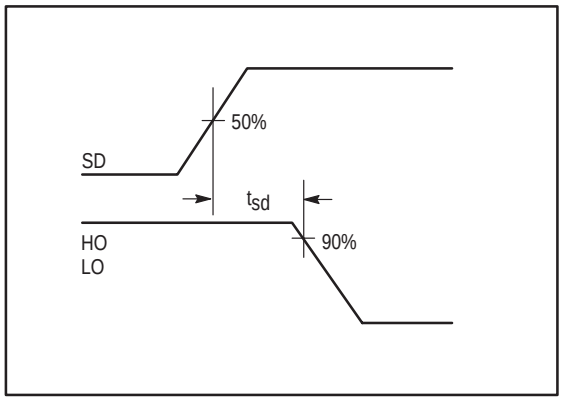


Figure 3. Shutdown Waveform Definitions

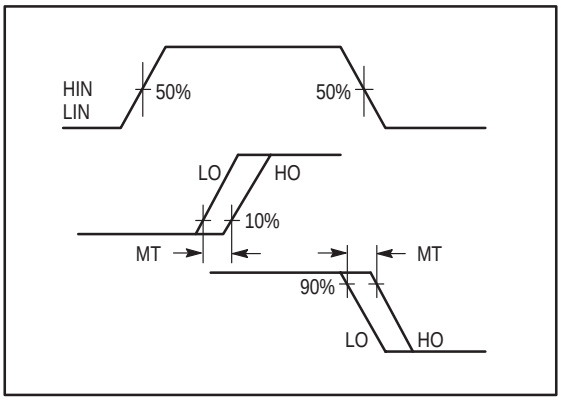


Figure 4. Delay Matching Waveform Definitions

Power Products Division

Advance Information

SINGLE CHANNEL DRIVER

MPIC2117

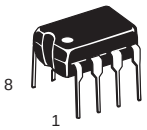
SINGLE CHANNEL DRIVER

The MPIC2117 is a high voltage, high speed, power MOSFET and IGBT driver. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross–conduction. The floating channel can be used to drive an N–channel power MOSFET or IGBT in the high side or low side configuration which operates from 10 to 600 volts.

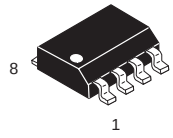
- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout
- CMOS Schmitt–triggered Input with Pull–down
- Output In Phase with Input

PRODUCT SUMMARY

V_{OFFSET}	**600 V MAX**
$I_{O+/-}$	**200 mA/420 mA**
V_{OUT}	**10 – 20 V**
$t_{on/off}$ (typical)	**125 & 105 ns**



P SUFFIX
PLASTIC PACKAGE
CASE 626–05



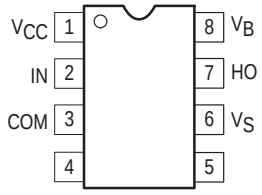
D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)

ORDERING INFORMATION

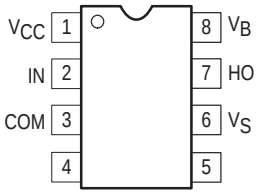
Device	Package
MPIC2117D	SOIC
MPIC2117P	PDIP

PIN CONNECTIONS

(TOP VIEW)



8 LEADS DIP
MPIC2117P

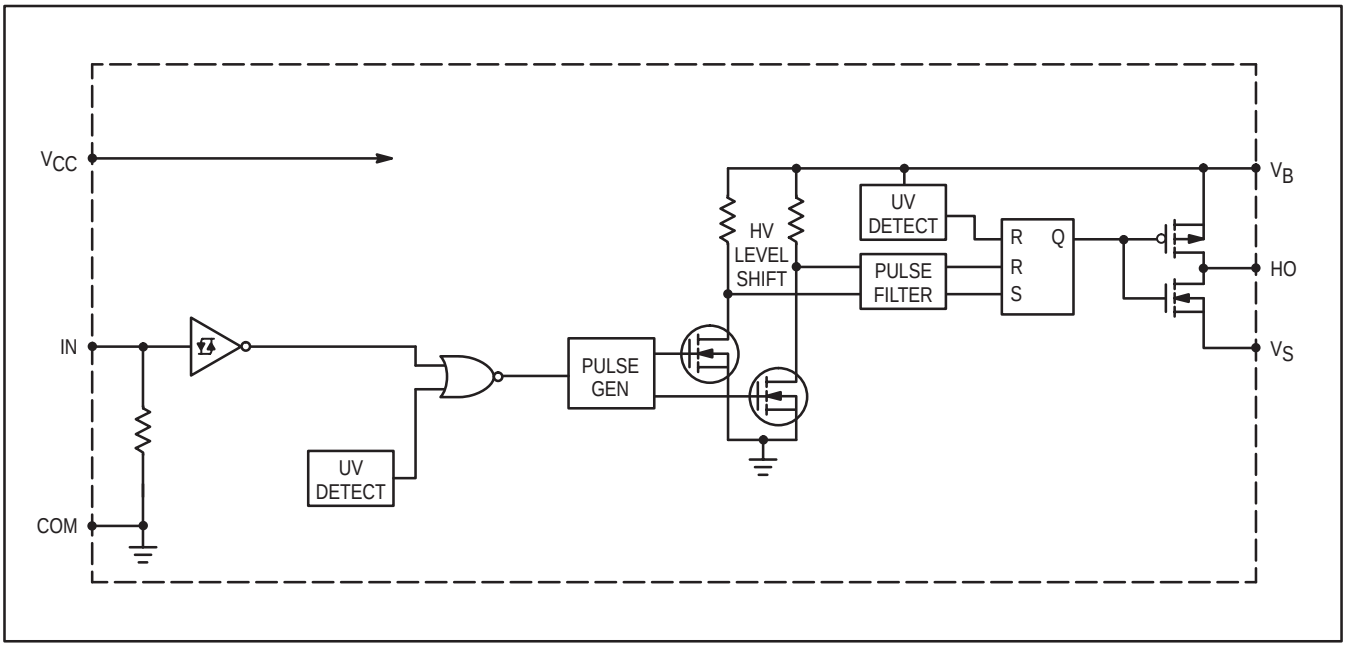


8 LEAD SOIC
MPIC2117D

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating		Symbol	Min	Max	Unit
High Side Floating Supply Absolute Voltage High Side Floating Supply Offset Voltage High Side Floating Output Voltage Logic Supply Voltage Logic Input Voltage		V_B V_S V_{HO} V_{CC} V_{IN}	–0.3 V_B–25 V_S–0.3 –0.3 –0.3	625 V_B+0.3 V_B+0.3 25 V_{CC}+0.3	V_{DC}
Allowable Offset Supply Voltage Transient		dV_S/dt	–	50	V/ns
*Package Power Dissipation @ $T_A \leq +25°C$	(8 Lead DIP) (8 Lead SOIC)	P_D –	– –	1.0 0.625	Watt
Thermal Resistance, Junction to Ambient	(8 Lead DIP) (8 Lead SOIC)	$R_{\theta JA}$	– –	125 200	°C/W
Operating and Storage Temperature		T_j, T_{stg}	–55	150	°C
Lead Temperature for Soldering Purposes, 10 seconds		T_L	–	260	°C

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differential.

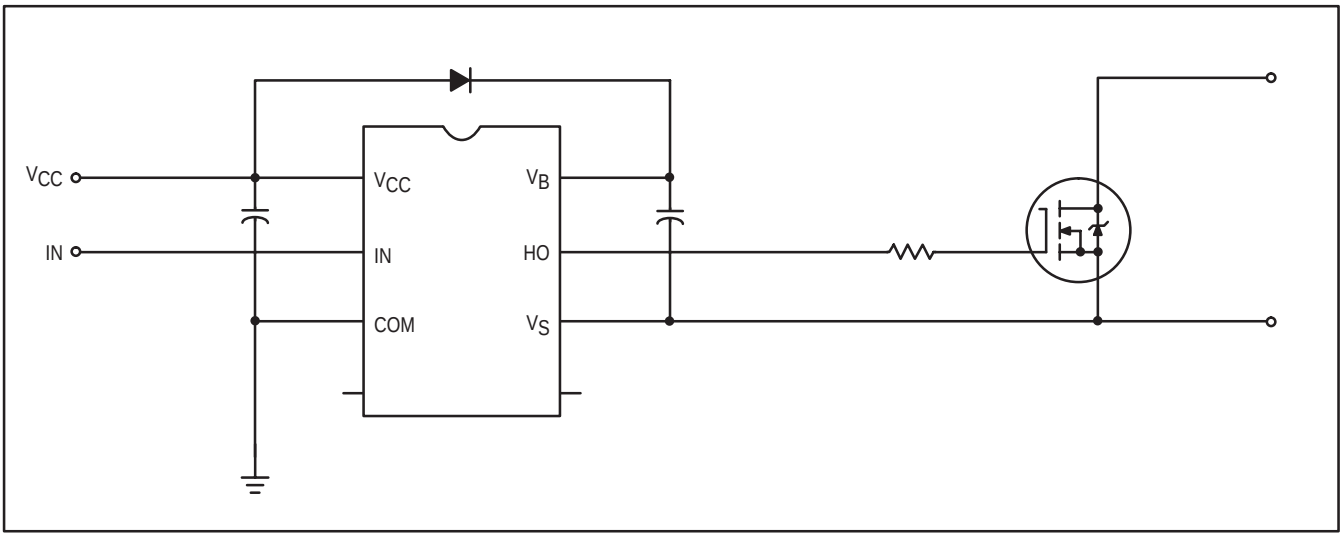
High Side Floating Supply Absolute Voltage	V_B	V_S+10	V_S+20	V
High Side Floating Supply Offset Voltage	V_S	Note 1	600	
High Side Floating Output Voltage	V_{HO}	V_S	V_B	
Logic Supply Voltage	V_{CC}	10	20	
Logic Input Voltage	V_{IN}	0	V_{CC}	
Ambient Temperature	T_A	–40	125	°C

Note 1: Logic operational for V_S of –5 to +600 V. Logic state held for V_S of –5 V to $–V_{BS}$.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS V_{BIAS} (V_{CC}, V_{BS}) = 15 V unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to COM. The VO and IO parameters are referenced to COM and are applicable to the respective output leads: HO or LO.					
Logic “1” Input Voltage @ V_{CC} = 10 V	V_{IH}	6.4	–	–	V_{DC}
Logic “1” Input Voltage @ V_{CC} = 15 V	V_{IH}	9.5	–	–	
Logic “1” Input Voltage @ V_{CC} = 20 V	V_{IH}	12.6	–	–	
Logic “0” Input Voltage @ V_{CC} = 10 V	V_{IL}	–	–	3.8	
Logic “0” Input Voltage @ V_{CC} = 15 V	V_{IL}	–	–	6.0	
Logic “0” Input Voltage @ V_{CC} = 20 V	V_{IL}	–	–	8.3	
High Level Output Voltage, V_{BS}–V_O @ V_{IN} = V_{IH}, I_O = 0 A	V_{OH}	–	–	100	mV
Low Level Output Voltage, V_O @ V_{IN} = V_{IL}, I_O = 0 A	V_{OL}	–	–	100	
Offset Supply Leakage Current @ V_B = V_S = 600 V	I_{LK}	–	–	50	μA
Quiescent V_{BS} Supply Current @ V_{IN} = 0 V or V_{CC}	I_{QBS}	–	50	–	
Quiescent V_{CC} Supply Current @ V_{IN} = 0 V or V_{CC}	I_{QCC}	–	70	–	
Logic “1” Input Bias Current @ V_{IN} = 15 V	I_{IN+}	–	20	40	
Logic “0” Input Bias Current @ V_{IN} = 0 V	$I_{IN–}$	–	–	1.0	
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	–	8.5	–	V
V_{BS} Supply Undervoltage Negative Going Threshold	$V_{BSUV–}$	–	8.2	–	
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	–	8.6	–	
V_{CC} Supply Undervoltage Negative Going Threshold	$V_{CCUV–}$	–	8.2	–	
Output High Short Circuit Pulsed Current @ V_{OUT} = 0 V, V_{IN} = 15 V, PW ≤ 10 μs	I_{O+}	200	250	–	mA
Output Low Short Circuit Pulsed Current @ V_{OUT} = 15 V, V_{IN} = 0 V, PW ≤ 10 μs	$I_{O–}$	420	500	–	
DYNAMIC ELECTRICAL CHARACTERISTICS V_{BIAS} (V_{CC}, V_{BS}) = 15 V unless otherwise specified					
Turn–On Propagation Delay @ V_S = 0 V	t_{on}	–	125	–	ns
Turn–Off Propagation Delay @ V_S = 600 V	t_{off}	–	105	–	
Turn–On Rise Time @ C_L = 1000 pF	t_r	–	80	–	
Turn–Off Fall Time @ C_L = 1000 pF	t_f	–	40	–	

TYPICAL CONNECTION



LEAD DEFINITIONS

Symbol	Lead Description
V_{CC}	Logic Supply
IN	Logic Input for High Side Gate Driver Outputs (HO), In Phase with HO
COM	Logic Ground
V_B	High Side Floating Supply
HO	High Side Gate Drive Output
V_S	High Side Floating Supply Return

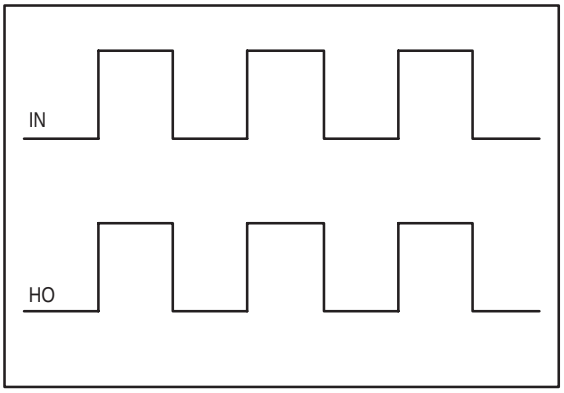


Figure 1. Input / Output Timing Diagram

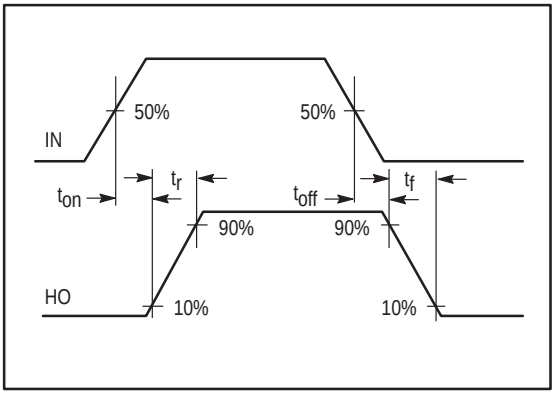


Figure 2. Switching Time Waveform Definitions

Power Products Division

Advance Information

3-PHASE BRIDGE DRIVER

MPIC2130

3–PHASE BRIDGE DRIVER

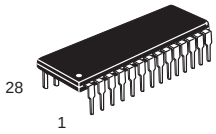
The MPIC2130 is a high voltage, high speed, power MOSFET and IGBT driver with three independent high side and low side referenced output channels for 3–Phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with 5 V CMOS or LSTTL outputs. A ground referenced operational amplifier provides an analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from this resistor. An open drain FAULT signal is provided to indicate that an over–current or undervoltage shutdown has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross–conduction. Propagation delays are matched to simplify use in high frequency applications.

The floating channels can be used to drive N–channel power MOSFET or IGBT's in the high side configuration which operate from 10 to 600 volts.

- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for All Channels
- Over–current Shut Down Turns Off All Six Drivers
- Independent Half–bridge Drivers
- Matched Propagation Delay for All Channels
- Outputs Out of Phase with Inputs

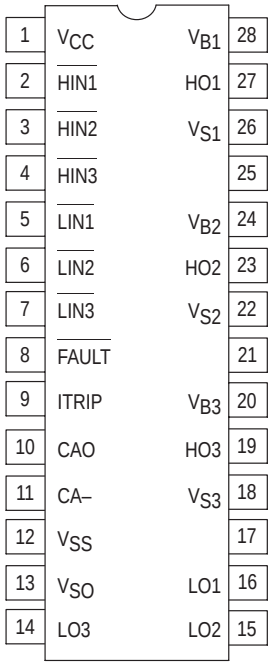
PRODUCT SUMMARY

V_{OFFSET}	600 V MAX
$I_{O+/-}$	200 mA/420 mA
V_{OUT}	10 – 20 V
$t_{on/off}$ (typical)	675 & 425 ns
Deadtime (typical)	2.5 μs



P SUFFIX
PLASTIC PACKAGE
CASE 710–02

PIN CONNECTIONS



(TOP VIEW)

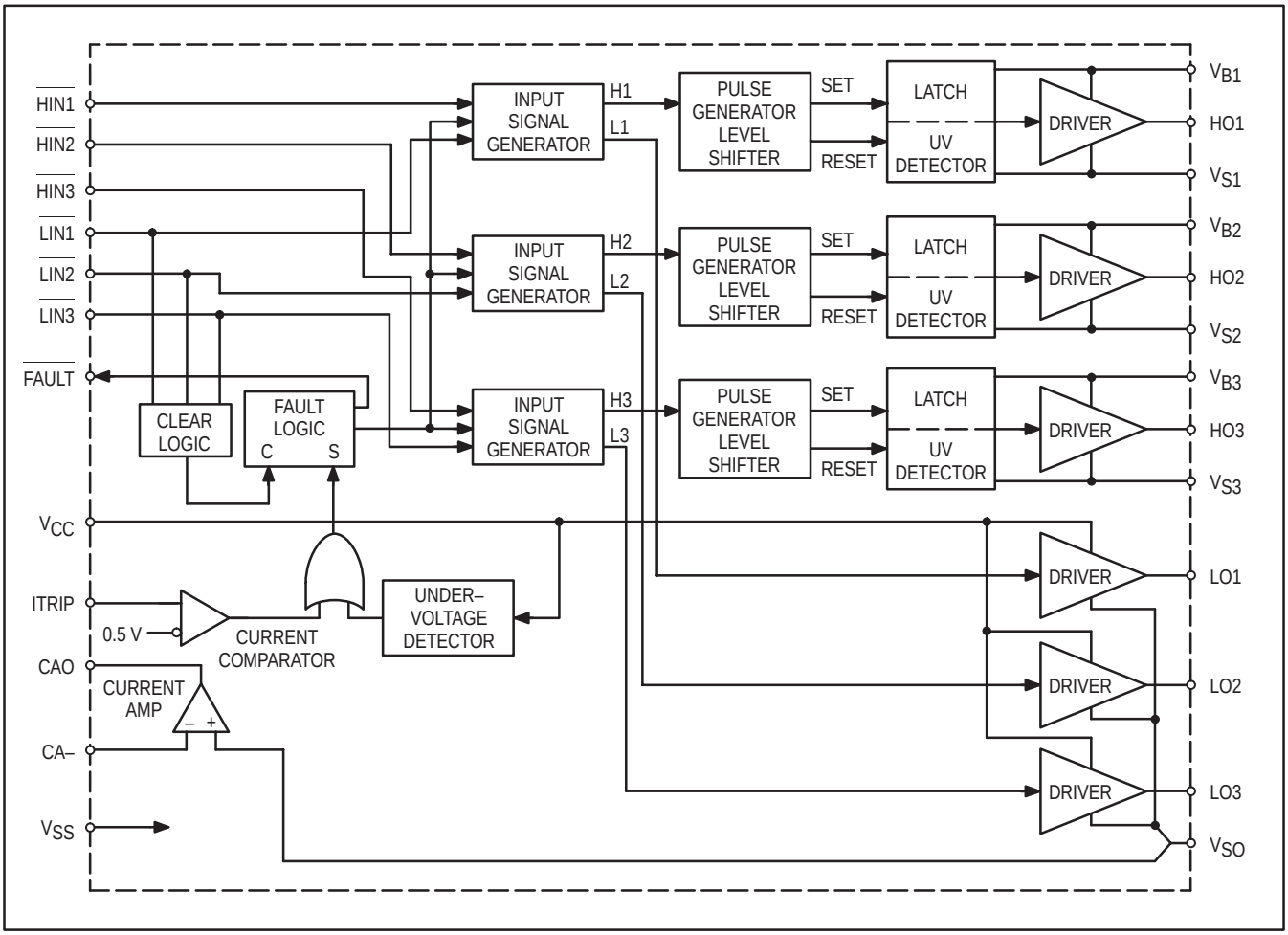
ORDERING INFORMATION

Device	Package
MPIC2130P	PDIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to V_{SS}. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating	Symbol	Min	Max	Unit
High Side Floating Absolute Voltage	$V_{B1,2,3}$	–0.3	625	V_{DC}
High Side Floating Supply Offset Voltage	$V_{S1,2,3}$	$V_{B1,2,3}$–25	$V_{B1,2,3}$+0.3	
High Side Floating Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$–0.3	$V_{B1,2,3}$+0.3	
Fixed Supply Voltage	V_{CC}	–0.3	25	
Low Side Driver Return	V_{SO}	V_{CC}–0.3	V_{CC}+0.3	
Low Side Output Voltage	$V_{LO1,2,3}$	V_{SO}–0.3	V_{CC}+0.3	
Logic Input Voltage (HIN–, LIN–, & ITRIP)	V_{IN}	–0.3	V_{CC}+0.3	
Fault Output Voltage	FAULT–	–0.3	V_{CC}+0.3	
Amplifier Output Voltage	CAO	–0.3	V_{CC}+0.3	
Amplifier Inverting Input Voltage	CA–	–0.3	V_{CC}+0.3	
Allowable Offset Supply Voltage Transient	dV_S/dt	–	50	V/ns
*Package Power Dissipation @ $T_A \le +25°C$	P_D	–	1.5	Watt
Operating and Storage Temperature	T_j, T_{stg}	–55	150	°C
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	–	83	°C/W
Lead Temperature for Soldering Purposes, 10 seconds	T_L	–	260	°C

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differential.

High Side Floating Supply Absolute Voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+10	$V_{S1,2,3}$+20	V
High Side Floating Supply Offset Voltage	$V_{S1,2,3}$	Note 1	V_{SO}+600	V
High Side Floating Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Fixed Supply Voltage	V_{CC}	10	20	V
Low Side Driver Return	V_{SO}	–5	5	V
Low Side Output Voltage	$V_{LO1,2,3}$	V_{SO}	V_{CC}	V
Logic Input Voltage (HIN–, LIN–, & ITRIP)	V_{IN}	V_{SS}	5	V
Fault Output Voltage	FAULT–	V_{SS}	V_{CC}	V
Amplifier Output Voltage	CAO	V_{SS}	5	V
Amplifier Inverting Input Voltage	CA–	V_{SS}	5	V
Ambient Temperature	T_A	–40	125	°C

Note 1: Logic operational for V_S of –5 V to +600 V. Logic state held for V_S of V_{SO}–5 V to V_{SO}–V_{BS}.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS					
V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V and V_{SO} = V_{SS} unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HS1,2,3 & LS1,2,3). The VO and IO parameters are referenced to $V_{SO1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.					
Logic “0” Input Voltage (OUT = LO)	V_{IH}	2.2	–	–	V
Logic “1” Input Voltage (OUT = HI)	V_{IL}	–	–	0.8	V
ITRIP Input Positive Going Threshold	$V_{IT,TH+}$	400	–	580	mV
High Level Output Voltage, V_{BIAS}–V_O @ V_{IN} = 0 V, I_O = 0 A	V_{OH}	–	–	100	mV
Low Level Output Voltage, V_O @ V_{IN} = 5 V, I_O = 0 A	V_{OL}	–	–	100	mV
Offset Supply Leakage Current @ $V_{B1,2,3}$ = $V_{S1,2,3}$ = 600 V	I_{LK}	–	–	50	µA
Quiescent V_{BS} Supply Current @ V_{IN} = 0 V or 5 V	I_{QBS}	–	15	30	µA
Quiescent V_{CC} Supply Current @ V_{IN} = 0 V or 5 V	I_{QCC}	–	3.0	4.0	mA
Logic “1” Input Bias Current (OUT = HI) @ V_{IN} = 0 V	I_{IN+}	–	400	500	µA
Logic “0” Input Bias Current (OUT = LO) @ V_{IN} = 5 V	$I_{IN–}$	–	200	320	µA
“High” ITRIP Bias Current @ ITRIP = 5 V	I_{TRIP+}	–	75	150	µA
“Low” ITRIP Bias Current @ ITRIP = 0 V	$I_{TRIP–}$	–	–	100	nA
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	8.0	–	9.2	V
V_{BS} Supply Undervoltage Negative Going Threshold	$V_{BSUV–}$	7.6	–	8.8	V
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	8.3	–	9.7	V
V_{CC} Supply Undervoltage Negative Going Threshold	$V_{CCUV–}$	8.0	–	9.4	V
FAULT – Low On Resistance	$R_{on,FLT}$	–	55	75	Ω
Output High Short Circuit Pulsed Current @ V_{out} = 0 V, V_{in} = 0 V, PW ≤ 10 µs	I_{O+}	200	250	–	mA
Output Low Short Circuit Pulsed Current @ V_{out} = 15 V, V_{in} = 5 V, PW ≤ 10 µs	$I_{O–}$	420	500	–	mA
Amplifier Input Offset Voltage @ V_{SO} = CA– = 0.2	V_{OS}	–	–	30	mV
CA– Input Bias Current @ CA– = 2.5 V	$I_{CA–}$	–	–	4.0	nA
Amplifier Common Mode Rejection Ratio @ V_{SO} = CA– = 0.1 V & 5 V	CMRR	60	80	–	dB

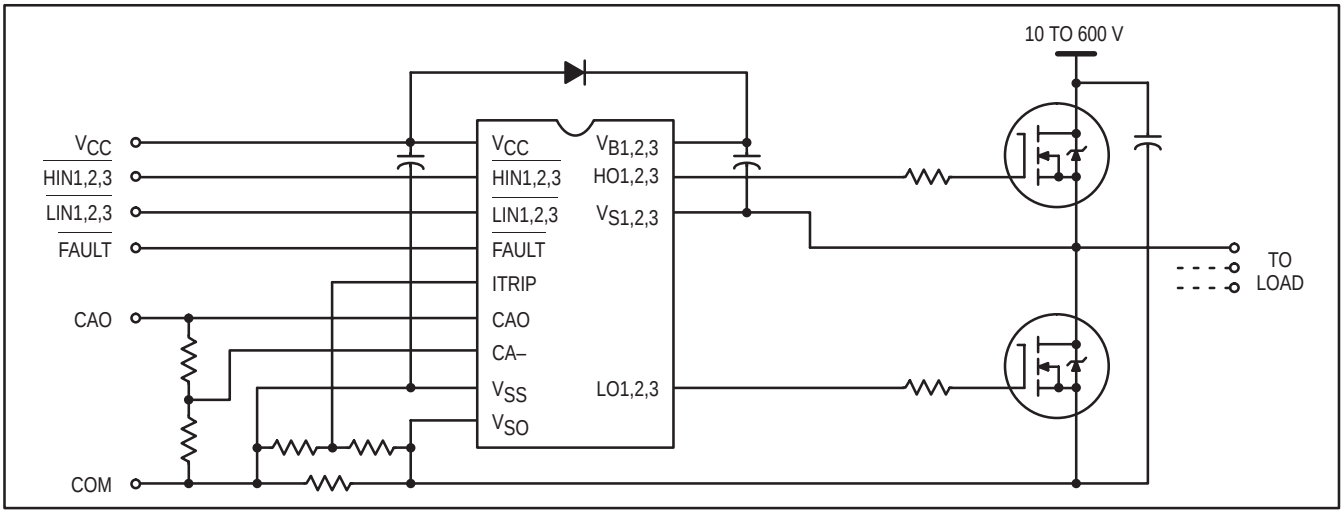
ELECTRICAL CHARACTERISTICS (continued) (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS					
V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V and V_{SO} = V_{SS} unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HS1,2,3 & LS1,2,3). The VO and IO parameters are referenced to $V_{SO1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.					
Amplifier Power Supply Rejection Ratio @ V_{SO} = CA–=0.2 V, V_{CC} = 10 & 20 V	PSRR	55	75	–	dB
Amplifier High Level Output Voltage @ CA– = 0 V, V_{SO} = 1 V	$V_{OH,Amp}$	5.0	–	5.4	V
Amplifier Low Level Output Voltage @ CA– = 1 V, V_{SO} = 0 V	$V_{OL,Amp}$	–	–	20	mV
Amplifier Output Source Current @ CA– = 0 V, V_{SO} = 1 V, CAO = 4 V	$I_{SRC,Amp}$	2.3	4.0	–	mA
Amplifier Output Sink Current @ CA– = 1 V, V_{SO} = 0 V, CAO = 2 V	$I_{SNK,Amp}$	1.0	2.1	–	mA
Amplifier Output High Short Circuit Current @ CA– = 1 V, V_{SO} = 5 V, CAO = 0 V	$I_{O+,Amp}$	–	4.5	6.5	mA
Amplifier Output Low Short Circuit Current @ CA– = 5 V, V_{SO} = 0 V, CAO = 5 V	$I_{O–,Amp}$	–	3.2	5.2	mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC ELECTRICAL CHARACTERISTICS					
V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V, $V_{SO1,2,3}$ = V_{SS} and C_L = 1000 pF unless otherwise specified. T_A = 25°C.					
Turn–On Propagation Delay @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_{on}	500	–	850	ns
Turn–Off Propagation Delay @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_{off}	300	–	550	ns
Turn–On Rise Time @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_r	–	80	125	ns
Turn–Off Fall Time @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_f	–	35	55	ns
ITRIP to Output Shutdown Propagation Delay @ V_{IN}, V_{ITRIP} = 0 & 5 V	t_{itrip}	400	–	920	ns
ITRIP Blanking Time @ ITRIP = 1 V	t_{bl}	–	400	–	ns
ITRIP to FAULT– Propagation Delay @ V_{IN}, V_{ITRIP} = 0 & 5 V	t_{flt}	335	–	845	ns
Input Filter Time (all six inputs) @ V_{IN} = 0 & 5 V	$t_{flt,in}$	–	310	–	ns
LIN1,2,3 to FAULT Clear Time @ V_{IN}, V_{ITRIP} = 0 & 5 V	t_{fltclr}	6.0	–	12	µs
Deadtime, LS Turn–Off to HS Turn–On & HS Turn–Off to LS Turn–On @ V_{IN} = 0 & 5 V	DT	1.3	–	3.7	µs
Amplifier Slew Rate (Positive)	SR+	4.4	6.2	–	V/µs
Amplifier Slew Rate (Negative)	SR–	2.4	3.2	–	V/µs

TYPICAL CONNECTION



LEAD DEFINITIONS

Symbol	Lead Description
HIN1,2,3	Logic Inputs for High Side Gate Driver Outputs (HO1,2,3), Out of Phase
LIN1,2,3	Logic Inputs for Low Side Gate Driver Outputs (LO1,2,3), Out of Phase
FAULT–	Indicates Over–current, or Undervoltage Lockout (Low Side) has Occurent, Negative Logic
V_{CC}	Logic and Low Side Fixed Supply
ITRIP	Input for Over–current Shut Down
CAO	Output of Current Amplifier
CA–	Negative Input of Current Amplifier
V_{SS}	Logic Ground
$V_{B1,2,3}$	High Side Floating Supplies
HO1,2,3	High Side Gate Drive Outputs
$V_{S1,2,3}$	High Side Floating Supply Returns
LO1,2,3	Low Side Gate Drive Outputs
V_{SO}	Low Side Return, Positive Input of Current Amplifier

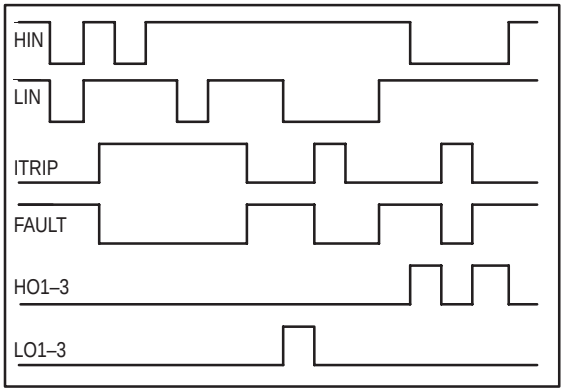


Figure 1. Input / Output Timing Diagram

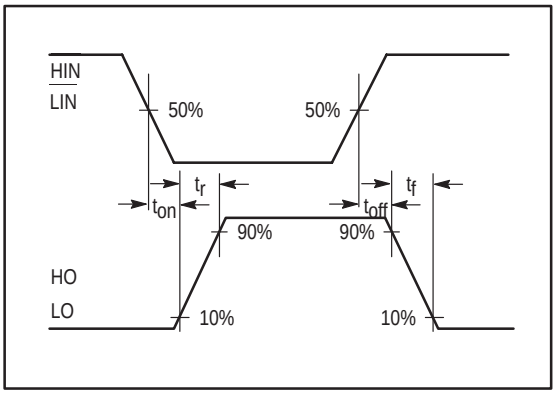


Figure 2. Switching Time Waveform Definitions

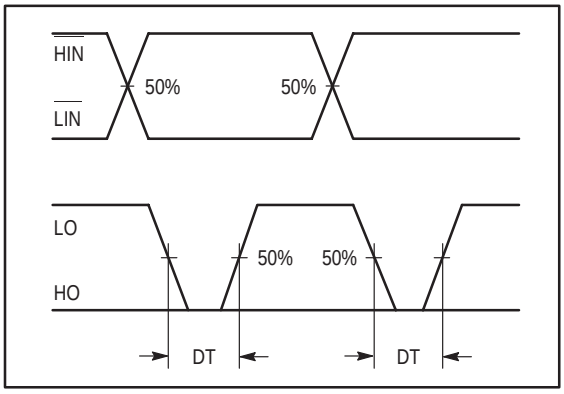


Figure 3. Deadtime Waveform Definitions

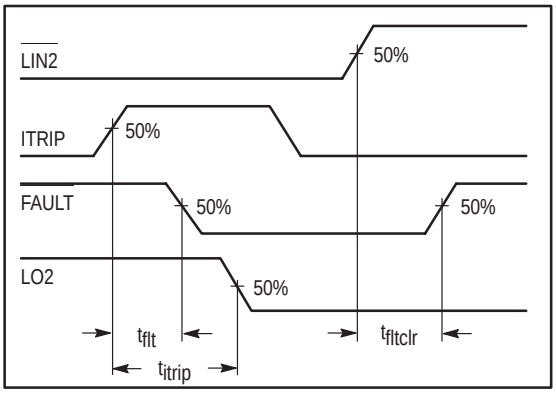


Figure 4. Overcurrent Shutdown Waveform Definitions

Power Products Division

Advance Information

3-HIGH SIDE & 3-LOW SIDE DRIVER

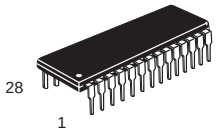
MPIC2131

3 HIGH SIDE & 3 LOW SIDE DRIVER

The MPIC2131 is a high voltage, high speed, power MOSFET and IGBT driver with three independent high side and low side referenced output channels for 3–Phase applications. Proprietary HVIC technology enables ruggedized monolithic construction. Logic inputs are compatible with 5 V CMOS or LSTTL outputs. A ground referenced operational amplifier provides an analog feedback of bridge current via an external current sense resistor. A current trip function which terminates all six outputs is also derived from an external current sense resistor. An extra shutdown input is provided for customizing the shutdown function. An open drain FAULT signal is provided to indicate that any of shutdown conditions has occurred. The output drivers feature a high pulse current buffer stage designed for minimum driver cross–conduction. Propagation delays are matched to simplify use in high frequency applications.

The floating channels can be used to drive N–channel power MOSFET or IGBT's in the high side configuration which operate from 10 to 600 volts.

- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Gate Drive Supply Range from 10 to 20 V
- Undervoltage Lockout for All Channels
- Over–current Shut Down Turns Off All Six Drivers
- Independent 3 High Side & 3 Low Side Drivers
- Matched Propagation Delay for All Channels
- Outputs Out of Phase with Inputs

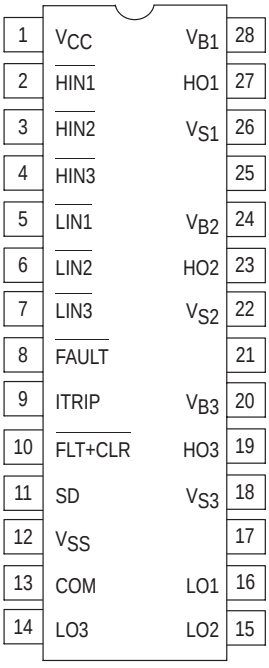


P SUFFIX
PLASTIC PACKAGE
CASE 710–02

PRODUCT SUMMARY

V_{OFFSET}	600 V MAX
$I_{O+/-}$	200 mA/420 mA
V_{OUT}	10 – 20 V
$t_{on/off}$ (typical)	1.4 & 0.7 µs
Delay Matching	700 ns

PIN CONNECTIONS



(TOP VIEW)

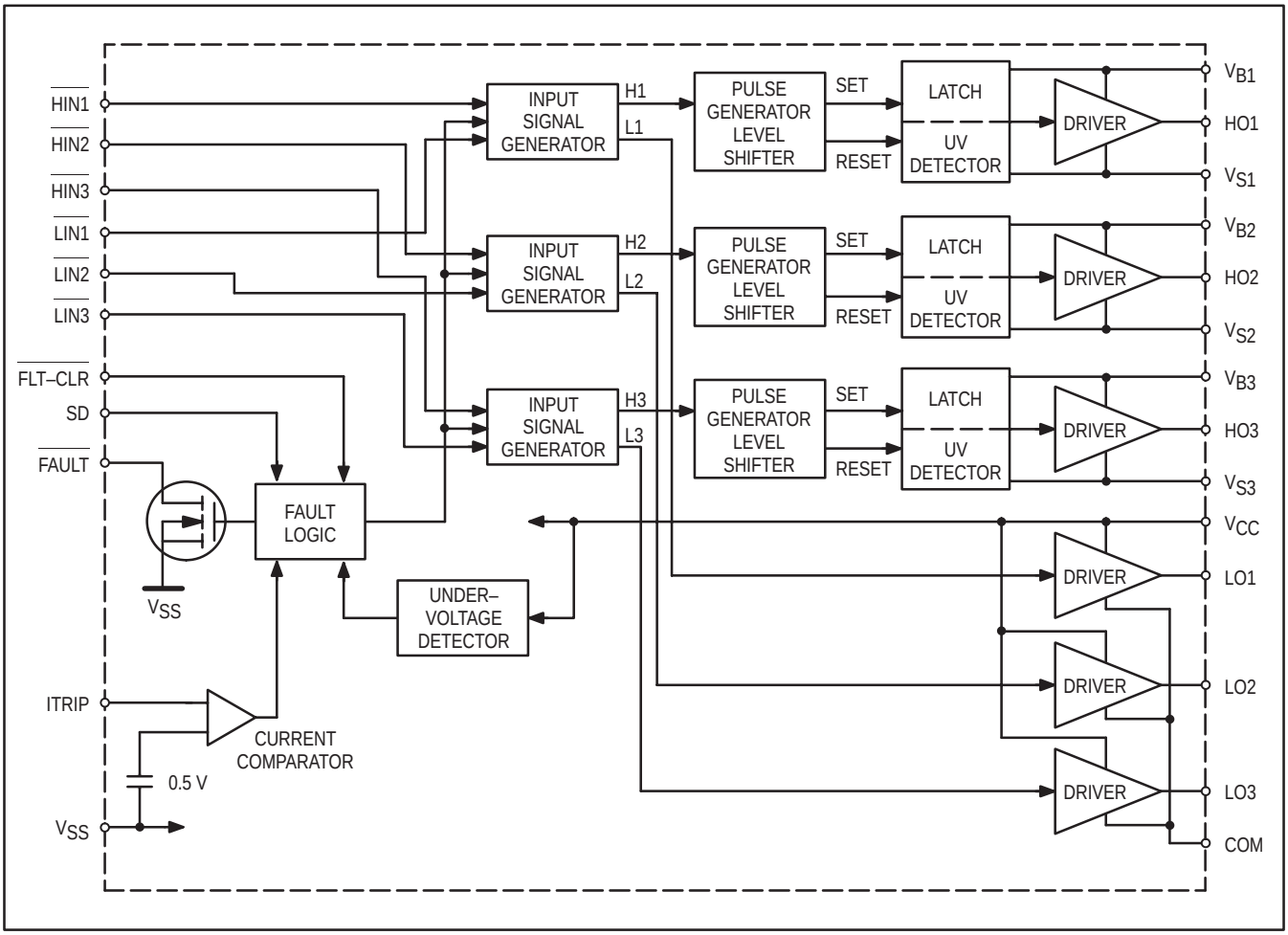
ORDERING INFORMATION

Device	Package
MPIC2131P	PDIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating	Symbol	Min	Max	Unit
High Side Floating Absolute Voltage High Side Floating Supply Offset Voltage High Side Floating Output Voltage Low Side Output Voltage Fixed Supply Voltage Fixed Supply Offset Voltage Logic Input Voltage (HIN–, LIN–, FLT–, CLR–, SD & ITRIP) Fault Output Voltage	$V_{B1,2,3}$ $V_{S1,2,3}$ $V_{HO1,2,3}$ $V_{LO1,2,3}$ V_{CC} V_{SS} V_{IN} FAULT	–0.3 $V_{B1,2,3}$–25 $V_{S1,2,3}$–0.3 –0.3 –0.3 V_{CC}–25 V_{SS}–0.3 V_{SS}–0.3	625 $V_{B1,2,3}$+0.3 $V_{B1,2,3}$+0.3 V_{CC}+0.3 25 V_{CC}+0.3 V_{CC}+0.3 V_{CC}+0.3	V_{DC}
Allowable Offset Supply Voltage Transient	dV_S/dt	–	50	V/ns
*Package Power Dissipation @ $T_C \leq +25°C$ (28 Lead DIP)	P_D	–	1.5	Watt
Operating and Storage Temperature	T_j, T_{stg}	–55	150	°C
Thermal Resistance, Junction to Ambient (8 Lead DIP)	$R_{\theta JA}$	–	83	°C/W
Lead Temperature for Soldering Purposes, 10 seconds	T_L	–	260	°C

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S offset rating is tested with all supplies biased at 15 V differential.

High Side Floating Supply Absolute Voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+10	$V_{S1,2,3}$+20	V
High Side Floating Supply Offset Voltage	$V_{S1,2,3}$	Note 1	V_{SO}+600	V
High Side Floating Output Voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$	$V_{B1,2,3}$	V
Fixed Supply Voltage	V_{CC}	10	20	V
Low Side Output Voltage	$V_{LO1,2,3}$	0	V_{CC}	V
Low Side Driver Return	V_{SS}	–5	5	V
Logic Input Voltage (HIN–, LIN–, FLT–CLR, SD & ITRIP)	V_{IN}	V_{SS}	5	V
Fault Output Voltage	FAULT–	V_{SS}	V_{CC}	V
Ambient Temperature	T_A	–40	125	°C

Note 1: Logic operational for V_S of –5 V to +600 V. Logic state held for V_S of –5 V to –V_{BS}.

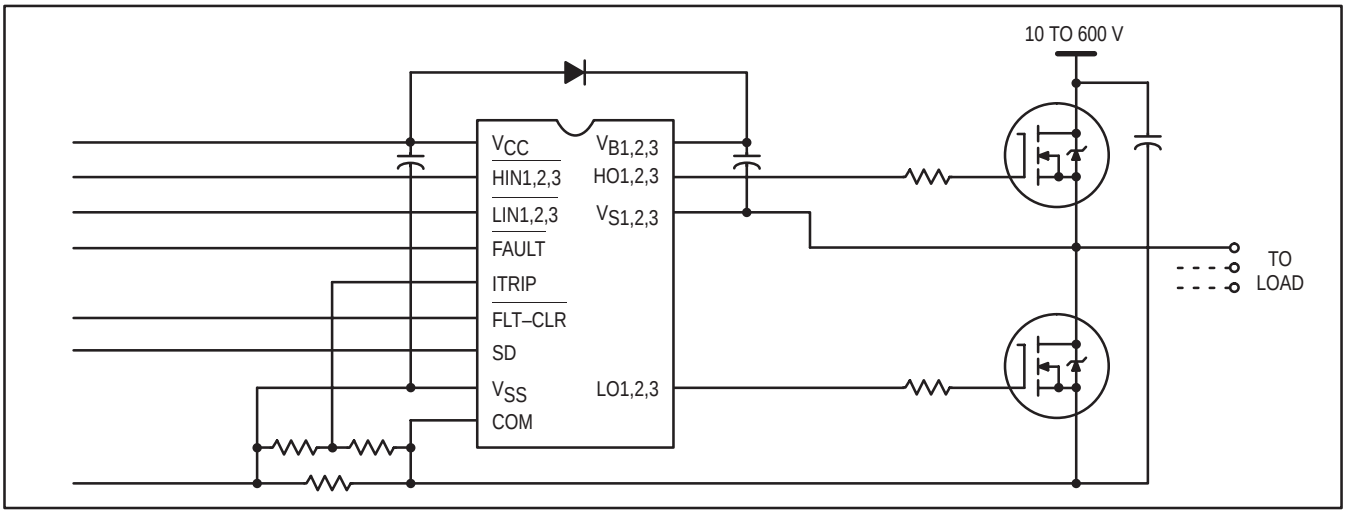
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS					
V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V and V_{SS} = COM unless otherwise specified. The V_{IN}, V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HS1,2,3 & LS1,2,3). The VO and IO parameters are referenced to COM and $V_{SO1,2,3}$ and are applicable to the respective output leads: HO1,2,3 or LO1,2,3.					
Logic “0” Input Voltage (OUT = LO)	V_{IH}	2.2	–	–	V
Logic “1” Input Voltage (OUT = HI)	V_{IL}	–	–	0.8	V
Logic “0” Fault Clear Input Voltage	$V_{FCLR,IH}$	2.2	–	–	V
Logic “1” Fault Clear Input Voltage	$V_{FCLR,IL}$	–	–	0.8	V
SD Input Positive Going Threshold	$V_{SD,TH+}$	–	1.8	–	V
SD Input Negative Going Threshold	$V_{SD,TH–}$	–	1.5	–	V
ITRIP Input Positive Going Threshold	$V_{IT,TH+}$	–	485	–	mV
ITRIP Input Negative Going Threshold	$V_{IT,TH–}$	–	400	–	mV
High Level Output Voltage, V_{BIAS}–V_O @ V_{IN} = 0 V, I_O = 0 A	V_{OH}	–	–	100	mV
Low Level Output Voltage, V_O @ V_{IN} = 5 V, I_O = 0 A	V_{OL}	–	–	100	mV
Offset Supply Leakage Current @ $V_{B1,2,3}$ = $V_{S1,2,3}$ = 600 V	I_{LK}	–	–	50	µA
Quiescent V_{BS} Supply Current @ V_{IN} = 0 V or 5 V	I_{QBS}	–	30	–	µA
Quiescent V_{CC} Supply Current @ V_{IN} = 0 V or 5 V	I_{QCC}	–	3.0	–	mA
Logic “1” Input Bias Current (OUT = HI) @ V_{IN} = 0 V	I_{IN+}	–	190	–	µA
Logic “0” Input Bias Current (OUT = LO) @ V_{IN} = 5 V	$I_{IN–}$	–	100	–	µA
“High” ITRIP Bias Current @ ITRIP = 5 V	I_{TRIP+}	–	60	–	µA
“Low” ITRIP Bias Current @ ITRIP = 0 V	$I_{TRIP–}$	–	–	50	nA
Logic “1” Fault Clear Bias Current @ FLT–CLR = 0 V	I_{FCLR+}	–	190	–	µA
Logic “0” Fault Clear Bias Current @ FLT–CLR = 5 V	$I_{FCLR–}$	–	100	–	µA
Logic “1” Shut Down Bias Current @ SD = 5 V	I_{SD+}	–	60	–	µA
Logic “0” Shut Down Bias Current @ SD = 5 V	$I_{SD–}$	–	–	150	nA
V_{BS} Supply Undervoltage Positive Going Threshold	V_{BSUV+}	–	8.6	–	V
V_{BS} Supply Undervoltage Negative Going Threshold	$V_{BSUV–}$	–	8.2	–	V
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	–	9.0	–	V
V_{CC} Supply Undervoltage Negative Going Threshold	$V_{CCUV–}$	–	8.7	–	V
FAULT – Low On Resistance	$R_{on,FLT}$	–	55	–	Ω
Output High Short Circuit Pulsed Current @ V_{out} = 0 V, V_{in} = 0 V, PW ≤ 10 µs	I_{O+}	200	250	–	mA
Output Low Short Circuit Pulsed Current @ V_{out} = 15 V, V_{in} = 5 V, PW ≤ 10 µs	$I_{O–}$	420	500	–	mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
DYNAMIC ELECTRICAL CHARACTERISTICS					
V_{BIAS} (V_{CC}, $V_{BS1,2,3}$) = 15 V, $V_{SO1,2,3}$ = V_{SS} and C_L = 1000 pF unless otherwise specified. T_A = 25°C.					
Turn–On Propagation Delay @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_{on}	–	1.4	–	µs
Turn–Off Propagation Delay @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_{off}	–	0.7	–	µs
Turn–On Rise Time @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_r	–	80	–	ns
Turn–On Fall Time @ V_{IN} = 0 & 5 V, $V_{S1,2,3}$ = 0 V to 600 V	t_f	–	40	–	ns
ITRIP to Output Shutdown Propagation Delay @ V_{IN}, V_{ITRIP} = 0 & 5 V	t_{itrip}	–	550	–	ns
ITRIP Blanking Time @ ITRIP = 1 V	t_{bl}	–	400	–	ns
ITRIP to FAULT– Propagation Delay @ V_{IN}, V_{ITRIP} = 0 & 5 V	t_{flt}	–	450	–	ns
Input Filter Time (all six inputs) @ V_{IN} = 0 & 5 V	$t_{flt,in}$	–	310	–	ns
FLT–CLR to FAULT Clear Time @ V_{IN}, V_{IT}, V_{FC} = 0 & 5 V	t_{fltclr}	–	450	–	ns
SD to OUTPUT Shutdown Propagation Delay @ V_{IN}, V_{SD} = 0 & 5 V	t_{sd}	–	550	–	ns
Deadtime, LS Turn–Off to HS Turn–On & HS Turn–Off to LS Turn–On @ V_{IN} = 0 & 5 V	DT	–	700	–	ns

TYPICAL CONNECTION



LEAD DEFINITIONS

Symbol	Lead Description
HIN1,2,3	Logic Inputs for High Side Gate Driver Outputs (HO1,2,3), Out of Phase
LIN1,2,3	Logic Inputs for Low Side Gate Driver Outputs (LO1,2,3), Out of Phase
FLT–CLR	Logic Inputs for Fault Clear
SD	Logic Input for Shut Down
FAULT	Indicates Over–current, Shut Down or Low Side Undervoltage Condition, Negative Logic
ITRIP	Input for Over–current Shut Down
V_{SS}	Logic Ground
$V_{B1,2,3}$	High Side Floating Supplies
HO1,2,3	High Side Gate Drive Outputs
$V_{S1,2,3}$	High Side Floating Supply Returns
V_{CC}	Logic and Low Side Fixed Supply
LO1,2,3	Low Side Gate Drive Outputs
COM	Low Side Return

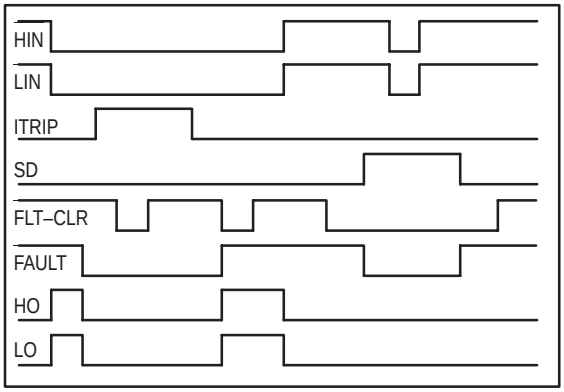


Figure 1. Input / Output Timing Diagram

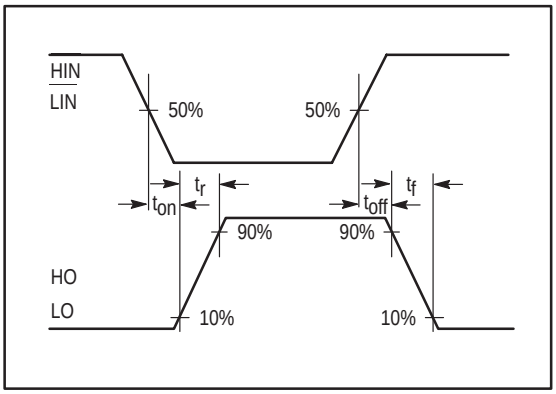


Figure 2. Switching Time Waveform Definitions

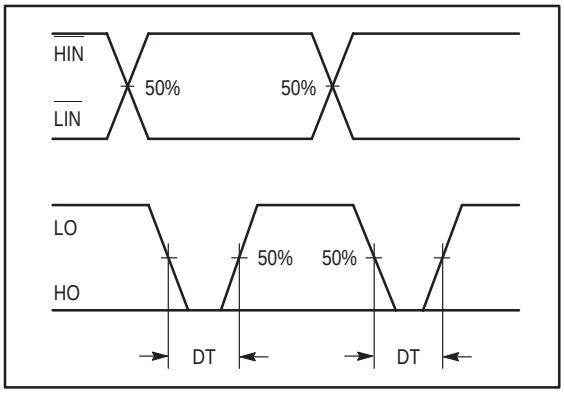


Figure 3. Deadtime Waveform Definitions

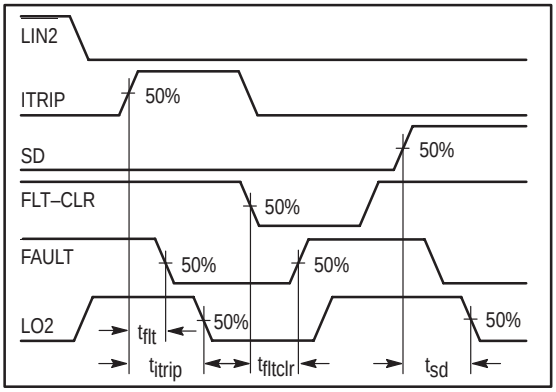


Figure 4. Shutdown Waveform Definitions

Power Products Division

Advance Information

SELF-OSCILLATING HALF-BRIDGE DRIVER

MPIC2151

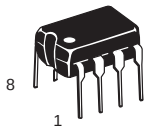
SELF–OSCILLATING HALF–BRIDGE DRIVER

The MPIC2151 is a high voltage, high speed, self–oscillating power MOSFET and IGBT driver with both high side and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The front–end features a programmable oscillator which is similar to the 555 timer. The output drivers feature a high pulse current buffer stage and an internal deadtime designed for minimum driver cross–conduction. Propagation delays for the two channels are matched to simplify use in 50% duty cycle applications. The floating channel can be used to drive an N–channel power MOSFET or IGBT in the high side configuration that operates off a high voltage rail from 10 to 600 volts.

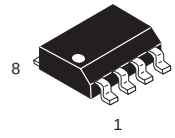
- Floating Channel Designed for Bootstrap Operation
- Fully Operational to +600 V
- Tolerant to Negative Transient Voltage
- dV/dt Immune
- Undervoltage Lockout
- Programmable Oscillator Frequency:

$$f = \frac{1}{1.4\ (RT + 75\Omega)\ CT}$$

- Matched Propagation Delay for Both Channels
- Low Side Output In Phase with RT



P SUFFIX
PLASTIC PACKAGE
CASE 626–05

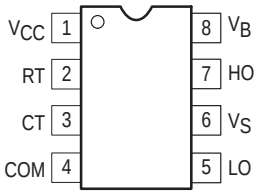


D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)

PRODUCT SUMMARY

V_{OFFSET}	600 V MAX
Duty Cycle	50%
V_{OUT}	10 – 20 V
$t_{r/f}$ (typical)	120 & 60 ns
Deadtime (typical)	1.2 μs

PIN CONNECTIONS



(TOP VIEW)

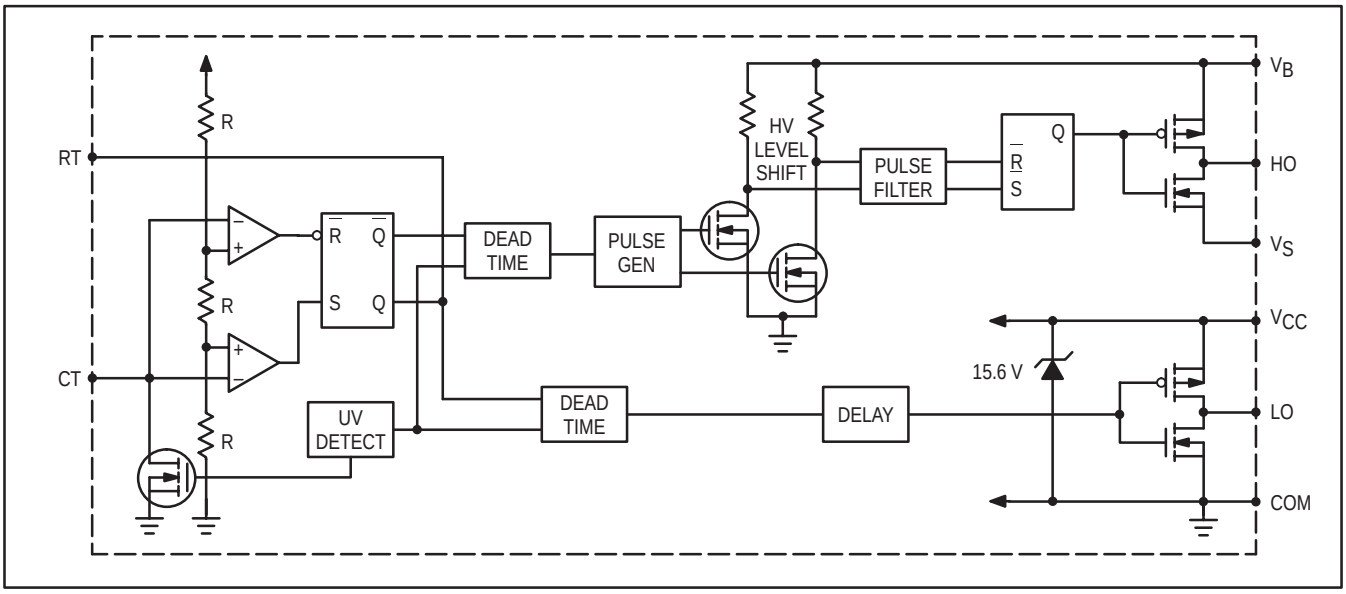
ORDERING INFORMATION

Device	Package
MPIC2151D	SOIC
MPIC2151P	PDIP

This document contains information on a new product. Specifications and information herein are subject to change without notice.

REV 1

SIMPLIFIED BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

Rating		Symbol	Min	Max	Unit
High Side Floating Supply Absolute Voltage High Side Floating Supply Offset Voltage High Side Floating Output Voltage Low Side Output Voltage RT Voltage CT Voltage		V_B V_S V_{HO} V_{LO} V_{RT} V_{CT}	–0.3 V_B–25 V_S–0.3 –0.3 –0.3 –0.3	625 V_B+0.3 V_B+0.3 V_{CC}+0.3 V_{CC}+0.3 V_{CC}+0.3	V_{DC}
Supply Current (Note 1) High Side Output Current Low Side Output Current RT Output Current		I_{CC} I_{HO} I_{LO} I_{RT}	– –500 –500 –5.0	25 500 500 5.0	mA_{DC}
Allowable Offset Supply Voltage Transient		dV_S/dt	–	50	V/ns
*Package Power Dissipation @ $T_C \leq +25°C$	(8 Lead DIP) (8 Lead SOIC)	P_D –	– –	1.0 0.625	Watt
Operating and Storage Temperature		T_j, T_{stg}	–55	150	°C
Thermal Resistance, Junction to Ambient	(8 Lead DIP) (8 Lead SOIC)	$R_{\theta JA}$	– –	125 200	°C/W
Lead Temperature for Soldering Purposes, 10 seconds		T_L	–	260	°C

RECOMMENDED OPERATING CONDITIONS

The Input/Output logic timing Diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions.

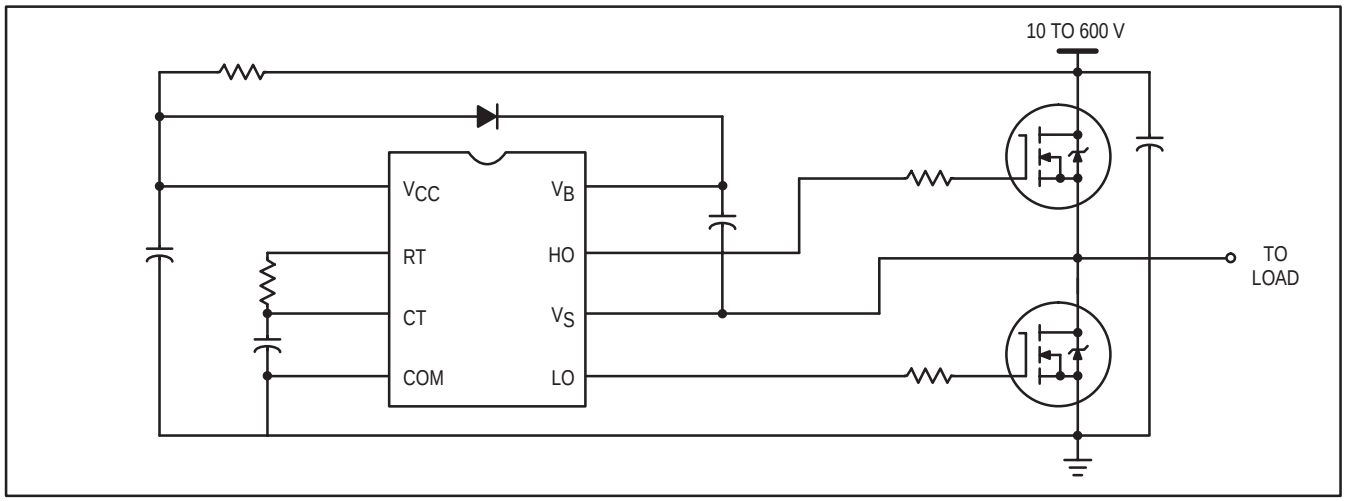
High Side Floating Supply Absolute Voltage	V_B	V_S+10	V_S+V_{clamp}	V
High Side Floating Supply Offset Voltage	V_S	–	600	
High Side Floating Output Voltage	V_{HO}	V_S	V_B	
Low Side Output Voltage	V_{LO}	0	V_{CC}	
Supply Current (Note 1)	I_{CC}	–	5.0	mA
Ambient Temperature	T_A	–40	125	°C

Note 1: Because the MPIC2151 is designed specifically for off–line supply systems, this IC contains a zener clamp structure between the chip V_{CC} and COM which has a nominal breakdown voltage of 15.6 V. Therefore, the IC supply voltage is normally derived by forcing current into the supply lead (typically by means of a high value resistor connected between the chip V_{CC} and the rectified line voltage and a local decoupling capacitor from V_{CC} to COM) and allowing the internal zener clamp circuit to determine the nominal supply voltage. Therefore, this circuit should not be driven by a DC, low impedance power source of greater than V_{CLAMP}.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
STATIC ELECTRICAL CHARACTERISTICS					
Supply Characteristics					
V_{BIAS} (V_{CC}, V_{BS}) = 12 V, V_{SS} = COM and C_L = 1000 pF unless otherwise specified.					
V_{CC} Supply Undervoltage Positive Going Threshold	V_{CCUV+}	–	8.4	–	V_{DC}
V_{CC} Supply Undervoltage Negative Going Threshold	$V_{CCUV–}$	–	8.0	–	
Quiescent V_{CC} Supply Current	I_{QCC}	–	400	–	µA
V_{CC} Zener Shunt Clamp Voltage @ I_{OC} = 5 mA	V_{CLAMP}	–	15.6	–	V_{DC}
Floating Supply Characteristics					
Offset Supply Leakage Current @ V_B = V_S = 600 V	I_{LK}	–	–	50	µA$_{DC}$
Quiescent V_{BS} Supply Current	I_{QBS}	–	10	–	
Oscillator I/O Characteristics					
Oscillator Frequency @ RT = 35.7 KΩ, CT = 1 nF	f_{OSC}	–	20	–	kHz
Oscillator Frequency @ RT = 7.04 KΩ, CT = 1 nF	f_{OSC}	–	100	–	
CT Input Current	I_{CT}	–	0.001	1.0	µA
CT Undervoltage Lockout @ 2.5 V < V_{CC} < V_{CCUV+}	V_{CTUV}	–	0	–	mV
RT High Level Output Voltage, V_{CC} – RT @ IRT = –100 µA @ IRT = –1 mA	V_{RT+} V_{RT+}	– –	20 200	– –	
RT Low Level Output Voltage, V_{CC} + RT @ IRT = 100 µA @ IRT = 1 mA	$V_{RT–}$ $V_{RT–}$	– –	20 200	– –	
RT Undervoltage Lockout, V_{CC} – RT @ 2.5 V < V_{CC} < V_{CCUV+}	V_{RTUV}	–	0	–	
2/3 V_{CC} Threshold	V_{CT+}	–	8.0	–	V_{DC}
1/3 V_{CC} Threshold	$V_{CT–}$	–	4.0	–	
Output Characteristics					
High Level Output Voltage, V_{BIAS}–V_O @ I_O = 0 A	V_{OH}	–	–	100	mV
Low Level Output Voltage, V_O @ I_O = 0 A	V_{OL}	–	–	100	
Dynamic Electrical Characteristics					
V_{BIAS} (V_{CC}, V_{BS}) = 12 V and C_L = 1000 pF unless otherwise specified. T_A = 25°C.					
Turn–On Rise Time	t_r	–	120	–	ns
Turn–Off Fall Time	t_f	–	60	–	
Deadtime, LS Turn–Off to HS Turn–On & HS Turn–Off to LS Turn–On	DT	–	1.2	–	µA
RT Duty Cycle, f_{OSC} = 20 kHz	DC	–	50	–	%

TYPICAL CONNECTION



LEAD DEFINITIONS

Symbol	Lead Description
RT	Oscillator timing resistor input; a resistor is connected from RT to CT. RT is in phase with LO for normal IC operation.
CT	Oscillator timing capacitor input; a capacitor is connected from CT to COM in order to program the oscillator frequency according to the following equation: $f = \frac{1}{1.4\ (RT + 75\Omega)\ CT}$ where 75Ω is the effective impedance of the R_T output stage.
V_B	High Side Floating Supply
HO	High Side Gate Drive Output
V_S	High Side Floating Supply Return
V_{CC}	Logic and Low Side Fixed Supply
LO	Low Side Gate Drive Output
COM	Logic and Low Side Return

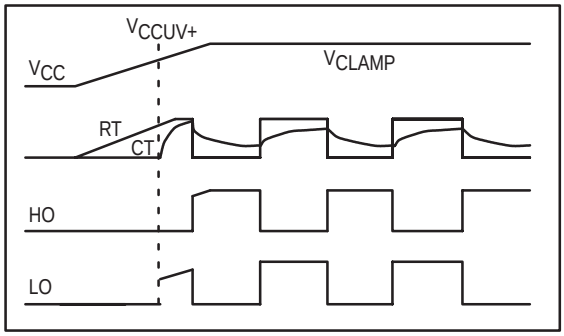


Figure 1. Input / Output Timing Diagram

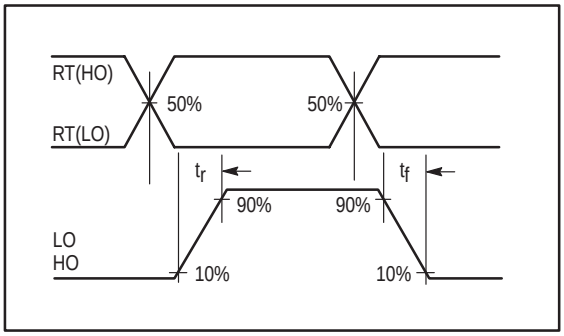


Figure 2. Switching Time Waveform Definitions

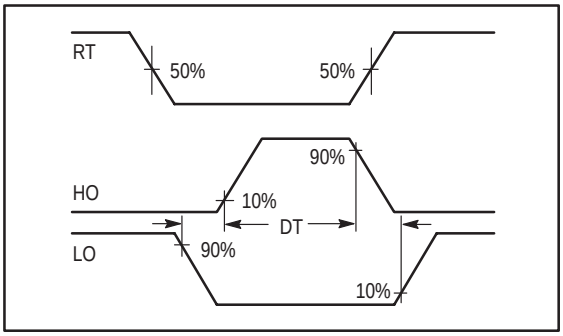


Figure 3. Deadtime Waveform Definitions

Designer's™ Data Sheet

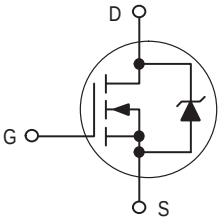
TMOS E-FET™
High Energy Power FET
D²PAK for Surface Mount

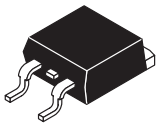
N–Channel Enhancement–Mode Silicon Gate

MTB1N100E

Motorola Preferred Device

TMOS POWER FET
1.0 AMPERES
1000 VOLTS
$R_{DS(on)}$ = 9.0 OHM





CASE 418B–02, Style 2
D²PAK

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	1000	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	1000	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	1.0 0.8 3.0	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted with the minimum recommended pad size	P_D	75 0.6 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.67 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	1000 —	— 1.251	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	— 6.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$R_{DS(on)}$	—	6.7	9.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 1.0 Adc) (I_D = 0.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	4.86 —	9.0 10.5	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 0.5 Adc)		g_{FS}	0.9	1.32	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	587	810	pF
Output Capacitance		C_{oss}	—	59.6	120	
Reverse Transfer Capacitance		C_{rss}	—	12.2	25	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 500 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	9.0	20	ns
Rise Time		t_r	—	12	25	
Turn–Off Delay Time		$t_{d(off)}$	—	28	50	
Fall Time		t_f	—	34	70	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	14.6	20	nC
		Q_1	—	2.8	—	
		Q_2	—	6.8	—	
		Q_3	—	5.2	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc) (I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.764 0.62	1.0 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	655	—	ns
		t_a	—	42	—	
		t_b	—	613	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.957	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

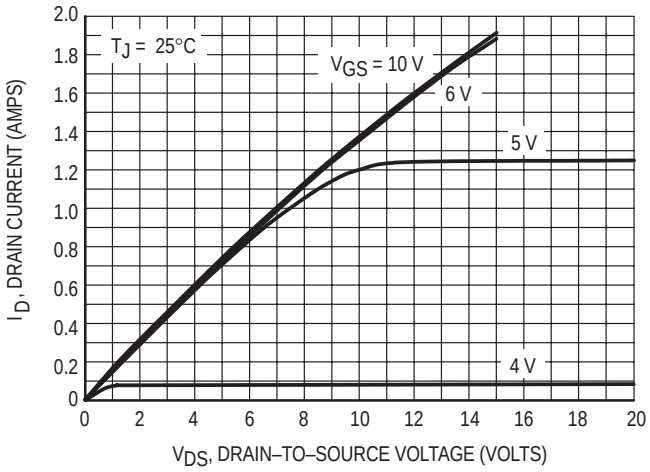


Figure 1. On–Region Characteristics

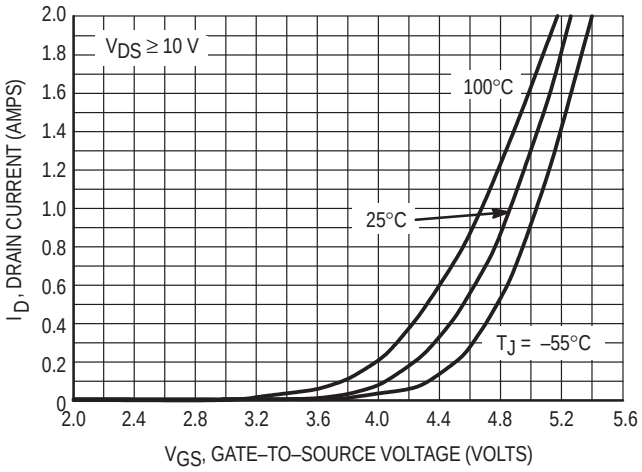


Figure 2. Transfer Characteristics

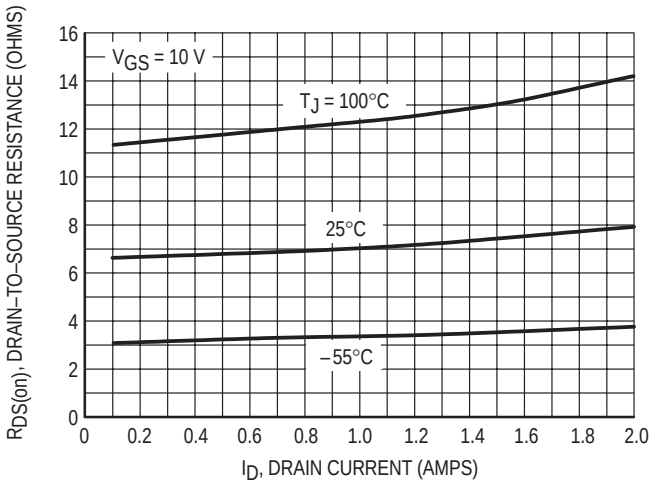


Figure 3. On–Resistance versus Drain Current and Temperature

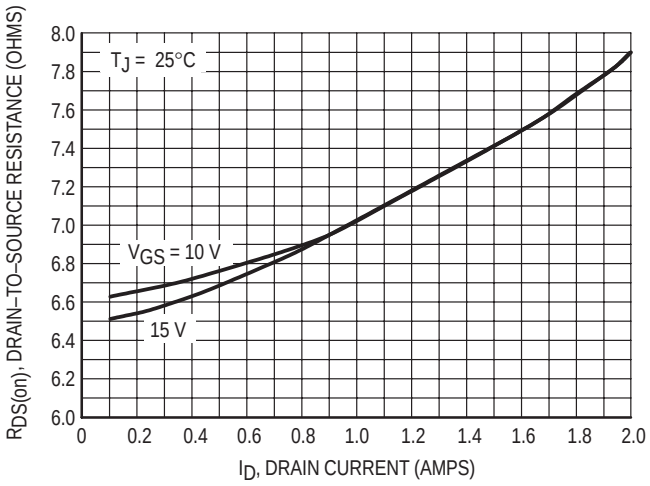


Figure 4. On–Resistance versus Drain Current and Gate Voltage

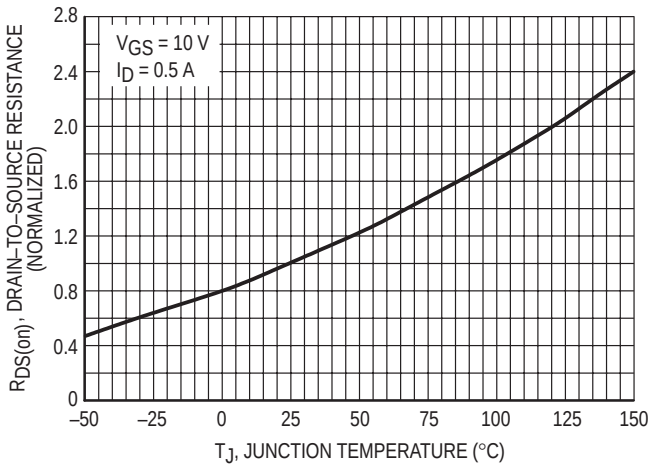


Figure 5. On–Resistance Variation with Temperature

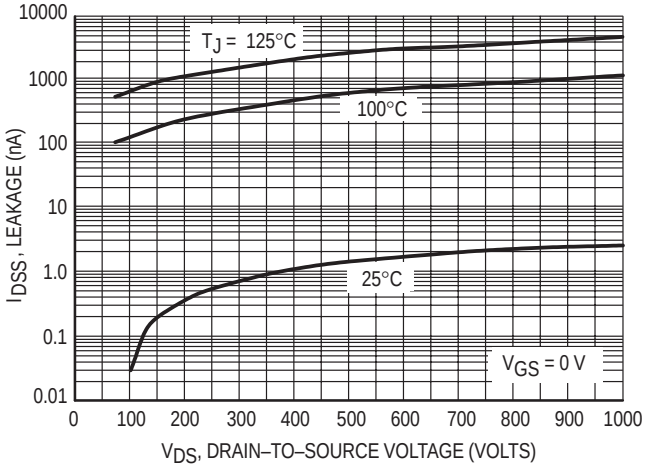


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

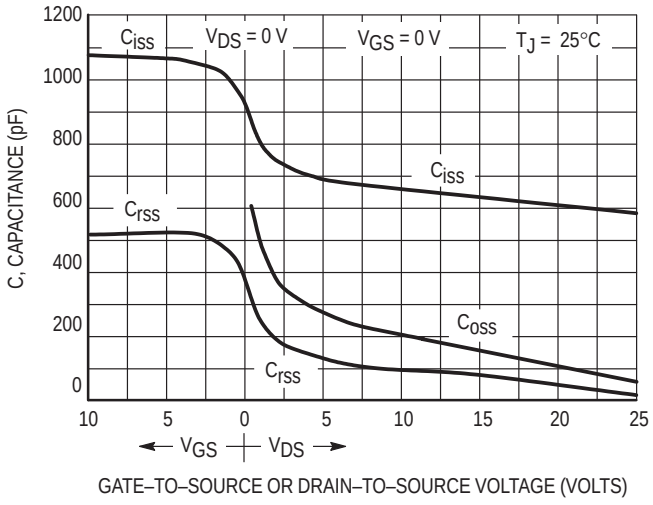


Figure 7a. Capacitance Variation

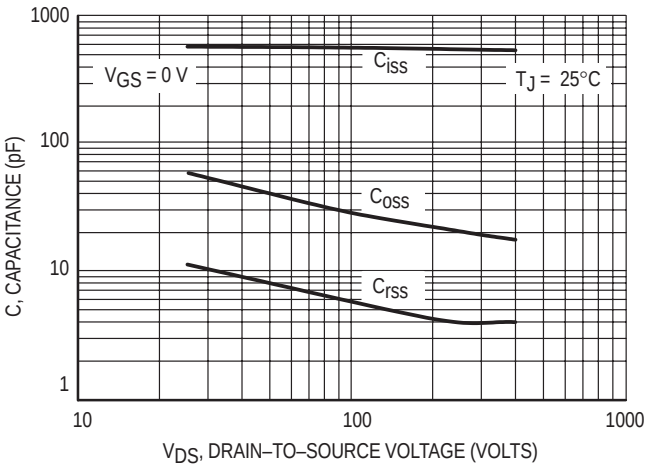


Figure 7b. High Voltage Capacitance Variation

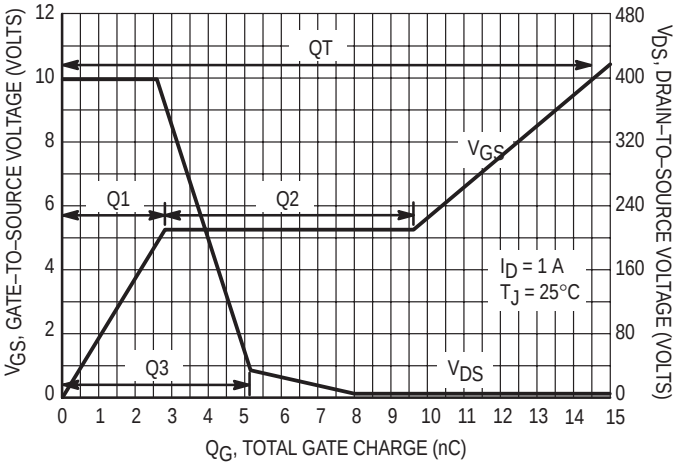


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

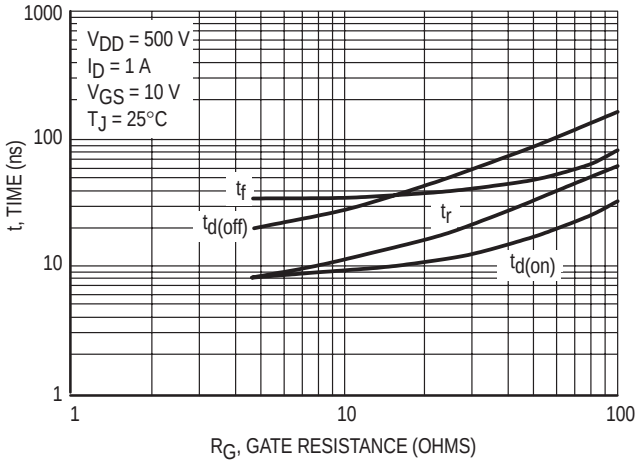


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

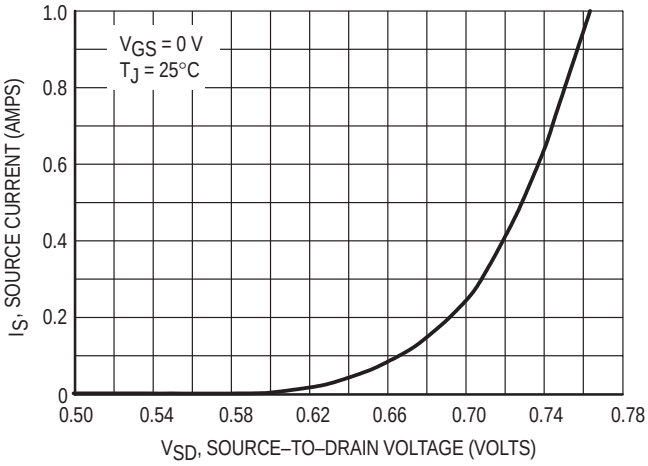


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

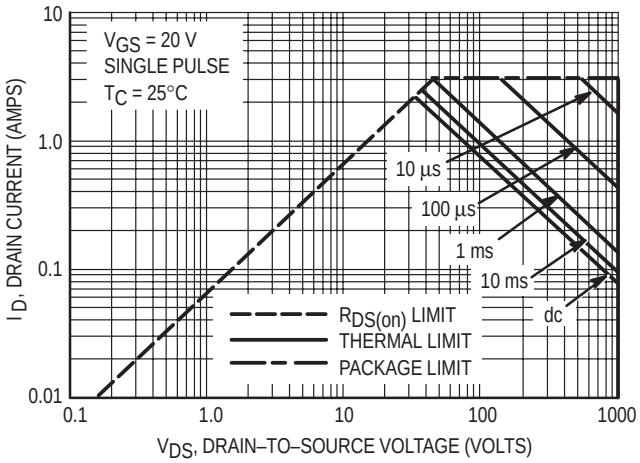


Figure 11. Maximum Rated Forward Biased Safe Operating Area

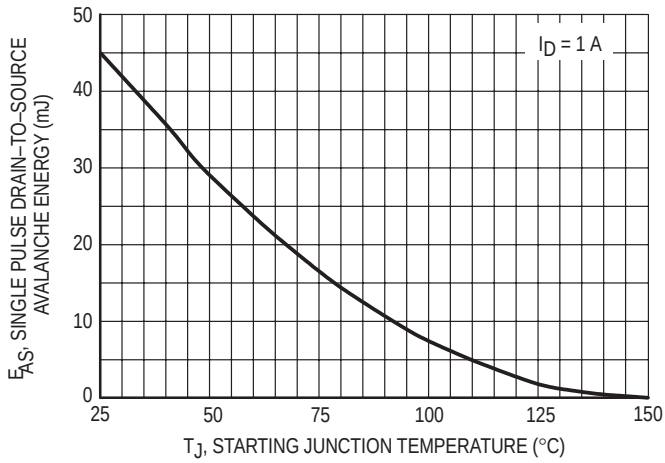


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

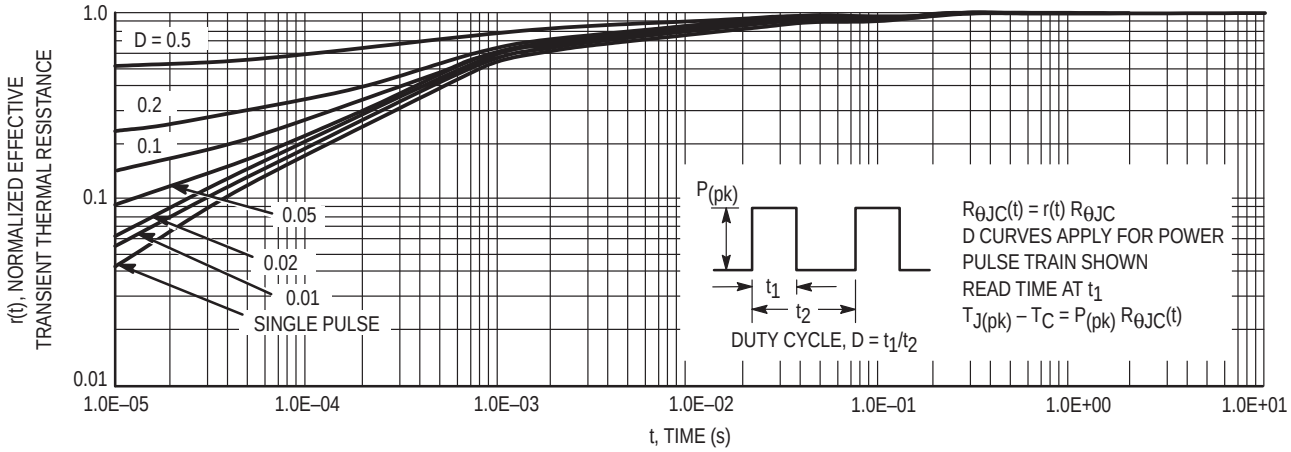


Figure 13. Thermal Response

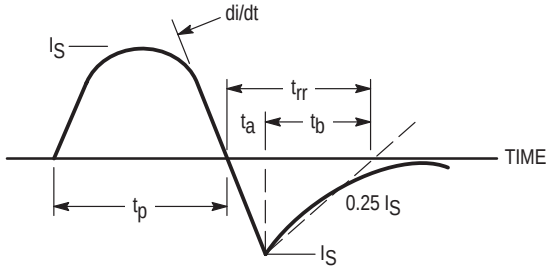


Figure 14. Diode Reverse Recovery Waveform

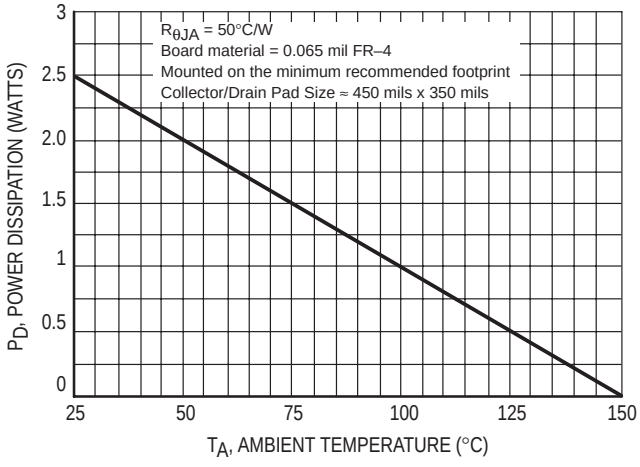


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

TMOS E-FET™
High Energy Power FET
D²PAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

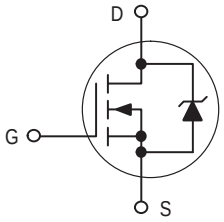
MTB2N40E

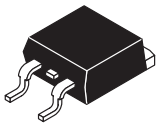
Motorola Preferred Device

TMOS POWER FET
2.0 AMPERES
400 VOLTS
$R_{DS(on)}$ = 3.8 OHM

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	400	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	2.0 1.5 6.0	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	40 0.32 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	400	—	—	Vdc
Temperature Coefficient (Positive)			—	451	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 400 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 400 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.2	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	—	3.1	3.5	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2.0 Adc)		$V_{DS(on)}$	—	7.3	8.4	Vdc
(V_{GS} = 10 Vdc, I_D = 1.0 Adc, T_J = 125°C)			—	—	7.4	
Forward Transconductance (V_{DS} = 50 Vdc, I_D = 1.0 Adc)		g_{FS}	0.5	1.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	229	320	pF
Output Capacitance		C_{oss}	—	34	40	
Transfer Capacitance		C_{rss}	—	7.3	10	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 200 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.0	16	ns
Rise Time		t_r	—	8.4	14	
Turn–Off Delay Time		$t_{d(off)}$	—	12	26	
Fall Time		t_f	—	11	20	
Gate Charge (See Figure 8)	(V_{DS} = 320 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	8.6	12	nC
		Q_1	—	2.6	—	
		Q_2	—	3.2	—	
		Q_3	—	5.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.88	1.2	Vdc
	(I_S = 2.0 Adc, V_{GS} = 0 Vdc , T_J = 125°C)		—	0.76	—	
Reverse Recovery Time (See Figure 14)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	156	—	ns
		t_a	—	99	—	
		t_b	—	57	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.89	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

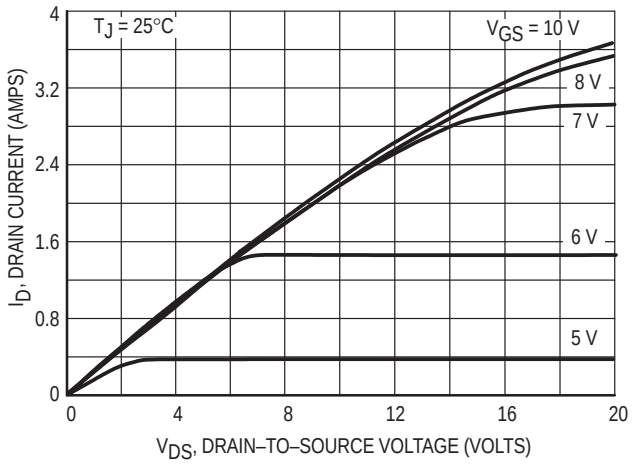


Figure 1. On–Region Characteristics

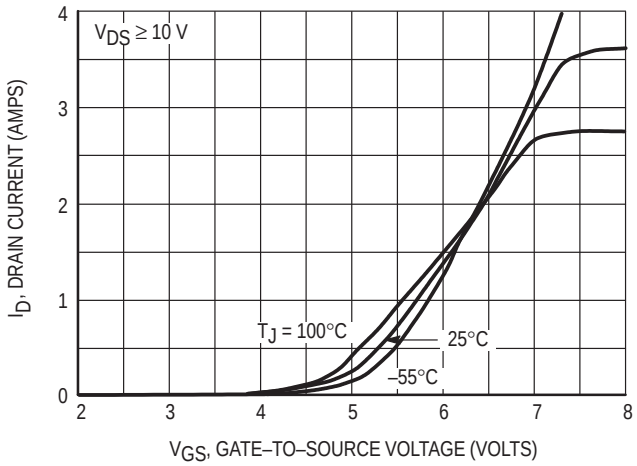


Figure 2. Transfer Characteristics

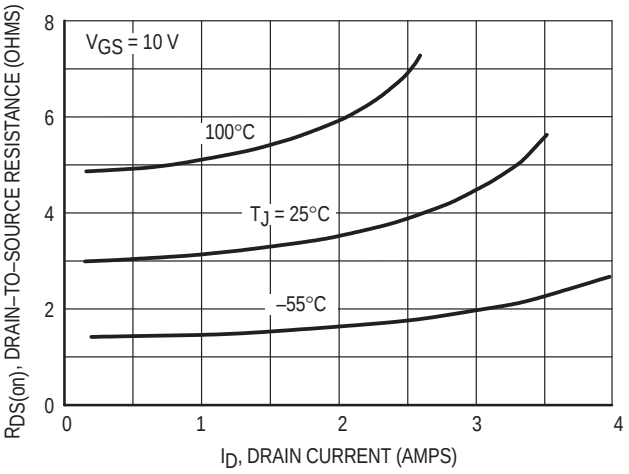


Figure 3. On–Resistance versus Drain Current and Temperature

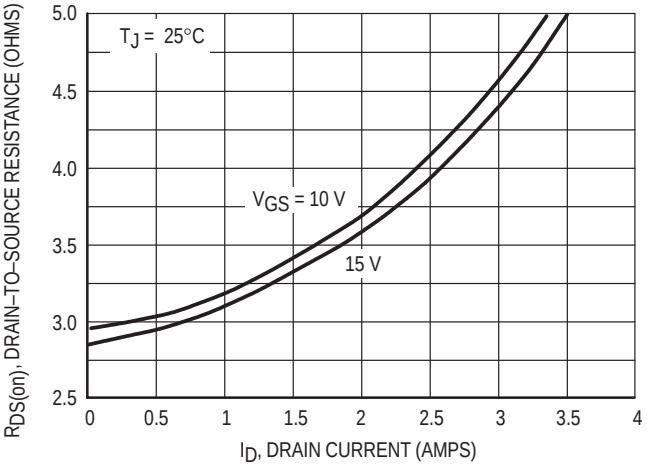


Figure 4. On–Resistance versus Drain Current and Gate Voltage

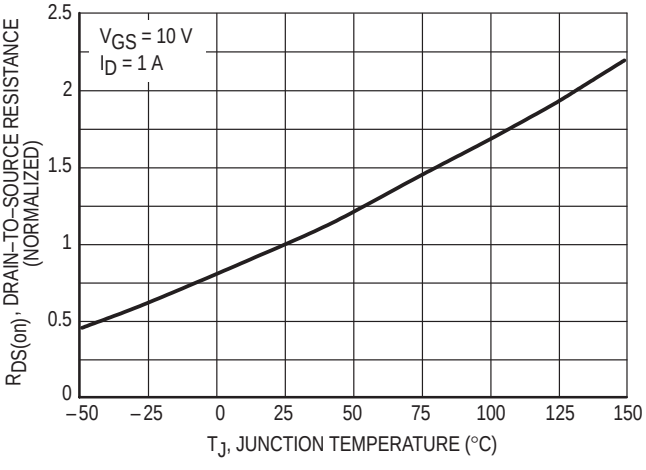


Figure 5. On–Resistance Variation with Temperature

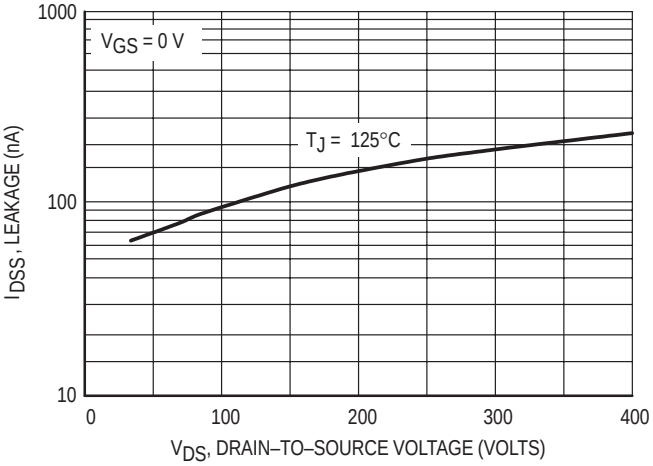


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

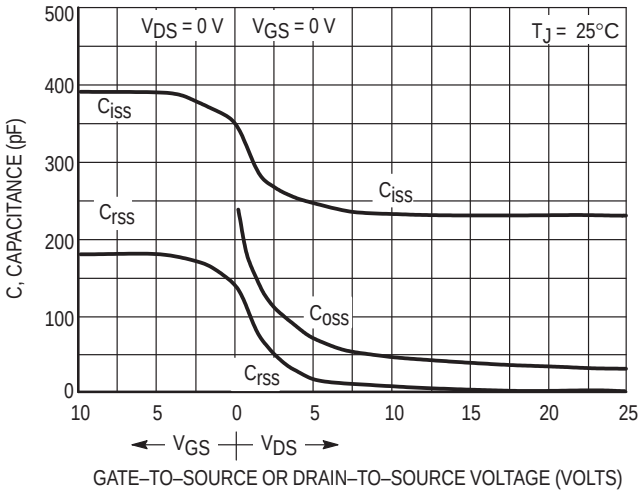


Figure 7a. Capacitance Variation

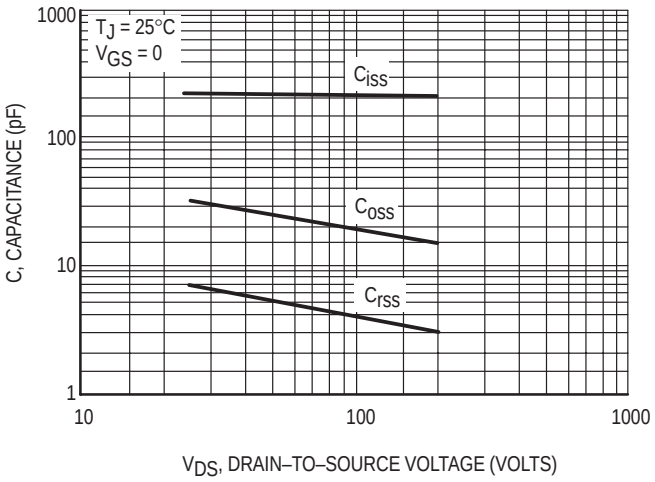


Figure 7b. High Voltage Capacitance Variation

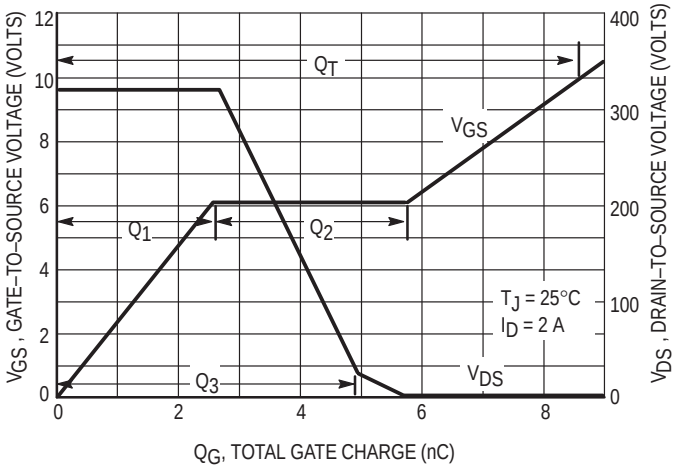


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

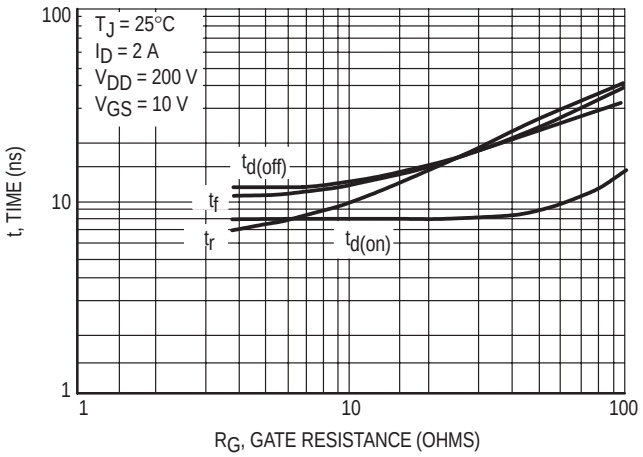


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

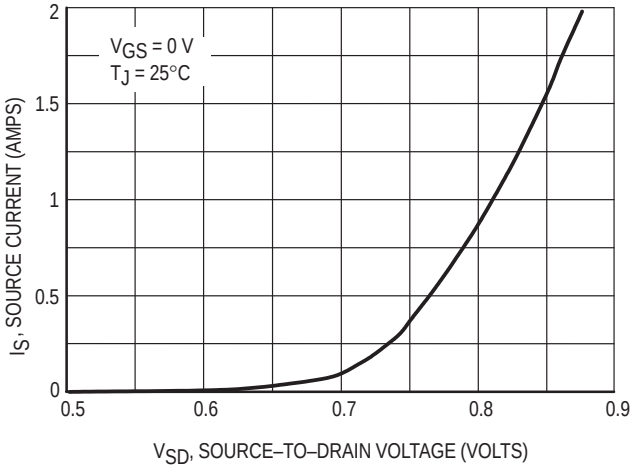


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

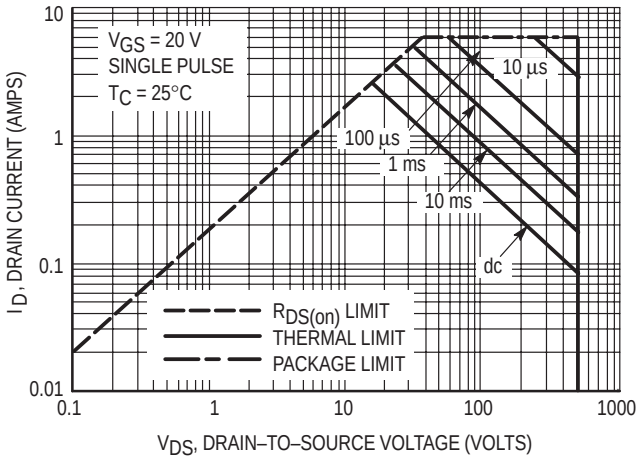


Figure 11. Maximum Rated Forward Biased Safe Operating Area

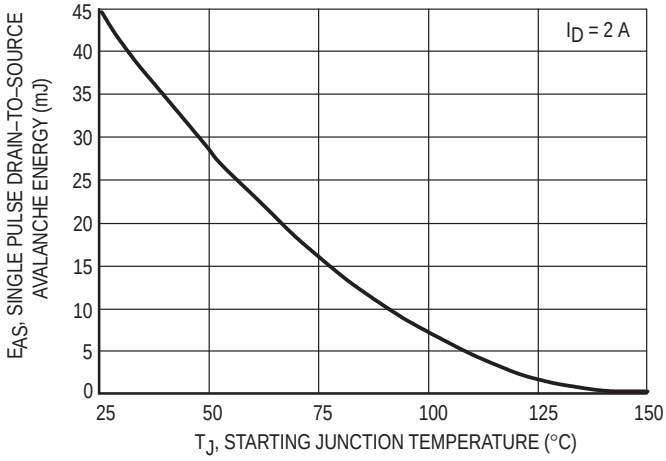


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

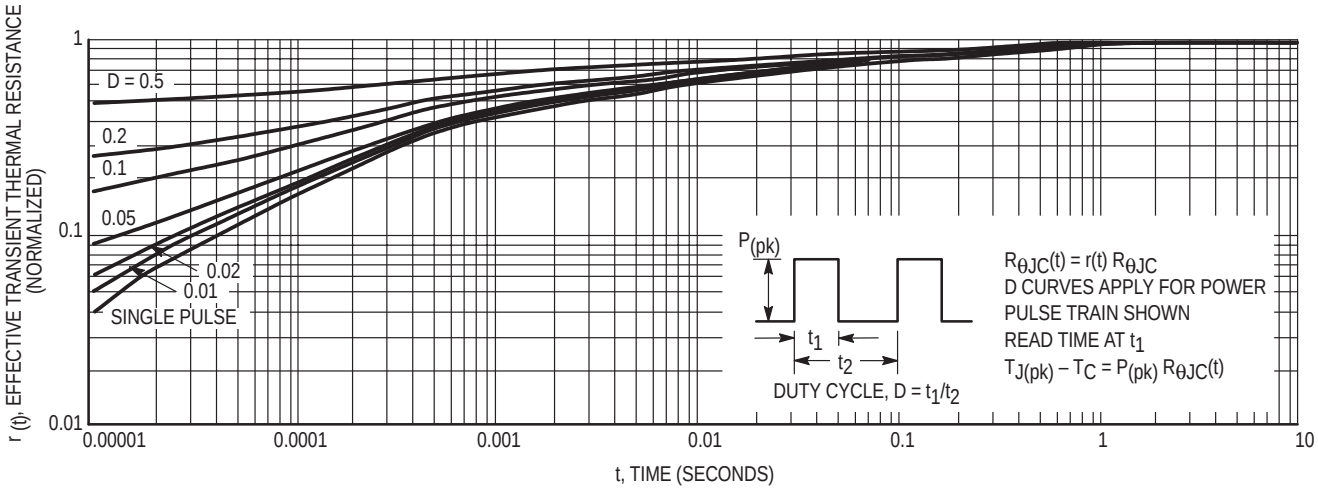


Figure 13. Thermal Response

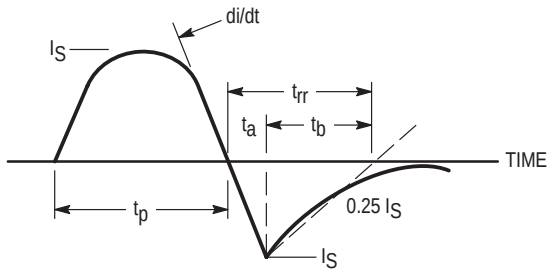


Figure 14. Diode Reverse Recovery Waveform

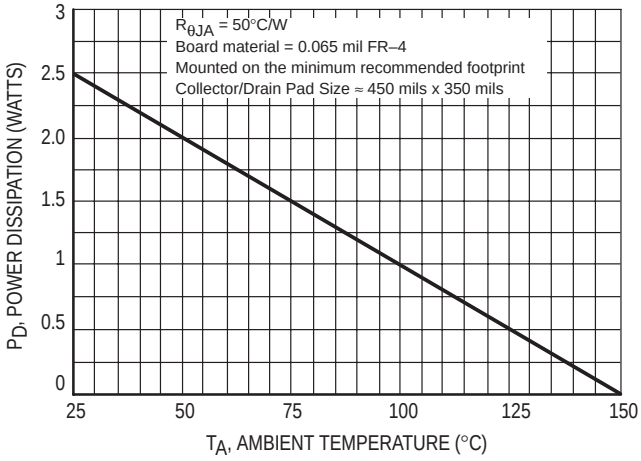


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

TMOS E-FET™
High Energy Power FET
D²PAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

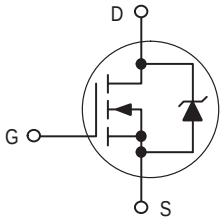
MTB2N60E

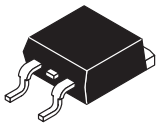
Motorola Preferred Device

TMOS POWER FET
2.0 AMPERES
600 VOLTS
$R_{DS(on)}$ = 3.8 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	600	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	2.0 1.3 7.0	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	50 0.4 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, Peak I_L = 2.0 Apk, L = 95 mH, R_G = 25 Ω)	E_{AS}	190	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.5 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

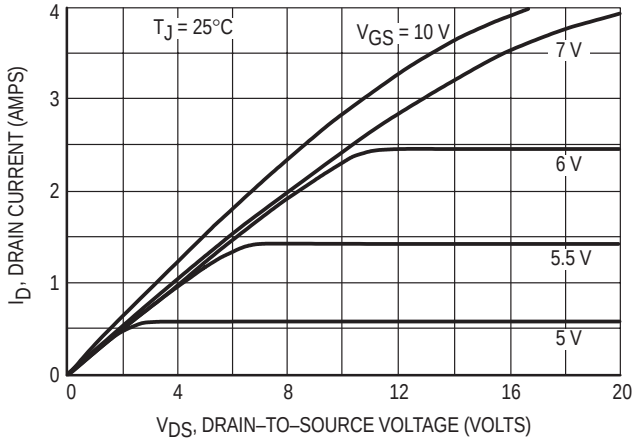
Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	480	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	0.25	μAdc
(V_{DS} = 480 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	1.0	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.1	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	8.5	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	—	3.0	3.8	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 2.0 Adc)		$V_{DS(on)}$	—	—	8.2	Vdc
(V_{GS} = 10 Vdc, I_D = 1.0 Adc, T_J = 125°C)			—	—	8.4	
Forward Transconductance (V_{DS} = 50 Vdc, I_D = 1.0 Adc)		g_{FS}	1.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	435	—	pF
Output Capacitance		C_{oss}	—	100	—	
Transfer Capacitance		C_{rss}	—	20	—	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 300 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 18 Ω)	$t_{d(on)}$	—	12	—	ns
Rise Time		t_r	—	21	—	
Turn–Off Delay Time		$t_{d(off)}$	—	30	—	
Fall Time		t_f	—	24	—	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	13	—	nC
		Q_1	—	2.0	—	
		Q_2	—	6.0	—	
		Q_3	—	5.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.6	Vdc
	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.9	—	
Reverse Recovery Time	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	340	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	3.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS



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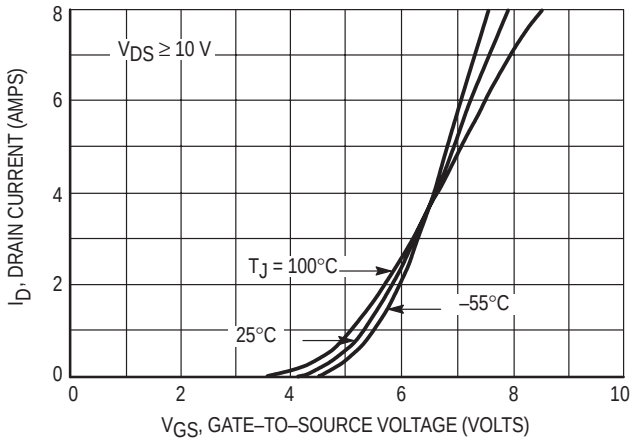

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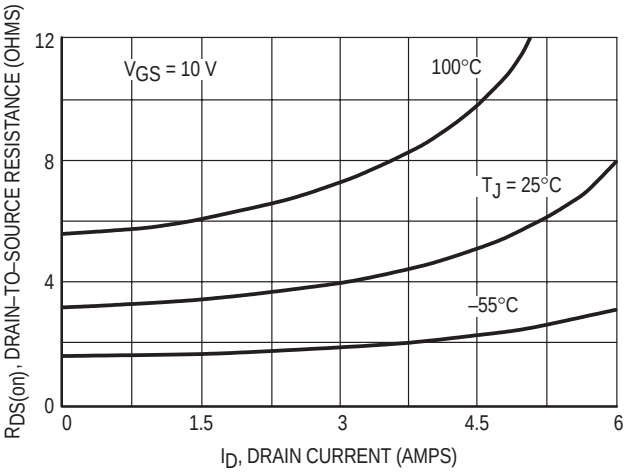


Figure 3. On–Resistance versus Drain Current and Temperature

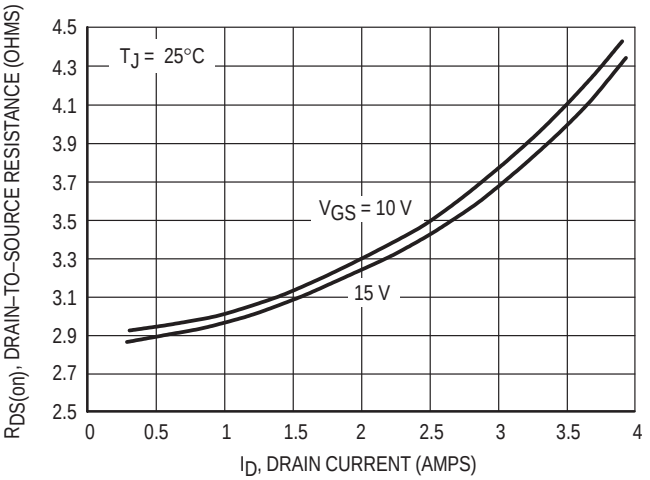


Figure 4. On–Resistance versus Drain Current and Gate Voltage

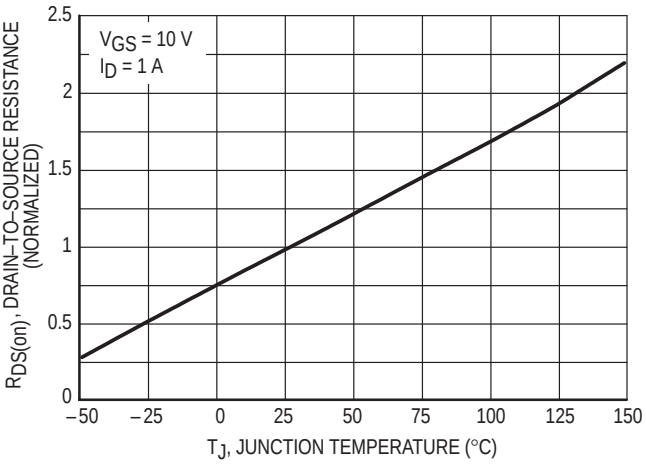
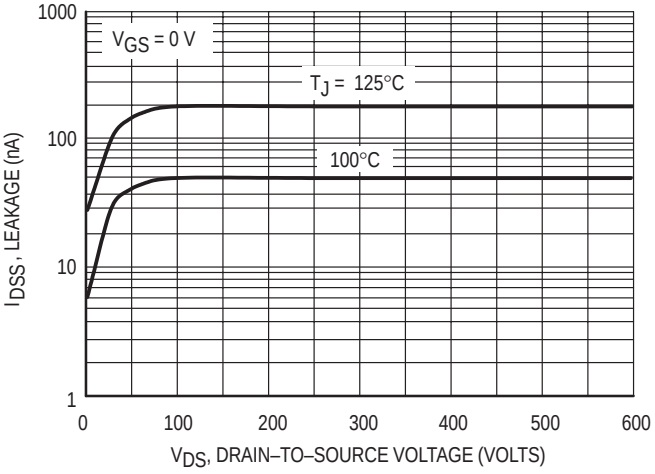


Figure 5. On–Resistance Variation with Temperature



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POWER MOSFET SWITCHING

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The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

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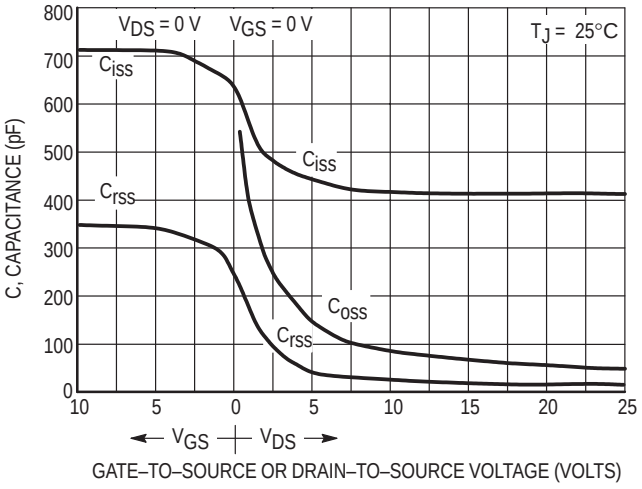

Figure 7a. Capacitance Variation

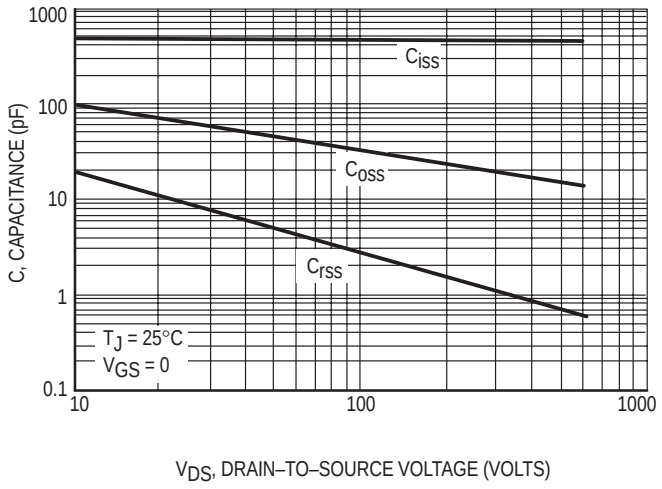

Figure 7b. High Voltage Capacitance Variation

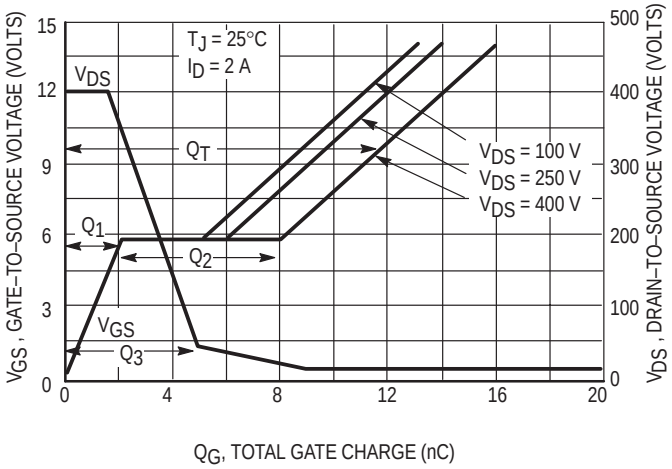

Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

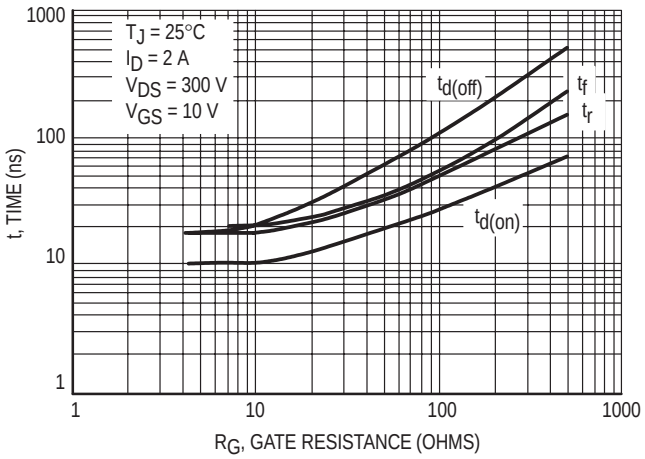

Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

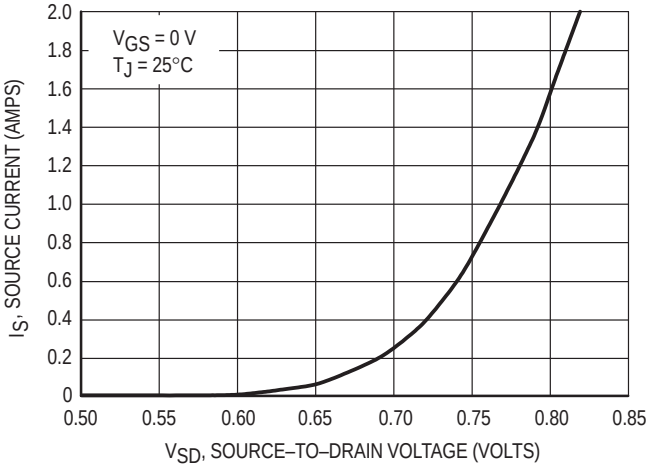

Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

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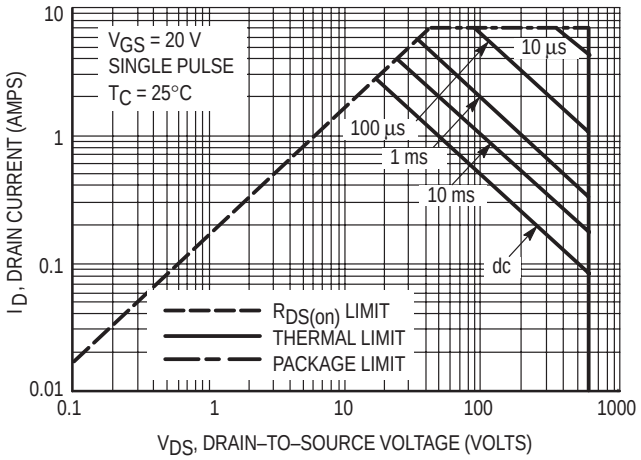


Figure 11. Maximum Rated Forward Biased Safe Operating Area

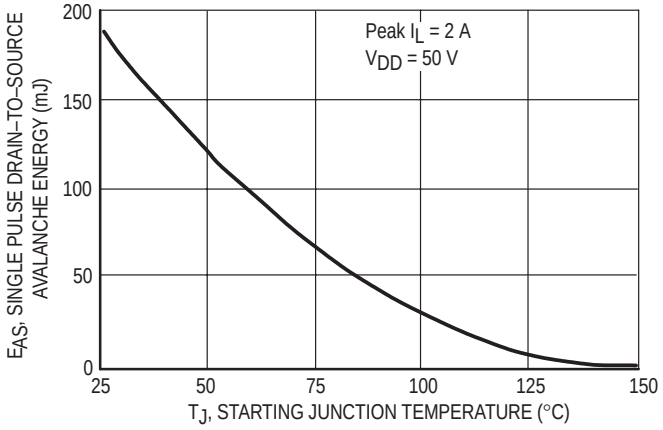


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

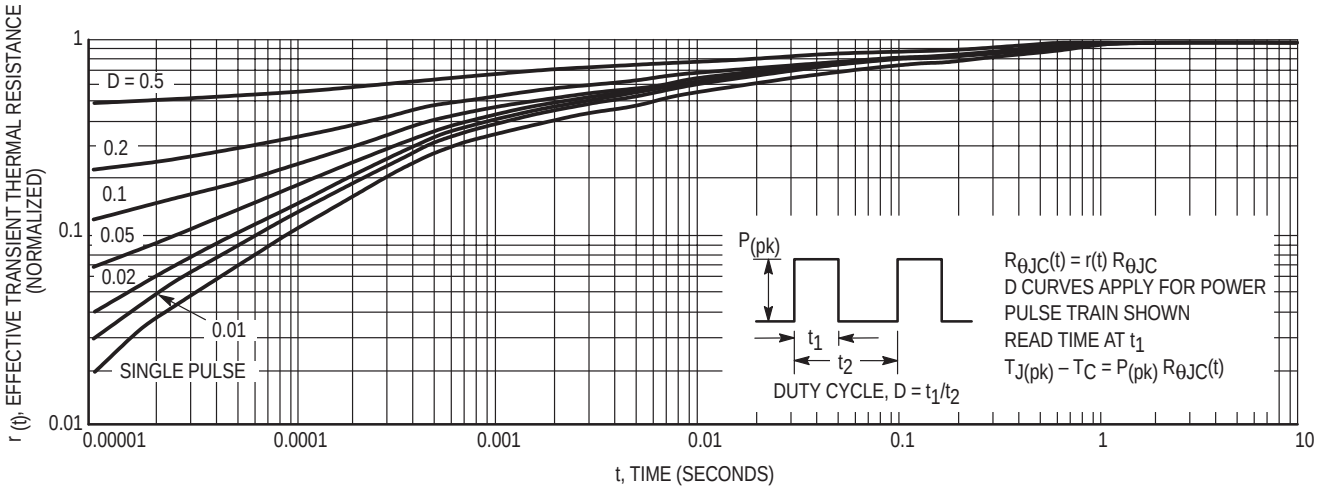


Figure 13. Thermal Response

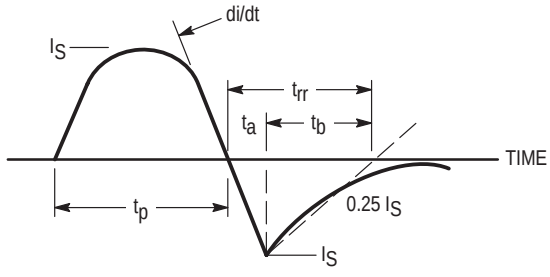


Figure 14. Diode Reverse Recovery Waveform

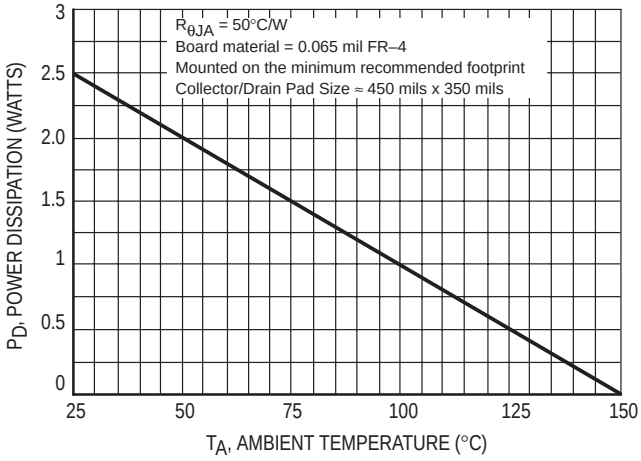


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

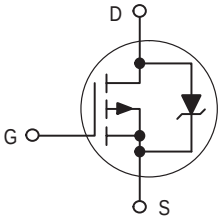
TMOS E-FET ™
High Energy Power FET
D²PAK for Surface Mount

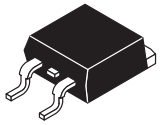
P–Channel Enhancement–Mode Silicon Gate

MTB2P50E

Motorola Preferred Device

TMOS POWER FET
2.0 AMPERES
500 VOLTS
$R_{DS(on)}$ = 6.0 OHM





CASE 418B–02, Style 2
D²PAK

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	2.0 1.6 6.0	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted with the minimum recommended pad size	P_D	75 0.6 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 4.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	80	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.67 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	500 —	— 564	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 4.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	—	4.5	6.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 2.0 Adc) (I_D = 1.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	9.5 —	14.4 12.6	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.0 Adc)		g_{FS}	1.5	2.9	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	845	1183	pF
Output Capacitance		C_{oss}	—	100	140	
Reverse Transfer Capacitance		C_{rss}	—	26	52	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 2.0 Adc, V_{GS} = 10 dc, R_G = 9.1 Ω)	$t_{d(on)}$	—	12	24	ns
Rise Time		t_r	—	14	28	
Turn–Off Delay Time		$t_{d(off)}$	—	21	42	
Fall Time		t_f	—	19	38	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	19	27	nC
		Q_1	—	3.7	—	
		Q_2	—	7.9	—	
		Q_3	—	9.9	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	2.3 1.85	3.5 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	223	—	ns
		t_a	—	161	—	
		t_b	—	62	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.92	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

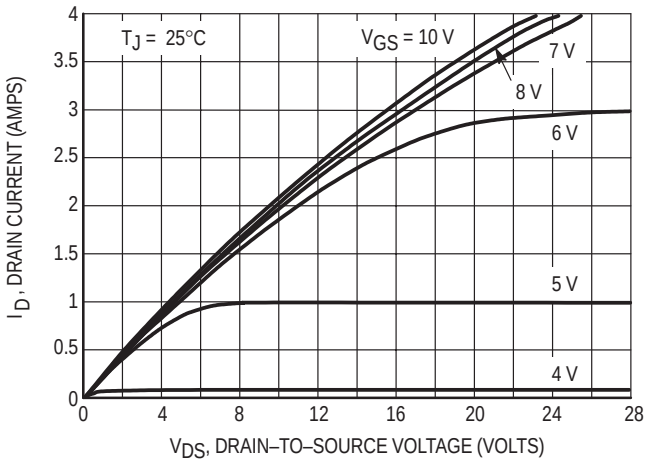


Figure 1. On–Region Characteristics

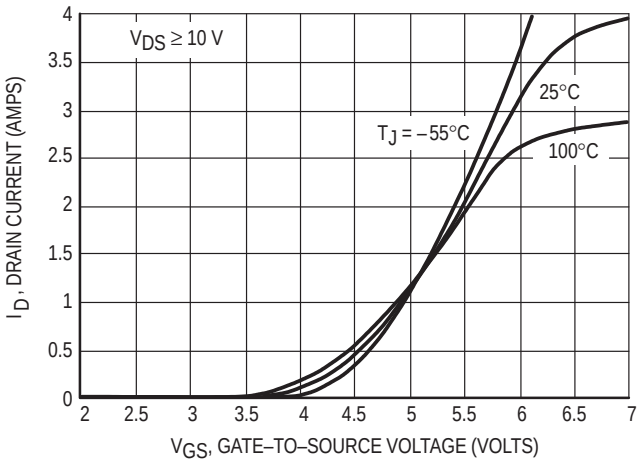


Figure 2. Transfer Characteristics

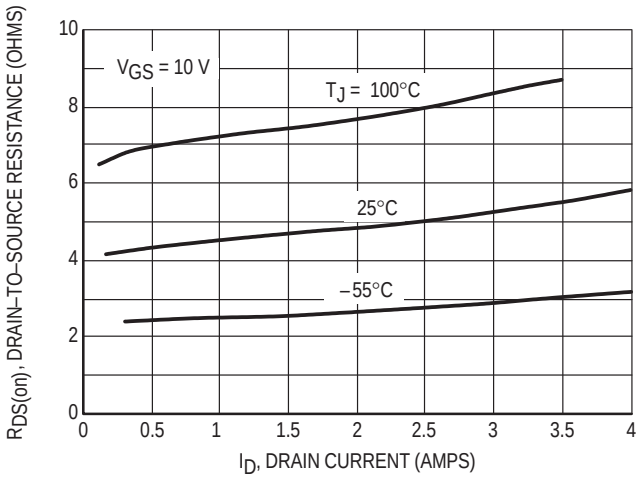


Figure 3. On–Resistance versus Drain Current and Temperature

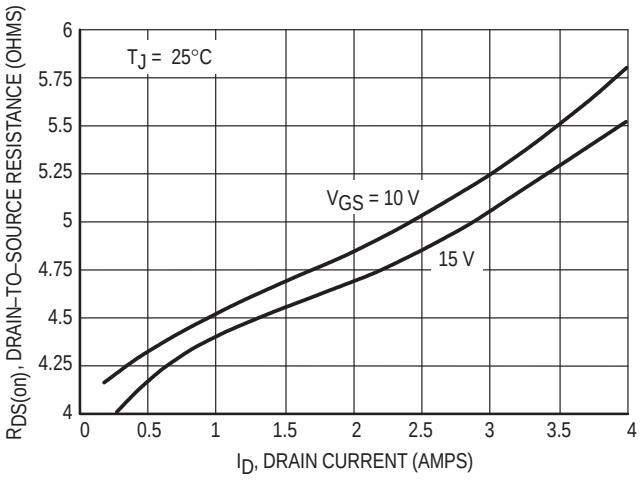


Figure 4. On–Resistance versus Drain Current and Gate Voltage

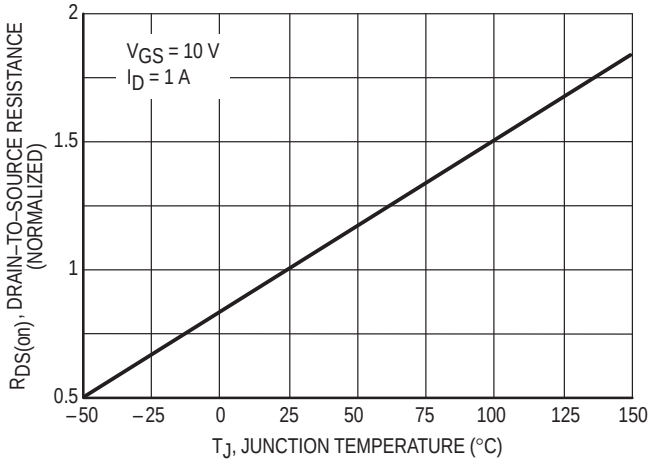


Figure 5. On–Resistance Variation with Temperature

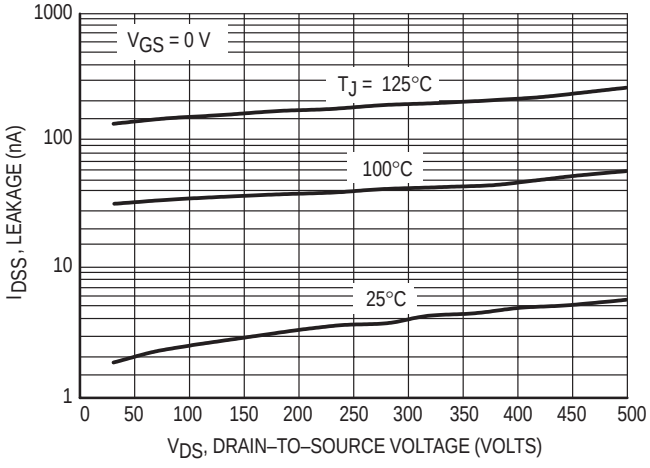


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

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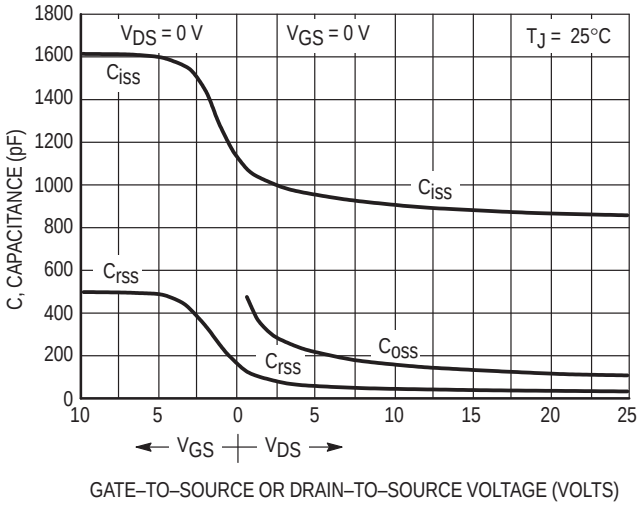

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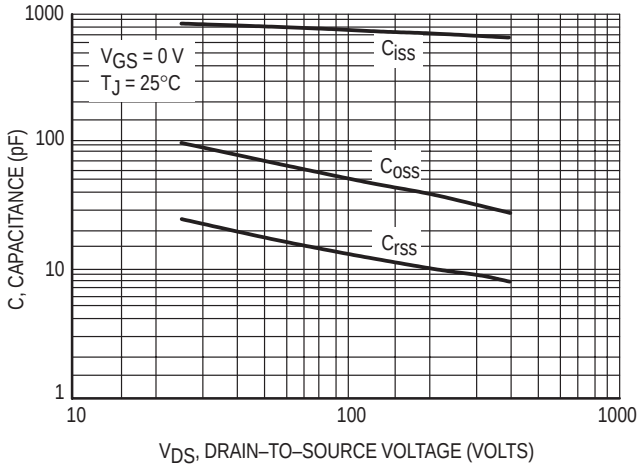
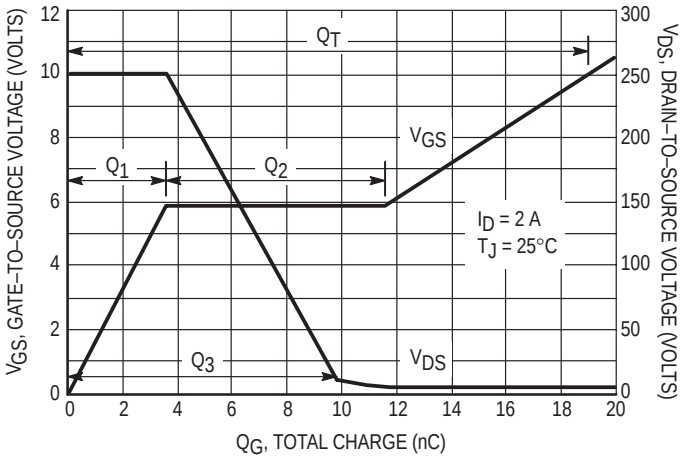


Figure 7b. High Voltage Capacitance Variation



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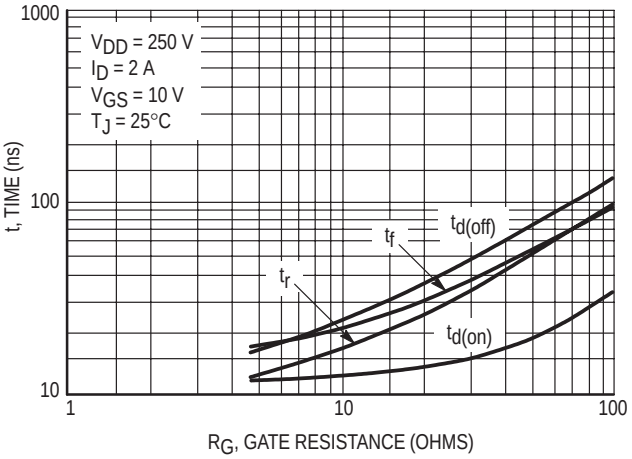

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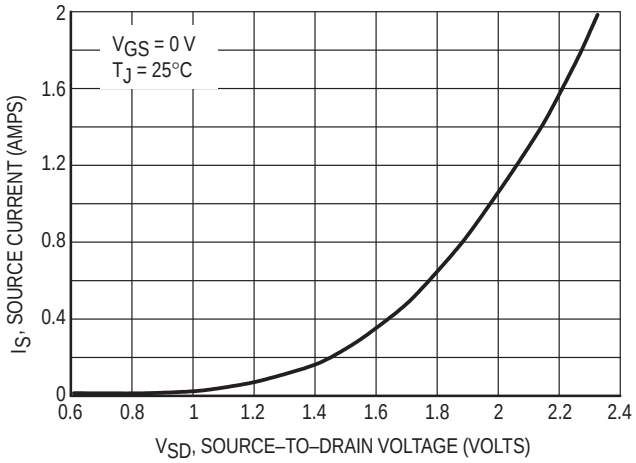
DRAIN–TO–SOURCE DIODE CHARACTERISTICS



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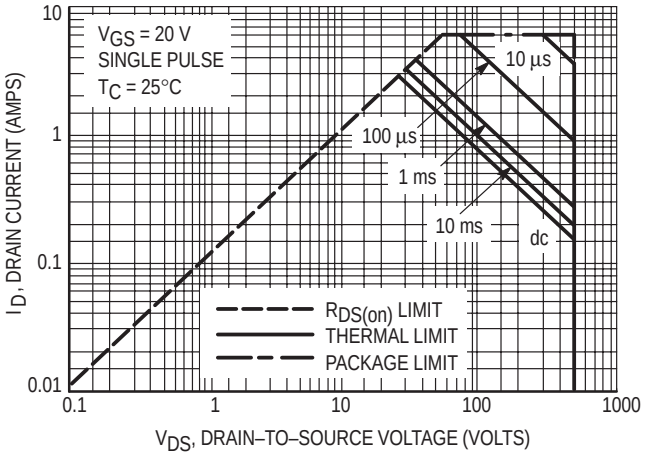


Figure 11. Maximum Rated Forward Biased Safe Operating Area

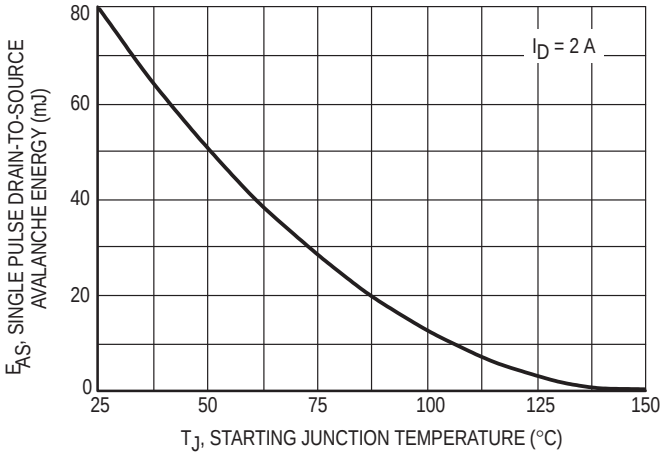


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

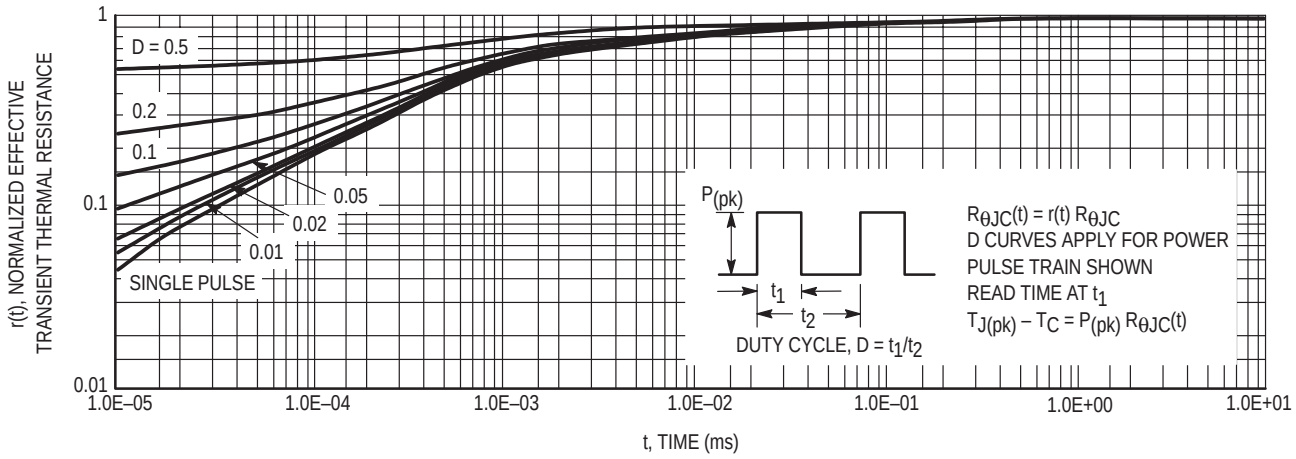


Figure 13. Thermal Response

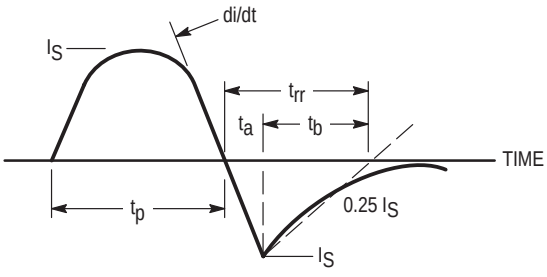


Figure 14. Diode Reverse Recovery Waveform

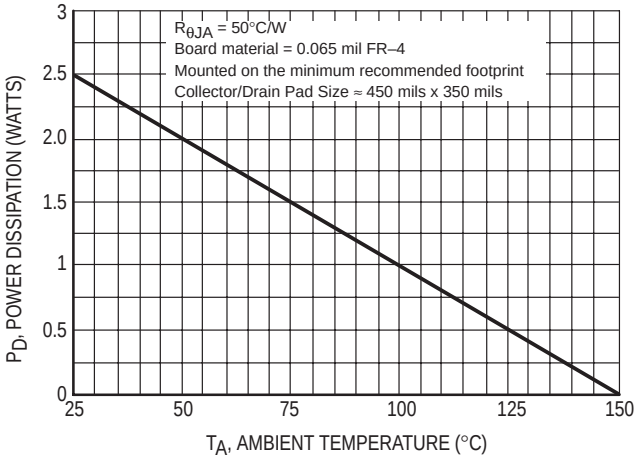


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

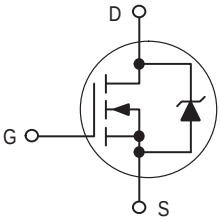
TMOS E-FET ™
High Energy Power FET
D²PAK for Surface Mount

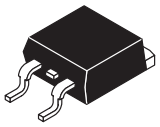
N–Channel Enhancement–Mode Silicon Gate

MTB3N100E

Motorola Preferred Device

TMOS POWER FET
3.0 AMPERES
1000 VOLTS
$R_{DS(on)}$ = 4.0 OHM





CASE 418B–02, Style 2
D²PAK

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	1000	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	1000	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	3.0 2.4 9.0	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted with the minimum recommended pad size	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 7.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	245	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	1000 —	— 1.23	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 6.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$R_{DS(on)}$	—	2.96	4.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 3.0 Adc) (I_D = 1.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	4.97 —	14.4 12.6	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.5 Adc)		g_{FS}	2.0	3.56	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1316	1800	pF
Output Capacitance		C_{oss}	—	117	260	
Reverse Transfer Capacitance		C_{rss}	—	26	75	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 400 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	13	25	ns
Rise Time		t_r	—	19	40	
Turn–Off Delay Time		$t_{d(off)}$	—	42	90	
Fall Time		t_f	—	33	55	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	32.5	45	nC
		Q_1	—	6.0	—	
		Q_2	—	14.6	—	
		Q_3	—	13.5	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.794 0.63	1.1 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	615	—	ns
		t_a	—	104	—	
		t_b	—	511	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.92	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

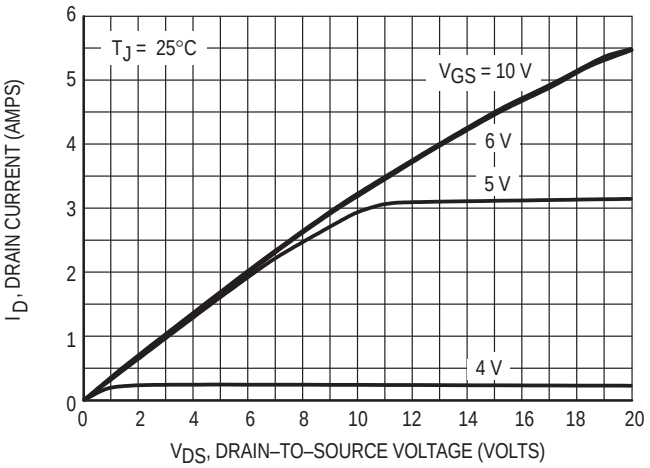


Figure 1. On–Region Characteristics

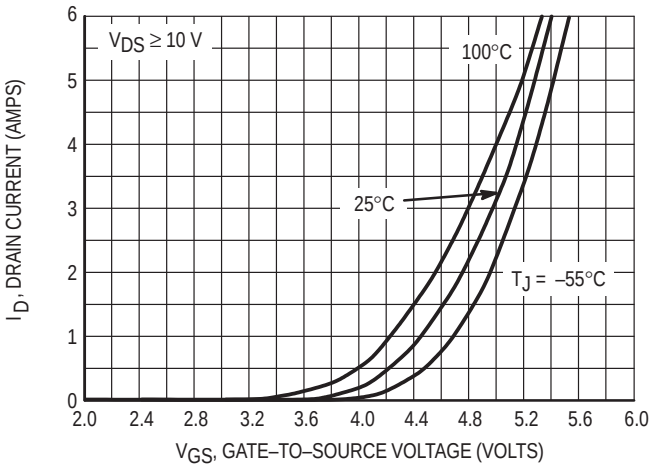


Figure 2. Transfer Characteristics

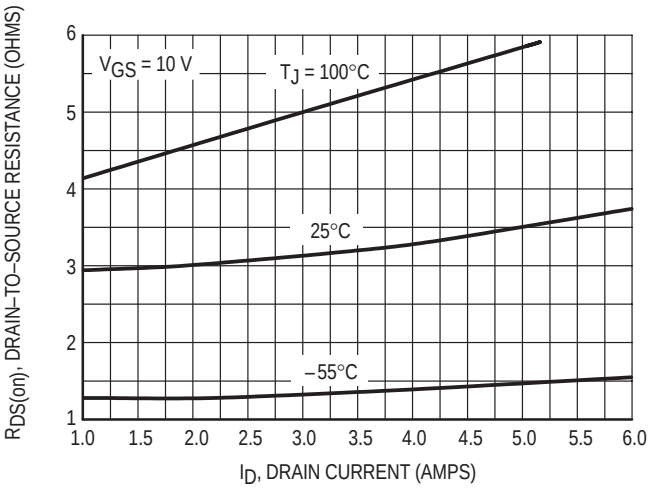


Figure 3. On–Resistance versus Drain Current and Temperature

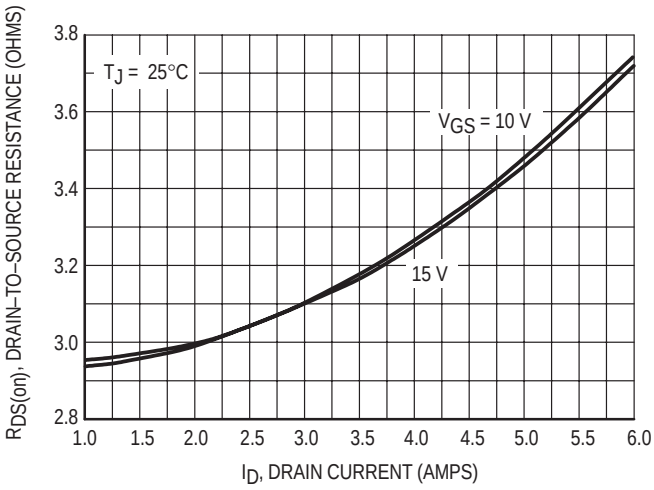


Figure 4. On–Resistance versus Drain Current and Gate Voltage

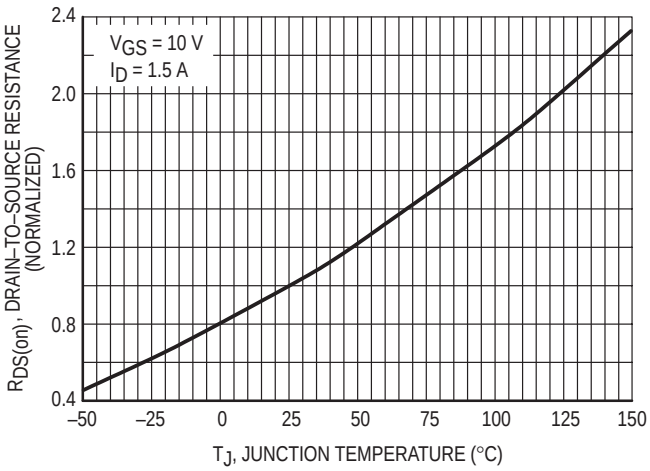


Figure 5. On–Resistance Variation with Temperature

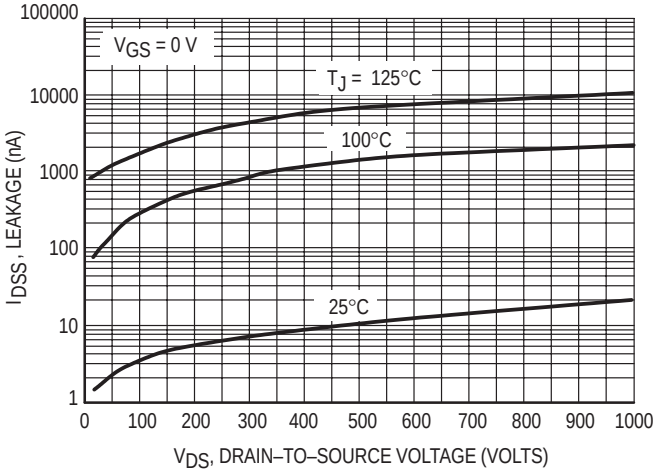


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

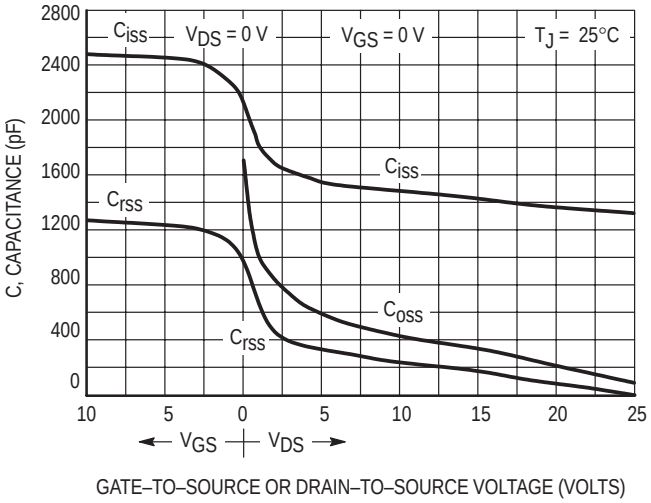


Figure 7a. Capacitance Variation

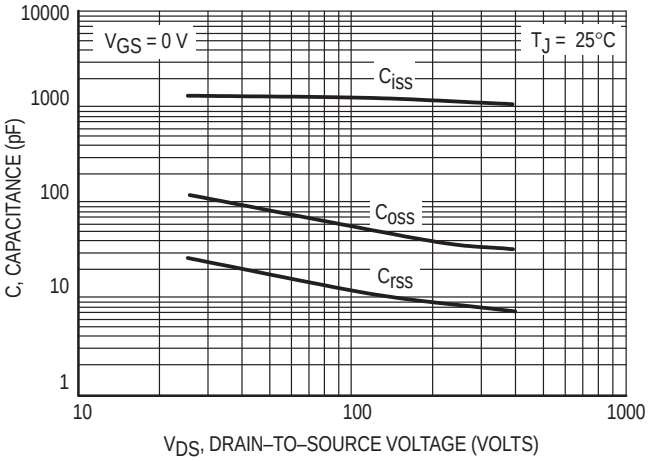


Figure 7b. High Voltage Capacitance Variation

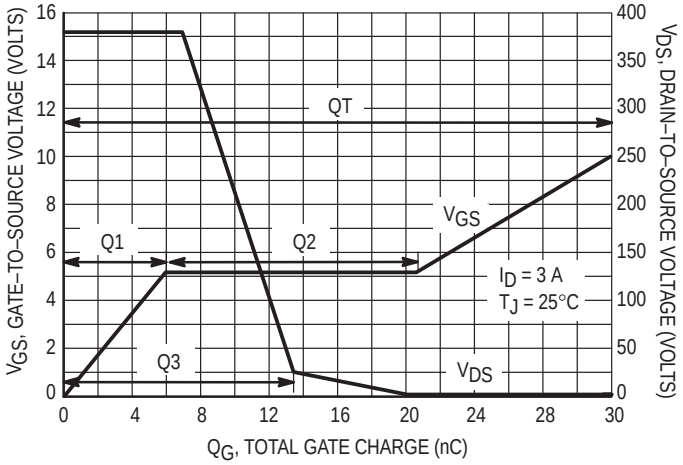


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

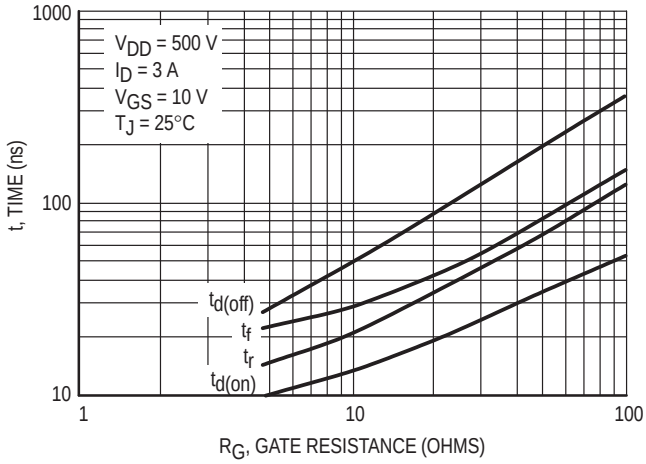


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

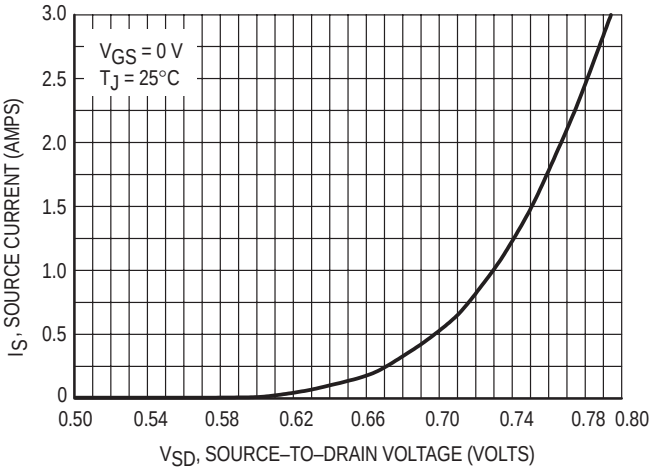


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

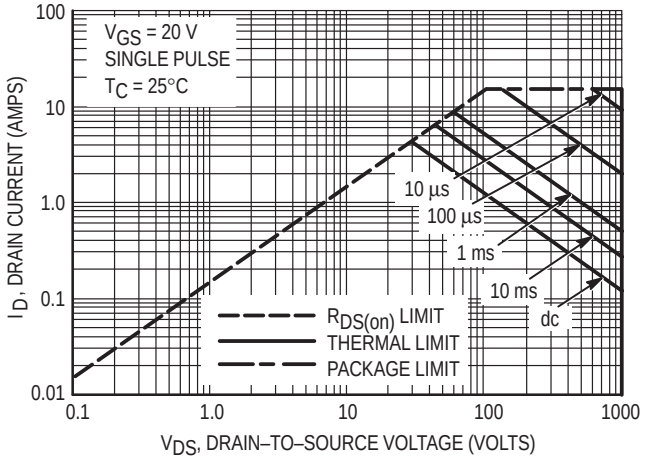


Figure 11. Maximum Rated Forward Biased Safe Operating Area

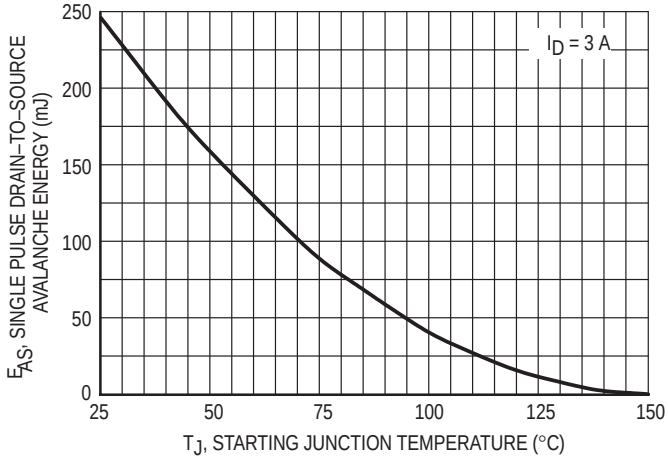


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

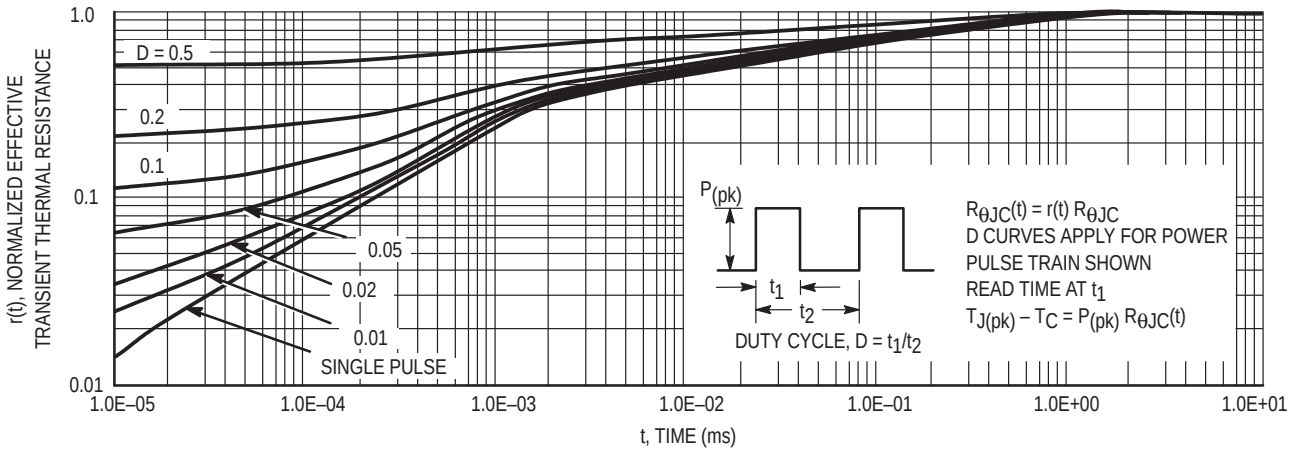


Figure 13. Thermal Response

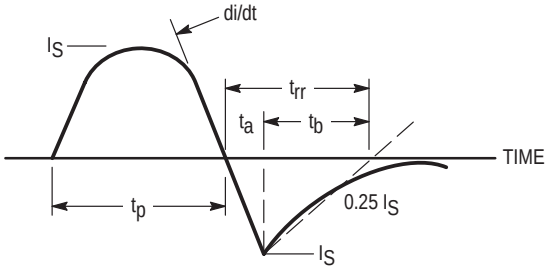


Figure 14. Diode Reverse Recovery Waveform

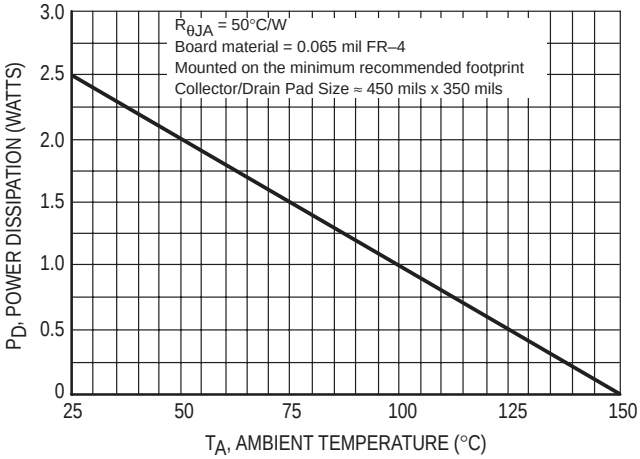


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

TMOS E-FET™
High Energy Power FET
D²PAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

MTB3N120E

Motorola Preferred Device

TMOS POWER FET
3.0 AMPERES
1200 VOLTS
$R_{DS(on)}$ = 5.0 OHM

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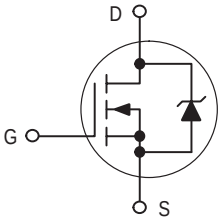
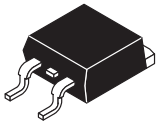




CASE 418B–02, Style 2
D²PAK

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery time Comparable to Discrete Fast Recovery Diode

* See App. Note AN1327 – Very Wide Input Voltage Range; Off–line Flyback Switching Power Supply

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	1200	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	1200	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	3.0 2.2 11	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, PEAK I_L = 4.5 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	101	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	1200 —	— 1.28	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 1200 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 1200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 7.1	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$R_{DS(on)}$	—	4.0	5.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 3.0 Adc) (I_D = 1.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	18.0 15.8	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.5 Adc)		g_{FS}	2.5	3.1	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	2130	2980	pF
Output Capacitance		C_{oss}	—	1710	2390	
Reverse Transfer Capacitance		C_{rss}	—	932	1860	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 600 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	13.6	30	ns
Rise Time		t_r	—	12.6	30	
Turn–Off Delay Time		$t_{d(off)}$	—	35.8	70	
Fall Time		t_f	—	20.7	40	
Gate Charge	(V_{DS} = 600 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	31	40	nC
		Q_1	—	8.0	—	
		Q_2	—	11	—	
		Q_3	—	14	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.80 0.65	1.0 —	Vdc
Reverse Recovery Time	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	394	—	ns
		t_a	—	118	—	
		t_b	—	276	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.11	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

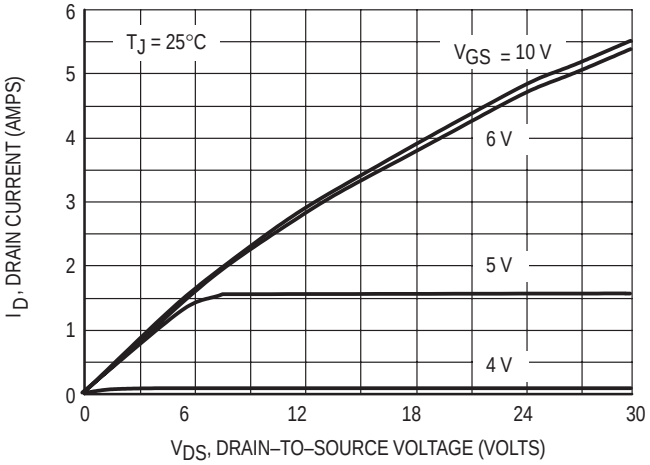


Figure 1. On–Region Characteristics

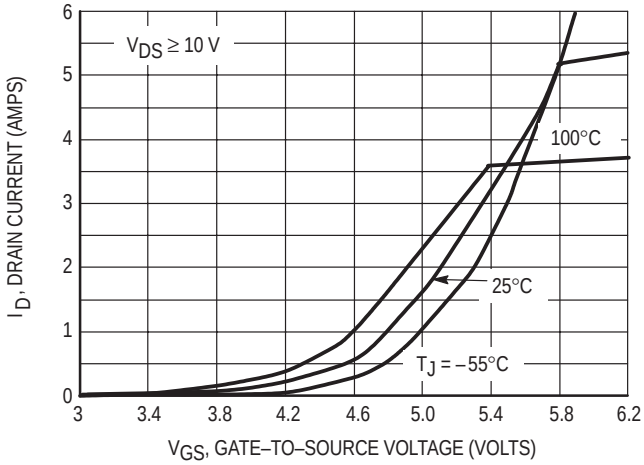


Figure 2. Transfer Characteristics

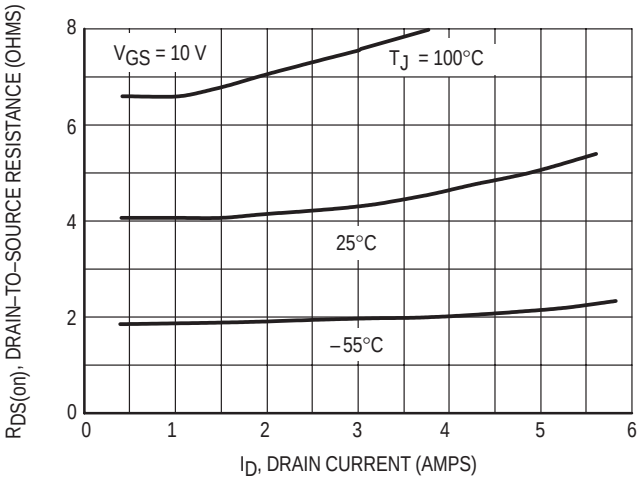


Figure 3. On–Resistance versus Drain Current and Temperature

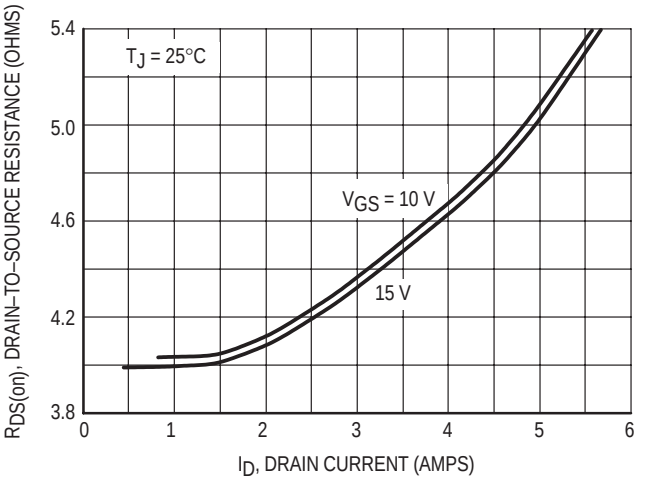


Figure 4. On–Resistance versus Drain Current and Gate Voltage

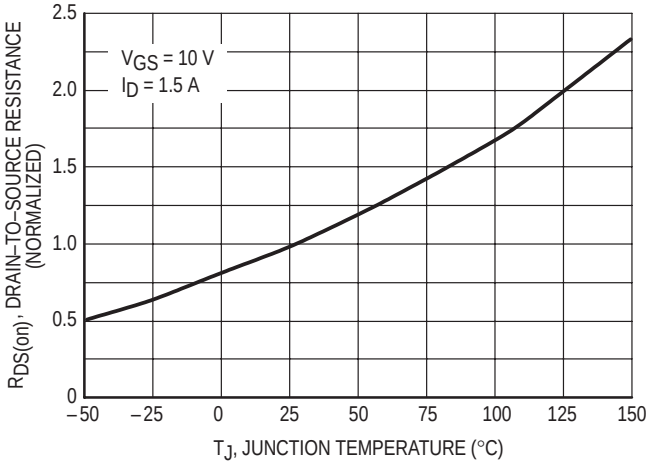


Figure 5. On–Resistance Variation with Temperature

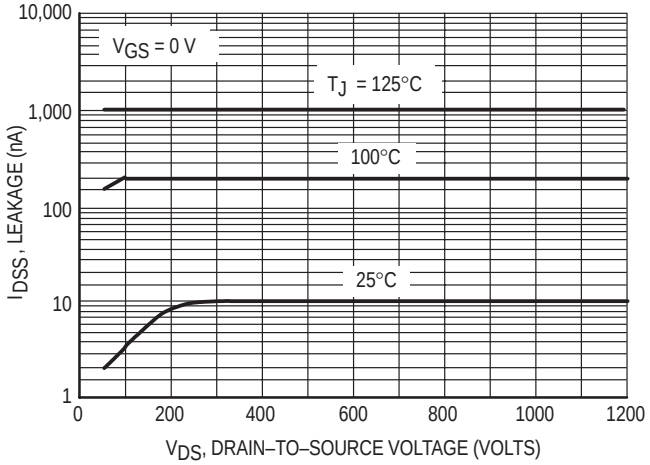


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

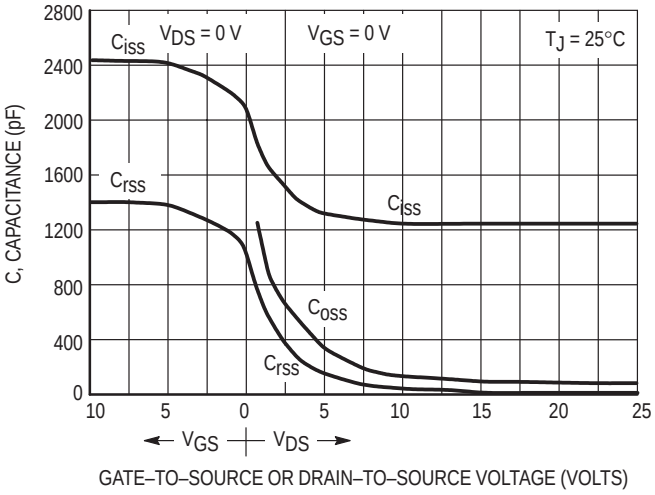


Figure 7a. Capacitance Variation

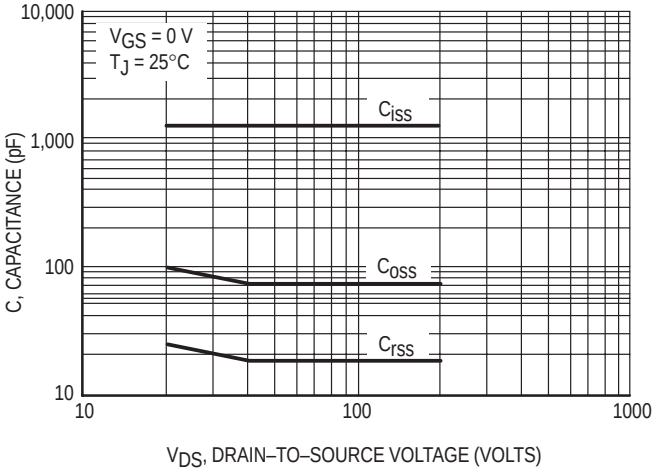


Figure 7b. High Voltage Capacitance Variation

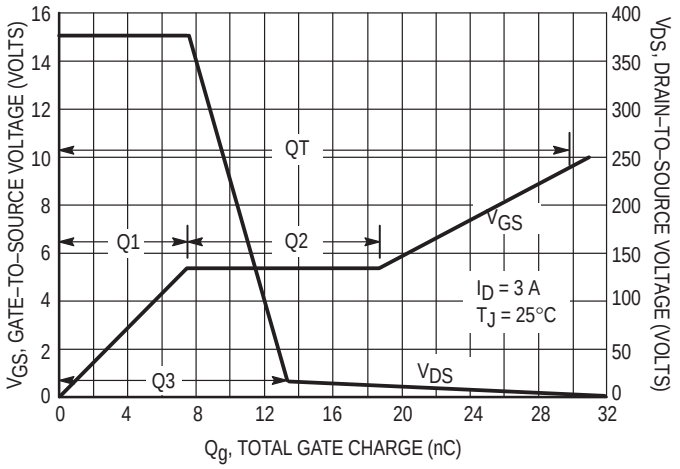


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

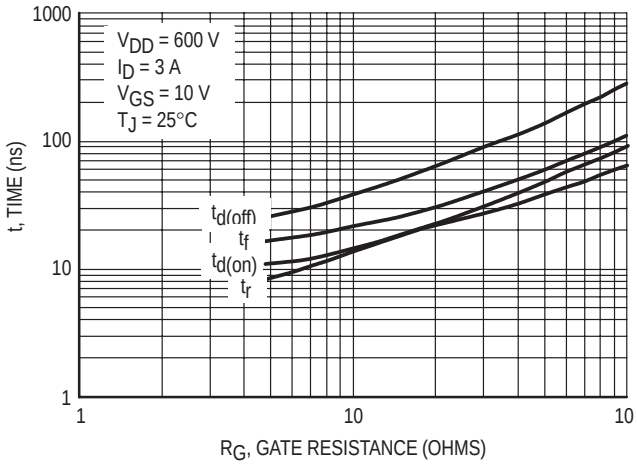


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

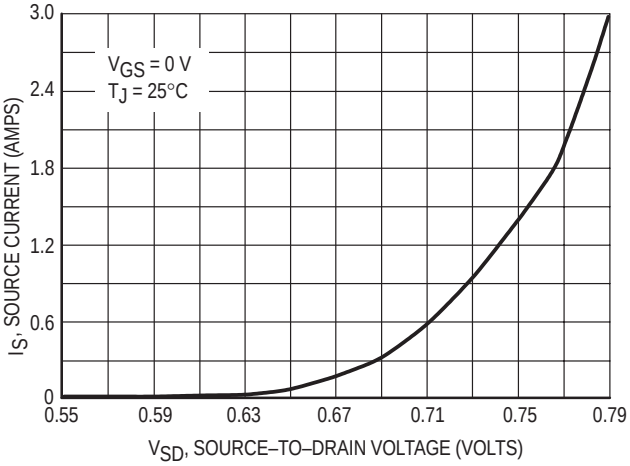


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

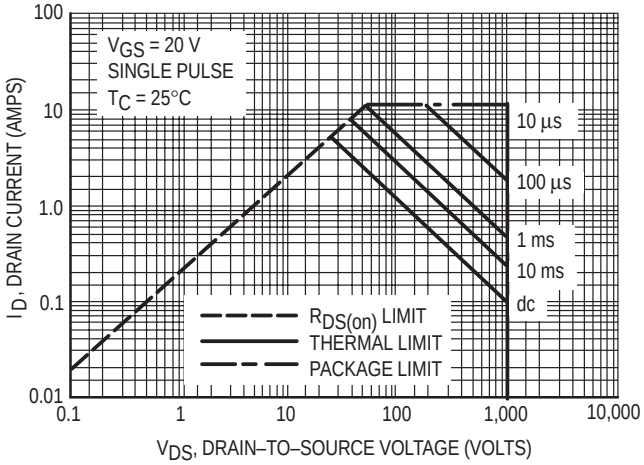


Figure 11. Maximum Rated Forward Biased Safe Operating Area

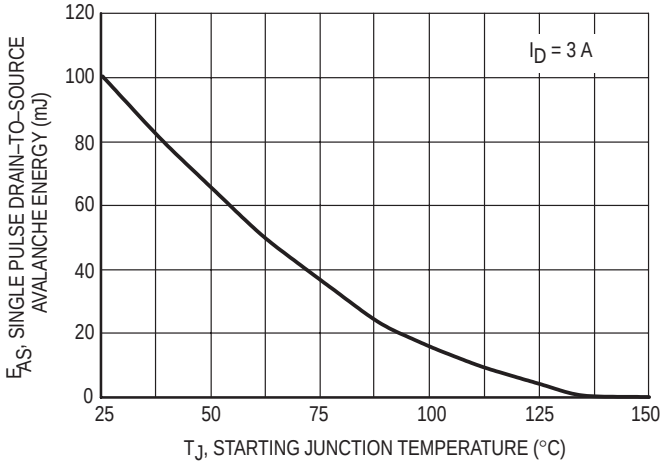


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

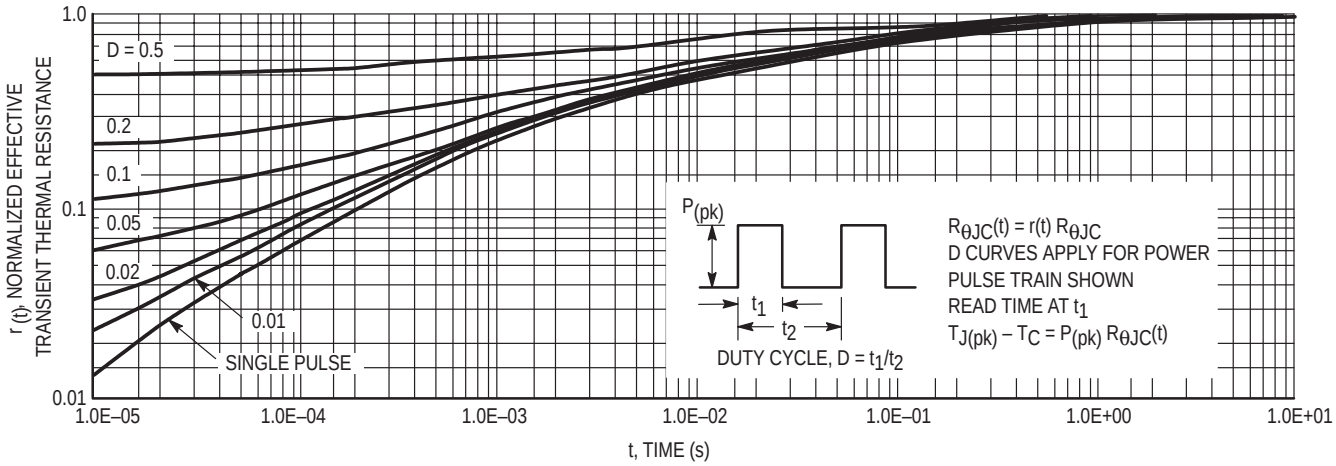


Figure 13. Thermal Response

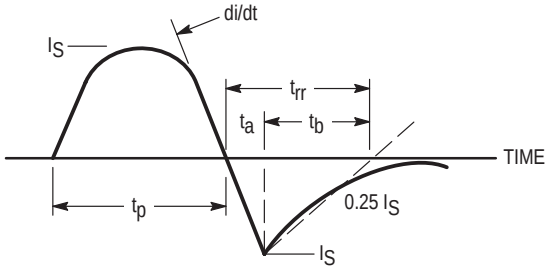


Figure 14. Diode Reverse Recovery Waveform

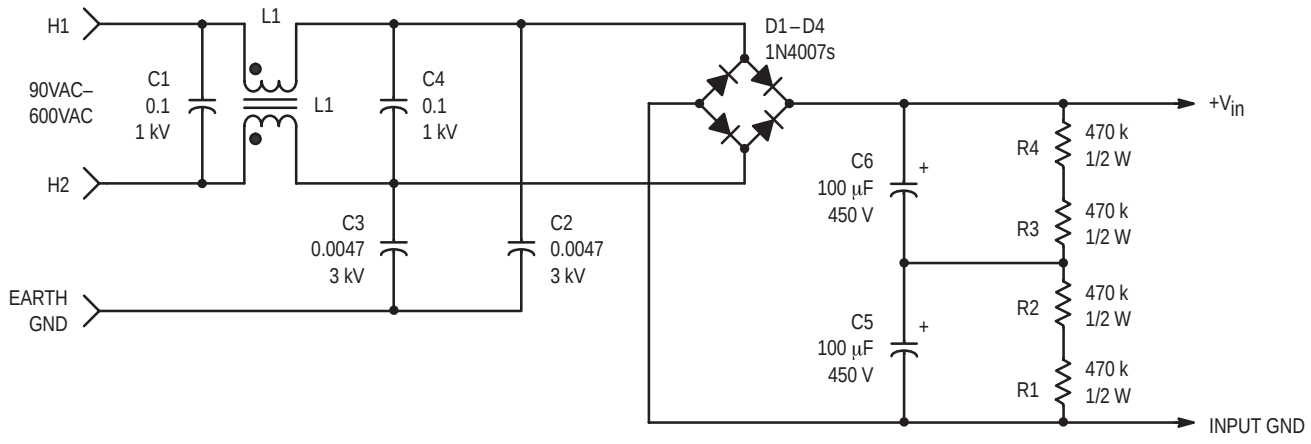


Figure 15. The AC Input/Filter Circuit Section

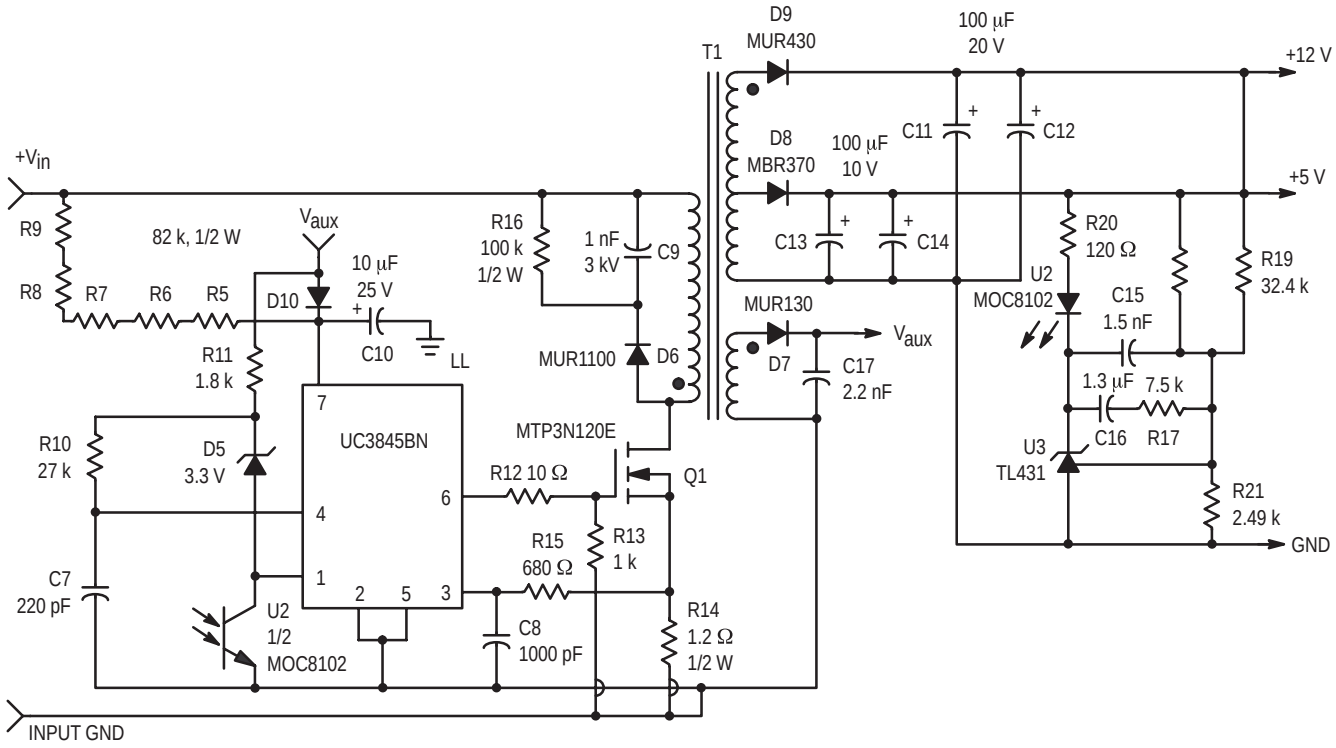


Figure 16. The DC/DC Converter Circuit Section

Designer's™ Data Sheet

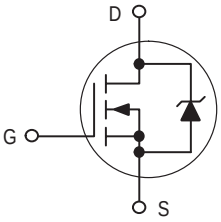
TMOS E-FET ™
High Energy Power FET
D²PAK for Surface Mount

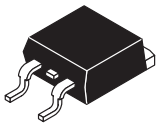
N–Channel Enhancement–Mode Silicon Gate

MTB4N80E

Motorola Preferred Device

TMOS POWER FET
4.0 AMPERES
800 VOLTS
$R_{DS(on)}$ = 3.0 OHM





CASE 418B–02, Style 2
D²PAK

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	800	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	800	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	4.0 2.9 12	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted with the minimum recommended pad size	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 8.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	320	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.
REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	800	—	—	Vdc
Temperature Coefficient (Positive)			—	1.02	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 800 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 800 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc)		$R_{DS(on)}$	—	1.95	3.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 4.0 Adc)		$V_{DS(on)}$	—	8.24	12	Vdc
(I_D = 2.0 Adc, T_J = 125°C)			—	—	10	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.0 Adc)		g_{FS}	2.0	4.3	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1320	2030	pF
Output Capacitance		C_{oss}	—	187	400	
Reverse Transfer Capacitance		C_{rss}	—	72	160	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 400 Vdc, I_D = 4.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	13	30	ns
Rise Time		t_r	—	36	90	
Turn–Off Delay Time		$t_{d(off)}$	—	40	80	
Fall Time		t_f	—	30	75	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 4.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	36	80	nC
		Q_1	—	7.0	—	
		Q_2	—	16.5	—	
		Q_3	—	12	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.812	1.5	Vdc
	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.7	—	
Reverse Recovery Time (See Figure 14)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	557	—	ns
		t_a	—	100	—	
		t_b	—	457	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.33	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

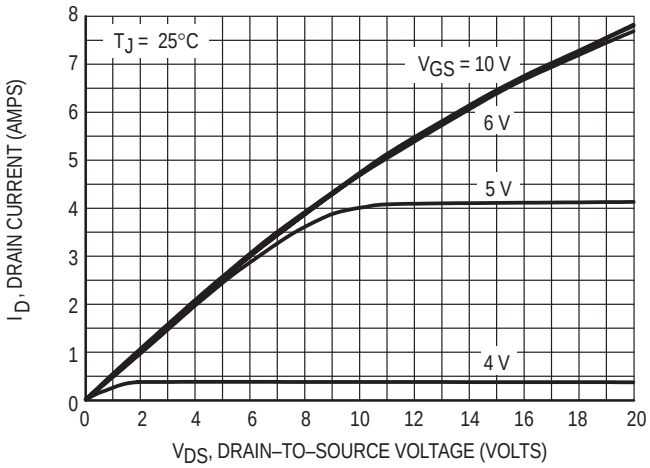


Figure 1. On–Region Characteristics

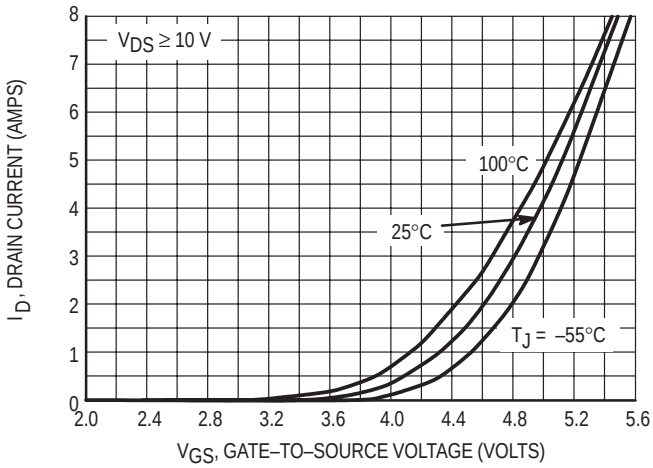


Figure 2. Transfer Characteristics

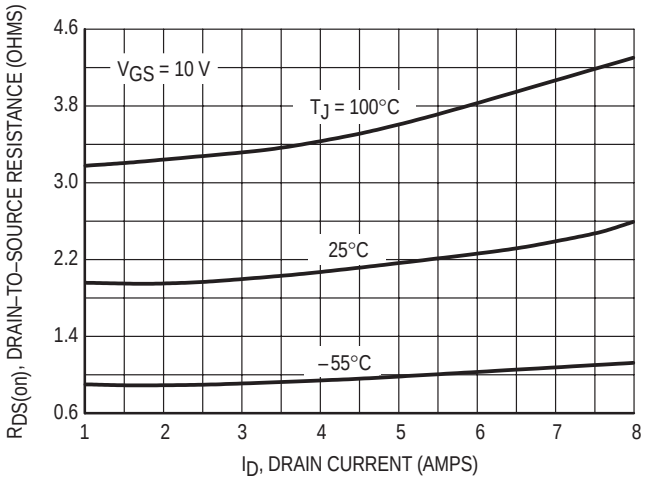


Figure 3. On–Resistance versus Drain Current and Temperature

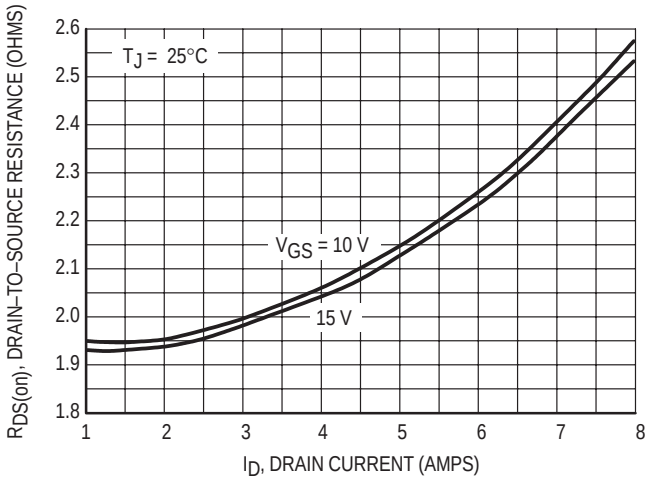


Figure 4. On–Resistance versus Drain Current and Gate Voltage

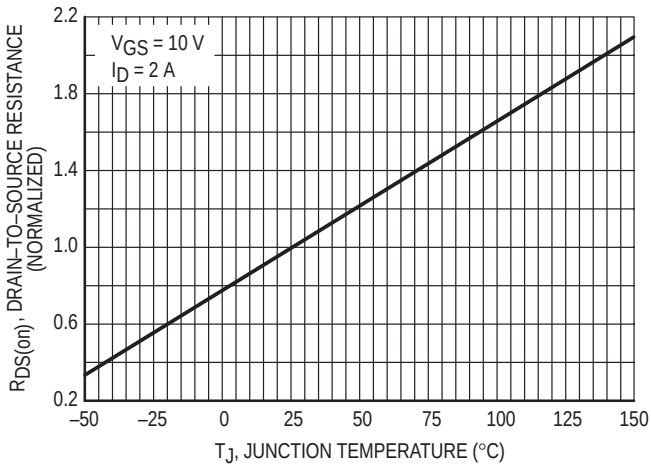


Figure 5. On–Resistance Variation with Temperature

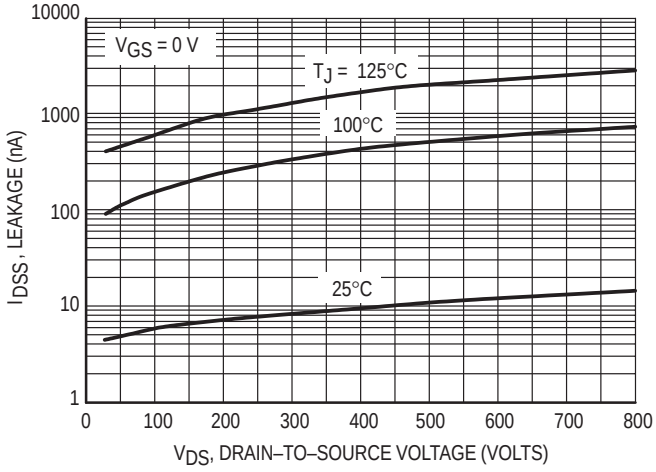


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

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$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

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At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

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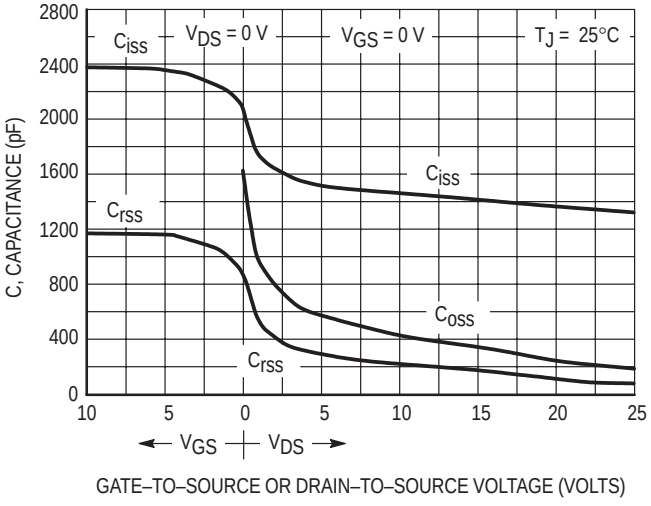


Figure 7a. Capacitance Variation

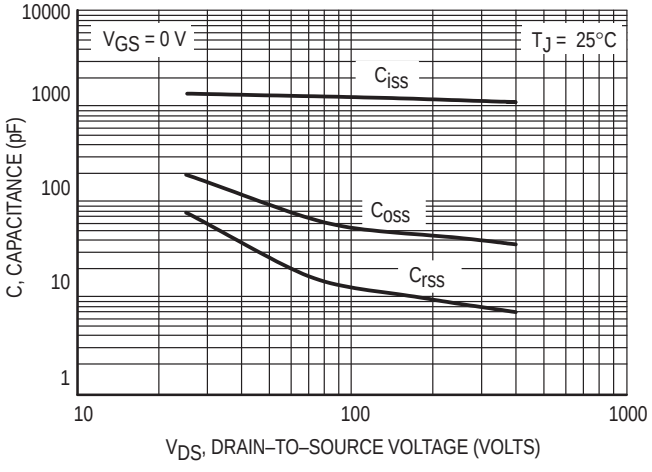


Figure 7b. High Voltage Capacitance Variation

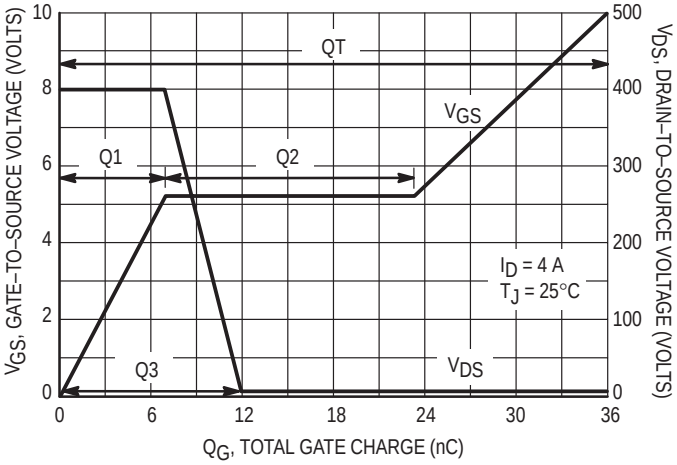


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

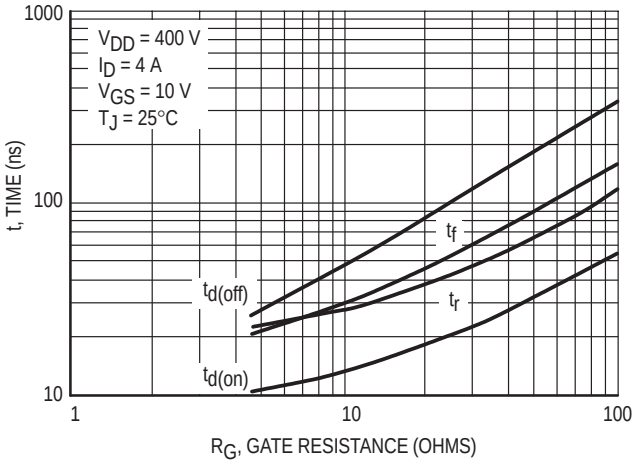


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

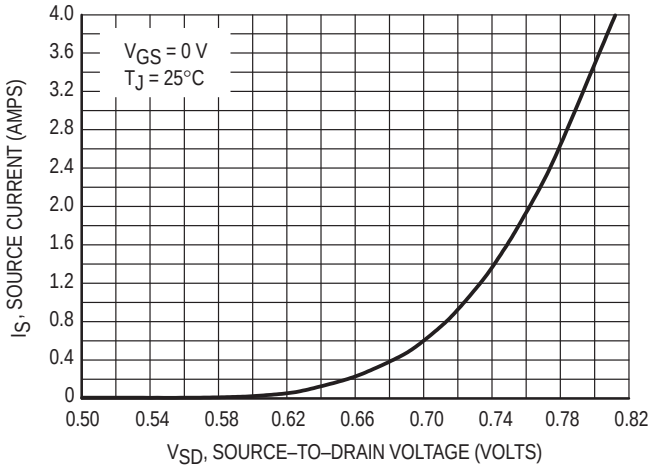


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

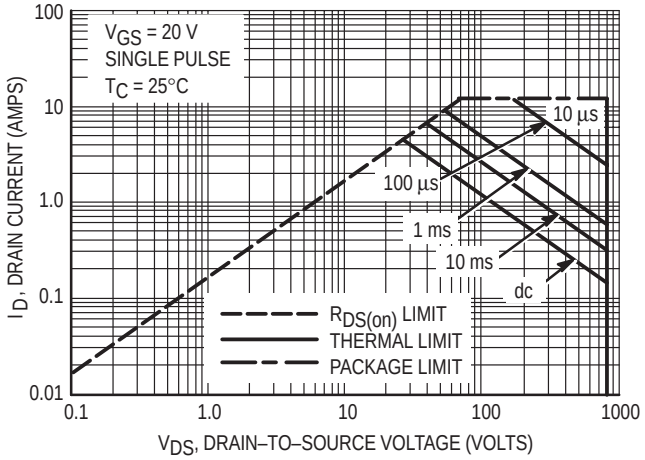


Figure 11. Maximum Rated Forward Biased Safe Operating Area

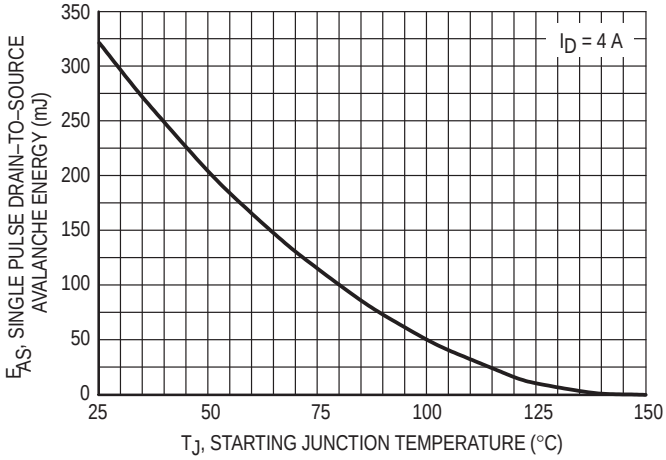


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

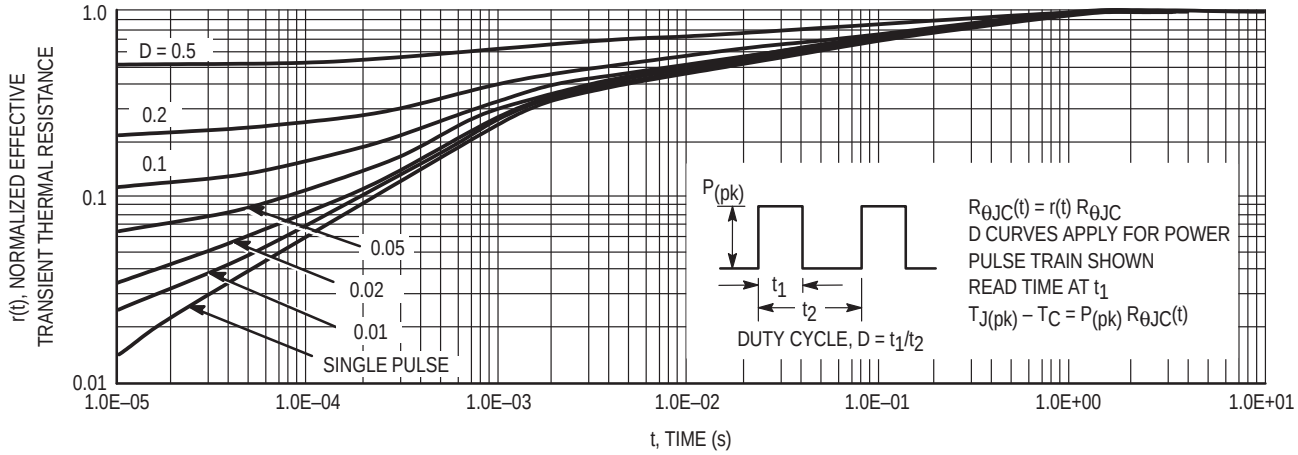


Figure 13. Thermal Response

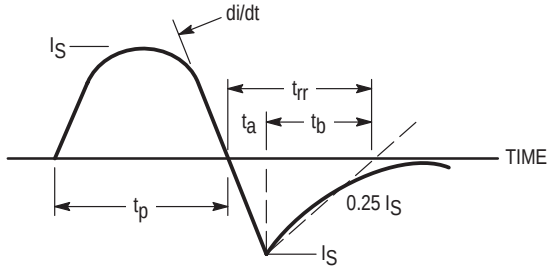


Figure 14. Diode Reverse Recovery Waveform

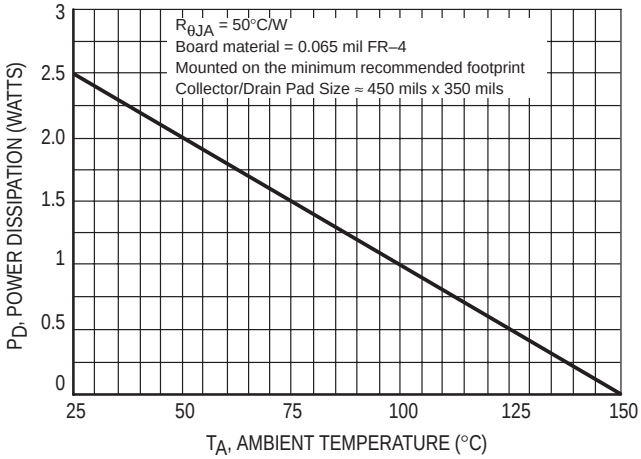


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

TMOS E-FET™
High Energy Power FET
D²PAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

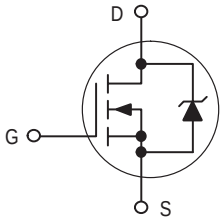
MTB6N60E

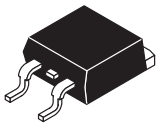
Motorola Preferred Device

TMOS POWER FET
6.0 AMPERES
600 VOLTS
$R_{DS(on)}$ = 1.2 OHM

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	600	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	6.0 4.6 18	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 9.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	405	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

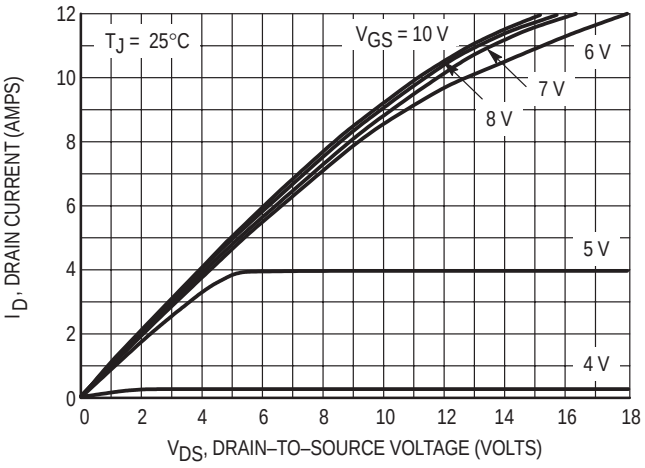
REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	600 —	— 689	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 7.1	4.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	—	0.94	1.2	Ohms
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 6.0 Adc) (V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	6.0 —	8.6 7.6	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 3.0 Adc)		g_{FS}	2.0	5.5	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1498	2100	pF
Output Capacitance		C_{oss}	—	158	217	
Reverse Transfer Capacitance		C_{rss}	—	29	56	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DS} = 300 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	14	30	ns
Rise Time		t_r	—	19	40	
Turn–Off Delay Time		$t_{d(off)}$	—	40	80	
Fall Time		t_f	—	26	50	
Gate Charge	(V_{DS} = 300 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	35.5	50	nC
		Q_1	—	8.1	—	
		Q_2	—	14.1	—	
		Q_3	—	15.8	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc) (I_S = 6.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.83 0.72	1.5 —	Vdc
Reverse Recovery Time	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	266	—	ns
		t_a	—	166	—	
		t_b	—	100	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.5	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS



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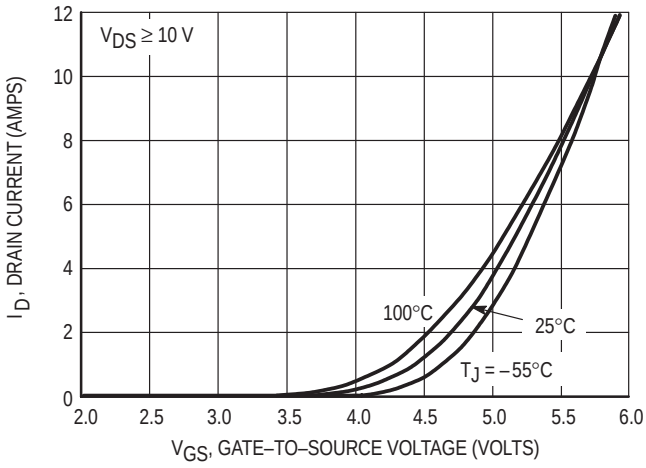

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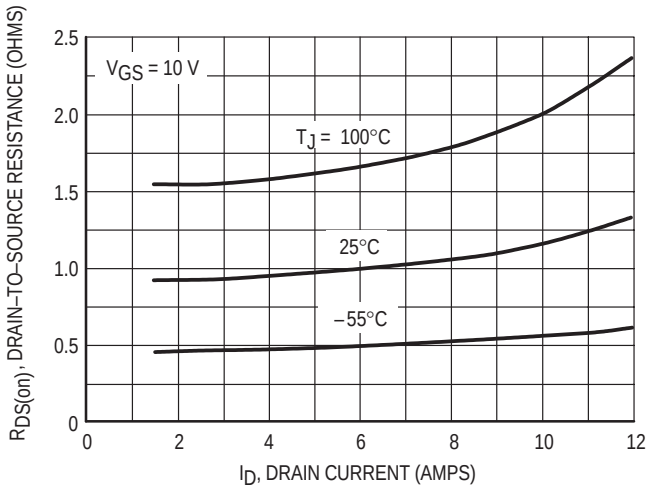

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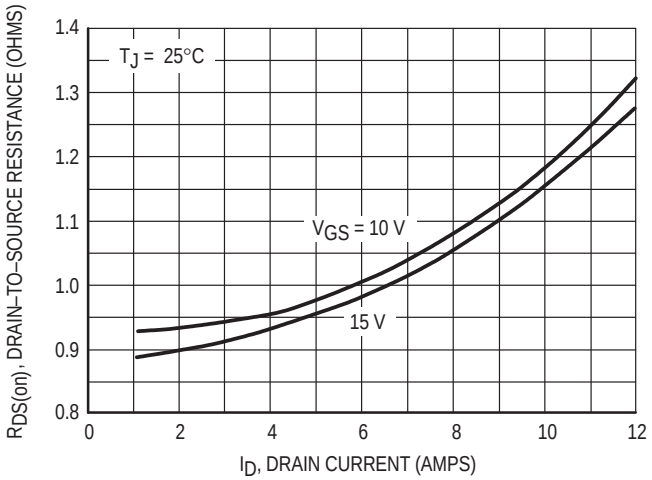

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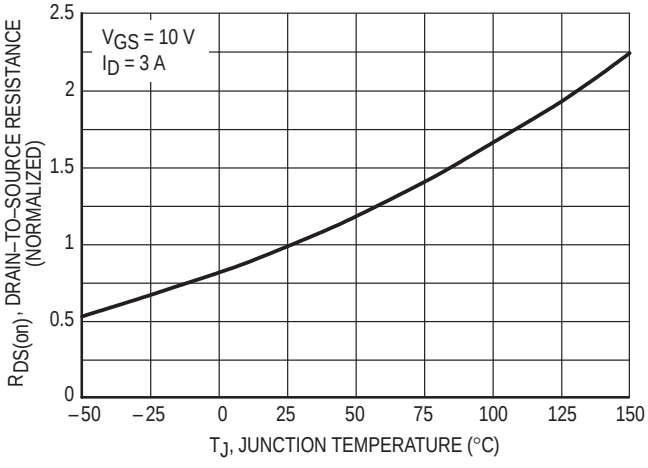

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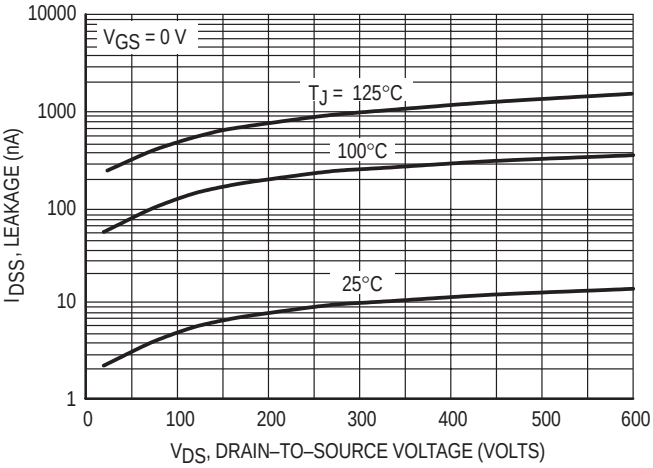

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$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

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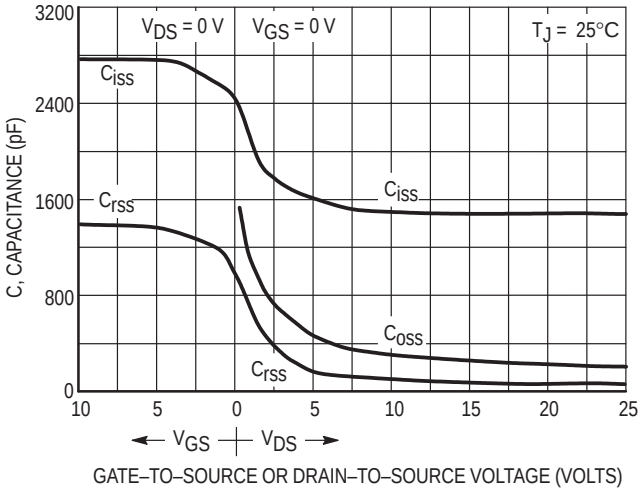


Figure 7a. Capacitance Variation

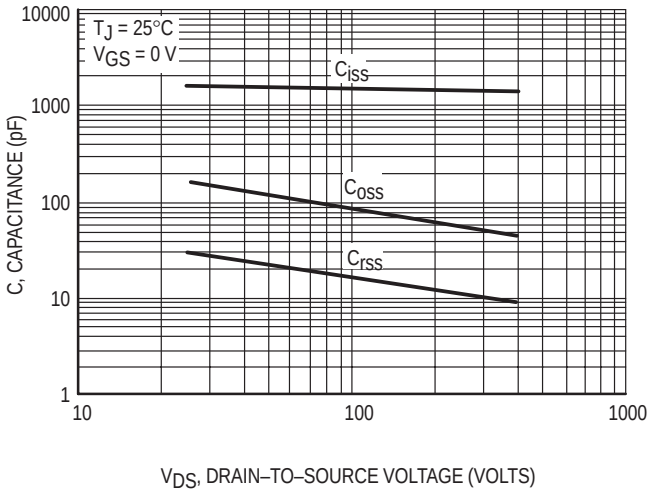


Figure 7b. High Voltage Capacitance Variation

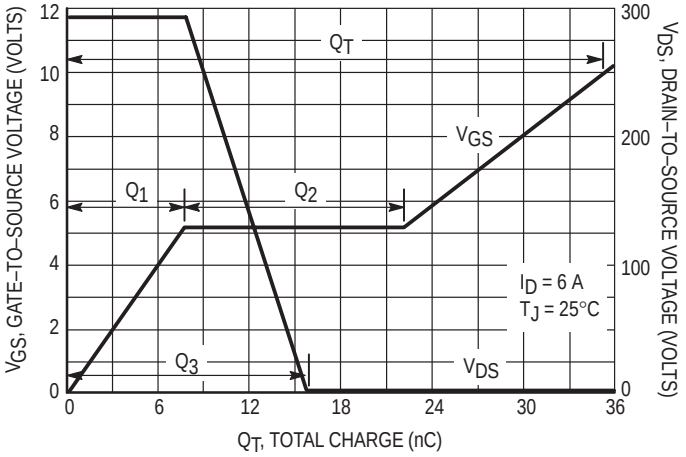


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

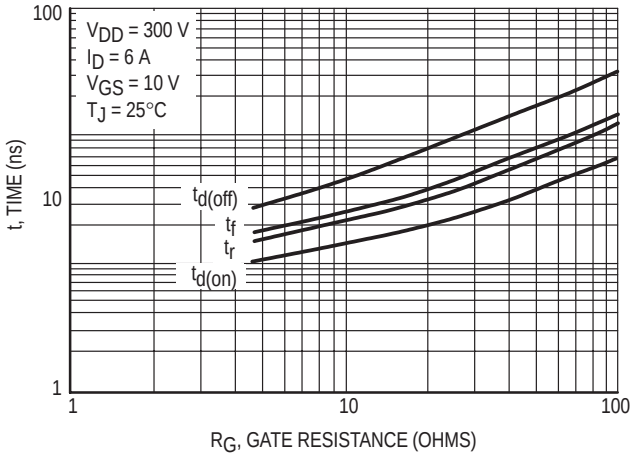


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

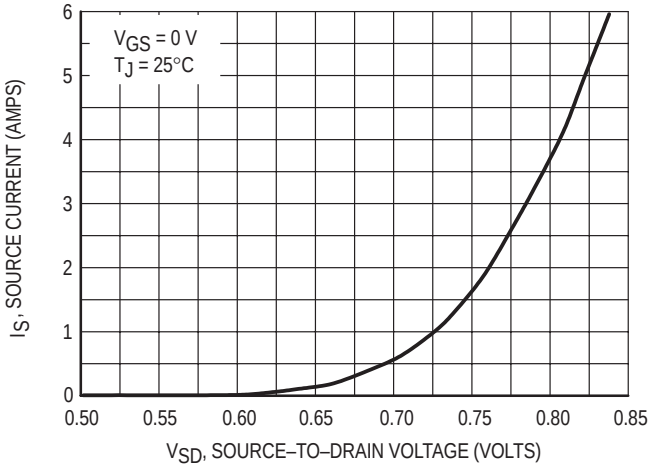


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

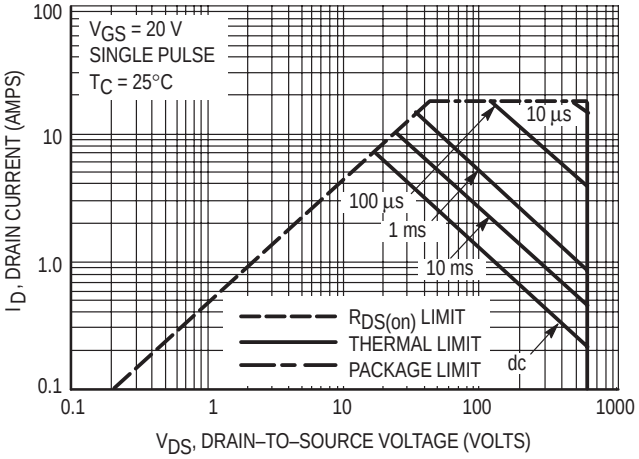


Figure 11. Maximum Rated Forward Biased Safe Operating Area

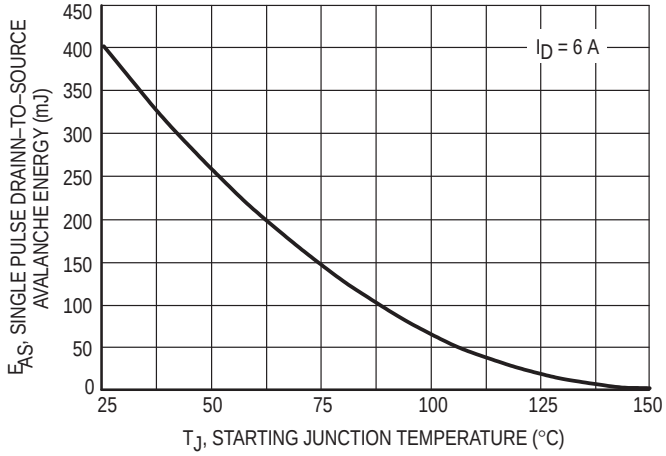


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

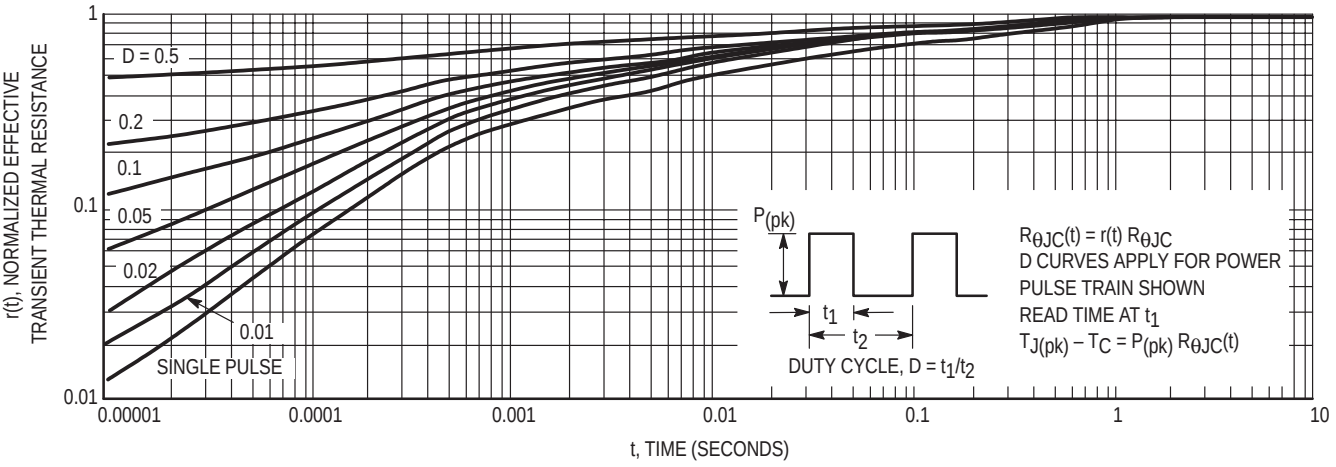


Figure 13. Thermal Response

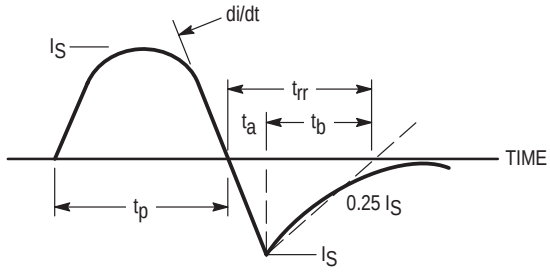


Figure 14. Diode Reverse Recovery Waveform

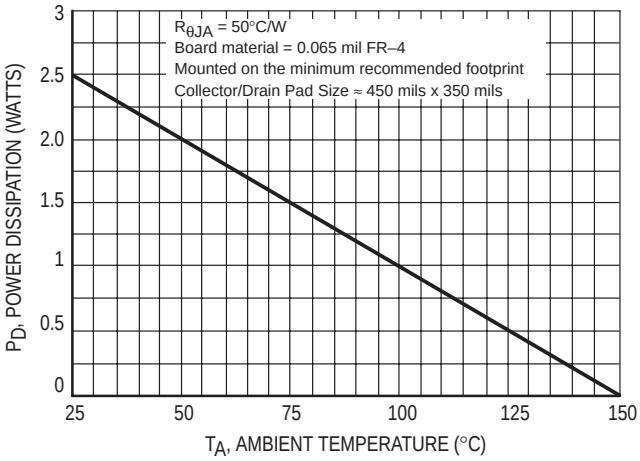


Figure 15. D^{2}PAK Power Derating Curve

Advance Information

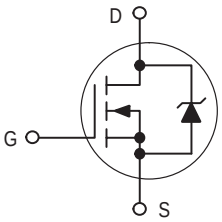
TMOS E-FET™
High Energy Power FET
D²PAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

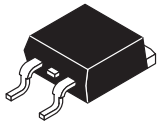
MTB8N50E

Motorola Preferred Device

TMOS POWER FET
8.0 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.8 OHM

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 418B–02, Style 2
D²PAK

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	8.0 5.0 32	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted with the minimum recommended pad size	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, I_L = 8.0 Apk, L = 15.9 mH, R_G = 25 Ω)	E_{AS}	510	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 40 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	500	—	—	Vdc
Temperature Coefficient (Positive)			—	500	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	250	μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	1000	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	—	4.0	Vdc
Temperature Coefficient (Negative)			—	5.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)		$R_{DS(on)}$	—	0.6	0.8	Ohms
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 8.0 Adc)		$V_{DS(on)}$	—	—	7.2	Vdc
(I_D = 4.0 Adc, T_J = 125°C)			—	—	6.4	
Forward Transconductance (V_{DS} = 50 Vdc, I_D = 4.0 Adc)		g_{FS}	4.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1200	1800	pF
Output Capacitance		C_{oss}	—	176	264	
Reverse Transfer Capacitance		C_{rss}	—	72	108	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 8.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	25	50	ns
Rise Time		t_r	—	36	72	
Turn–Off Delay Time		$t_{d(off)}$	—	75	150	
Fall Time		t_f	—	30	60	
Gate Charge	(V_{DS} = 400 Vdc, I_D = 8.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	92	125	nC
		Q_1	—	12	—	
		Q_2	—	45	—	
		Q_3	—	35	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 8.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.1	2.0	Vdc
	(I_S = 8.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.0	—	
Reverse Recovery Time	(I_S = 8.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	420	—	ns
		t_a	—	280	—	
		t_b	—	140	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4.4	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

Designer's™ Data Sheet

TMOS E-FET ™
High Energy Power FET
D²PAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

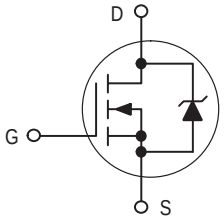
MTB9N25E

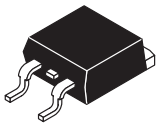
Motorola Preferred Device

TMOS POWER FET
9.0 AMPERES
250 VOLTS
$R_{DS(on)}$ = 0.45 OHM

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	250	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	250	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	9.0 5.7 32	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	80 0.64 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, Peak I_L = 9.0 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	 122	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.56 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	250	—	—	Vdc
Temperature Coefficient (Positive)			—	328	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 250 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 250 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 4.5 Adc)		$R_{DS(on)}$	—	0.37	0.45	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 9.0 Adc)		$V_{DS(on)}$	—	3.5	5.4	Vdc
(V_{GS} = 10 Vdc, I_D = 4.5 Adc, T_J = 125°C)			—	—	4.7	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 4.5 Adc)		g_{FS}	3.0	5.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	783	1100	pF
Output Capacitance		C_{oss}	—	144	200	
Transfer Capacitance		C_{rss}	—	32	65	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 125 Vdc, I_D = 9.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	10	20	ns
Rise Time		t_r	—	36	70	
Turn–Off Delay Time		$t_{d(off)}$	—	27	55	
Fall Time		t_f	—	26	50	
Gate Charge (See Figure 8)	(V_{DS} = 200 Vdc, I_D = 9.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	26	40	nC
		Q_1	—	4.8	—	
		Q_2	—	12.7	—	
		Q_3	—	9.2	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 9.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.9	1.5	Vdc
	(I_S = 9.0 Adc, V_{GS} = 0 Vdc , T_J = 125°C)		—	0.81	—	
Reverse Recovery Time (See Figure 14)	(I_S = 9.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	191	—	ns
		t_a	—	126	—	
		t_b	—	65	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.387	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

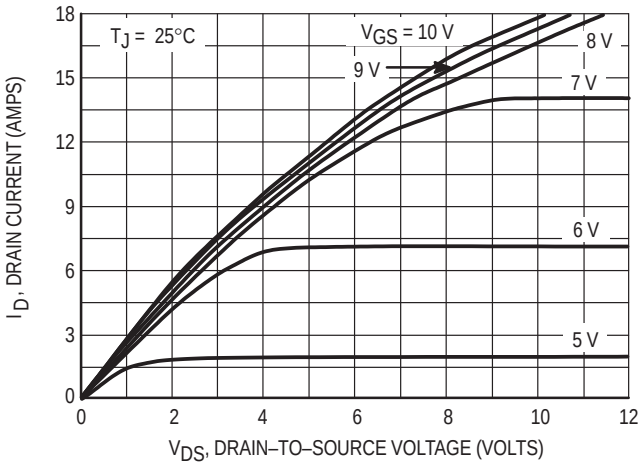


Figure 1. On–Region Characteristics

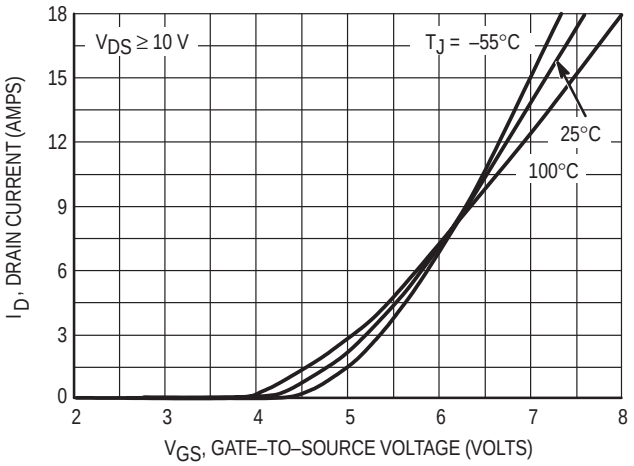


Figure 2. Transfer Characteristics

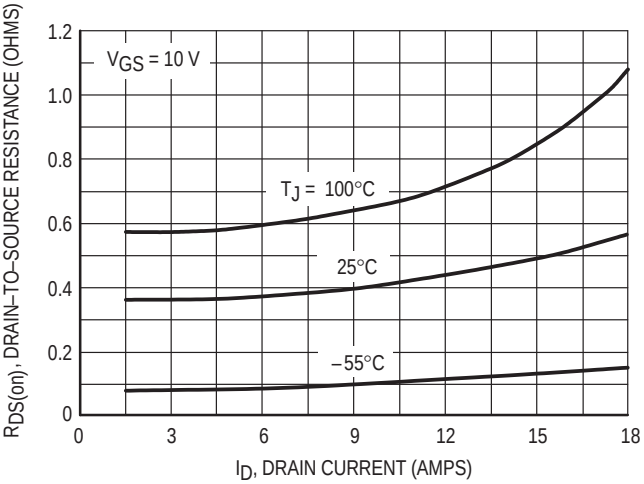


Figure 3. On–Resistance versus Drain Current and Temperature

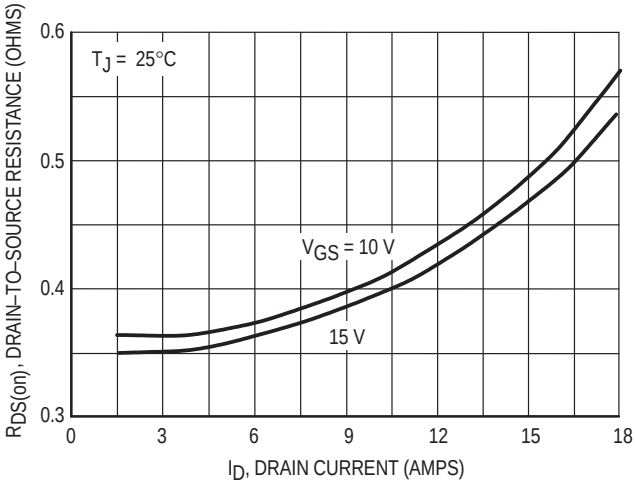


Figure 4. On–Resistance versus Drain Current and Gate Voltage

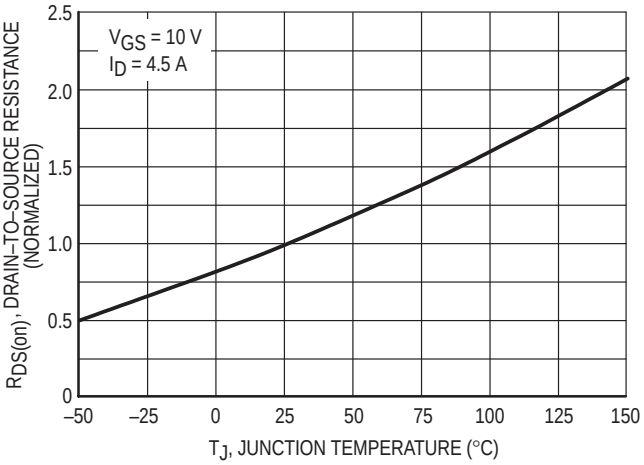


Figure 5. On–Resistance Variation with Temperature

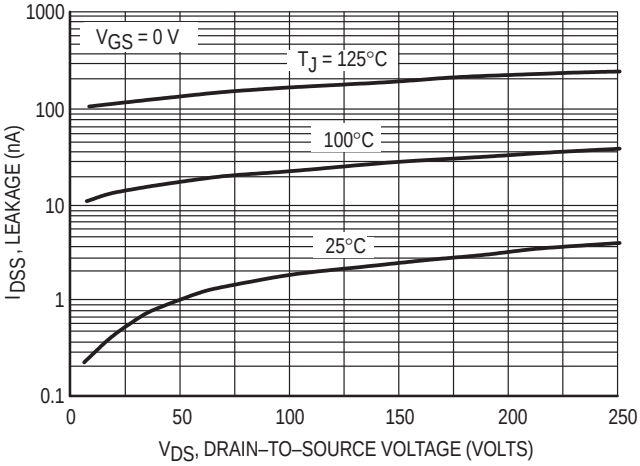


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

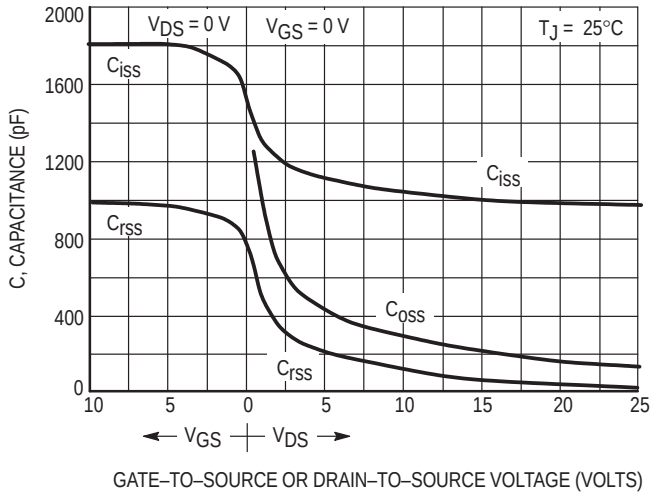


Figure 7. Capacitance Variation

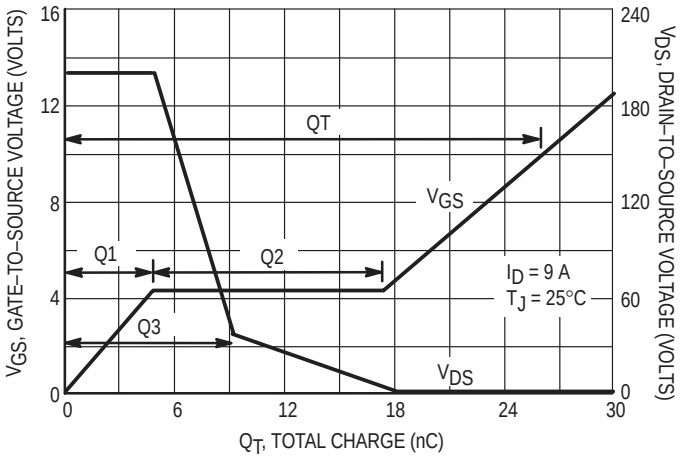


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

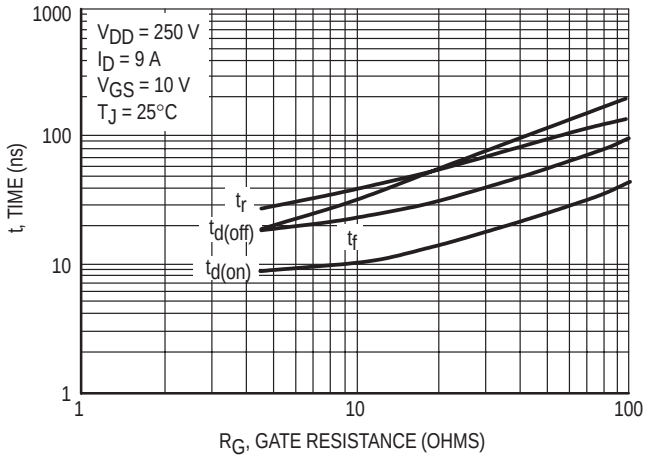


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

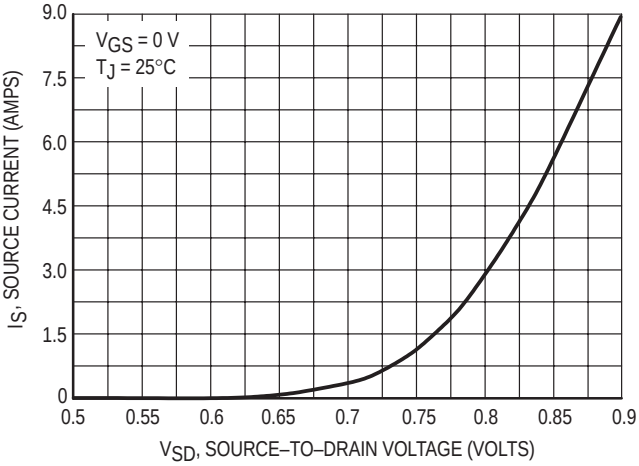


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

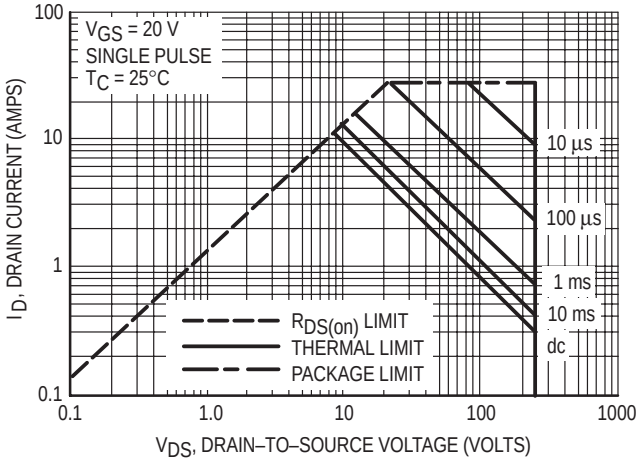


Figure 11. Maximum Rated Forward Biased Safe Operating Area

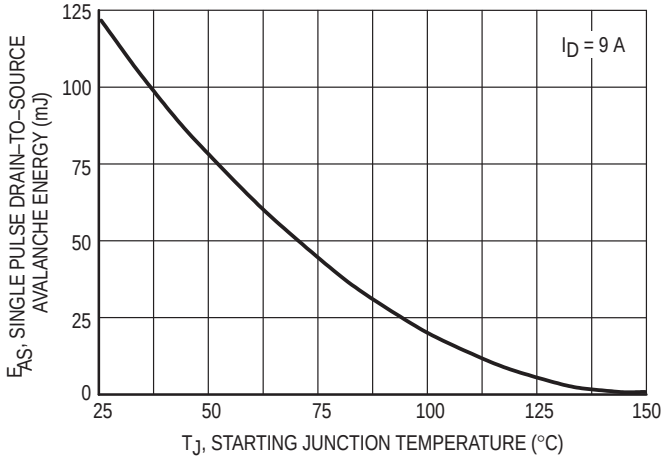


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

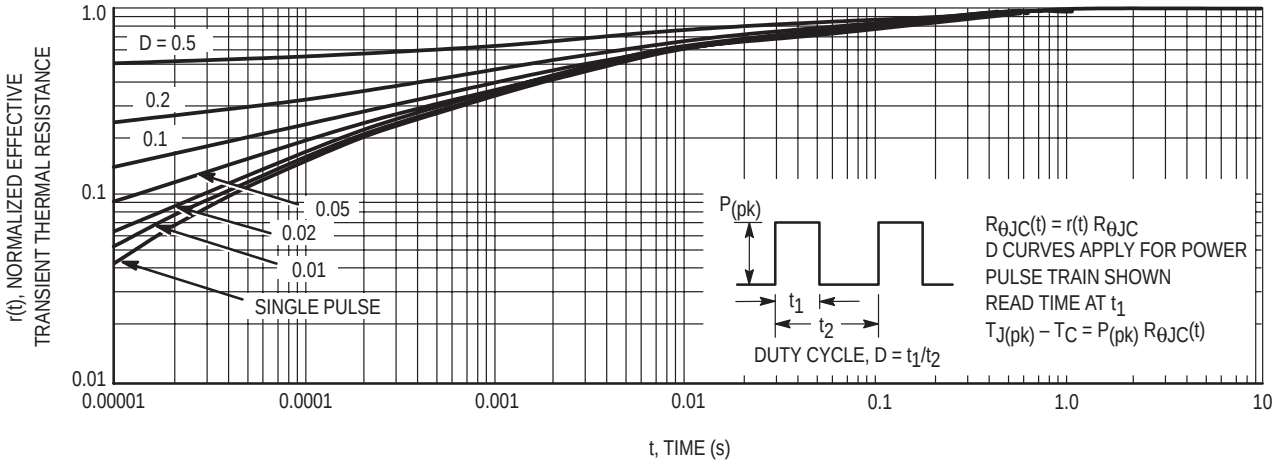


Figure 13. Thermal Response

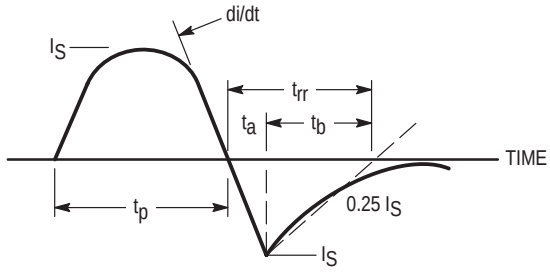


Figure 14. Diode Reverse Recovery Waveform

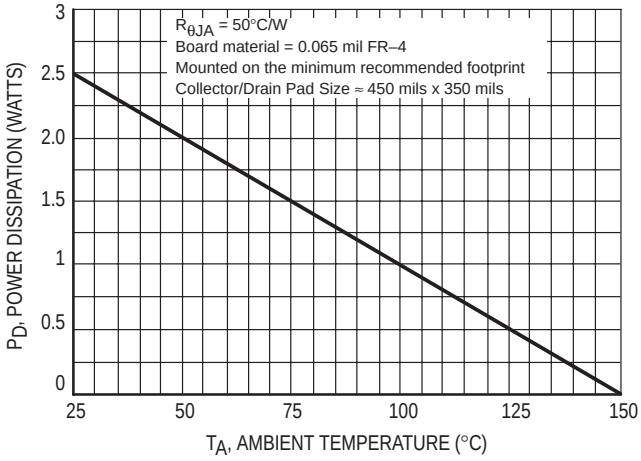


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

TMOS E-FET ™
High Energy Power FET
D²PAK for Surface Mount

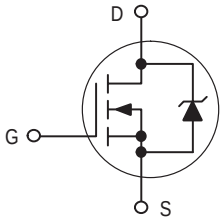
N–Channel Enhancement–Mode Silicon Gate

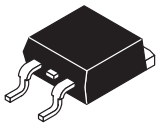
MTB10N40E

Motorola Preferred Device

TMOS POWER FET
10 AMPERES
400 VOLTS
$R_{DS(on)}$ = 0.55 OHM

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 418B–02, Style 2
D²PAK

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	400	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	10 6.0 40	Amps Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted with the minimum recommended pad size	P_D	125 1.00 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vpk, I_L = 10 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	520	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.00 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	400 —	— 398	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 400 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 400 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	0.1 1.0	μAdc
Gate–Body Leakage Current–Forward (V_{gsf} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current–Reverse (V_{gsr} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	2.8 6.3	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc)		$R_{DS(on)}$	—	0.4	0.55	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 10 Adc) (I_D = 5.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	5.61 —	6.6 5.5	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 5.0 Adc)		g_{FS}	4.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1570	2200	pF
Output Capacitance		C_{oss}	—	230	325	
Reverse Transfer Capacitance		C_{rss}	—	55	110	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 200 Vdc, I_D = 10 Adc, V_{GS} = 10 Vdc, R_G = 10 Ω)	$t_{d(on)}$	—	25	50	ns
Rise Time		t_r	—	37	75	
Turn–Off Delay Time		$t_{d(off)}$	—	75	150	
Fall Time		t_f	—	31	65	
Gate Charge (See Figure 8)	(V_{DS} = 320 Vdc, I_D = 10 Adc, V_{GS} = 10 Vdc)	Q_T	—	46	63	nC
		Q_1	—	10	—	
		Q_2	—	23	—	
		Q_3	—	—	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 10 Adc, V_{GS} = 0 Vdc) (I_S = 10 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.9 —	2.0 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 10 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	250	—	ns
Reverse Recovery Stored Charge		Q_{RR}	—	3000	—	nC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

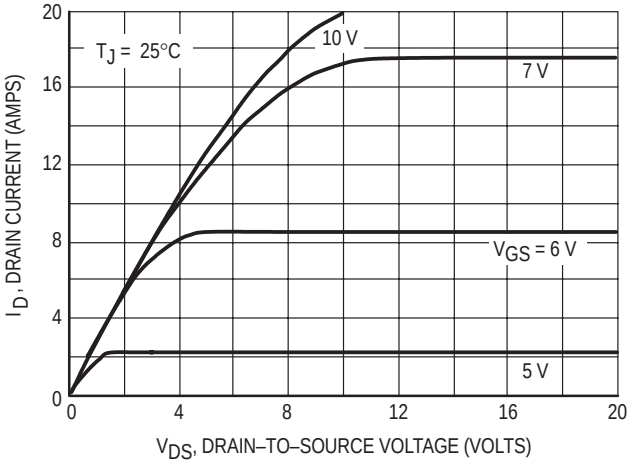


Figure 1. On–Region Characteristics

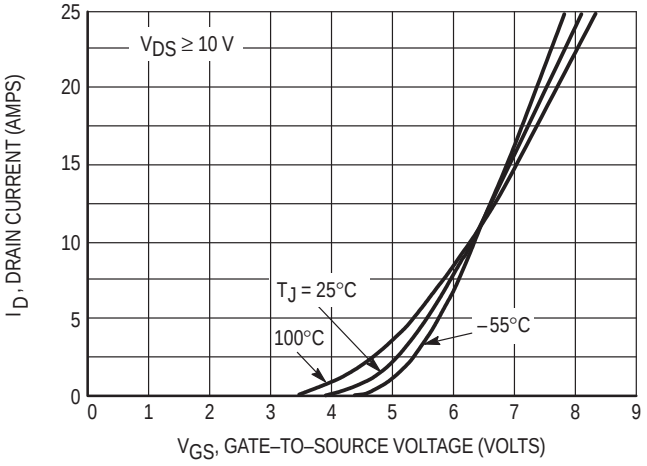


Figure 2. Transfer Characteristics

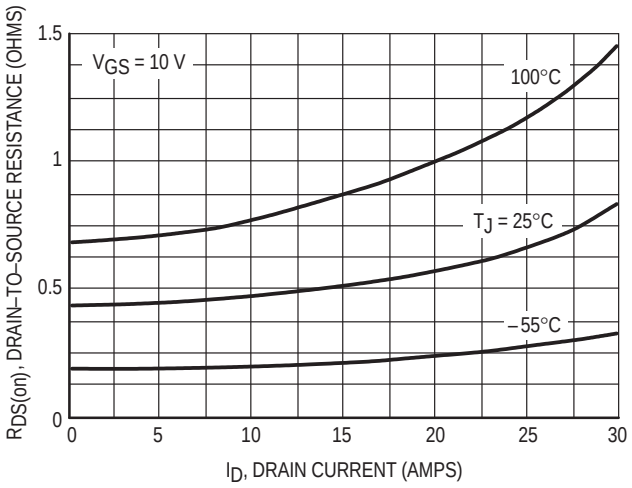


Figure 3. On–Resistance versus Drain Current and Temperature

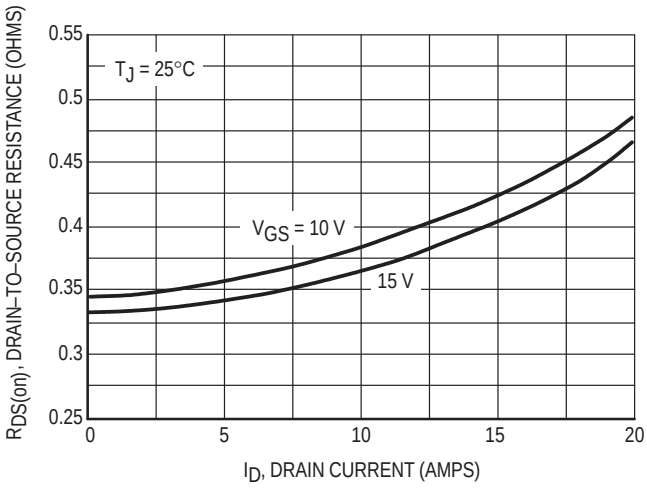


Figure 4. On–Resistance versus Drain Current and Gate Voltage

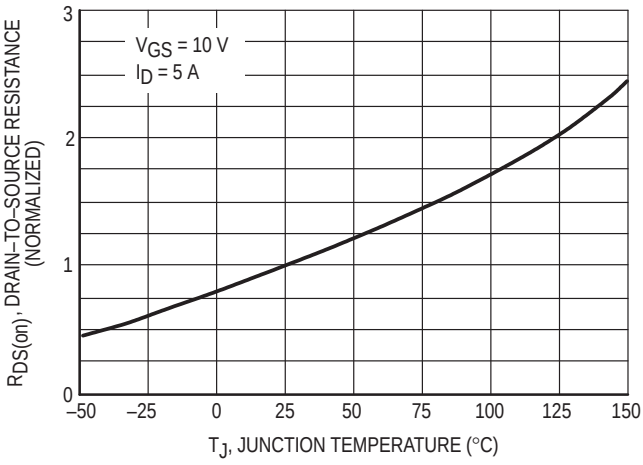


Figure 5. On–Resistance Variation with Temperature

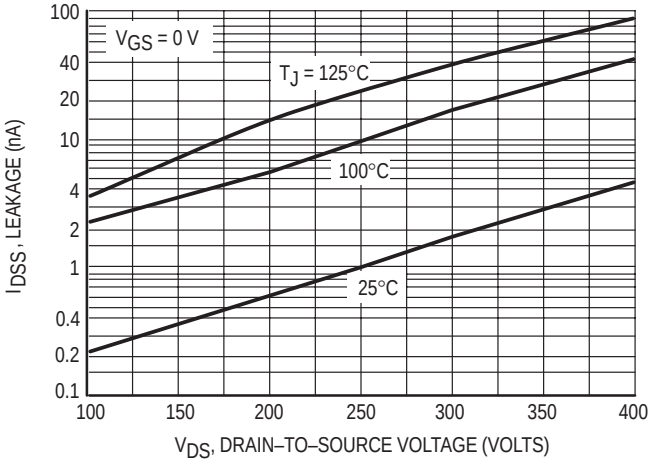


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

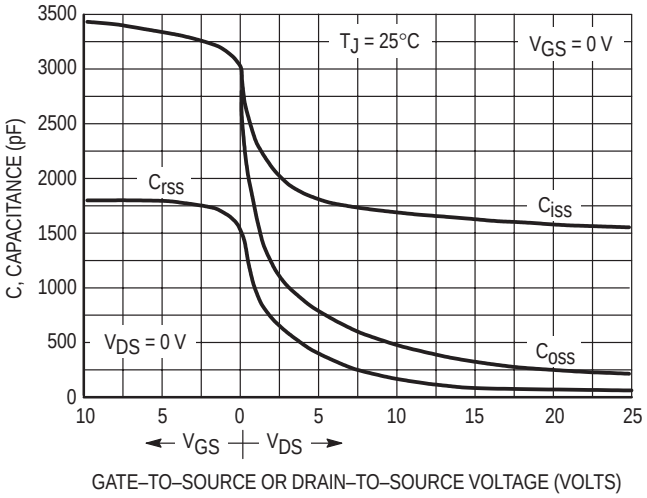
$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.



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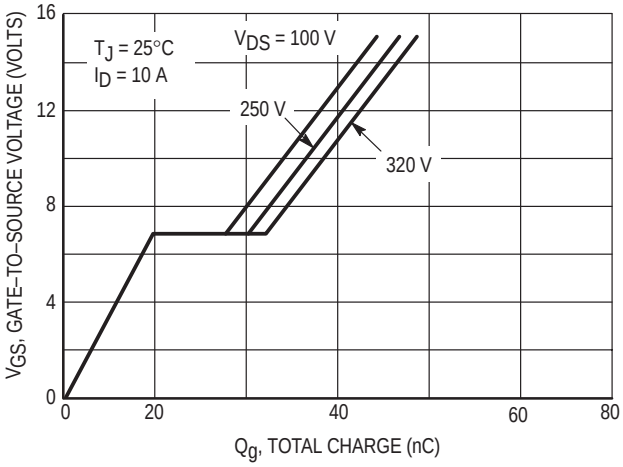

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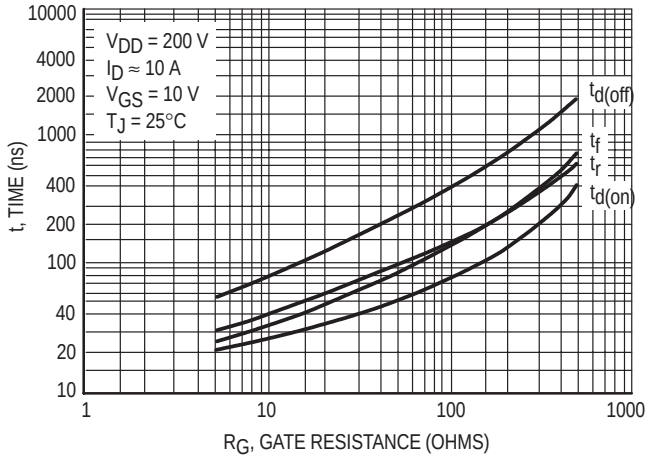

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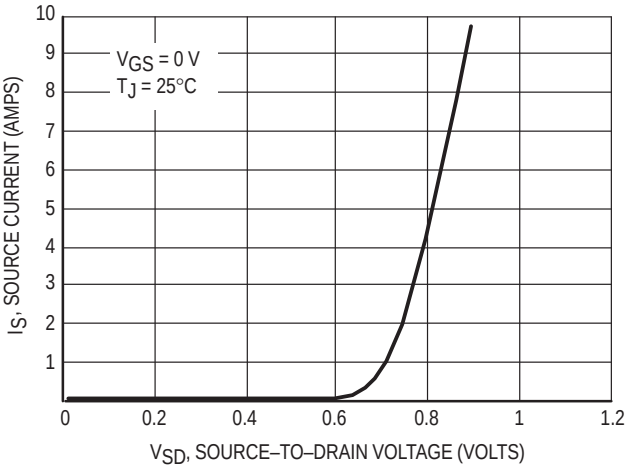
DRAIN–TO–SOURCE DIODE CHARACTERISTICS



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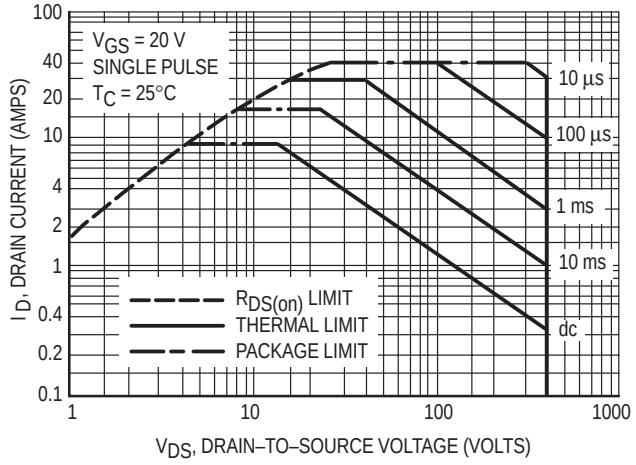

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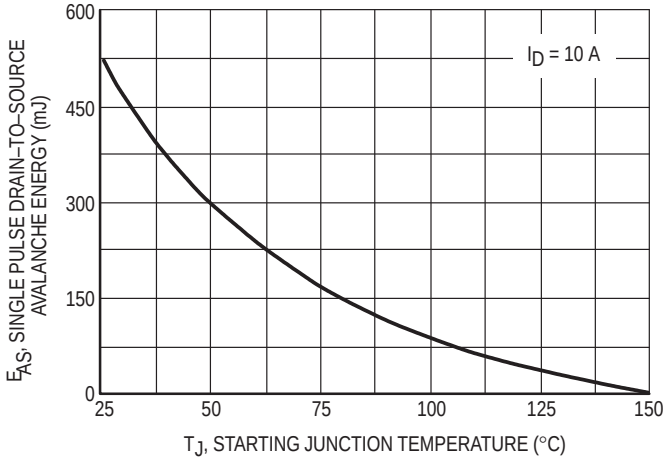


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

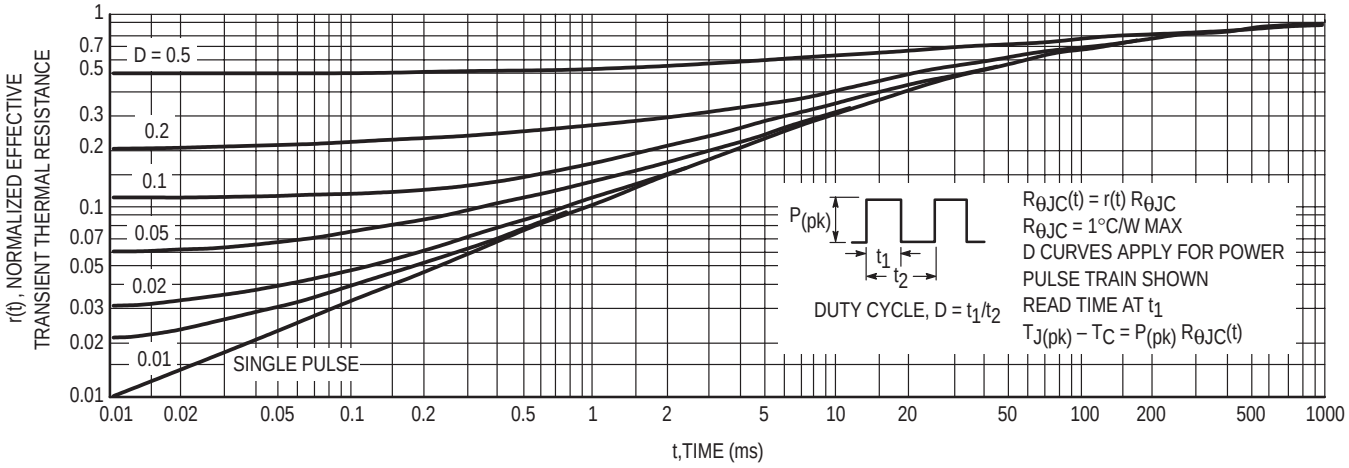


Figure 13. Thermal Response

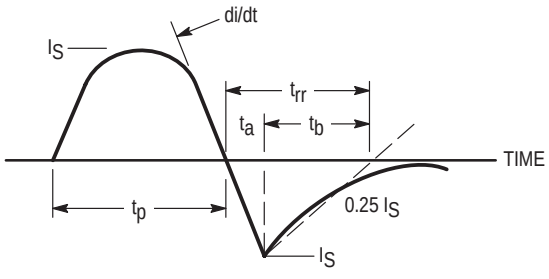


Figure 14. Diode Reverse Recovery Waveform

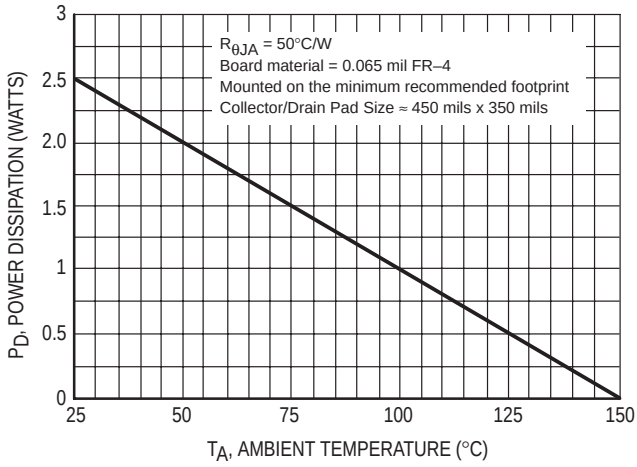


Figure 15. D²PAK Power Derating Curve

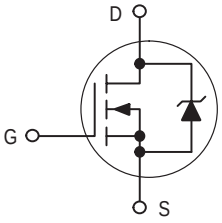
Designer's™ Data Sheet

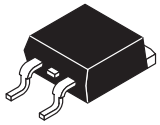
TMOS V™
Power Field Effect Transistor
D²PAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

MTB15N06V

TMOS POWER FET
15 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.12 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 418B–02, Style 2
D²PAK

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETs
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	15 8.7 45	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	55 0.37 3.0	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 15 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	113	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.73 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	67	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.7	4.0	Vdc
Temperature Coefficient (Negative)			—	5.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$R_{DS(on)}$	—	0.08	0.12	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 15 Adc)			—	2.0	2.2	
(I_D = 7.5 Adc, T_J = 150°C)			—	—	1.9	
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 7.5 Adc)		g_{FS}	4.0	6.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	469	660	pF
Output Capacitance		C_{oss}	—	148	200	
Reverse Transfer Capacitance		C_{rss}	—	35	60	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 15 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	7.6	20	ns
Rise Time		t_r	—	51	100	
Turn–Off Delay Time		$t_{d(off)}$	—	18	40	
Fall Time		t_f	—	33	70	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 15 Adc, V_{GS} = 10 Vdc)	Q_T	—	14.4	20	nC
		Q_1	—	2.8	—	
		Q_2	—	6.4	—	
		Q_3	—	6.1	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 15 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.05	1.6	Vdc
	(I_S = 15 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.9	—	
Reverse Recovery Time (See Figure 14)	(I_S = 15 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	59.3	—	ns
		t_a	—	46	—	
		t_b	—	13.3	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.165	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

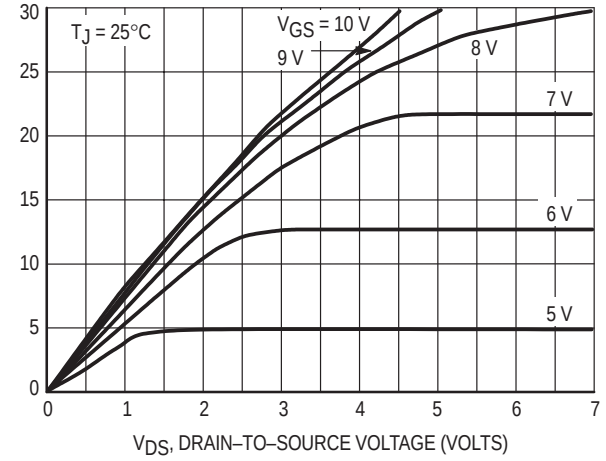


Figure 1. On–Region Characteristics

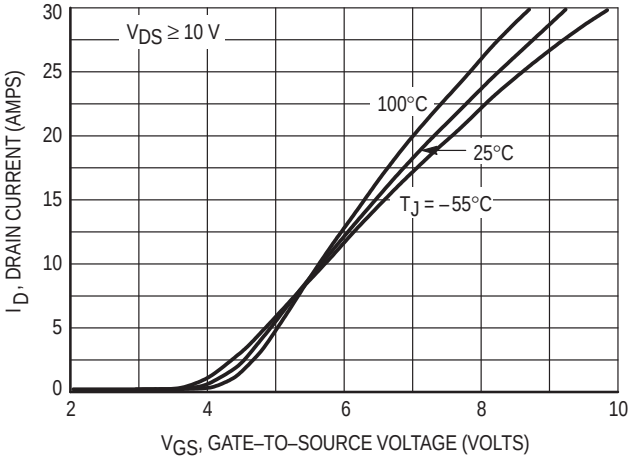


Figure 2. Transfer Characteristics

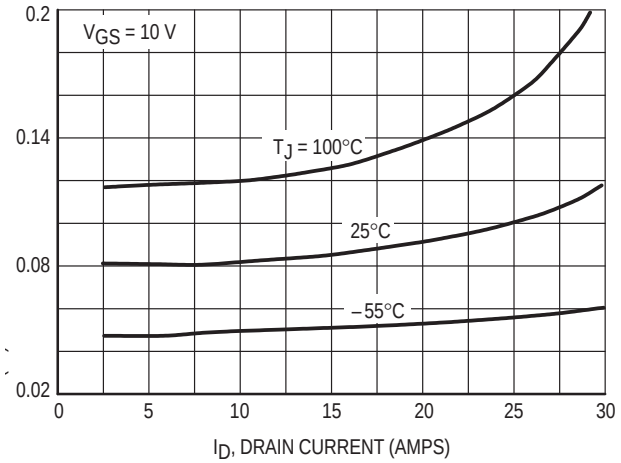


Figure 3. On–Resistance versus Drain Current and Temperature

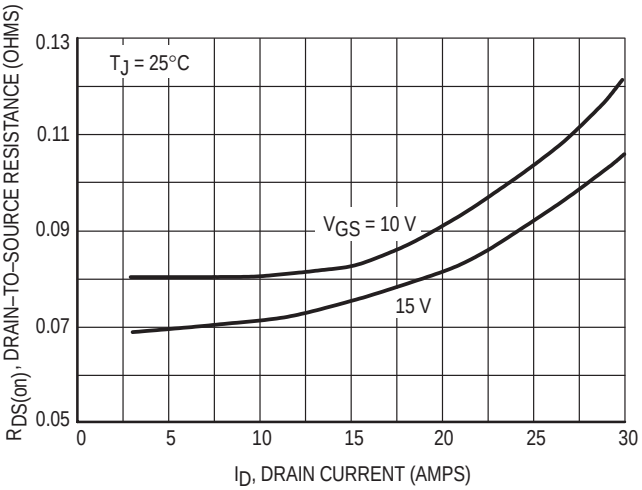


Figure 4. On–Resistance versus Drain Current and Gate Voltage

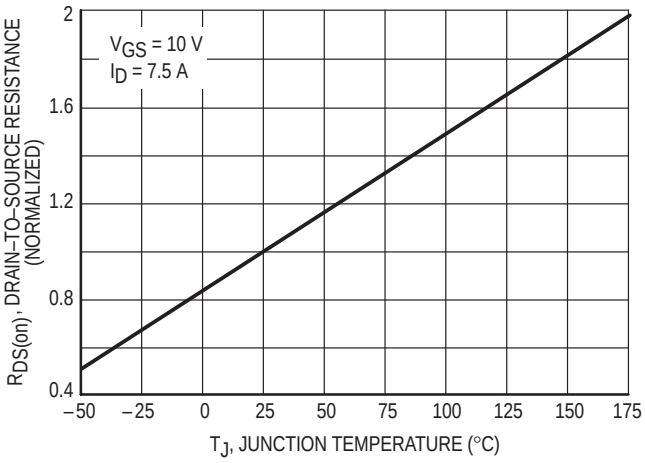


Figure 5. On–Resistance Variation with Temperature

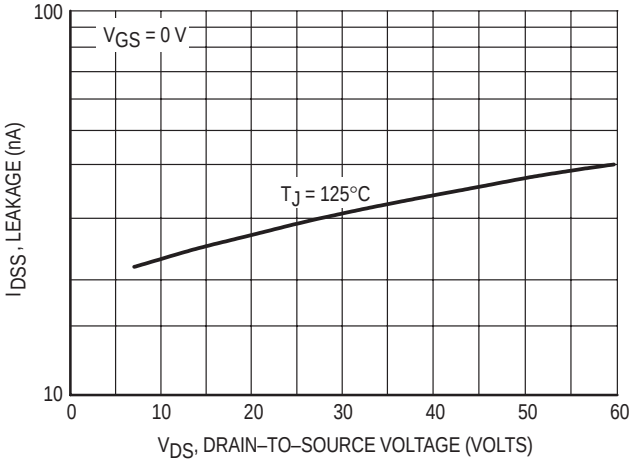


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

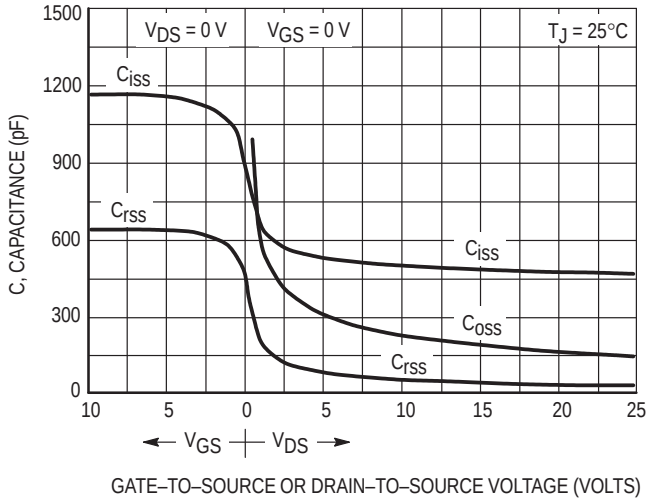


Figure 7. Capacitance Variation

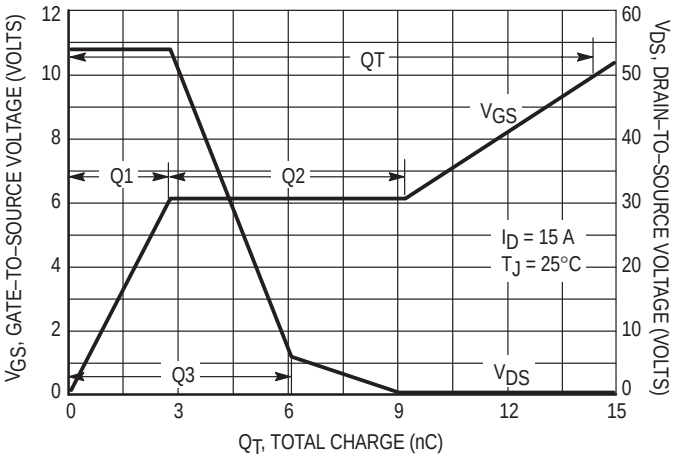


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

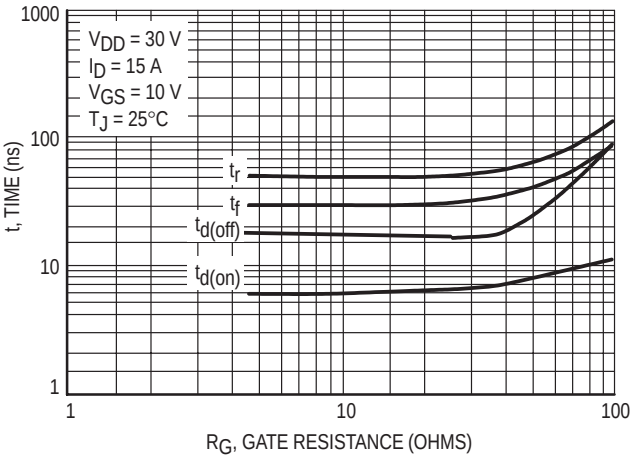


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

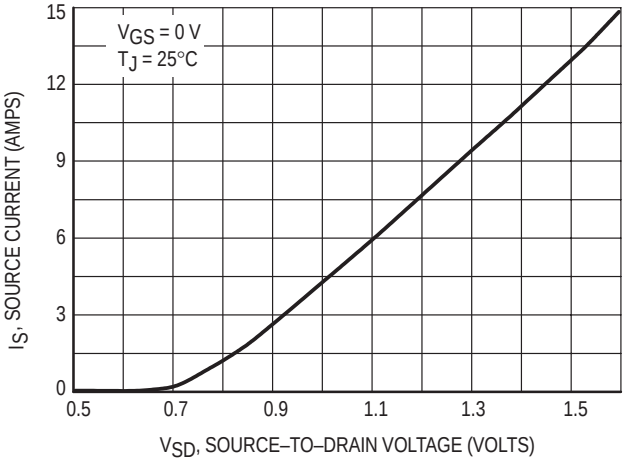


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

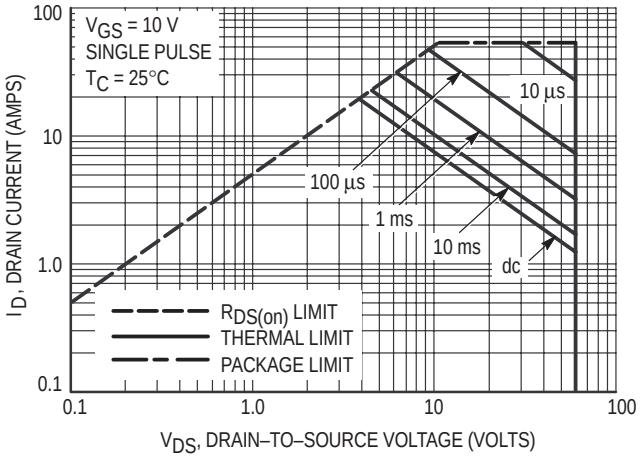


Figure 11. Maximum Rated Forward Biased Safe Operating Area

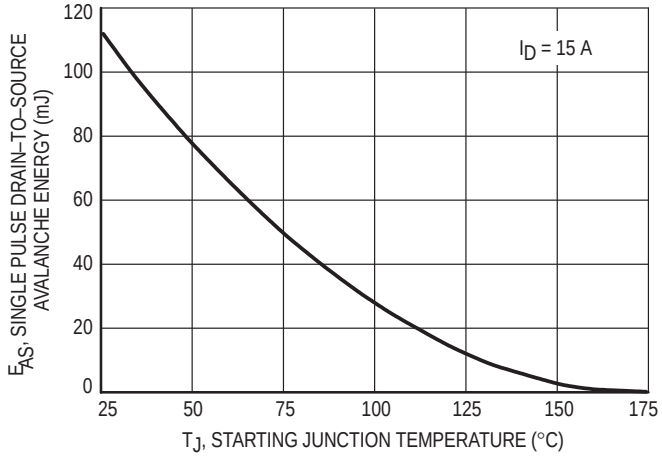


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

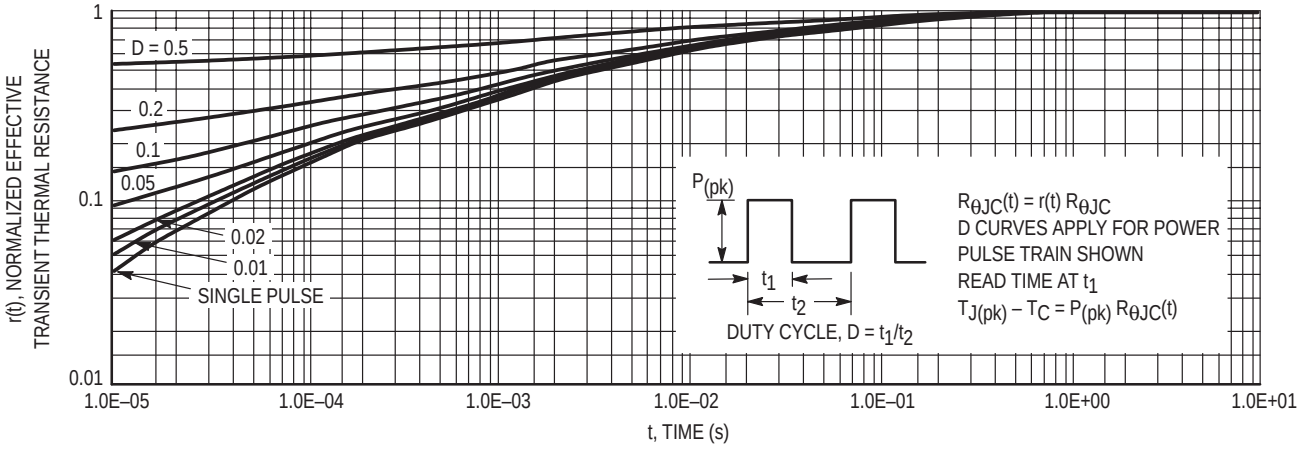


Figure 13. Thermal Response

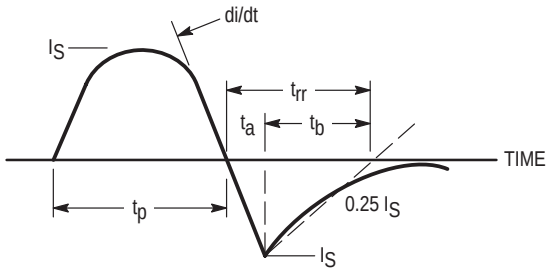


Figure 14. Diode Reverse Recovery Waveform

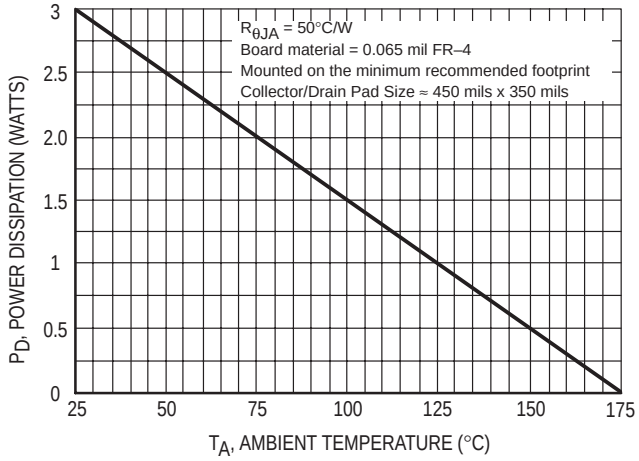


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

TMOS E-FET ™
High Energy Power FET
D²PAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

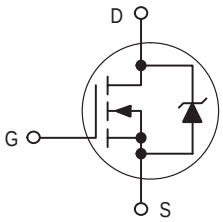
MTB16N25E

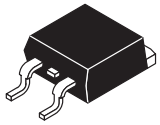
Motorola Preferred Device

TMOS POWER FET
16 AMPERES
250 VOLTS
$R_{DS(on)}$ = 0.25 OHM

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add –T4 Suffix to Part Number





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	250	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	250	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ T_C = 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	16 10 56	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted with the minimum recommended pad size	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, I_L = 16 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	384	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	250	—	—	Vdc
Temperature Coefficient (Positive)			—	333	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 250 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 250 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 8.0 Adc)		$R_{DS(on)}$	—	0.17	0.25	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 16 Adc)		$V_{DS(on)}$	—	3.6	4.8	Vdc
(I_D = 8.0 Adc, T_J = 125°C)			—	—	4.2	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 8.0 Adc)		g_{FS}	3.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1558	2180	pF
Output Capacitance		C_{oss}	—	281	390	
Reverse Transfer Capacitance		C_{rss}	—	130	260	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 125 Vdc, I_D = 16 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	15	30	ns
Rise Time		t_r	—	64	130	
Turn–Off Delay Time		$t_{d(off)}$	—	56	110	
Fall Time		t_f	—	44	90	
Gate Charge (See Figure 8)	(V_{DS} = 200 Vdc, I_D = 16 Adc, V_{GS} = 10 Vdc)	Q_T	—	53.4	70	nC
		Q_1	—	9.3	—	
		Q_2	—	27.5	—	
		Q_3	—	17.1	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 16 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.915	1.5	Vdc
	(I_S = 16 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.39	—	
Reverse Recovery Time (See Figure 14)	(I_S = 16 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	234	—	ns
		t_a	—	170	—	
		t_b	—	64	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.165	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

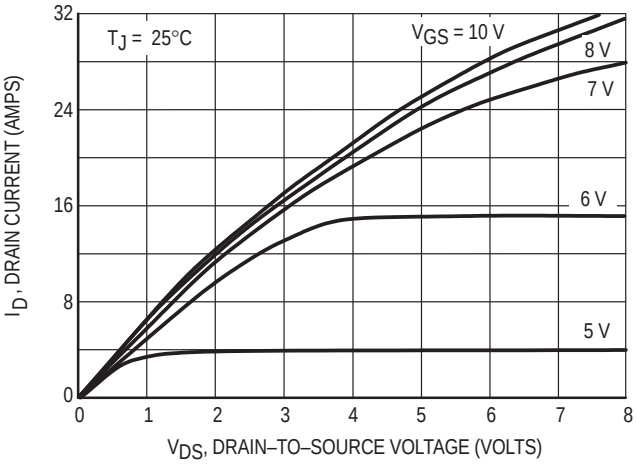


Figure 1. On–Region Characteristics

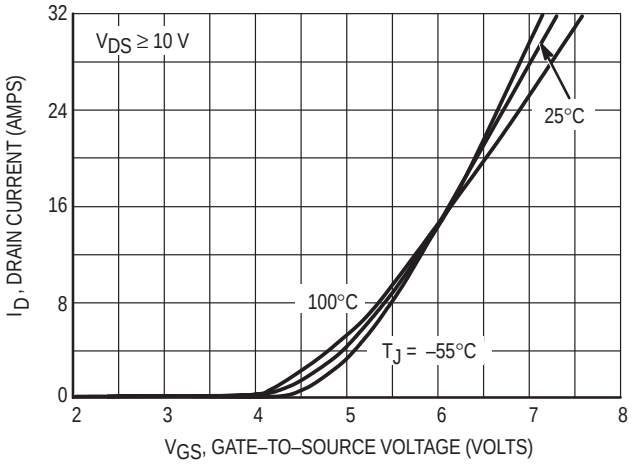


Figure 2. Transfer Characteristics

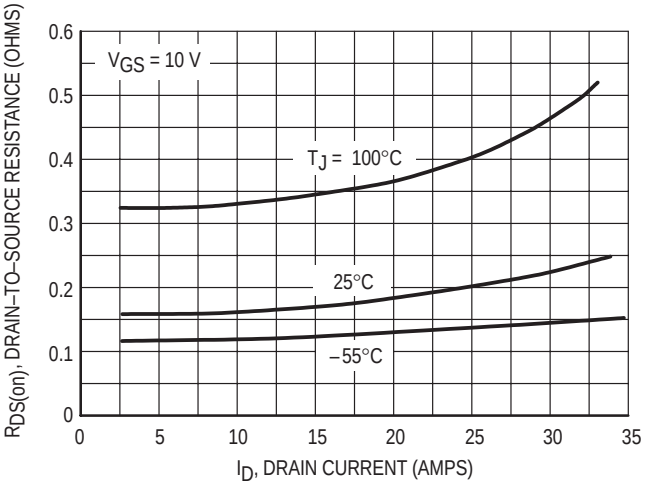


Figure 3. On–Resistance versus Drain Current and Temperature

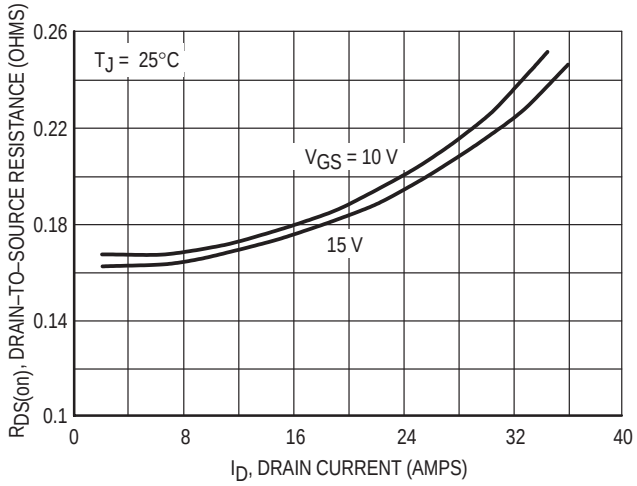


Figure 4. On–Resistance versus Drain Current and Gate Voltage

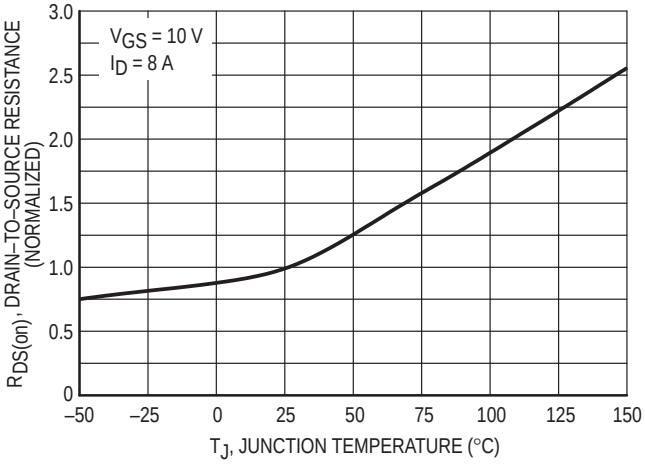


Figure 5. On–Resistance Variation with Temperature

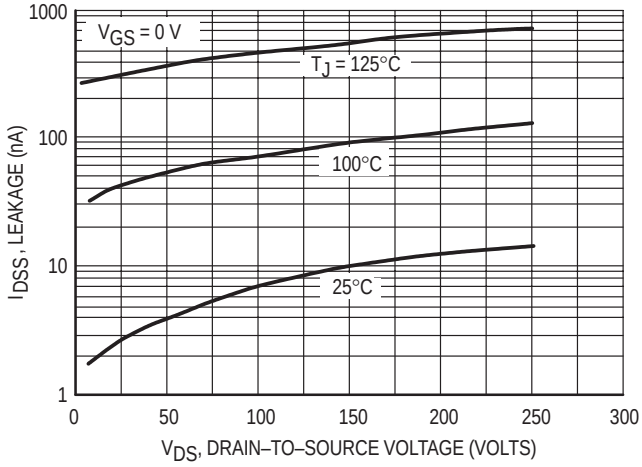


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

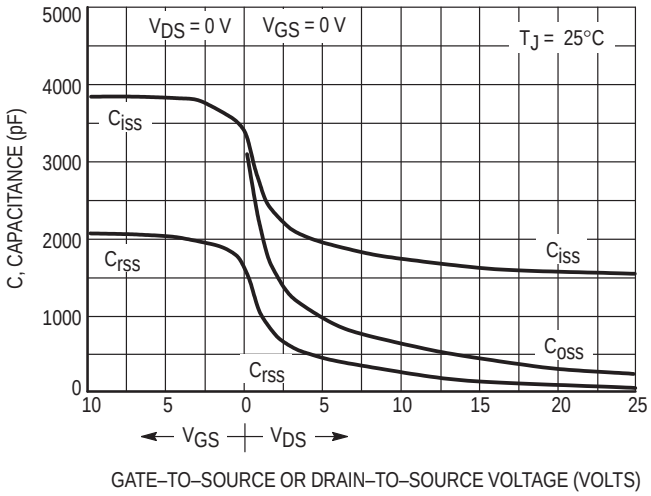


Figure 7. Capacitance Variation

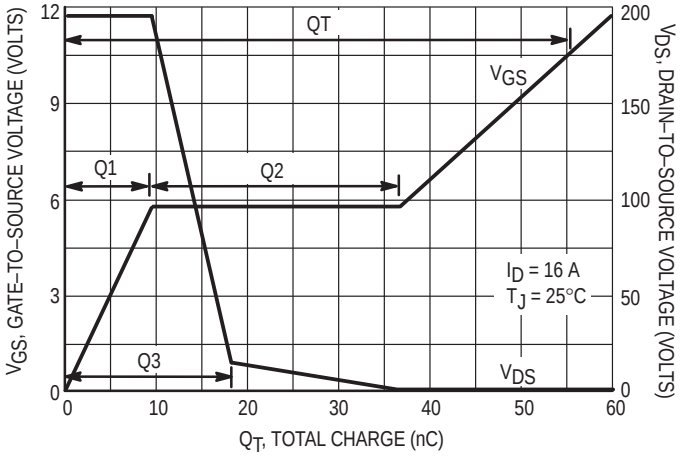


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

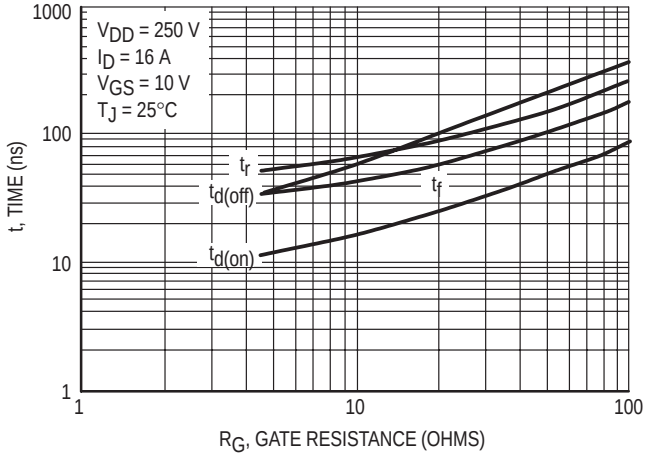


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

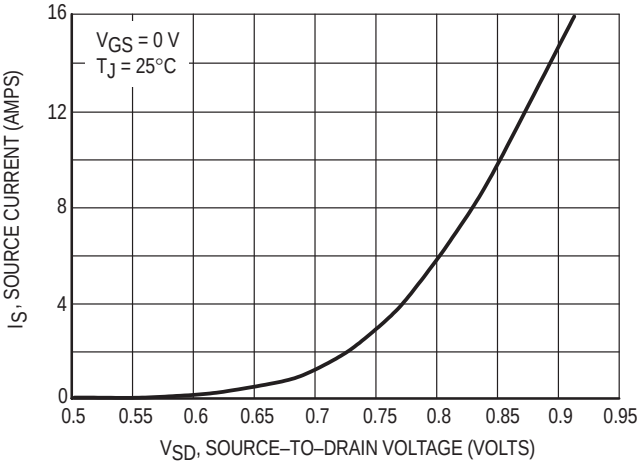


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

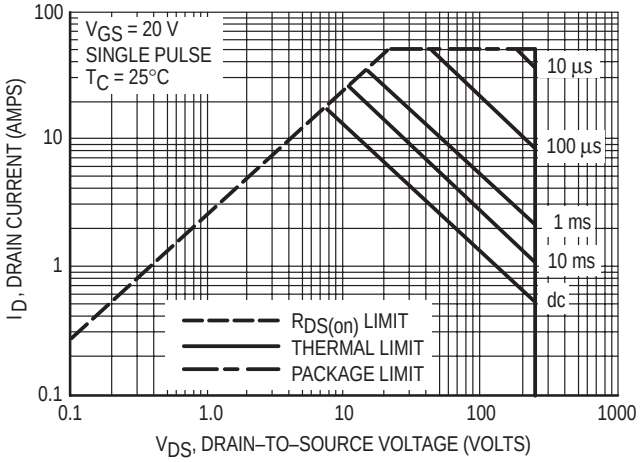


Figure 11. Maximum Rated Forward Biased Safe Operating Area

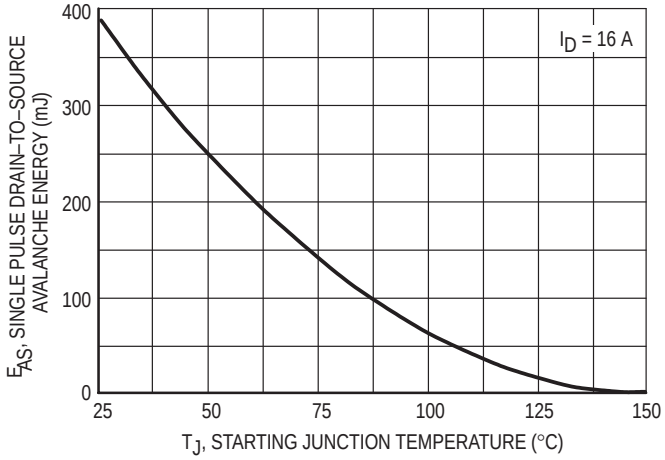


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

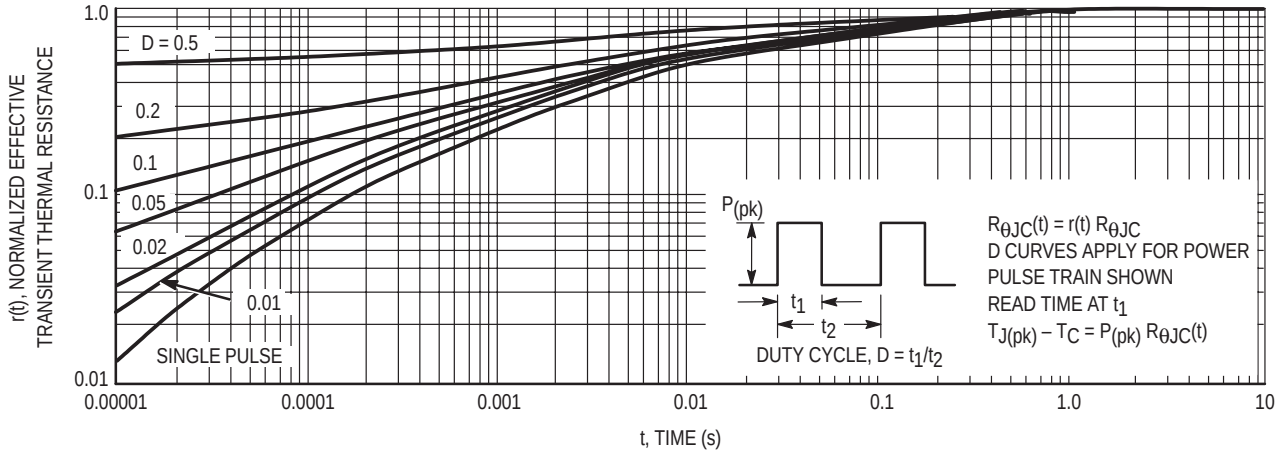


Figure 13. Thermal Response

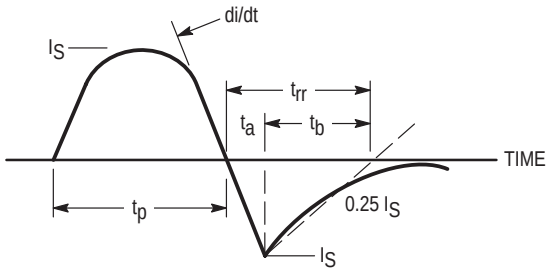


Figure 14. Diode Reverse Recovery Waveform

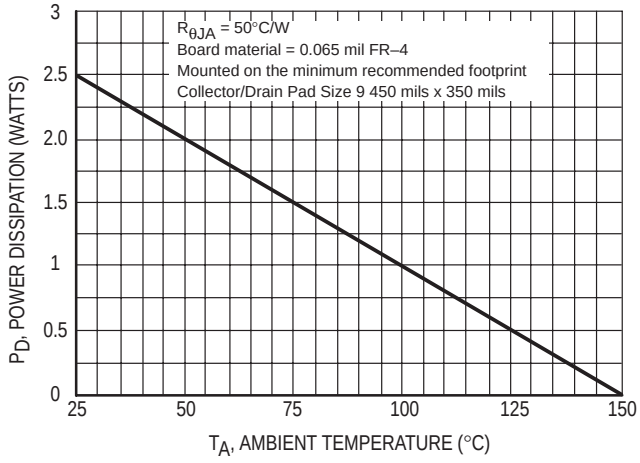


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

TMOS E-FET™
High Energy Power FET
D²PAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

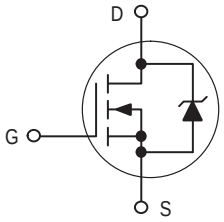
MTB20N20E

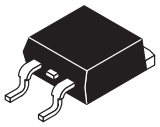
Motorola Preferred Device

TMOS POWER FET
20 AMPERES
200 VOLTS
$R_{DS(on)}$ = 0.16 OHM

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	200	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	20 12 60	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted with the minimum recommended pad size	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 20 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	600	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	200 —	— 263	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	— 7.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$R_{DS(on)}$	—	0.12	0.16	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 20 Adc) (I_D = 10 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	3.84 3.36	Vdc
Forward Transconductance (V_{DS} = 13 Vdc, I_D = 10 Adc)		g_{FS}	8.0	11	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1880	2700	pF
Output Capacitance		C_{oss}	—	378	535	
Reverse Transfer Capacitance		C_{rss}	—	68	100	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 100 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	17	40	ns
Rise Time		t_r	—	86	180	
Turn–Off Delay Time		$t_{d(off)}$	—	50	100	
Fall Time		t_f	—	60	120	
Gate Charge (See Figure 8)	(V_{DS} = 160 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc)	Q_T	—	54	75	nC
		Q_1	—	12	—	
		Q_2	—	24	—	
		Q_3	—	22	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 20 Adc, V_{GS} = 0 Vdc) (I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	1.0 0.82	1.35 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 20 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	239	—	ns
		t_a	—	136	—	
		t_b	—	103	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.09	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
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TYPICAL ELECTRICAL CHARACTERISTICS

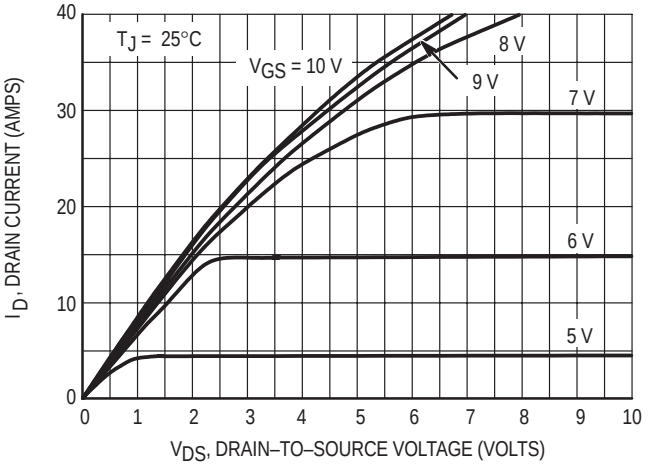
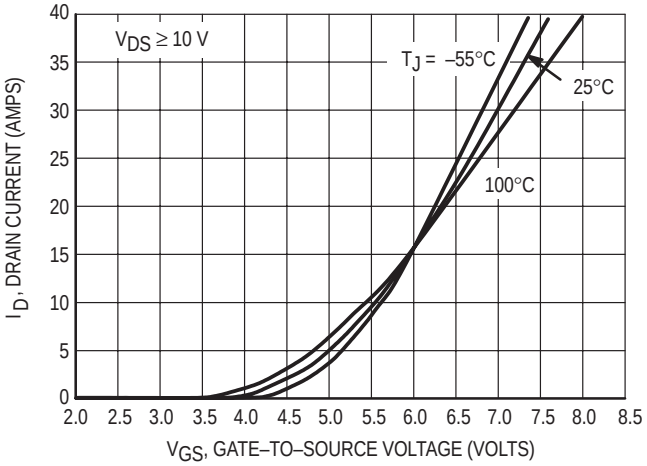


Figure 1. On–Region Characteristics



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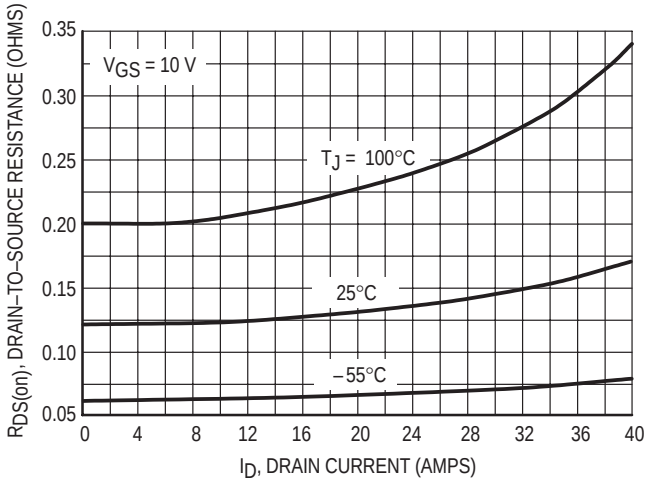

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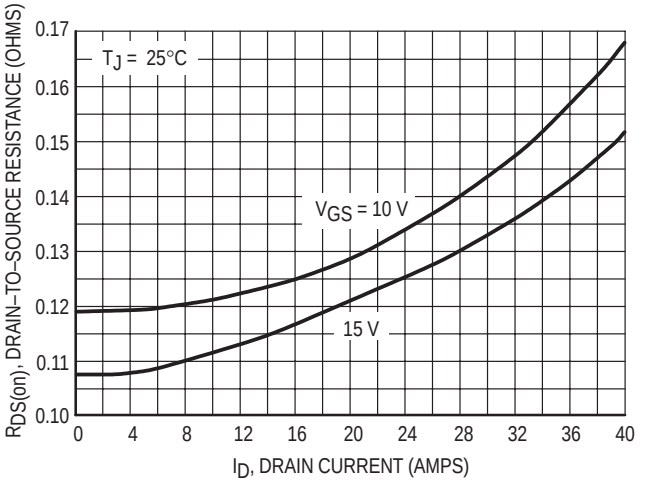

Figure 4. On–Resistance versus Drain Current and Gate Voltage

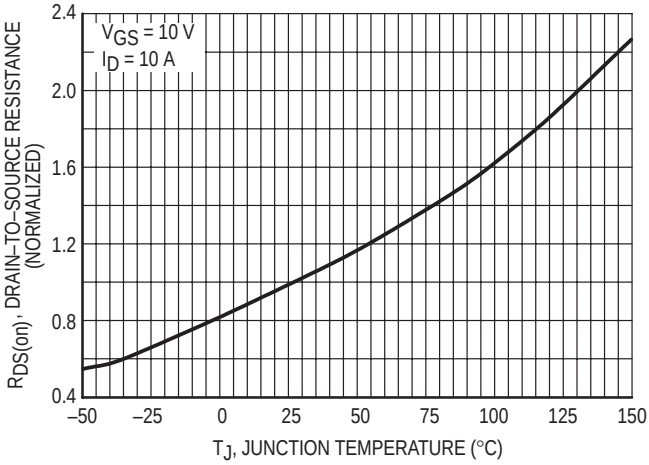

Figure 5. On–Resistance Variation with Temperature

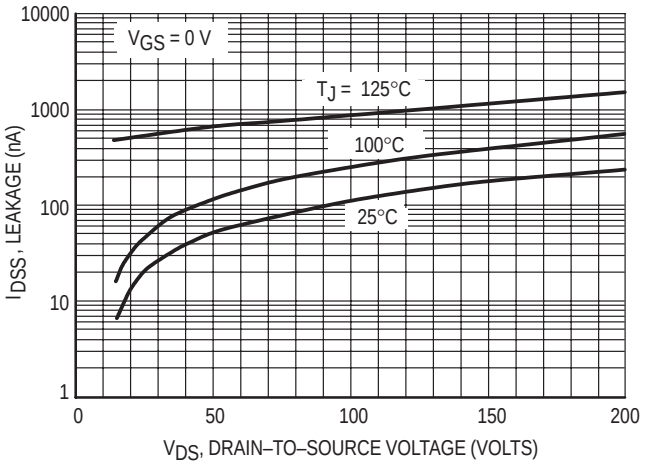

Figure 6. Drain–To–Source Leakage Current versus Voltage

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During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

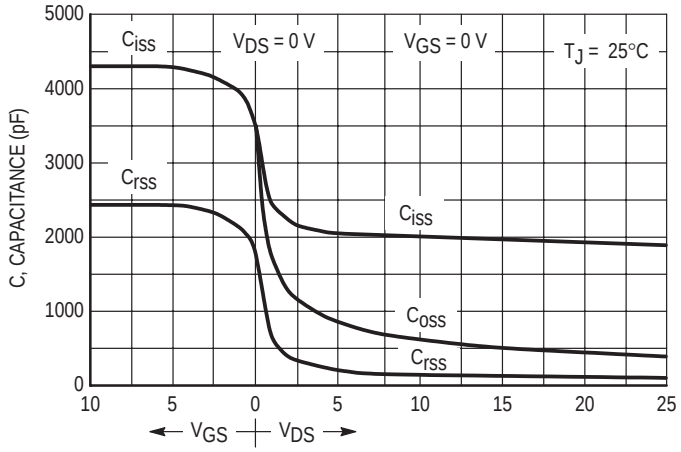


Figure 7. Capacitance Variation

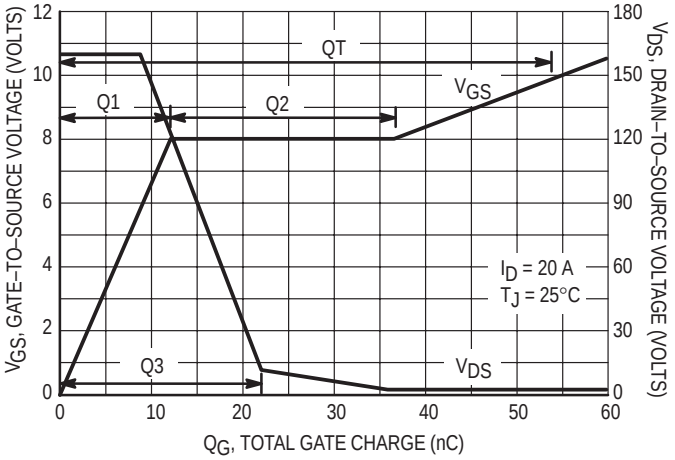


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

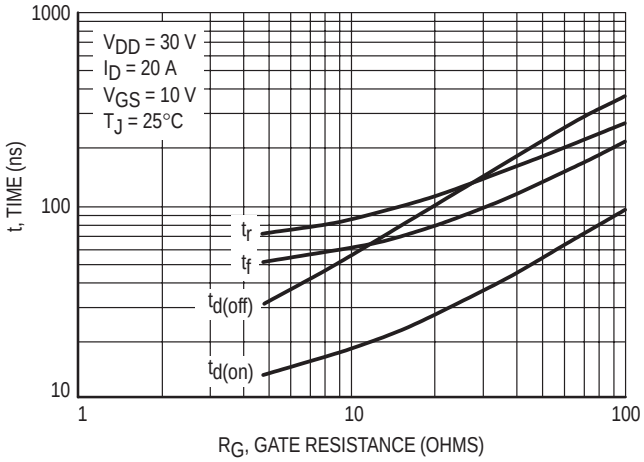


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

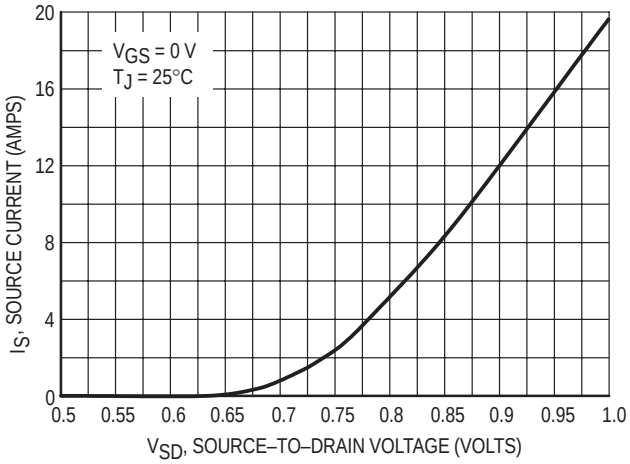


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

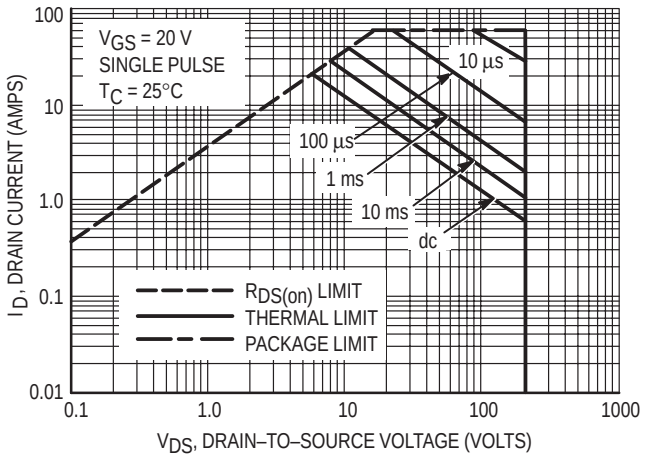


Figure 11. Maximum Rated Forward Biased Safe Operating Area

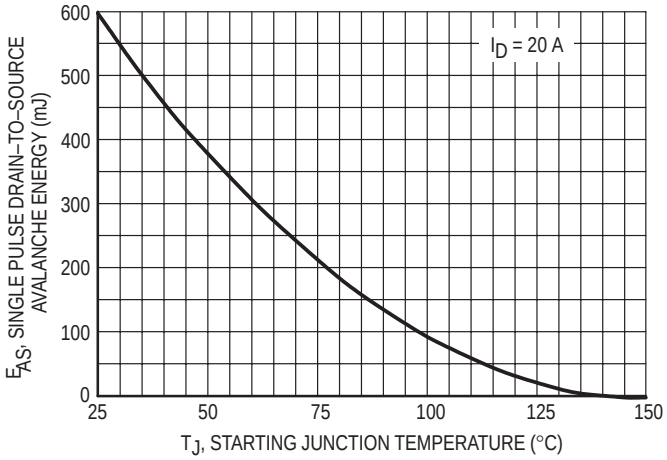


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

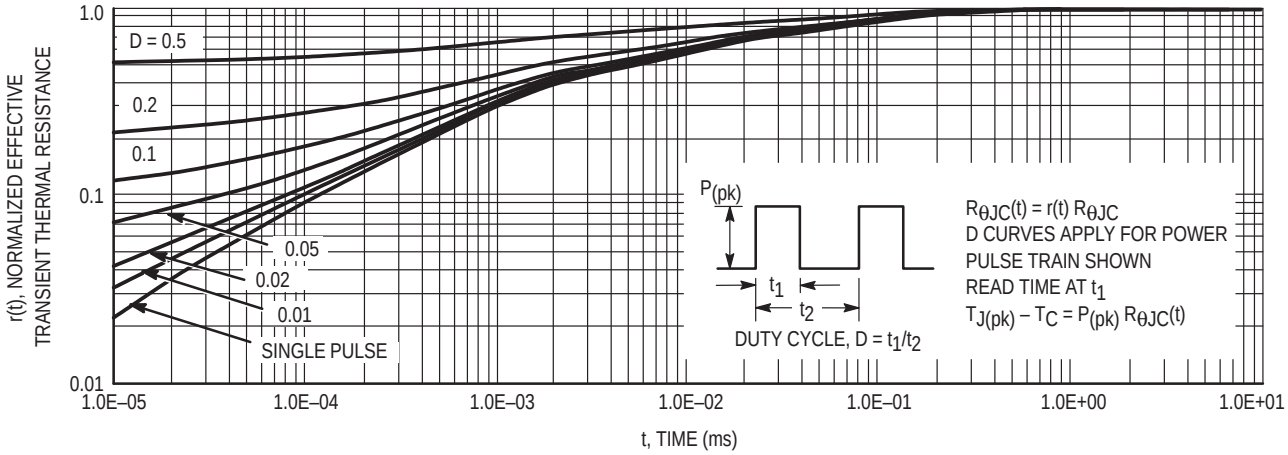


Figure 13. Thermal Response

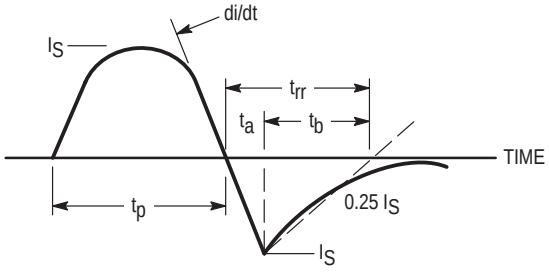


Figure 14. Diode Reverse Recovery Waveform

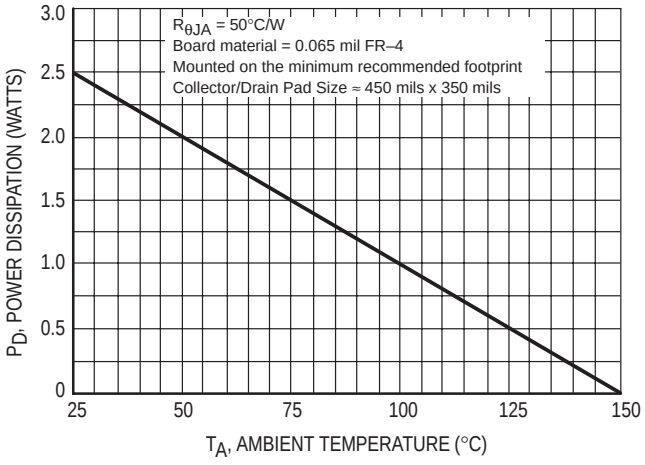


Figure 15. D²PAK Power Derating Curve

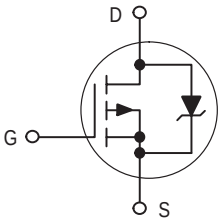
Designer's™ Data Sheet

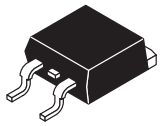
TMOS V™
Power Field Effect Transistor
D²PAK for Surface Mount
P–Channel Enhancement–Mode Silicon Gate

MTB23P06V
Motorola Preferred Device

TMOS POWER FET
23 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.120 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 418B–02, Style 2
D²PAK

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	23 15 81	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	90 0.60 3.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, PEAK I_L = 23 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	794	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.67 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	60.5	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.8	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	5.3	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 11.5 Adc)		$R_{DS(on)}$	—	0.093	0.12	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 23 Adc)		$V_{DS(on)}$	—	2.1	3.3	Vdc
(V_{GS} = 10 Vdc, I_D = 11.5 Adc, T_J = 150°C)			—	—	3.2	
Forward Transconductance (V_{DS} = 10.9 Vdc, I_D = 11.5 Adc)		g_{FS}	5.0	11.5	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1160	1620	pF
Output Capacitance		C_{oss}	—	380	530	
Transfer Capacitance		C_{rss}	—	105	210	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 23 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	13.8	30	ns
Rise Time		t_r	—	98.3	200	
Turn–Off Delay Time		$t_{d(off)}$	—	41	80	
Fall Time		t_f	—	62	120	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 23 Adc, V_{GS} = 10 Vdc)	Q_T	—	38	50	nC
		Q_1	—	7.0	—	
		Q_2	—	18	—	
		Q_3	—	14	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 23 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	2.2	3.5	Vdc
	(I_S = 23 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	1.8	—	
Reverse Recovery Time	(I_S = 23 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	142	—	ns
		t_a	—	100	—	
		t_b	—	41	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.804	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)				4.5		
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

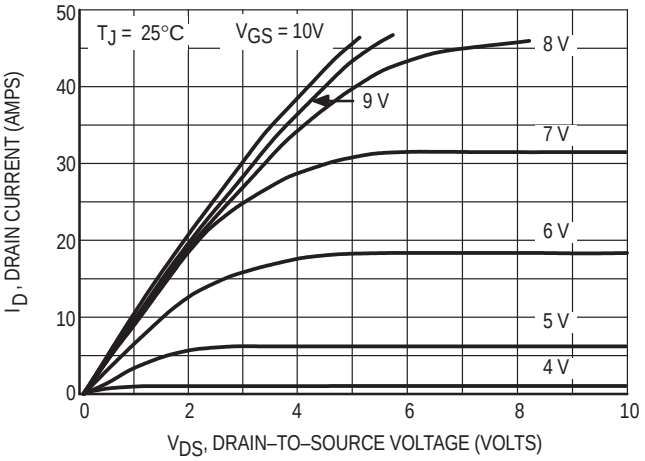


Figure 1. On–Region Characteristics

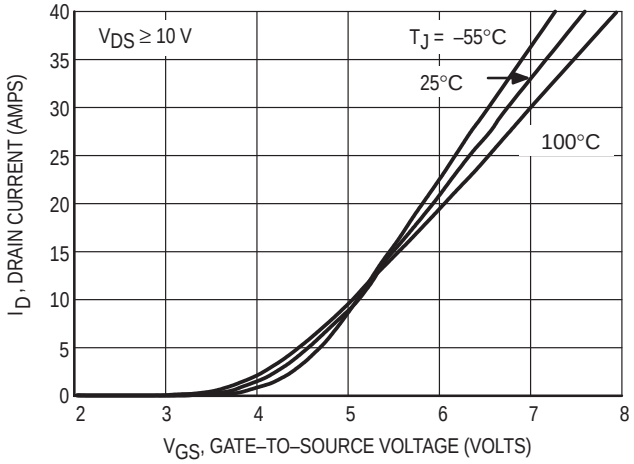


Figure 2. Transfer Characteristics

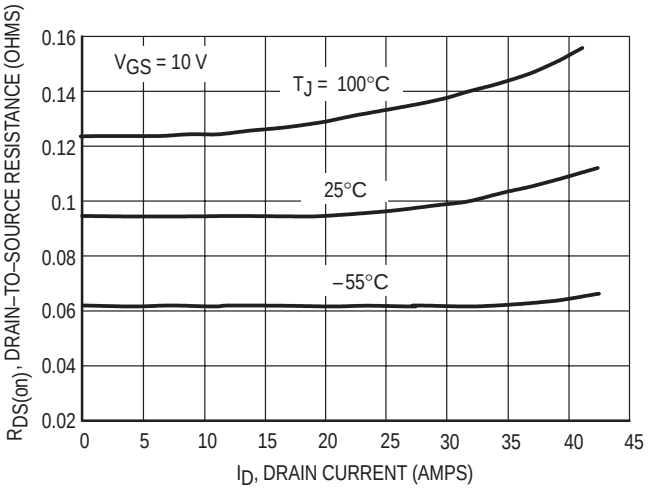


Figure 3. On–Resistance versus Drain Current and Temperature

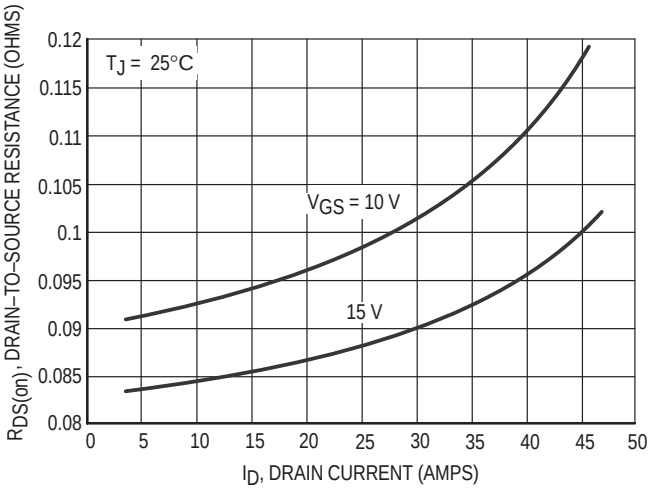


Figure 4. On–Resistance versus Drain Current and Gate Voltage

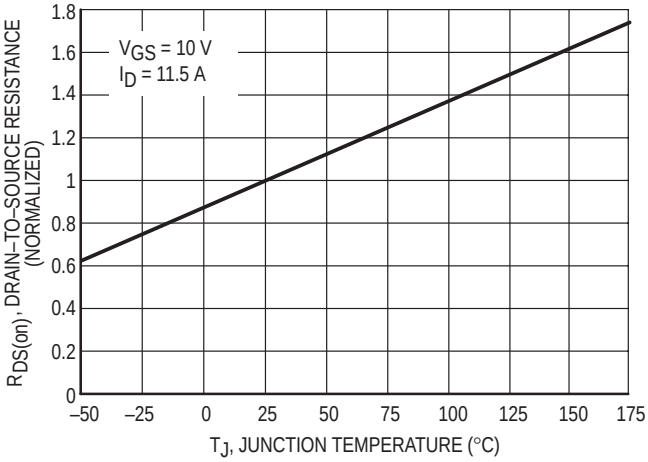


Figure 5. On–Resistance Variation with Temperature

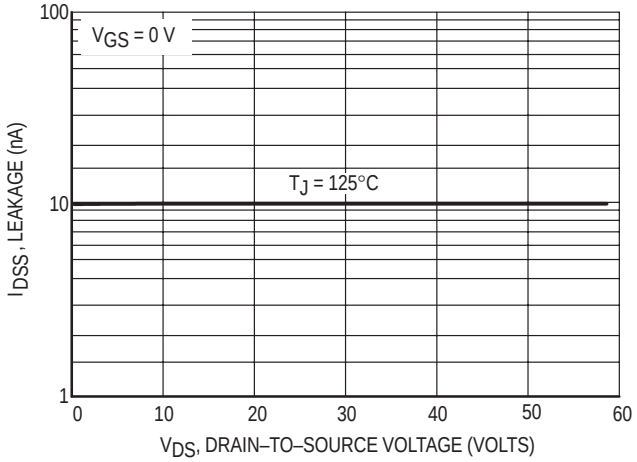


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

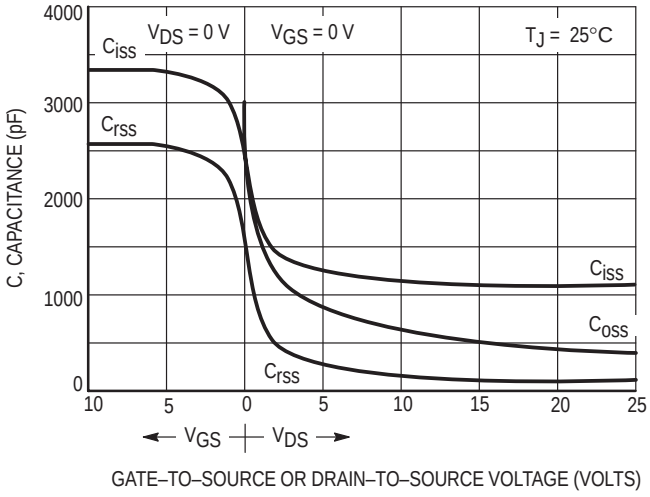
$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.



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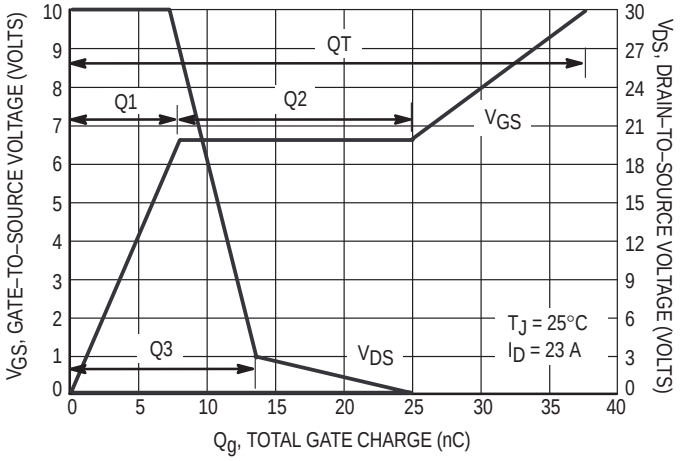

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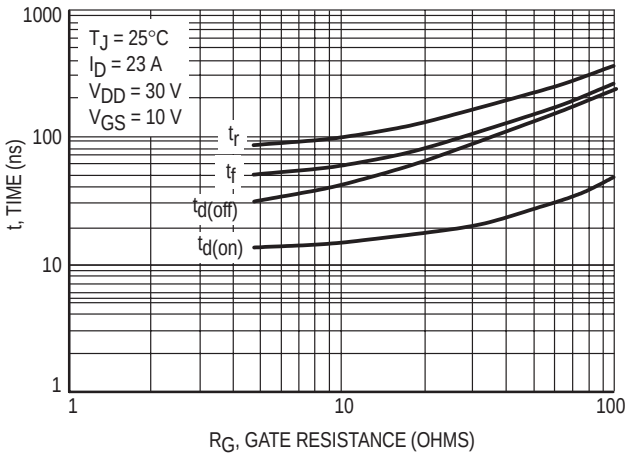

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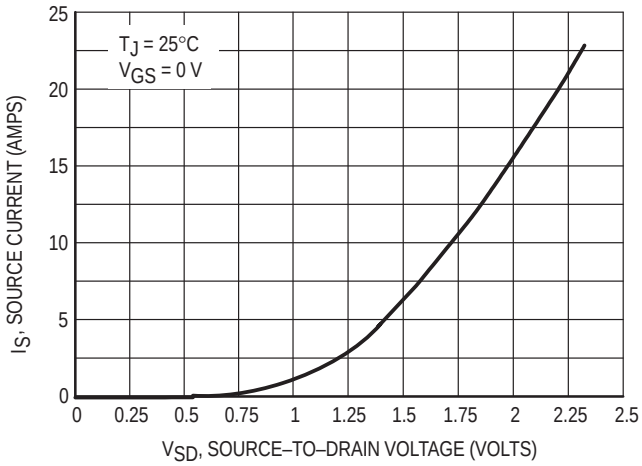
DRAIN–TO–SOURCE DIODE CHARACTERISTICS



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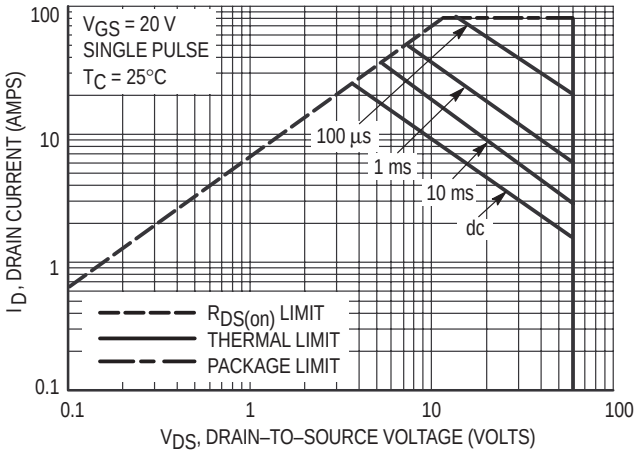

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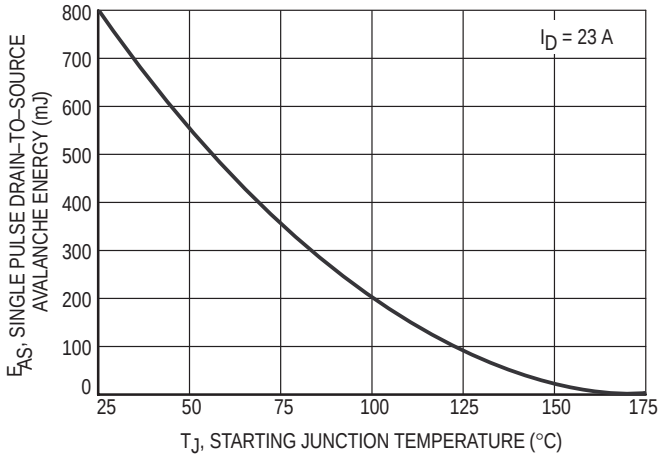


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

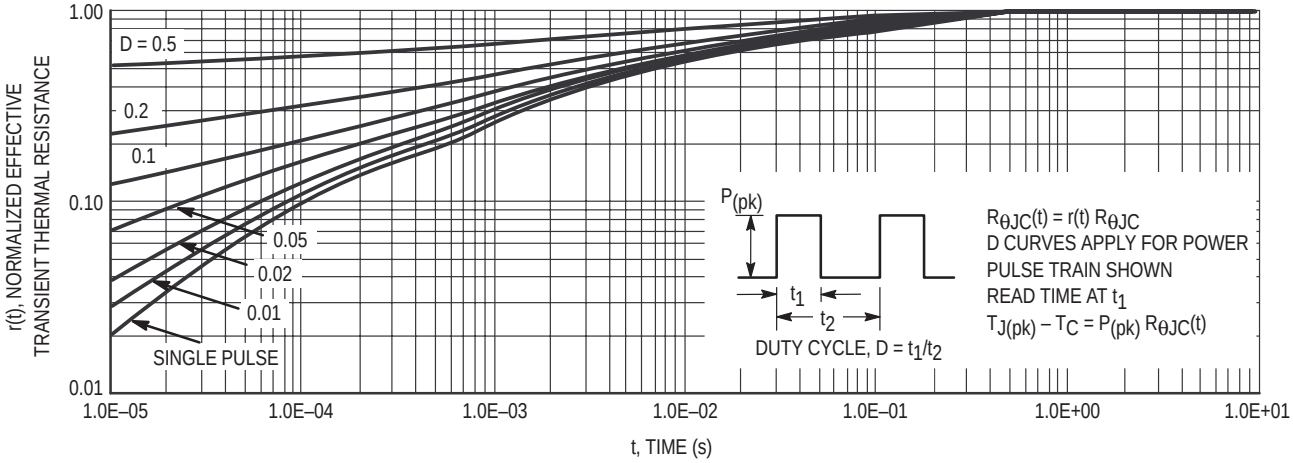


Figure 13. Thermal Response

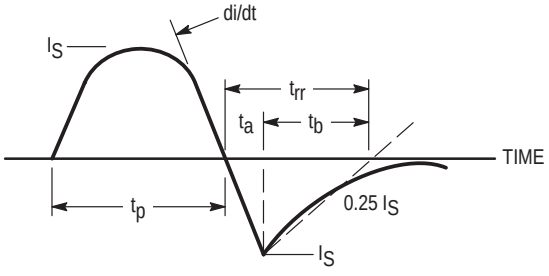


Figure 14. Diode Reverse Recovery Waveform

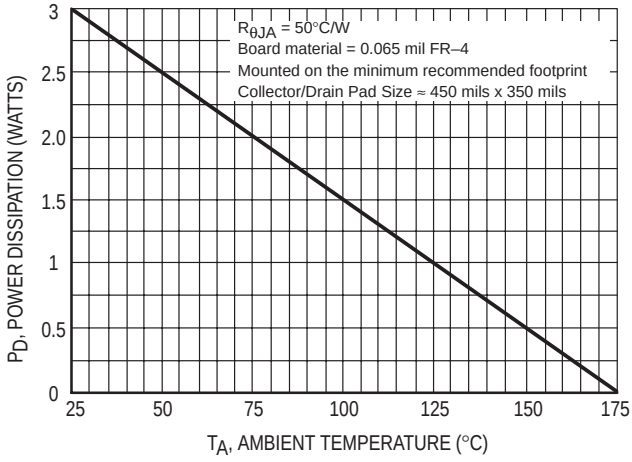


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

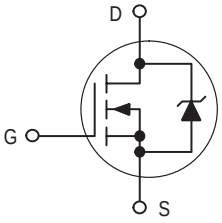
TMOS V™
Power Field Effect Transistor
D²PAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

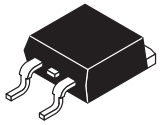
MTB30N06VL

Motorola Preferred Device

TMOS POWER FET
30 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.050 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 418B–02, Style 2
D²PAK

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETs
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±15 ±20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	30 20 105	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	90 0.6 3.0	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5 Vdc, PEAK I_L = 30 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	154	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.67 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 3

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	63	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Threshold Temperature Coefficient (Negative)			—	4.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 5 Vdc, I_D = 15 Adc)		$R_{DS(on)}$	—	0.033	0.05	Ohms
Drain–to–Source On–Voltage (V_{GS} = 5 Vdc, I_D = 30 Adc)		$V_{DS(on)}$	—	1.1	1.8	Vdc
(V_{GS} = 5 Vdc, I_D = 15 Adc, T_J = 150°C)			—	—	1.73	
Forward Transconductance (V_{DS} = 6.25 Vdc, I_D = 15 Adc)		g_{FS}	13	21	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1130	1580	pF
Output Capacitance		C_{oss}	—	360	500	
Transfer Capacitance		C_{rss}	—	95	190	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 30 Adc, V_{GS} = 5 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	14	30	ns
Rise Time		t_r	—	260	520	
Turn–Off Delay Time		$t_{d(off)}$	—	54	110	
Fall Time		t_f	—	108	220	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 30 Adc, V_{GS} = 5 Vdc)	Q_T	—	27	40	nC
		Q_1	—	5	—	
		Q_2	—	17	—	
		Q_3	—	15	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 30 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.98	1.6	Vdc
	(I_S = 30 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.89	—	
Reverse Recovery Time	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	86	—	ns
		t_a	—	49	—	
		t_b	—	37	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.228	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

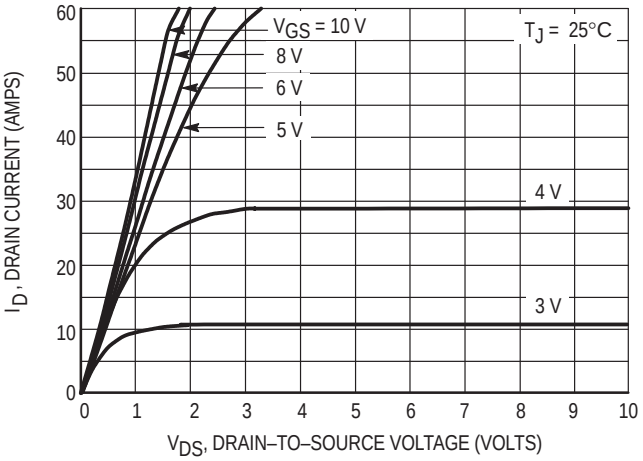


Figure 1. On–Region Characteristics

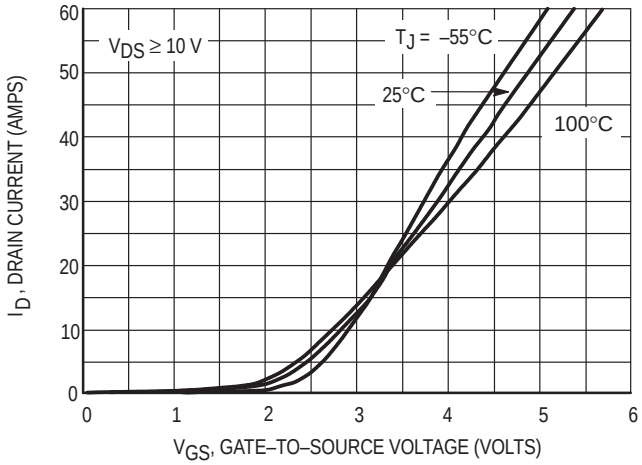


Figure 2. Transfer Characteristics

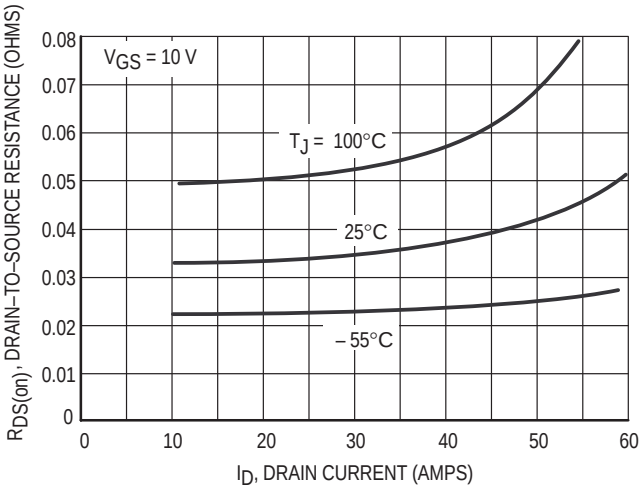


Figure 3. On–Resistance versus Drain Current and Temperature

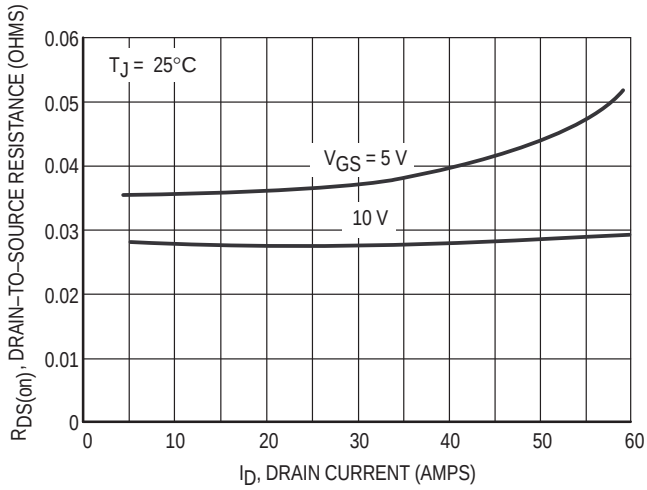


Figure 4. On–Resistance versus Drain Current and Gate Voltage

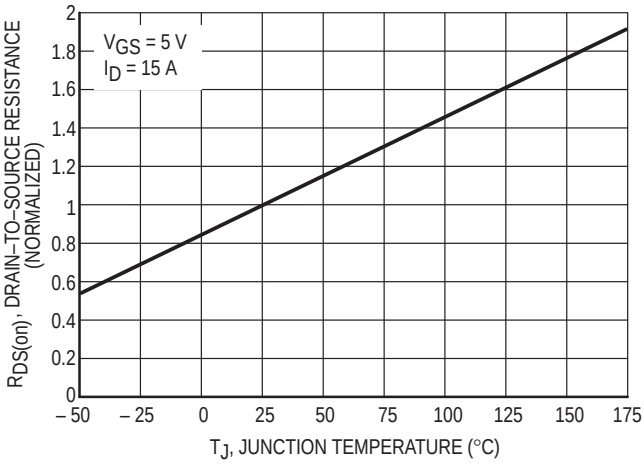


Figure 5. On–Resistance Variation with Temperature

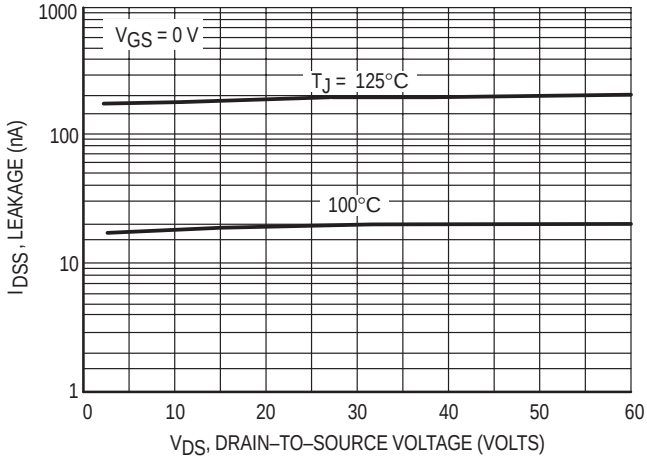


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

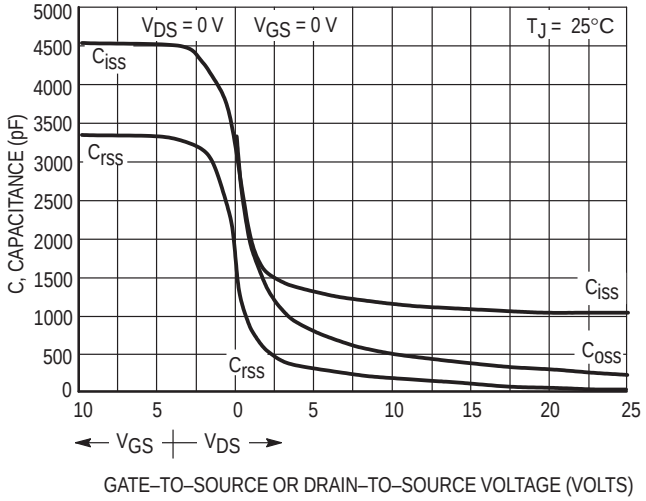


Figure 7. Capacitance Variation

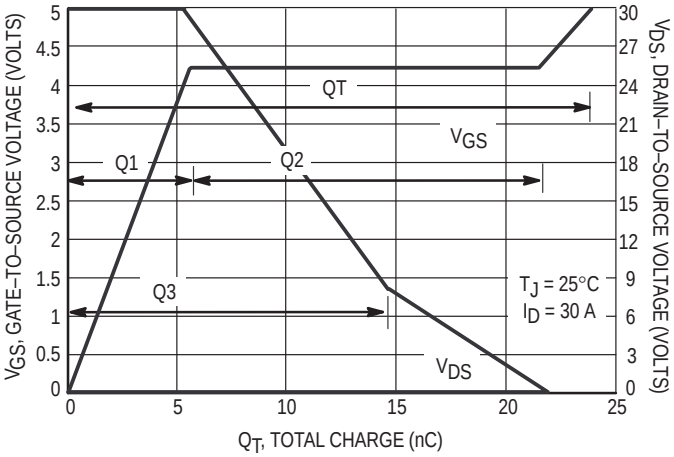


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

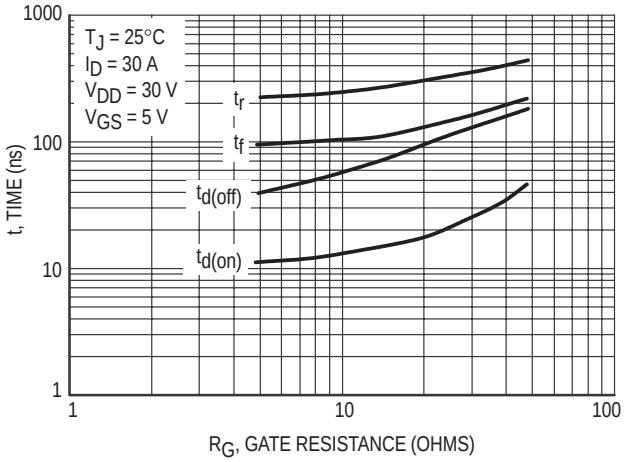


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

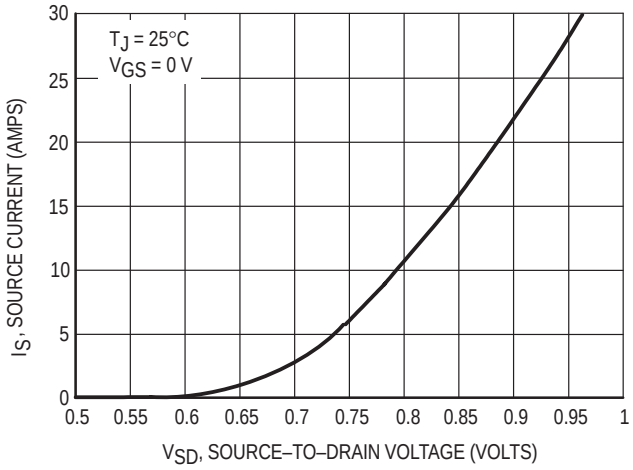


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

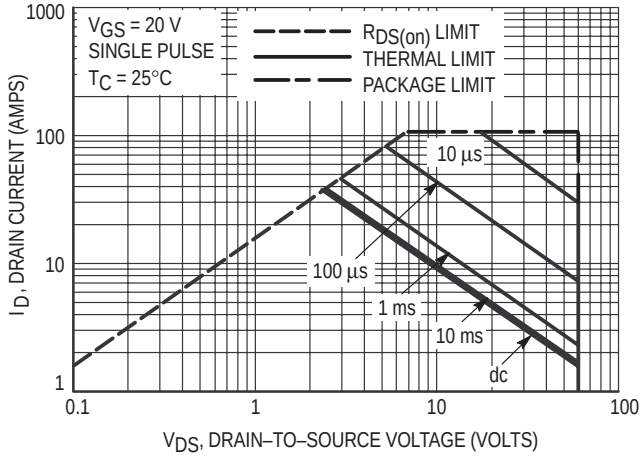
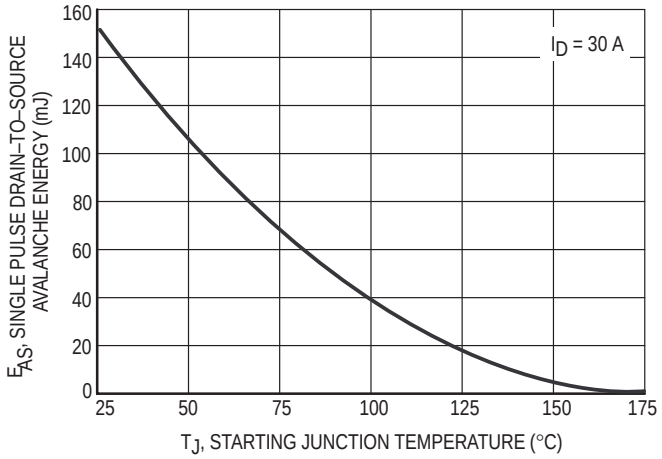


Figure 11. Maximum Rated Forward Biased Safe Operating Area



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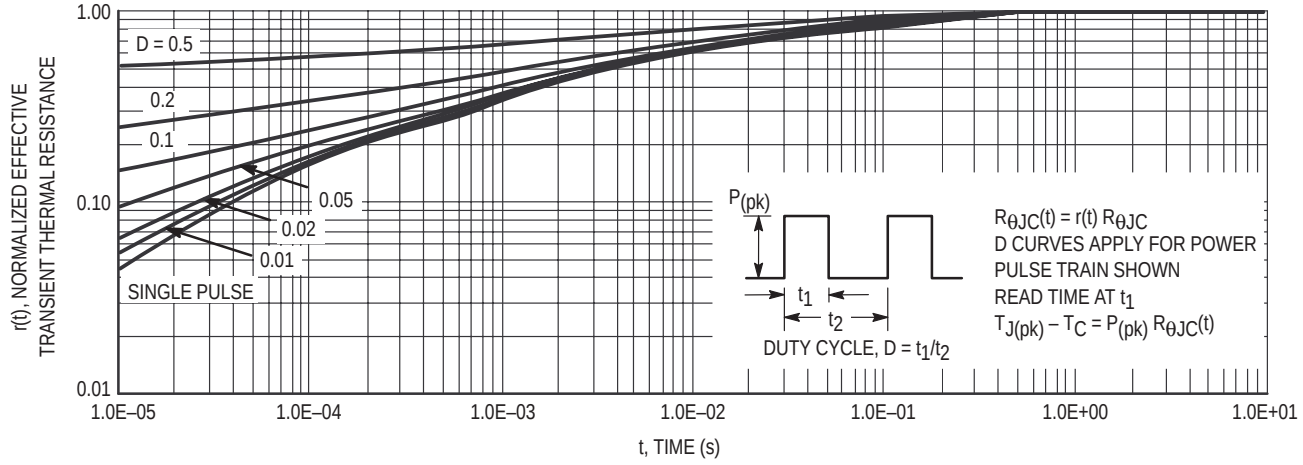

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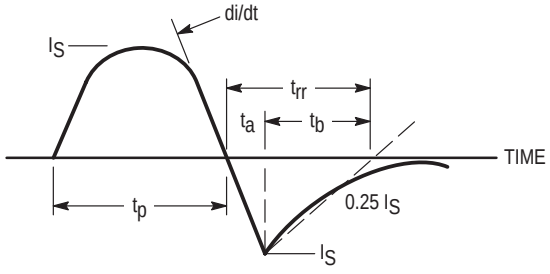

Figure 14. Diode Reverse Recovery Waveform

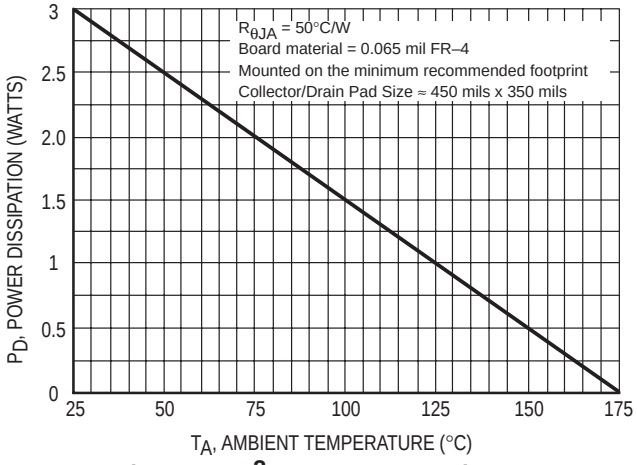

Figure 15. D²PAK Power Derating Curve

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TMOS V™
Power Field Effect Transistor
D²PAK for Surface Mount
P–Channel Enhancement–Mode Silicon Gate

MTB30P06V

Motorola Preferred Device

TMOS POWER FET
30 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.080 OHM

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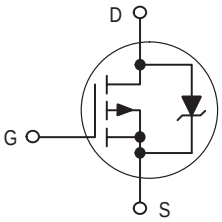
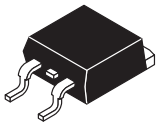




CASE 418B–02, Style 2
D²PAK

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	30 19 105	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	125 0.83 3.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, PEAK I_L = 30 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	450	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.2 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	62	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.6	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	5.3	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)		$R_{DS(on)}$	—	0.067	0.08	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 30 Adc)		$V_{DS(on)}$	—	2.0	2.9	Vdc
(V_{GS} = 10 Vdc, I_D = 15 Adc, T_J = 150°C)			—	—	2.8	
Forward Transconductance (V_{DS} = 8.3 Vdc, I_D = 15 Adc)		g_{FS}	5.0	7.9	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1562	2190	pF
Output Capacitance		C_{oss}	—	524	730	
Transfer Capacitance		C_{rss}	—	154	310	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 30 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	14.7	30	ns
Rise Time		t_r	—	25.9	50	
Turn–Off Delay Time		$t_{d(off)}$	—	98	200	
Fall Time		t_f	—	52.4	100	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 30 Adc, V_{GS} = 10 Vdc)	Q_T	—	54	80	nC
		Q_1	—	9.0	—	
		Q_2	—	26	—	
		Q_3	—	20	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 30 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	2.3	3.0	Vdc
	(I_S = 30 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	1.9	—	
Reverse Recovery Time	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	175	—	ns
		t_a	—	107	—	
		t_b	—	68	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.965	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)				4.5		
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

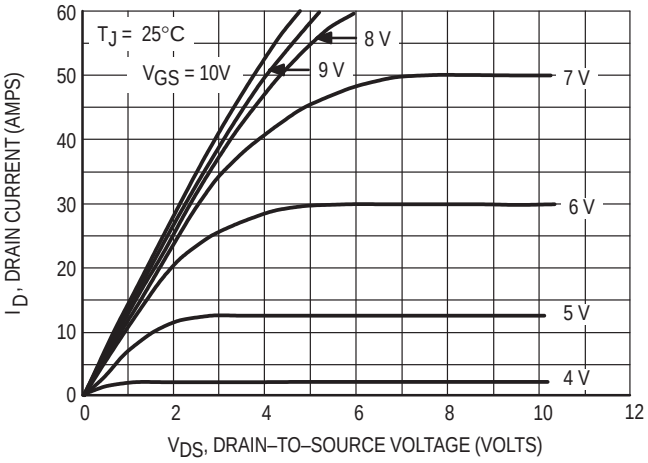


Figure 1. On–Region Characteristics

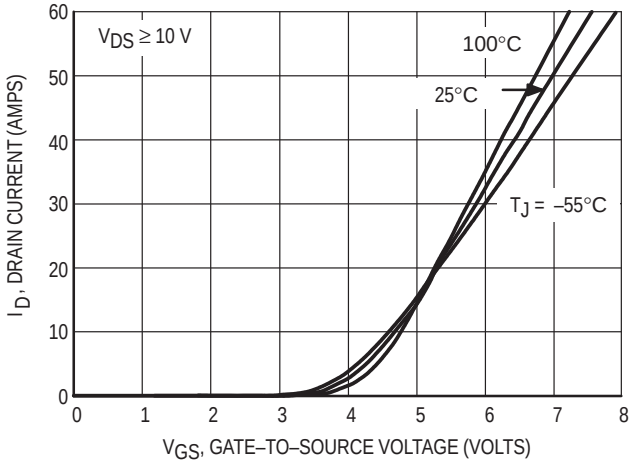


Figure 2. Transfer Characteristics

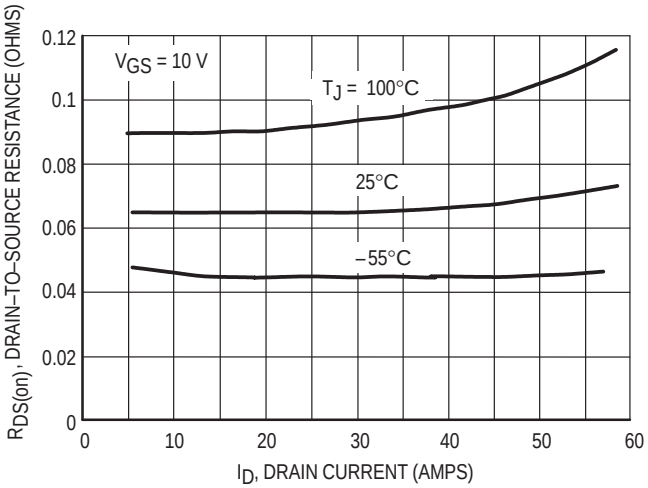


Figure 3. On–Resistance versus Drain Current and Temperature

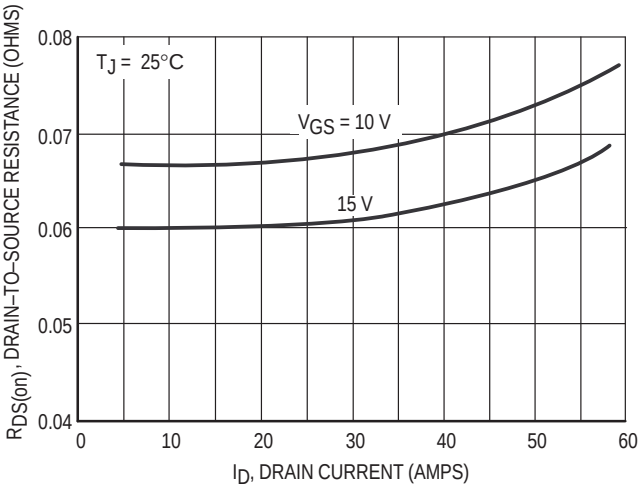


Figure 4. On–Resistance versus Drain Current and Gate Voltage

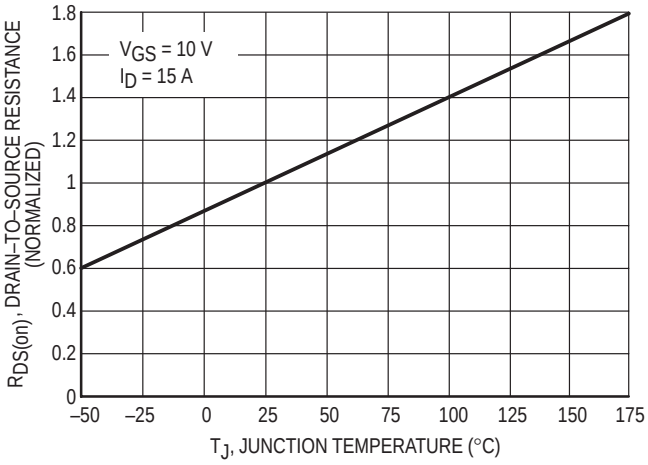


Figure 5. On–Resistance Variation with Temperature

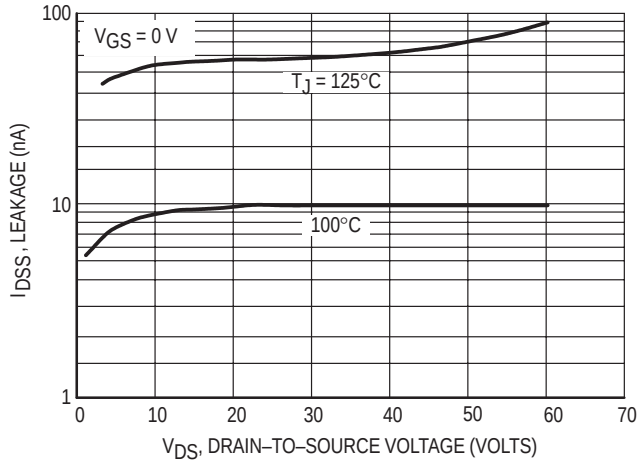


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

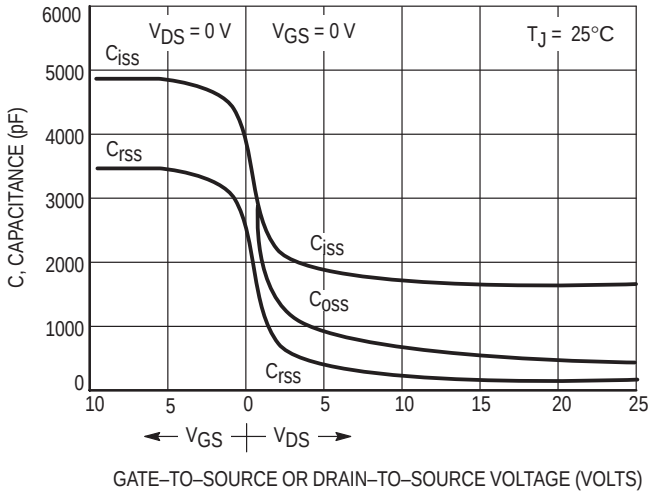


Figure 7. Capacitance Variation

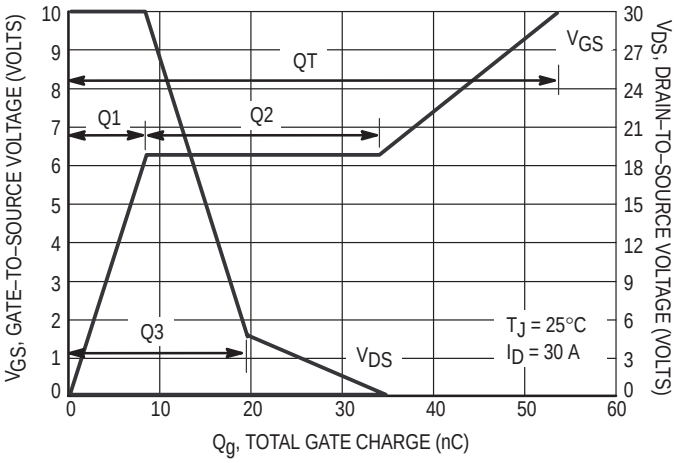


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

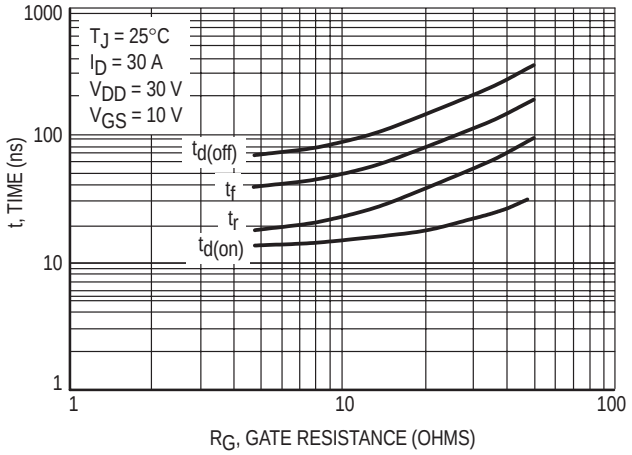


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

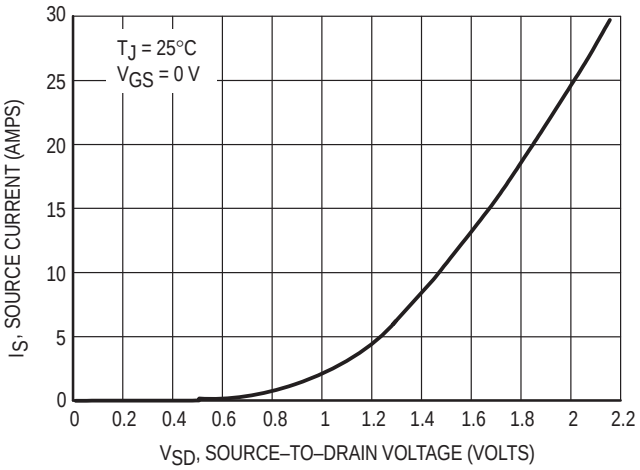


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

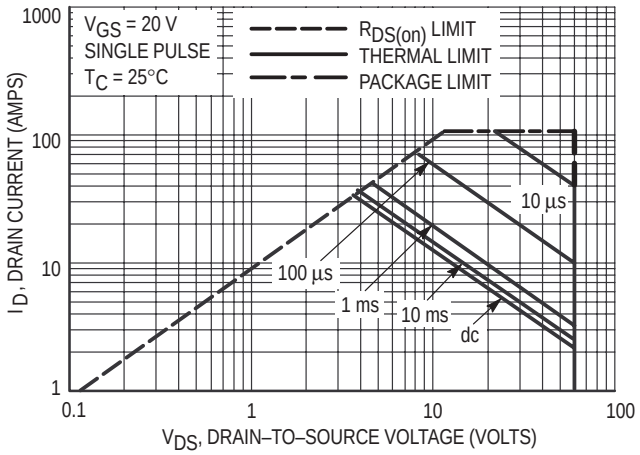


Figure 11. Maximum Rated Forward Biased Safe Operating Area

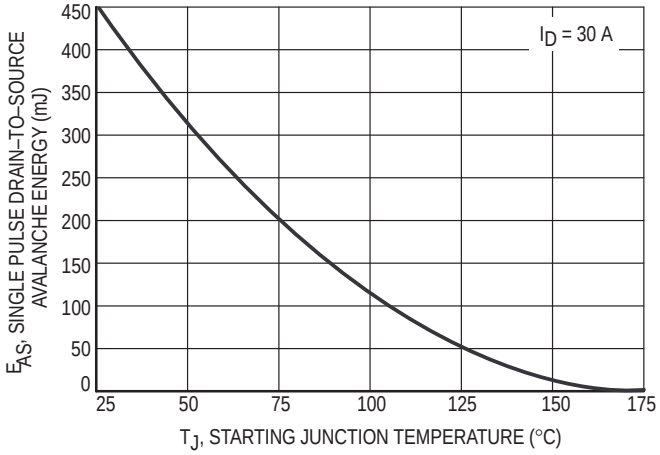


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

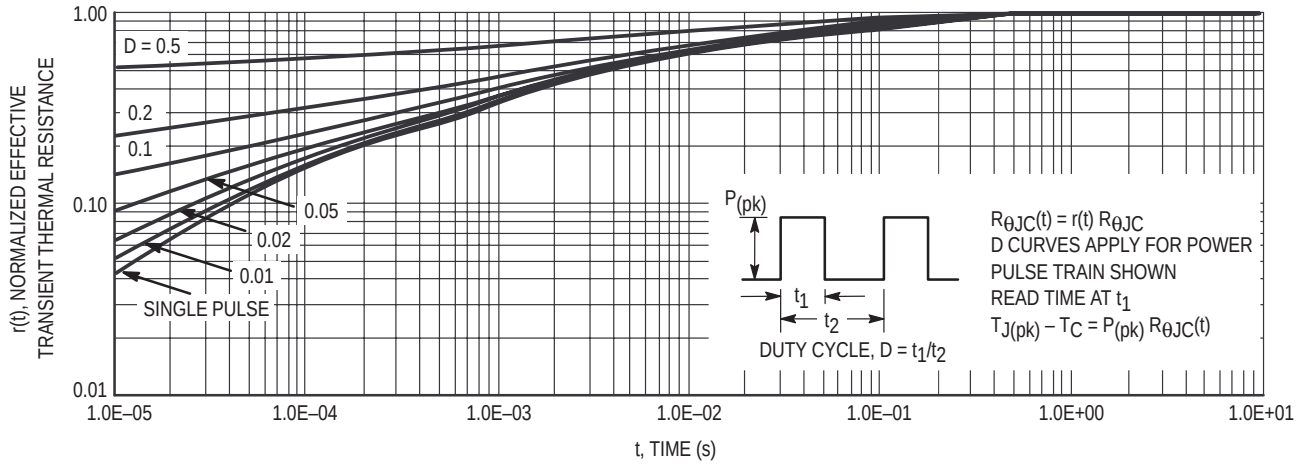


Figure 13. Thermal Response

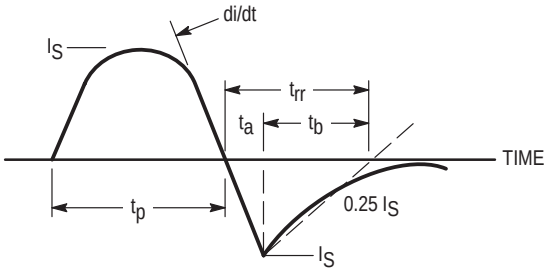


Figure 14. Diode Reverse Recovery Waveform

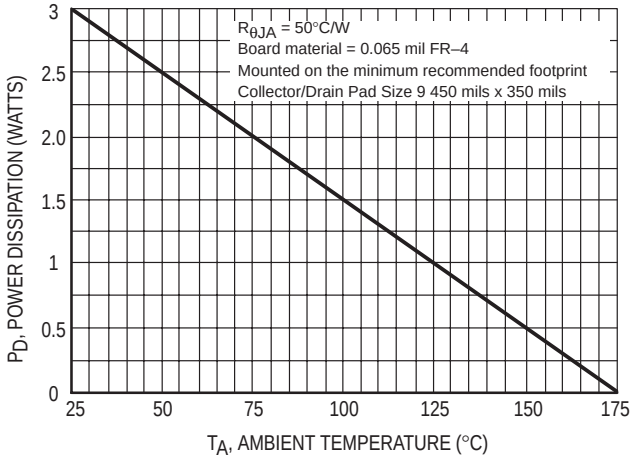


Figure 15. D^{2}PAK Power Derating Curve

Designer's™ Data Sheet

TMOS E-FET ™
High Energy Power FET
D²PAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

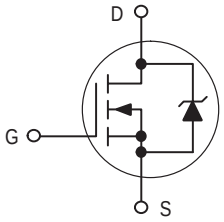
MTB33N10E

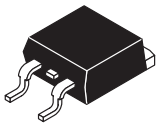
Motorola Preferred Device

TMOS POWER FET
33 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.06 OHM

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	100	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	33 20 99	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted with the minimum recommended pad size	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 33 Apk, L = 1.000 mH, R_G = 25 Ω)	E_{AS}	545	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	100 —	— 118	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = – 25°C)	I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)	$V_{GS(th)}$	2.0 —	— 7.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 16.5 Adc)	$R_{DS(on)}$	—	0.04	0.06	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 33 Adc) (I_D = 16.5 Adc, T_J = – 25°C)	$V_{DS(on)}$	— —	1.6 —	2.4 2.1	Vdc
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 16.5 Adc)	g_{FS}	8.0	—	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1830	2500	pF
Output Capacitance		C_{oss}	—	678	1200	
Reverse Transfer Capacitance		C_{rss}	—	559	1100	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 50 Vdc, I_D = 33 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	18	40	ns
Rise Time		t_r	—	164	330	
Turn–Off Delay Time		$t_{d(off)}$	—	48	100	
Fall Time		t_f	—	83	170	
Gate Charge (See Figure 8)	(V_{DS} = 80 Vdc, I_D = 33 Adc, V_{GS} = 10 Vdc)	Q_T	—	52	110	nC
		Q_1	—	12	—	
		Q_2	—	32	—	
		Q_3	—	24	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 33 Adc, V_{GS} = 0 Vdc) (I_S = 33 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	1.0 0.98	2.0 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 33 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	144	—	ns
		t_a	—	108	—	
		t_b	—	36	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.93	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

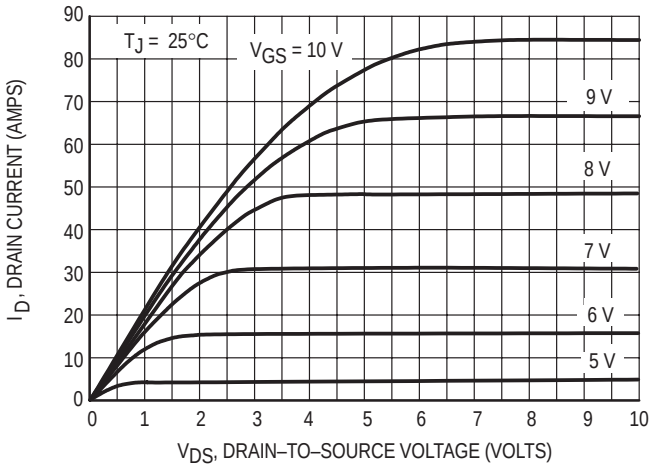


Figure 1. On–Region Characteristics

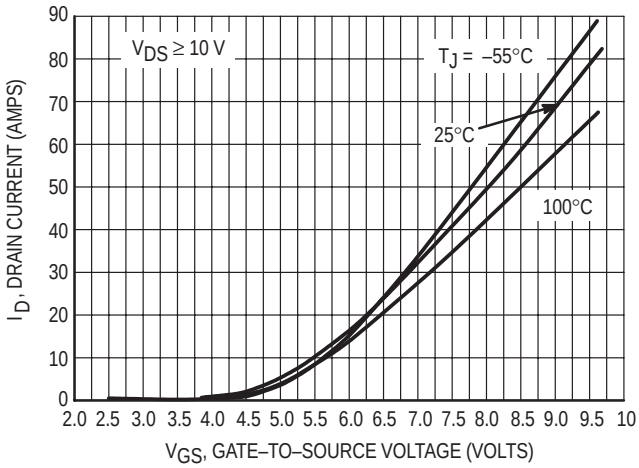


Figure 2. Transfer Characteristics

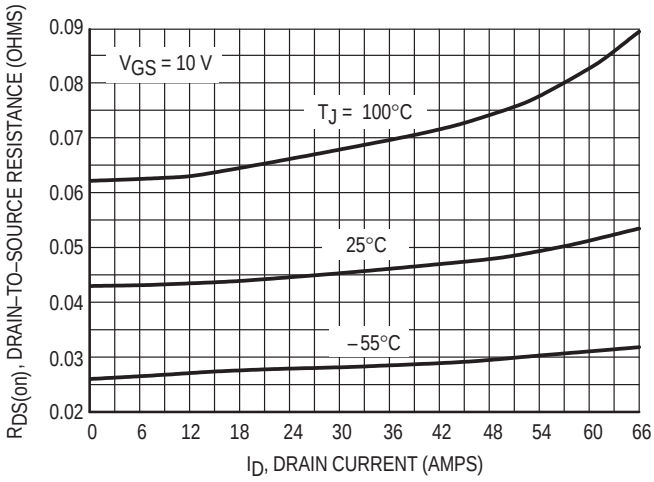


Figure 3. On–Resistance versus Drain Current and Temperature

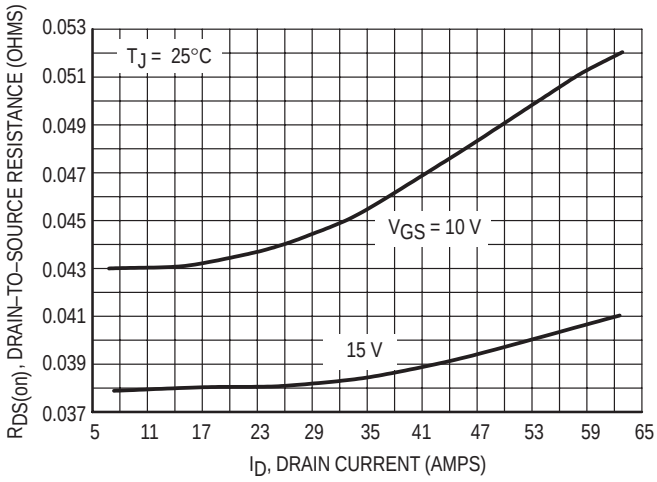


Figure 4. On–Resistance versus Drain Current and Gate Voltage

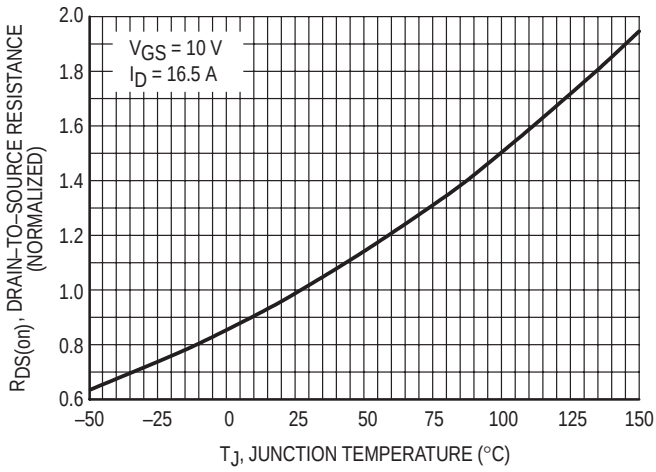


Figure 5. On–Resistance Variation with Temperature

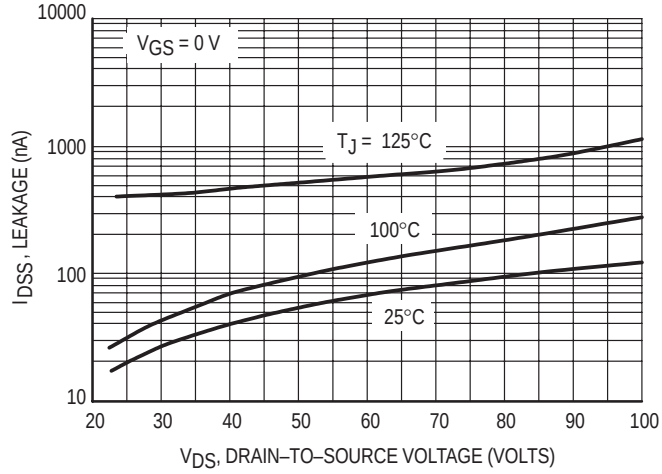


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

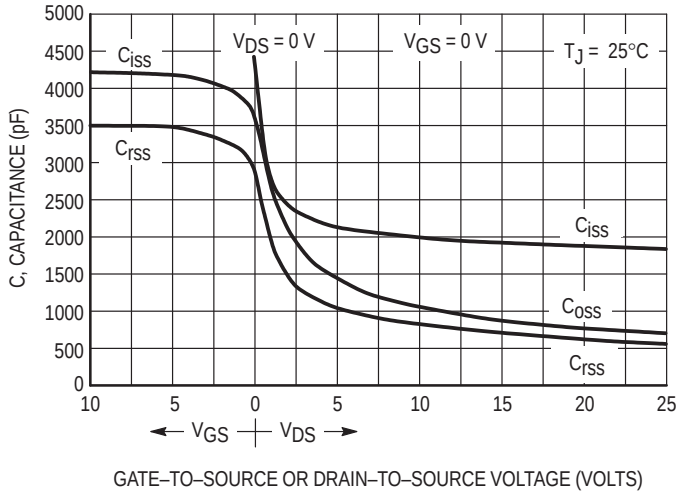


Figure 7. Capacitance Variation

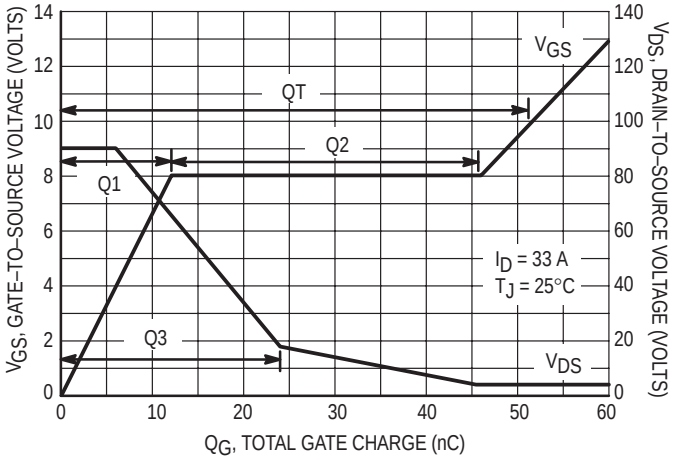


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

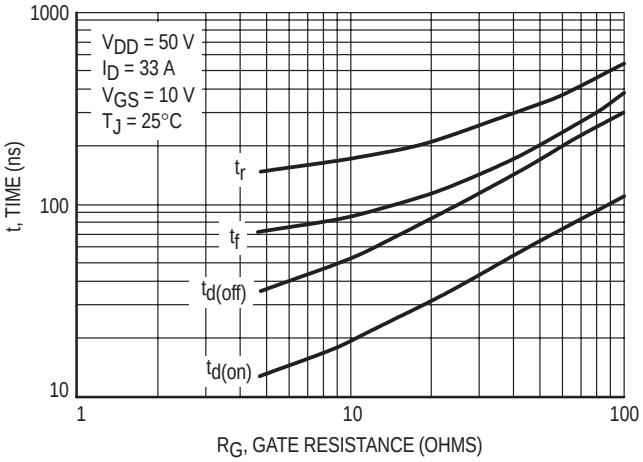


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

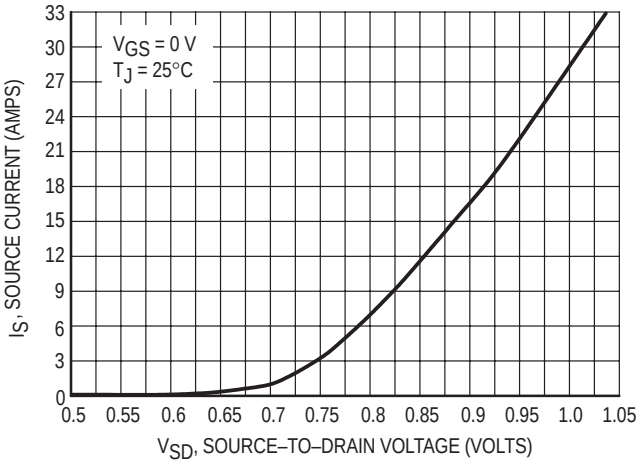


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

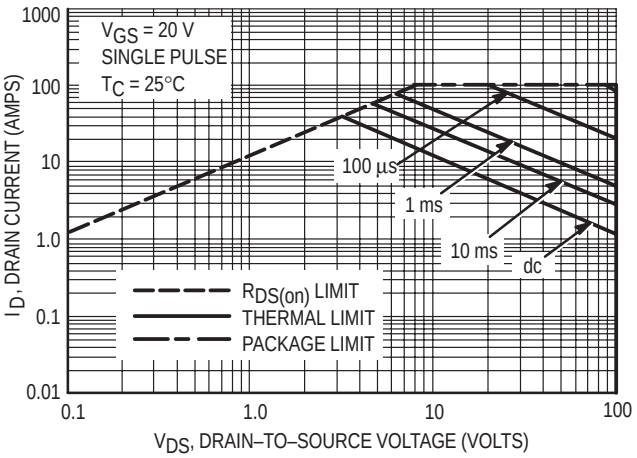


Figure 11. Maximum Rated Forward Biased Safe Operating Area

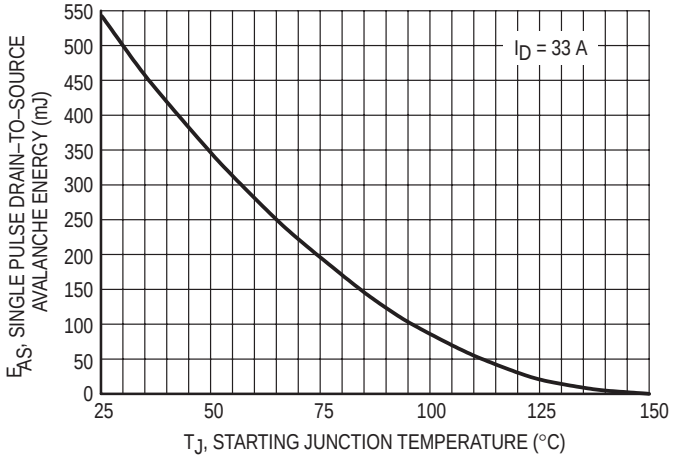


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

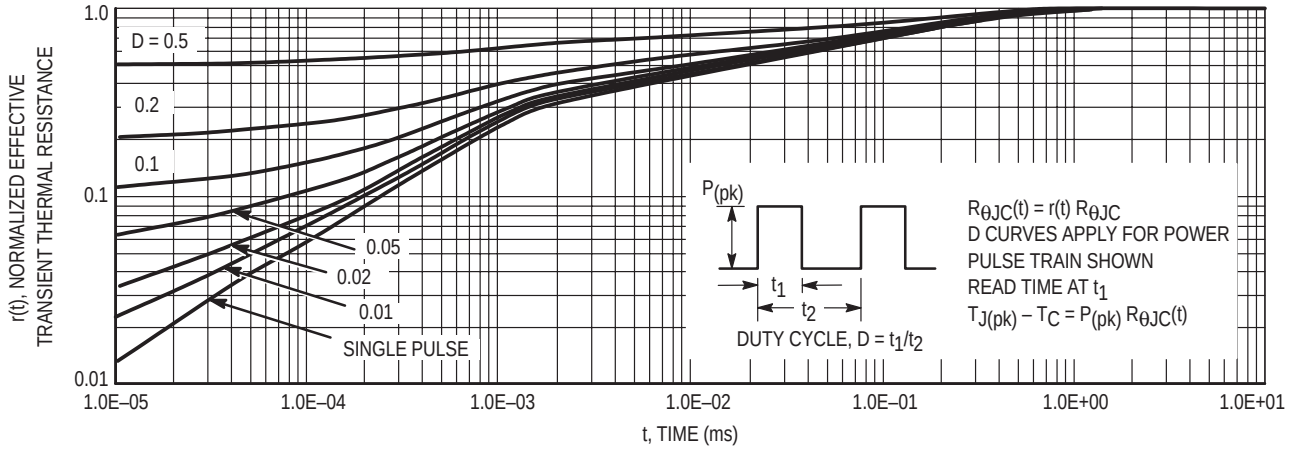


Figure 13. Thermal Response

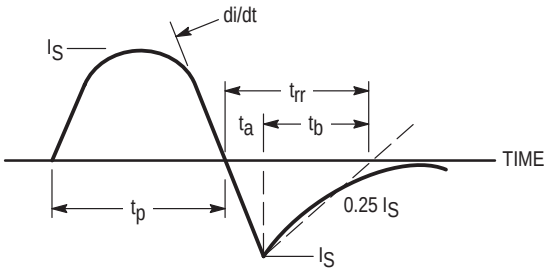


Figure 14. Diode Reverse Recovery Waveform

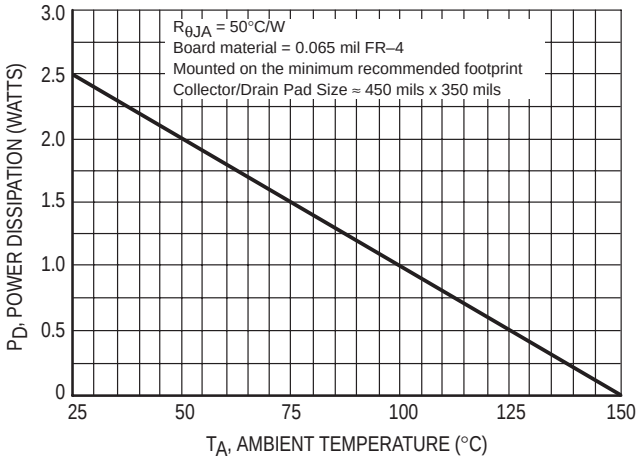


Figure 15. D²PAK Power Derating Curve

Product Preview

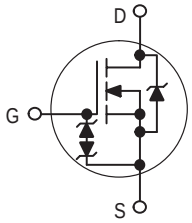
HDTMOS E-FET™
High Energy Power FET
D²PAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

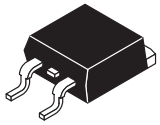
MTB35N06ZL

TMOS POWER FET
35 AMPERES
60 VOLTS
$R_{DS(on)}$ = 26 mΩ

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor–Absorbs High Energy in the Avalanche Mode
- ESD Protected. 400 V Machine Model Level and 4000 V Human Body Model Level.





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±15 ±20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	35 22.8 105	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	94 0.63 3.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{DS} = 60 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 35 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	184	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.6 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 3.0)		$V_{(BR)DSS}$	60	—	—	Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)			—	52	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	5.0	μAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (Cpk ≥ 3.0)		$V_{GS(th)}$	1.0	1.5	2.0	Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)			—	4.0	—	mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (V_{GS} = 5.0 Vdc, I_D = 11.5 Adc)		$R_{DS(on)}$	—	22	26	mΩ
Drain–to–Source On–Voltage (V_{GS} = 5.0 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 23 Adc)			—	0.78	1.1	
(I_D = 11.5 Adc, T_J = 125°C)			—	0.7	1.0	
Forward Transconductance (V_{DS} = 4.0 Vdc, I_D = 11.5 Adc)		g_{FS}	10	12	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1600	—	pF
Output Capacitance		C_{oss}	—	560	—	
Transfer Capacitance		C_{rss}	—	140	—	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 23 Adc, $V_{GS(on)}$ = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	40		ns
Rise Time		t_r	—	250		
Turn–Off Delay Time		$t_{d(off)}$	—	130		
Fall Time		t_f	—	170		
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 23 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	45		nC
		Q_1	—	8.0	—	
		Q_2	—	22	—	
		Q_3	—	19	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 23 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.92	1.1	Vdc
	(I_S = 23 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.81	—	
Reverse Recovery Time	(I_S = 23 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	43	—	ns
		t_a	—	24	—	
		t_b	—	20	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.055	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

Designer's™ Data Sheet

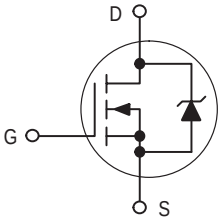
TMOS V™
Power Field Effect Transistor
D²PAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

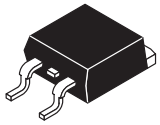
MTB36N06V

Motorola Preferred Device

TMOS POWER FET
32 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.04 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 418B–02, Style 2
D²PAK

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETs
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 50$ μs)	V_{GS} V_{GSM}	±20 ±25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	32 22.6 112	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	90 0.6 3.0	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, PEAK I_L = 32 Apk, L = 0.1 mH, R_G = 25 Ω)	E_{AS}	205	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.67 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	61	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.6	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	6.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc)		$R_{DS(on)}$	—	0.034	0.04	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 32 Adc)		$V_{DS(on)}$	—	1.25	1.54	Vdc
(V_{GS} = 10 Vdc, I_D = 16 Adc, T_J = 150°C)			—	—	1.47	
Forward Transconductance (V_{DS} = 7.6 Vdc, I_D = 16 Adc)		g_{FS}	5.0	7.83	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1220	1700	pF
Output Capacitance		C_{oss}	—	337	470	
Reverse Transfer Capacitance		C_{rss}	—	74.8	150	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	14	30	ns
Rise Time		t_r	—	138	270	
Turn–Off Delay Time		$t_{d(off)}$	—	54	100	
Fall Time		t_f	—	91	180	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc)	Q_T	—	39	50	nC
		Q_1	—	7	—	
		Q_2	—	17	—	
		Q_3	—	13	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 32 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.03	2.0	Vdc
	(I_S = 32 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.94	—	
Reverse Recovery Time	(I_S = 32 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	92	—	ns
		t_a	—	64	—	
		t_b	—	28	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.332	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	3.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

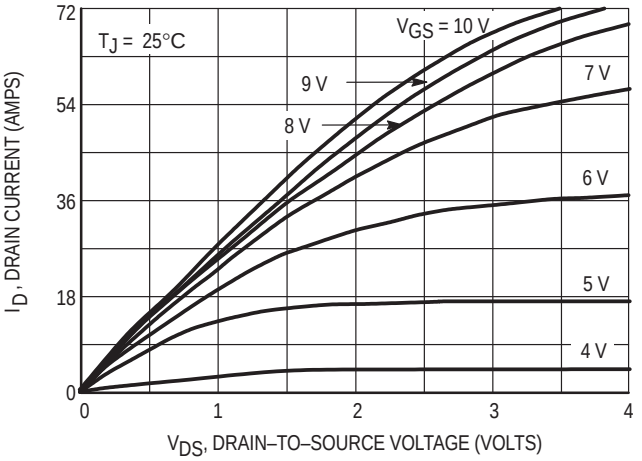


Figure 1. On–Region Characteristics

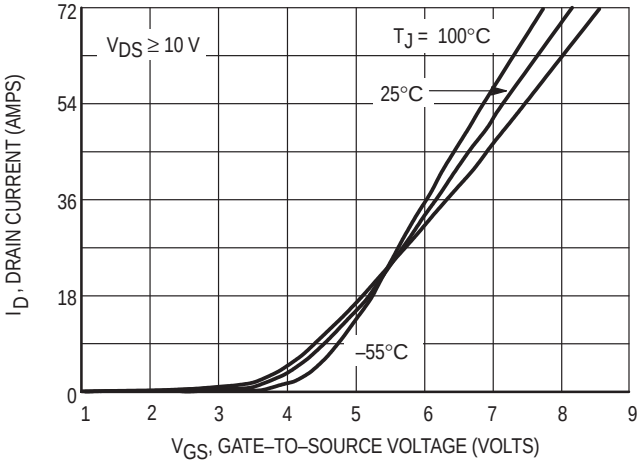


Figure 2. Transfer Characteristics

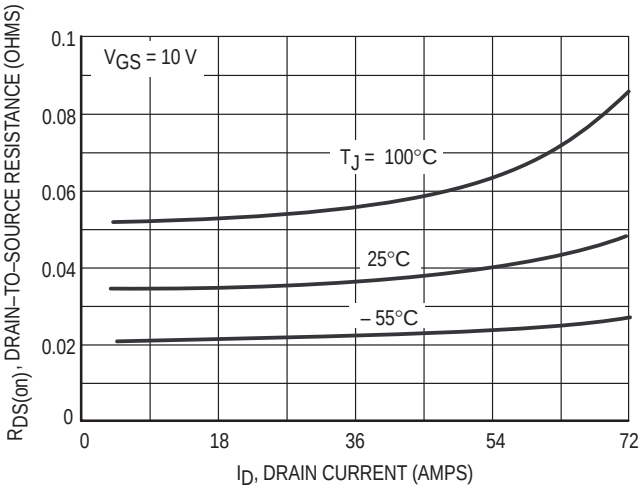


Figure 3. On–Resistance versus Drain Current and Temperature

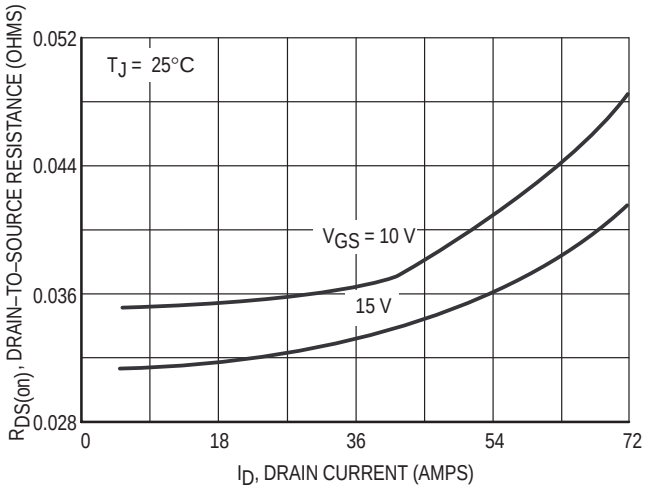


Figure 4. On–Resistance versus Drain Current and Gate Voltage

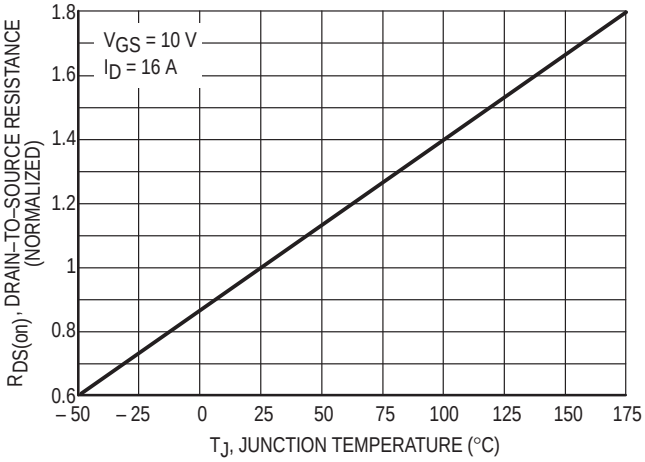


Figure 5. On–Resistance Variation with Temperature

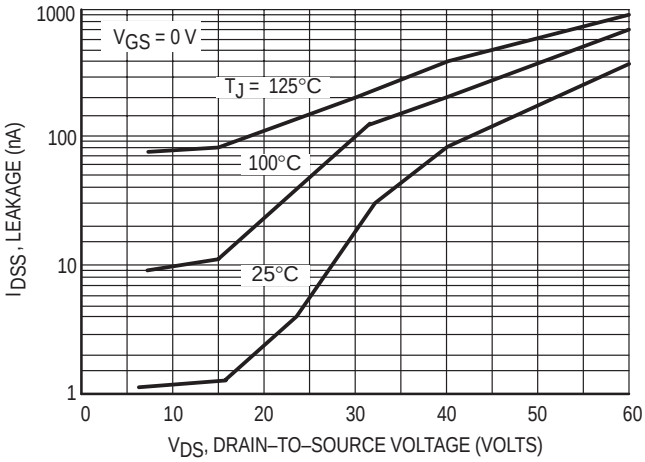


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

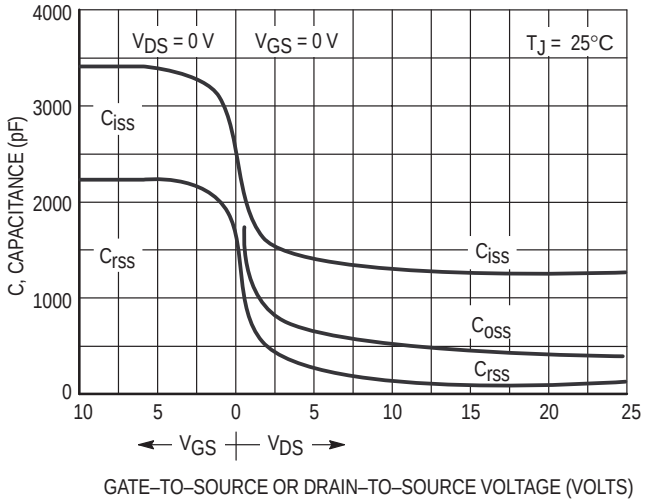


Figure 7. Capacitance Variation

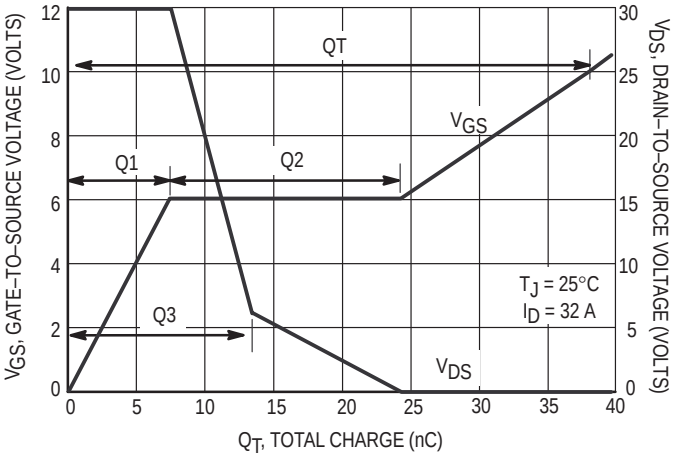


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

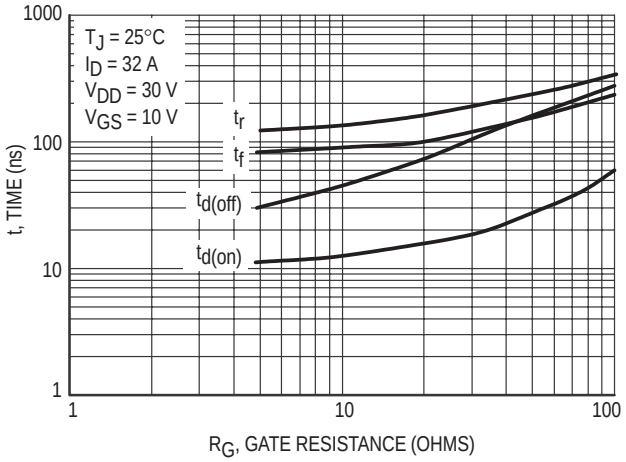


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

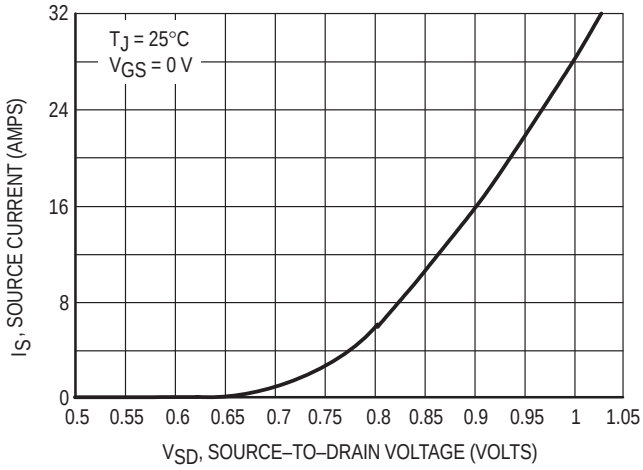


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

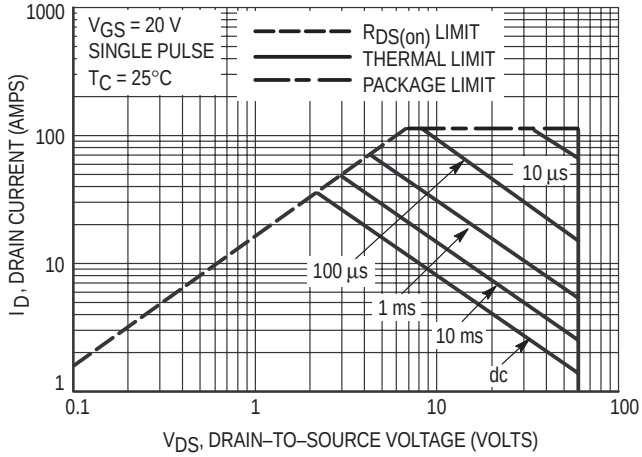


Figure 11. Maximum Rated Forward Biased Safe Operating Area

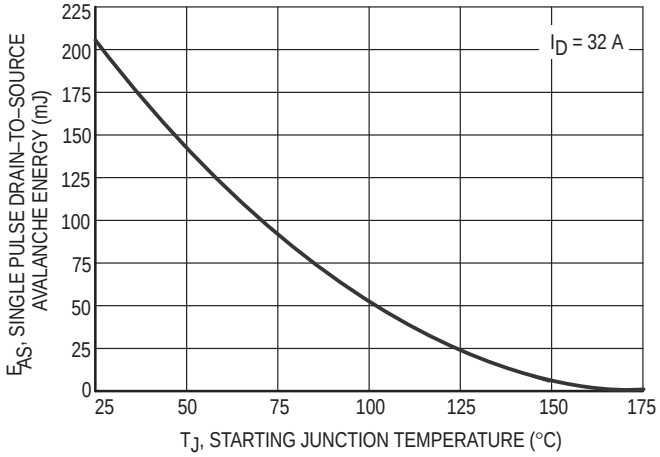


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

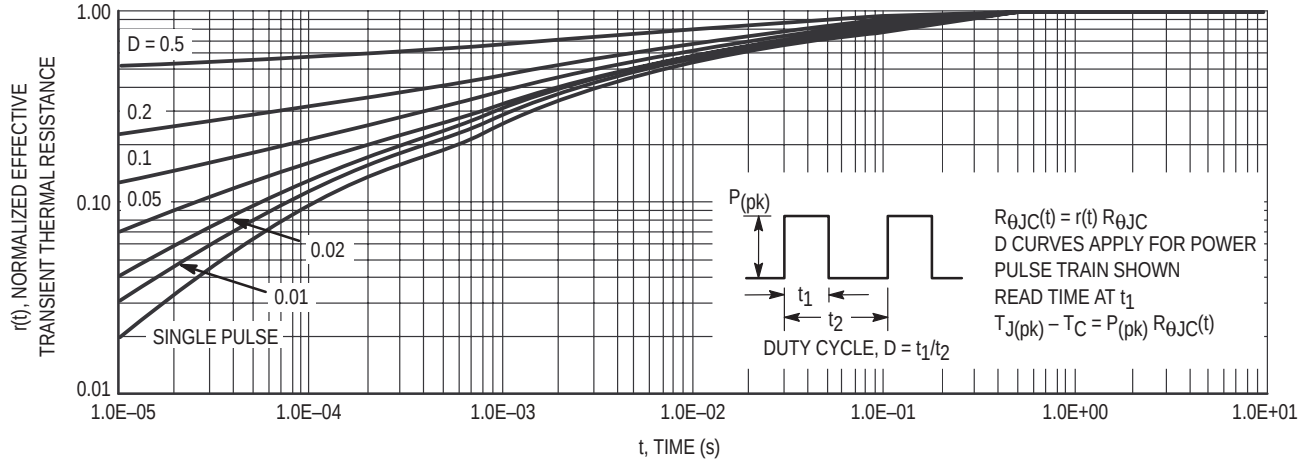


Figure 13. Thermal Response

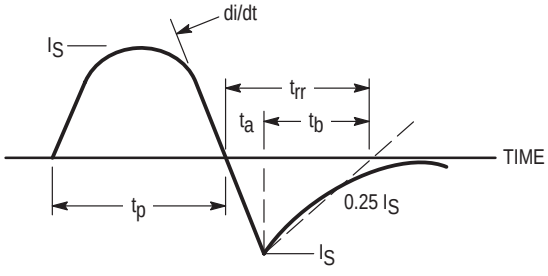


Figure 14. Diode Reverse Recovery Waveform

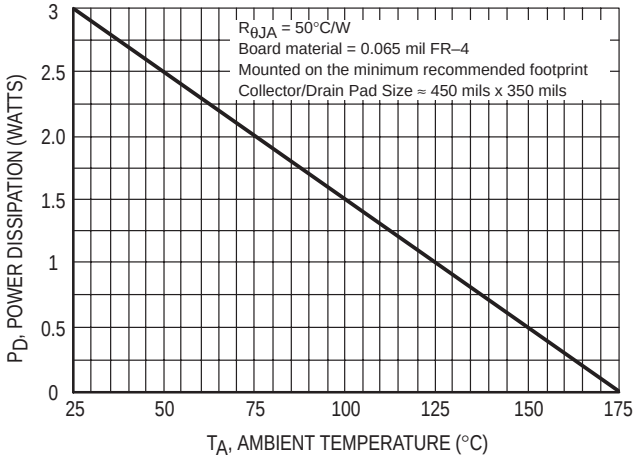


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

HDTMOS E-FET ™
High Energy Power FET
D²PAK for Surface Mount

P–Channel Enhancement–Mode Silicon Gate

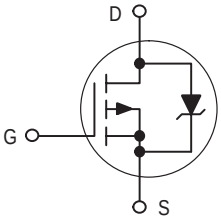
MTB50P03HDL

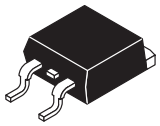
Motorola Preferred Device

TMOS POWER FET
LOGIC LEVEL
50 AMPERES
30 VOLTS
$R_{DS(on)}$ = 0.025 OHM

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced high–cell density HDTMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	30	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±15 ± 20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	50 31 150	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_C = 25°C, when mounted with the minimum recommended pad size	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 50 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	1250	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage ($C_{pk} \geq 2.0$) (3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 30 —	 — 26	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	 —	 —	 100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($C_{pk} \geq 3.0$) (3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 —	 1.5 4.0	 2.0 —	Vdc mV/°C
Static Drain–Source On–Resistance ($C_{pk} \geq 3.0$) (3) (V_{GS} = 5.0 Vdc, I_D = 25 Adc)		$R_{DS(on)}$	 —	 20.9	 25	mOhm
Drain–Source On–Voltage (V_{GS} = 5.0 Vdc) (I_D = 50 Adc) (I_D = 25 Adc, T_J =125°C)		$V_{DS(on)}$	 — —	 0.83 —	 1.5 1.3	Vdc
Forward Transconductance (V_{DS} = 5.0 Vdc, I_D = 25 Adc)		g_{FS}	 15	 20	 —	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3500	4900	pF
Output Capacitance		C_{oss}	—	1550	2170	
Transfer Capacitance		C_{rss}	—	550	770	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD}= 15 Vdc, I_D = 50 Adc, V_{GS} = 5.0 Vdc, R_G = 2.3 Ω)	$t_{d(on)}$	—	22	30	ns
Rise Time		t_r	—	340	466	
Turn–Off Delay Time		$t_{d(off)}$	—	90	117	
Fall Time		t_f	—	218	300	
Gate Charge (See Figure 8)	(V_{DS} = 24 Vdc, I_D = 50 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	74	100	nC
		Q_1	—	13.6	—	
		Q_2	—	44.8	—	
		Q_3	—	35	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 50 Adc, V_{GS} = 0 Vdc) (I_S = 50 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 2.39 1.84	 3.0 —	Vdc
Reverse Recovery Time (See Figure 15)	(I_S = 50 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	106	—	ns
		t_a	—	58	—	
		t_b	—	48	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.246	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	3.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

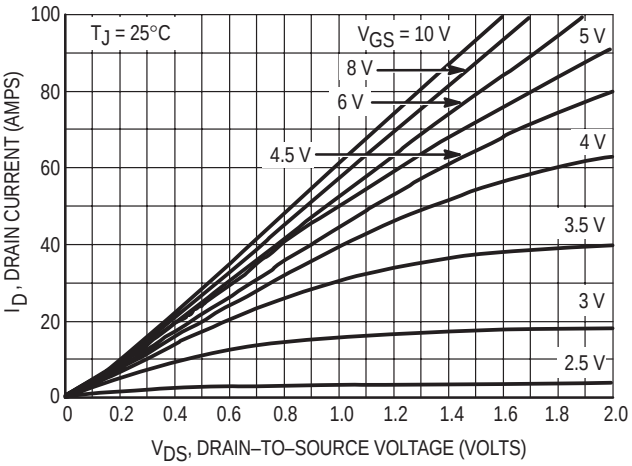


Figure 1. On–Region Characteristics

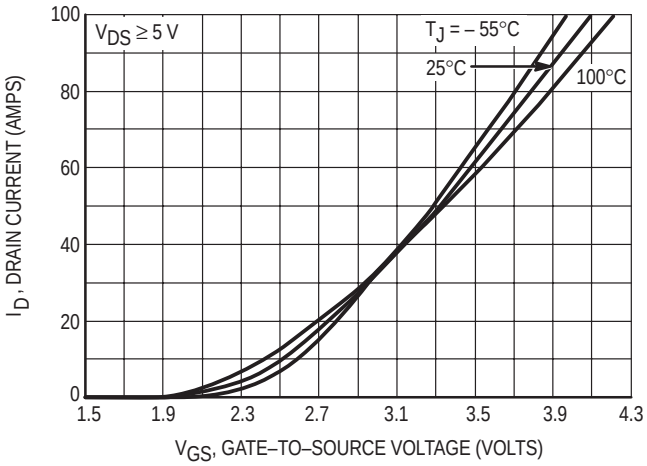


Figure 2. Transfer Characteristics

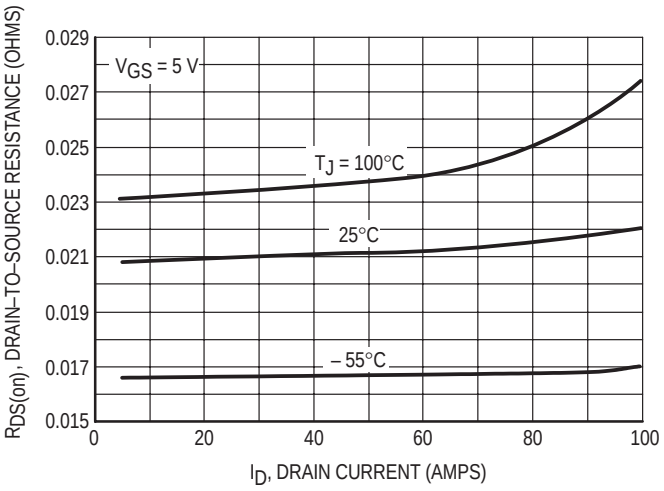
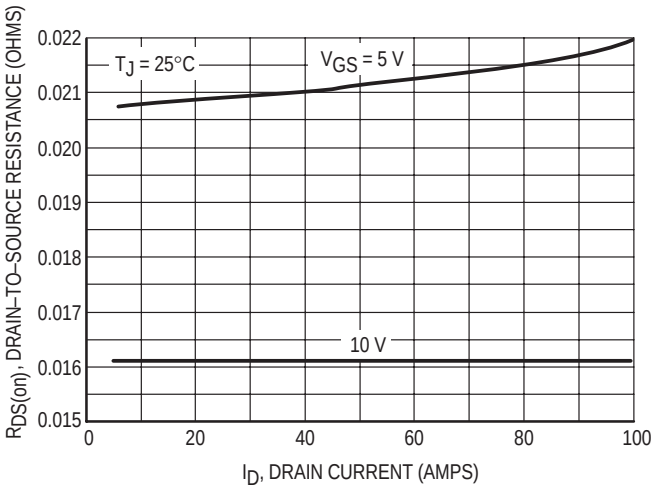


Figure 3. On–Resistance versus Drain Current and Temperature



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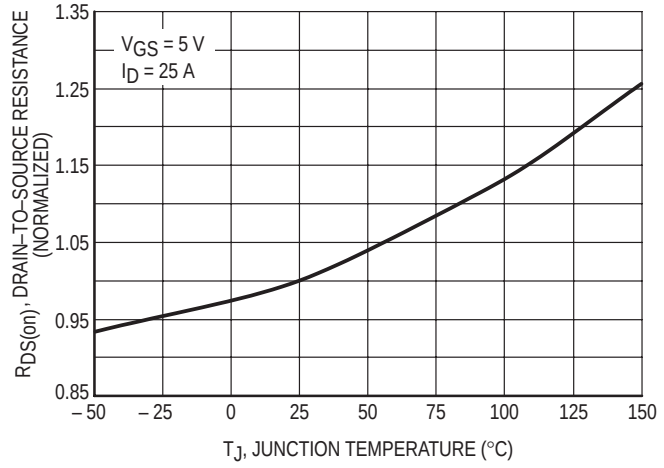
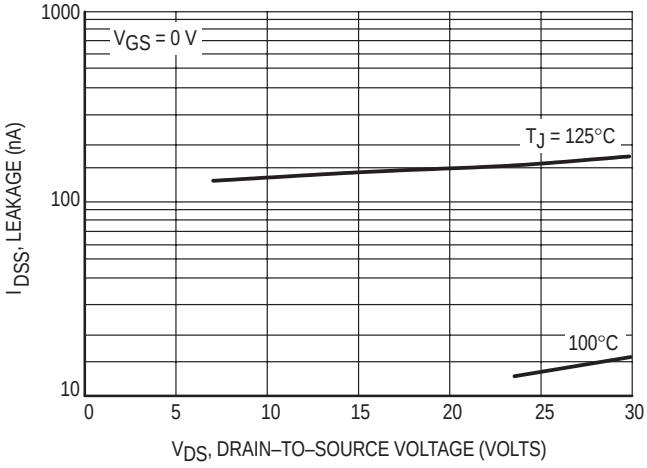


Figure 5. On–Resistance Variation with Temperature



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During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

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where

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R_G = the gate drive resistance

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During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

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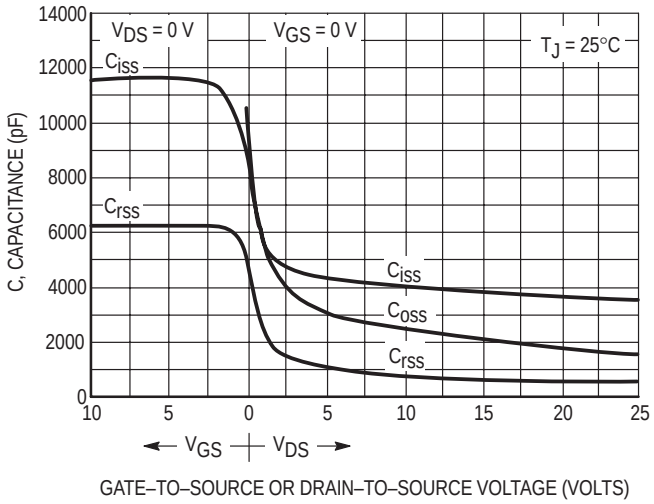
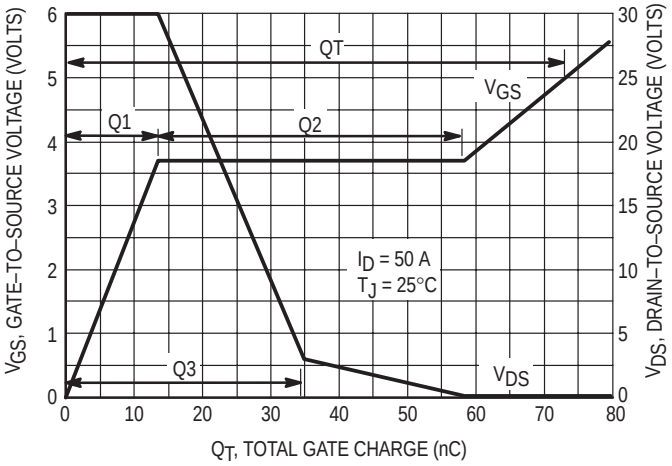


Figure 7. Capacitance Variation



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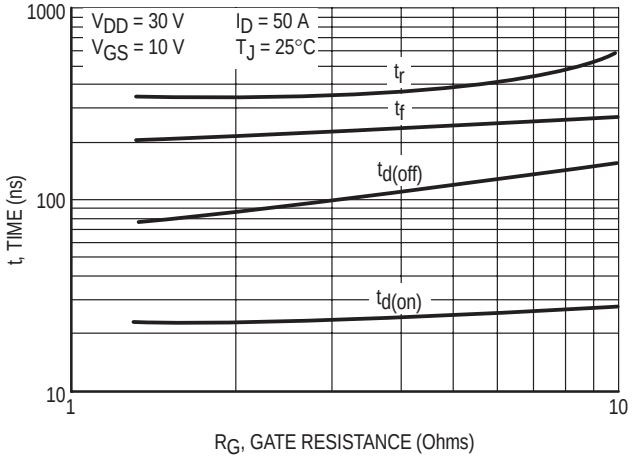


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

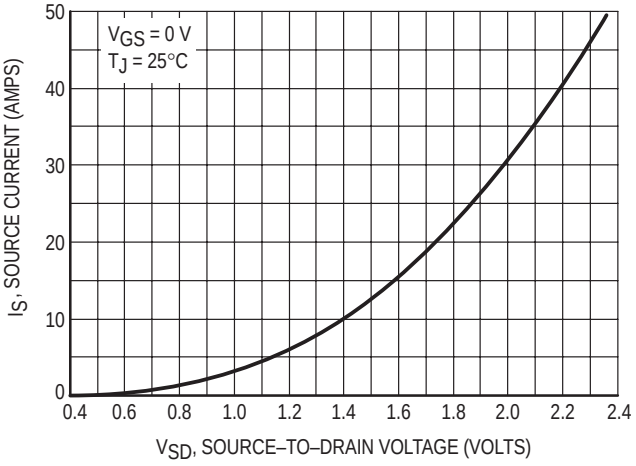


Figure 10. Diode Forward Voltage versus Current

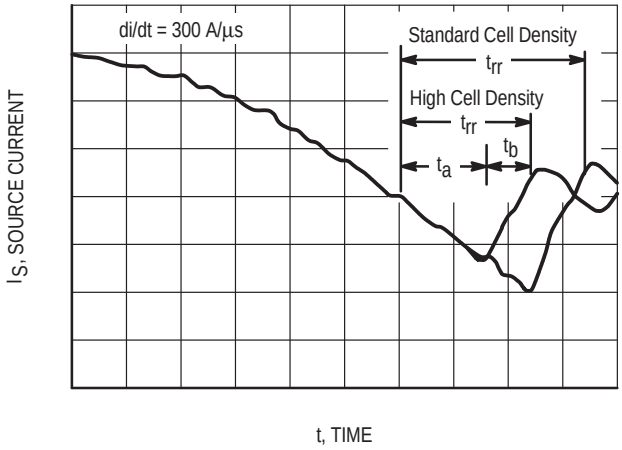


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

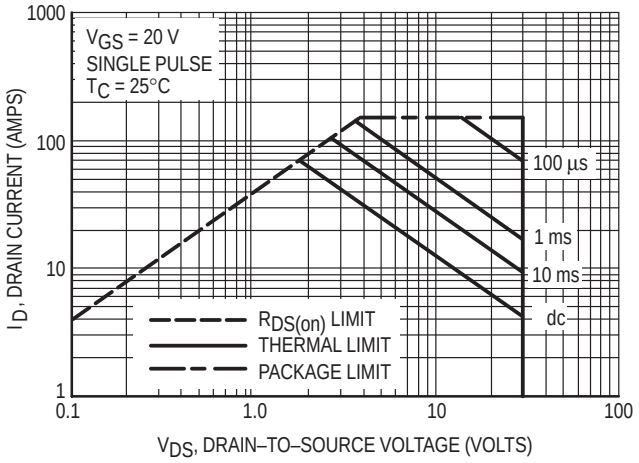


Figure 12. Maximum Rated Forward Biased Safe Operating Area

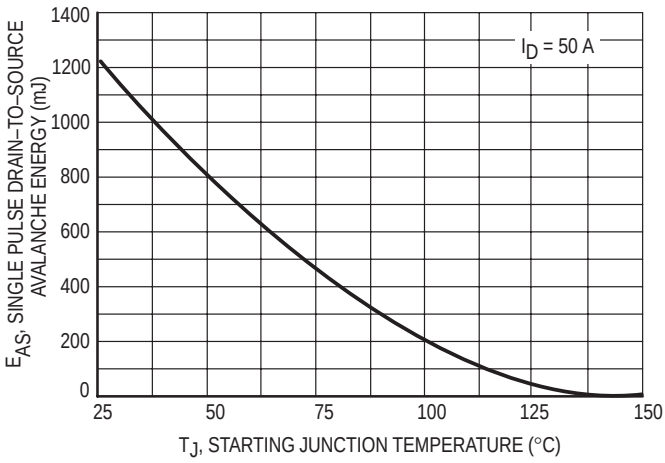


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

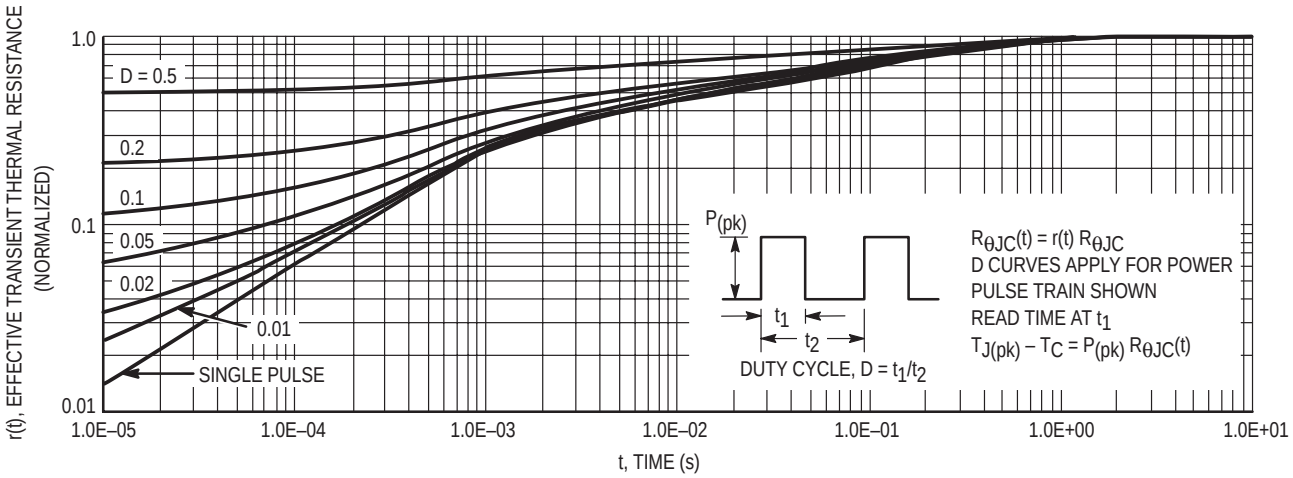


Figure 14. Thermal Response

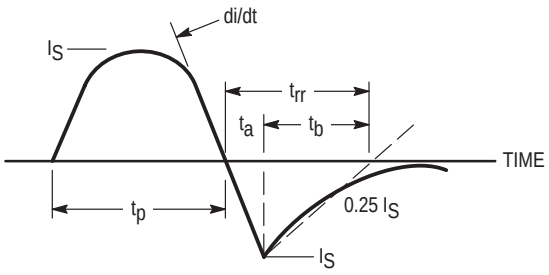


Figure 15. Diode Reverse Recovery Waveform

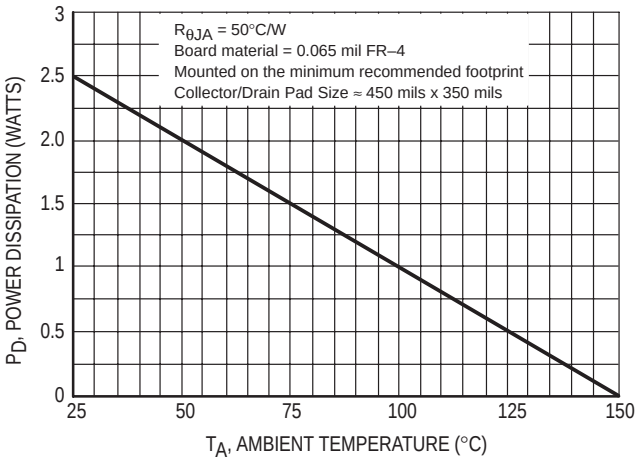


Figure 16. D²PAK Power Derating Curve

Product Preview

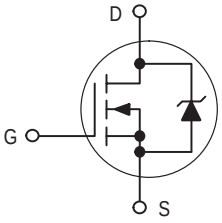
TMOS V™
Power Field Effect Transistor
D²PAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

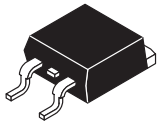
MTB52N06V

Motorola Preferred Device

TMOS POWER FET
52 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.022 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 418B–02, Style 2
D²PAK

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETs
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±25	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	52 41 182	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	165 1.1 3.0	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 52 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	406	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	0.91 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 26 Adc)		$R_{DS(on)}$	—	0.019	0.022	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 52 Adc)		$V_{DS(on)}$	—	—	1.4	Vdc
(V_{GS} = 10 Vdc, I_D = 26 Adc, T_J = 150°C)			—	—	1.2	
Forward Transconductance (V_{DS} = 6.3 Vdc, I_D = 20 Adc)		g_{FS}	17	25	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1700	2380	pF
Output Capacitance		C_{oss}	—	500	700	
Reverse Transfer Capacitance		C_{rss}	—	150	300	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 52 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	15	30	ns
Rise Time		t_r	—	130	260	
Turn–Off Delay Time		$t_{d(off)}$	—	68	140	
Fall Time		t_f	—	70	140	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 52 Adc, V_{GS} = 10 Vdc)	Q_T	—	70	80	nC
		Q_1	—	10	—	
		Q_2	—	30	—	
		Q_3	—	20	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 52 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.5	Vdc
	(I_S = 52 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.9	—	
Reverse Recovery Time (See Figure 14)	(I_S = 52 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	90	—	ns
		t_a	—	80	—	
		t_b	—	10	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.3	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

Product Preview

TMOS V™
Power Field Effect Transistor
D²PAK for Surface Mount

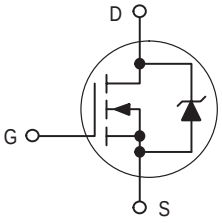
N–Channel Enhancement–Mode Silicon Gate

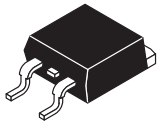
MTB52N06VL

Motorola Preferred Device

TMOS POWER FET
52 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.025 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 418B–02, Style 2
D²PAK

New Features of TMOS V

- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETs

- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±15 ±25	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	52 41 182	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	165 1.1 3.0	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5 Vdc, PEAK I_L = 52 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	406	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	0.91 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = .25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage		$V_{GS(th)}$				
(V_{DS} = V_{GS}, I_D = 250 μAdc)			1.0	1.5	2.0	Vdc
Threshold Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 5 Vdc, I_D = 26 Adc)		$R_{DS(on)}$	—	0.022	0.025	Ohm
Drain–to–Source On–Voltage		$V_{DS(on)}$				Vdc
(V_{GS} = 5 Vdc, I_D = 52 Adc)			—	—	1.5	
(V_{GS} = 5 Vdc, I_D = 26 Adc, T_J = 150°C)			—	—	1.3	
Forward Transconductance (V_{DS} = 6.3 Vdc, I_D = 20 Adc)		g_{FS}	17	30	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1600	2240	pF
Output Capacitance		C_{oss}	—	550	770	
Transfer Capacitance		C_{rss}	—	170	340	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 52 Adc, V_{GS} = 5 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	18	40	ns
Rise Time		t_r	—	370	740	
Turn–Off Delay Time		$t_{d(off)}$	—	90	180	
Fall Time		t_f	—	170	340	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 52 Adc, V_{GS} = 5 Vdc)	Q_T	—	45	60	nC
		Q_1	—	12	—	
		Q_2	—	22	—	
		Q_3	—	18	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 52 Adc, V_{GS} = 0 Vdc)	V_{SD}				Vdc
	(I_S = 52 Adc, V_{GS} = 0 Vdc, T_J = 150 °C)		—	1.0	1.5	
			—	0.9	—	
Reverse Recovery Time	(I_S = 52 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	93	—	ns
		t_a	—	65	—	
		t_b	—	28	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.3	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance		L_S				nH
(Measured from the source lead 0.25″ from package to source bond pad)			—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

Product Preview

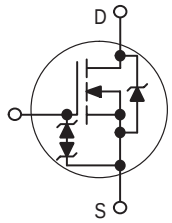
TMOS E-FET™
High Energy Power FET
D²PAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

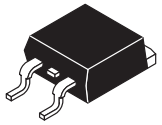
MTB55N06Z

TMOS POWER FET
55 AMPERES
60 VOLTS
$R_{DS(on)}$ = 16 mΩ

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor–Absorbs High Energy in the Avalanche Mode
- ESD Protected. 400 V Machine Model Level and 4000 V Human Body Model Level.





CASE 418B–02, Style 2
D²PAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±30	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	55 35.5 165	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	136 0.91 3.0	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{DS} = 60 Vdc, V_{GS} = 10 Vdc, Peak I_L = 55 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	454	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.1 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 —	 — 53	 — —	 Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	5.0	μAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 2.0 —	 3.0 6.0	 4.0 —	 Vdc mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (V_{GS} = 10 Vdc, I_D = 15 Adc)		$R_{DS(on)}$	—	14	16	mΩ
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 30 Adc) (I_D = 15 Adc, T_J = 125°C)		$V_{DS(on)}$	 — —	 0.825 0.74	 1.2 1.0	Vdc
Forward Transconductance (V_{DS} = 4.0 Vdc, I_D = 15 Adc)		g_{FS}	12	15	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1390	1950	pF
Output Capacitance		C_{oss}	—	520	730	
Transfer Capacitance		C_{rss}	—	119	238	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 30 Adc, $V_{GS(on)}$ = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	27	54	ns
Rise Time		t_r	—	157	314	
Turn–Off Delay Time		$t_{d(off)}$	—	116	232	
Fall Time		t_f	—	126	252	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 30 Adc, V_{GS} = 10 Vdc)	Q_T	—	40	56	nC
		Q_1	—	7.0	—	
		Q_2	—	18	—	
		Q_3	—	15	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 30 Adc, V_{GS} = 0 Vdc) (I_S = 30 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 0.93 0.82	 1.1 —	Vdc
Reverse Recovery Time	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	57	—	ns
		t_a	—	32	—	
		t_b	—	25	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.11	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from drain lead 0.25″ from package to center of die)		L_D	 — —	 3.5 4.5	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

Designer's™ Data Sheet

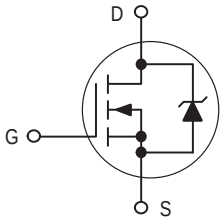
HDTMOS E-FET™
High Energy Power FET
D²PAK for Surface Mount

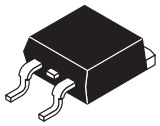
N–Channel Enhancement–Mode Silicon Gate

MTB60N06HD

Motorola Preferred Device

TMOS POWER FET
60 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.014 OHM





CASE 418B–02, Style 2
D²PAK

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced high–cell density HDTMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 30	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	60 42.3 180	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 60 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	540	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When mounted with the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage ($C_{pk} \geq 2.0$) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			60	—	—	
Temperature Coefficient (Positive)			—	71	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($C_{pk} \geq 3.0$) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			2.0	3.0	4.0	
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance ($C_{pk} \geq 3.0$) (3)		$R_{DS(on)}$				Ohm
(V_{GS} = 10 Vdc, I_D = 30 Adc)			—	0.011	0.014	
Drain–Source On–Voltage (V_{GS} = 10 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 60 Adc)			—	—	1.0	
(I_D = 30 Adc, T_J =125°C)			—	—	0.9	
Forward Transconductance		g_{FS}				mhos
(V_{DS} = 4.0 Vdc, I_D = 30 Adc)			15	20	—	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1950	2800	pF
Output Capacitance		C_{oss}	—	660	920	
Transfer Capacitance		C_{rss}	—	147	300	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD}= 30 Vdc, I_D = 60 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	14	26	ns
Rise Time		t_r	—	197	394	
Turn–Off Delay Time		$t_{d(off)}$	—	50	102	
Fall Time		t_f	—	124	246	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 60 Adc, V_{GS} = 10 Vdc)	Q_T	—	51	71	nC
		Q_1	—	12	—	
		Q_2	—	24	—	
		Q_3	—	21	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 60 Adc, V_{GS} = 0 Vdc)	V_{SD}				Vdc
	(I_S = 60 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.99	1.0	
			—	0.89	—	
Reverse Recovery Time (See Figure 15)	(I_S = 60 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	60	—	ns
		t_a	—	36	—	
		t_b	—	24	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.143	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

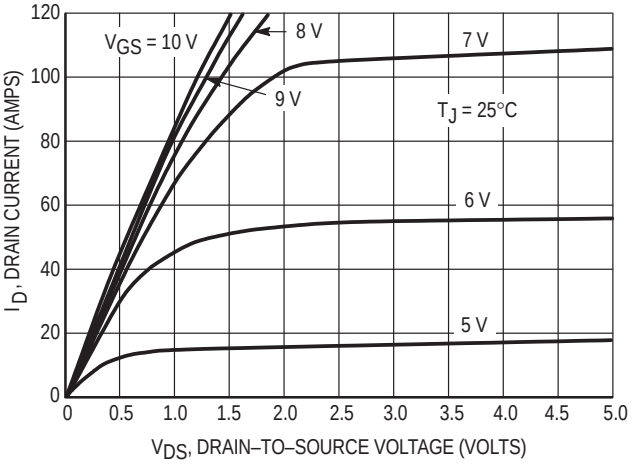


Figure 1. On–Region Characteristics

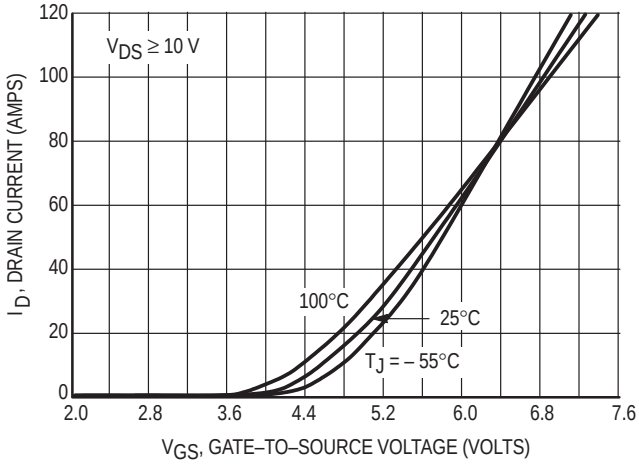


Figure 2. Transfer Characteristics

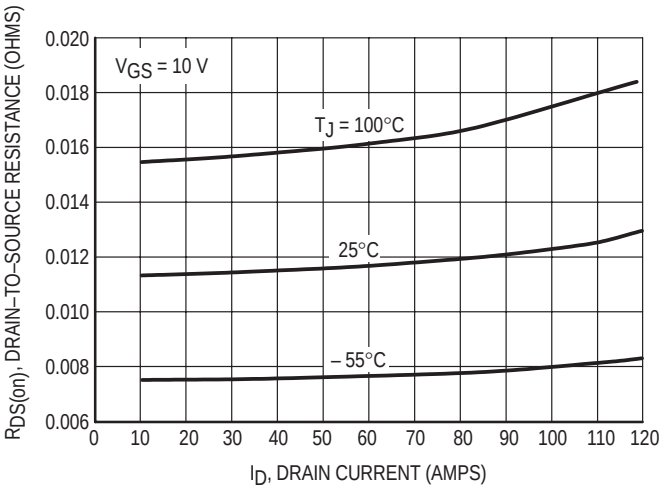


Figure 3. On–Resistance versus Drain Current and Temperature

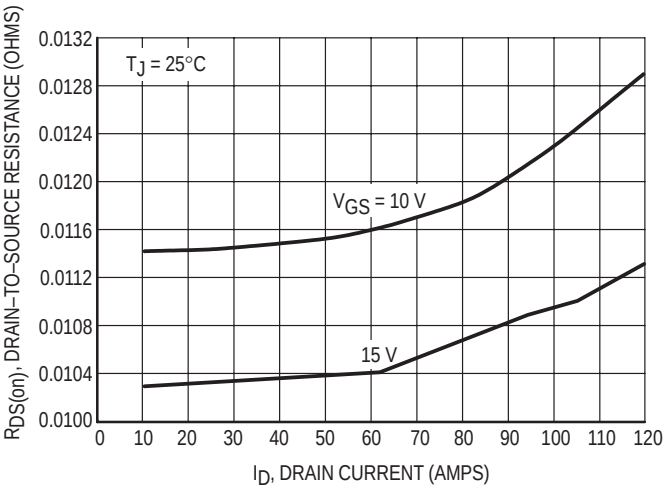


Figure 4. On–Resistance versus Drain Current and Gate Voltage

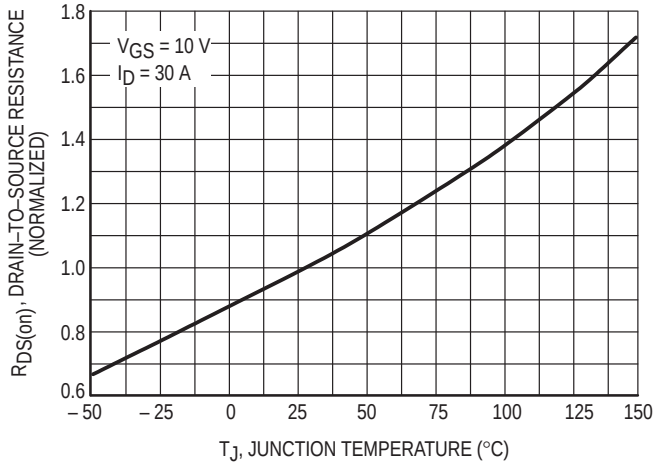


Figure 5. On–Resistance Variation with Temperature

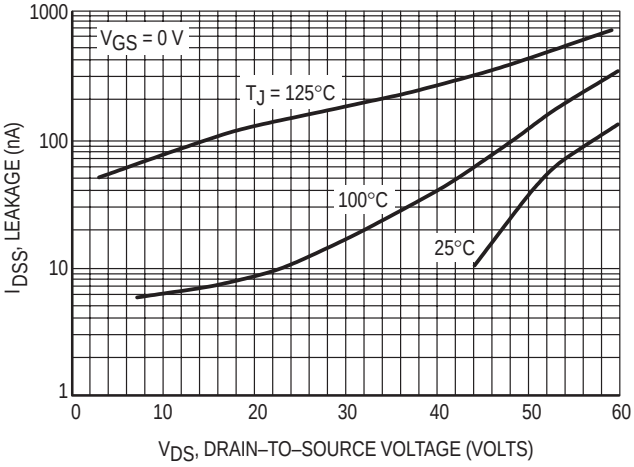


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

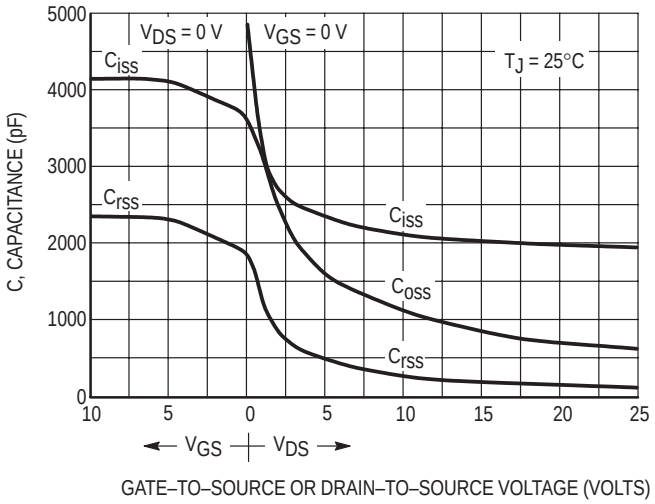


Figure 7. Capacitance Variation

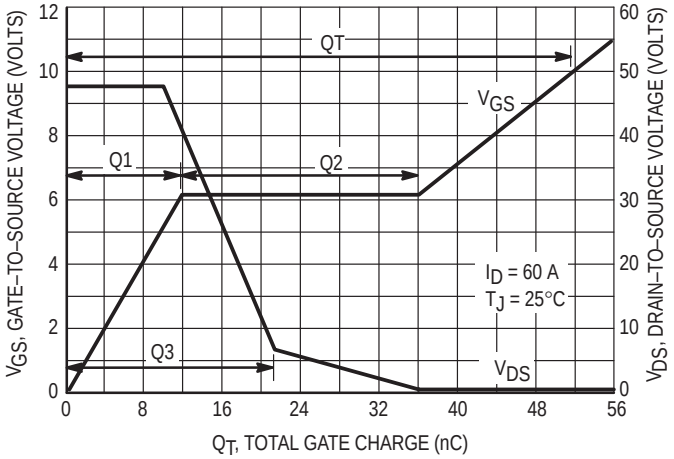


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

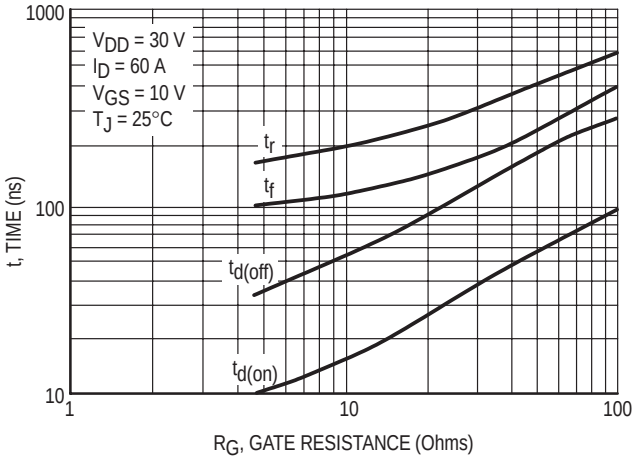


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

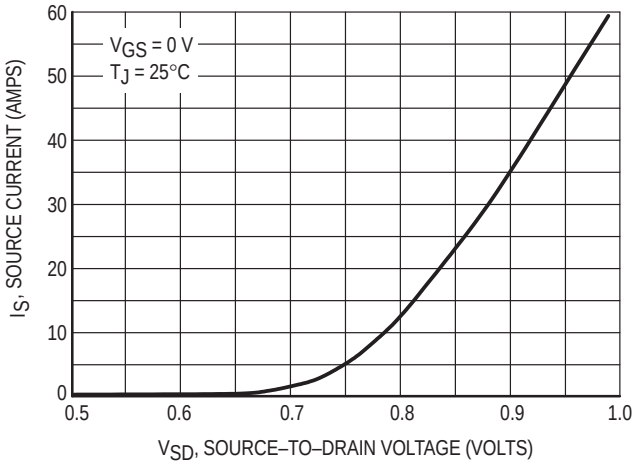


Figure 10. Diode Forward Voltage versus Current

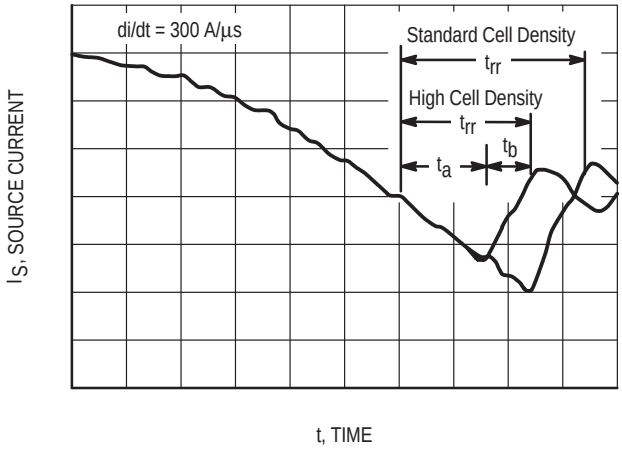


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

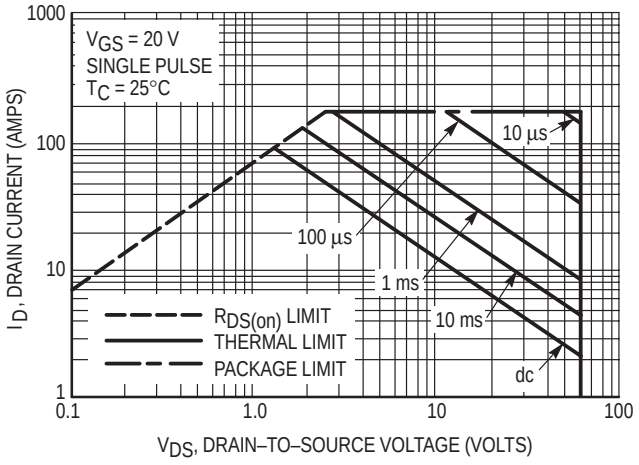


Figure 12. Maximum Rated Forward Biased Safe Operating Area

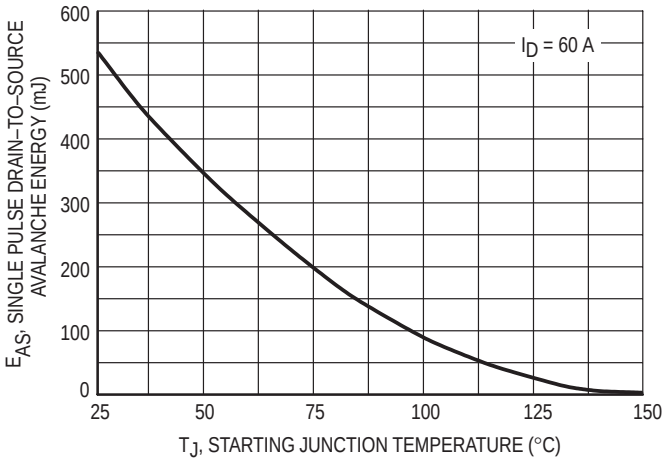


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

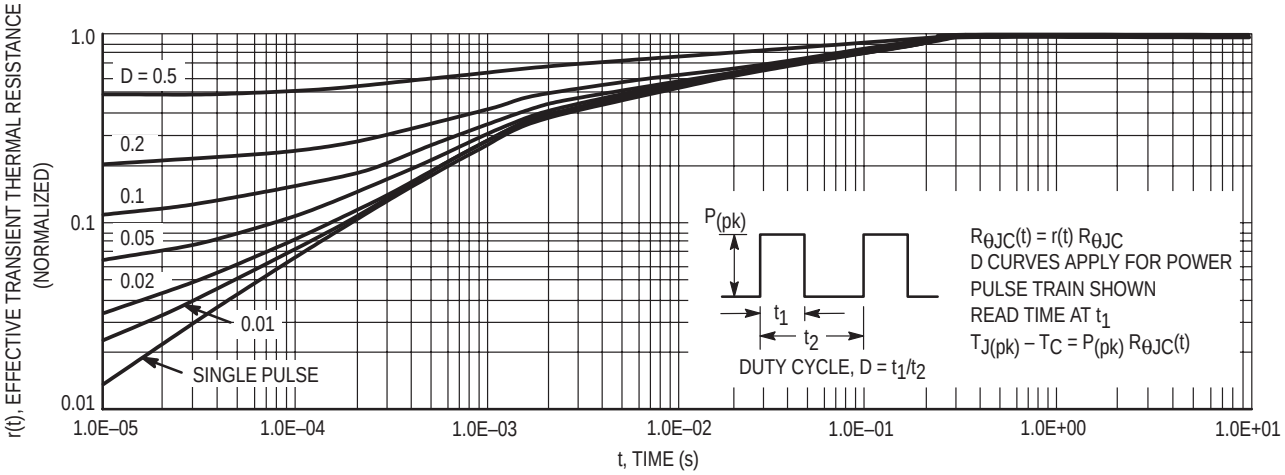


Figure 14. Thermal Response

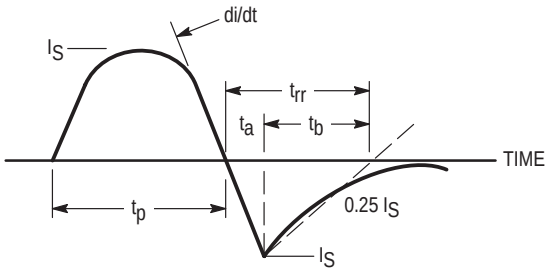


Figure 15. Diode Reverse Recovery Waveform

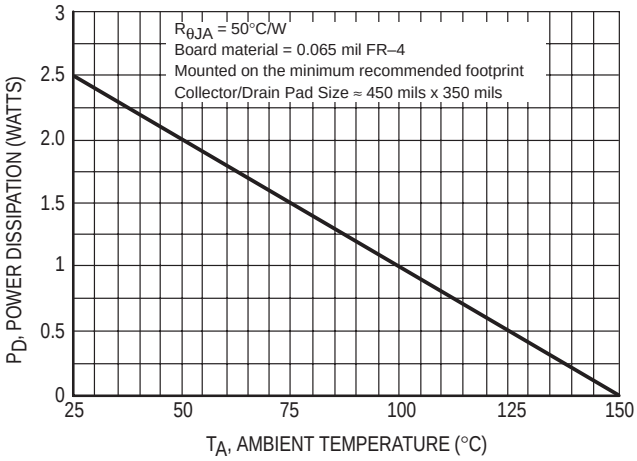


Figure 16. D²PAK Power Derating Curve

Advanced Information

HDTMOS E-FET™
High Density Power FET
D²PAK for Surface Mount

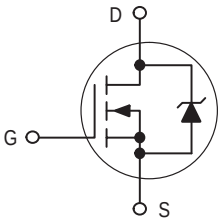
N–Channel Enhancement–Mode Silicon Gate

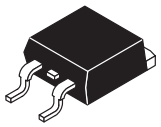
MTB75N03HDL

Motorola Preferred Device

TMOS POWER FET
LOGIC LEVEL
75 AMPERES
25 VOLTS
$R_{DS(on)}$ = 9 mOHM

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced high–cell density HDTMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 418B–02, Style 2
D²PAK

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Ultra Low $R_{DS(on)}$, High–Cell Density, HDTMOS
- Short Heatsink Tab Manufactured — Not sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	25	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	25	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	75 59 225	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	– 55 to 150		°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 75 Apk, L = 0.1 mH, R_G = 25 Ω)	E_{AS}	280	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When mounted with the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage ($C_{pk} \geq 2.0$) (3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	25	—	—	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 100 500	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 V)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($C_{pk} \geq 3.0$) (3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	1.0	1.5	2.0	Vdc mV/°C
Static Drain–Source On–Resistance ($C_{pk} \geq 2.0$) (3) (V_{GS} = 5.0 Vdc, I_D = 37.5 Adc)		$R_{DS(on)}$	—	6.0	9.0	mΩ
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 75 Adc) (I_D = 37.5 Adc, T_J = 125°C)		$V_{DS(on)}$	 — —	 — —	 0.68 0.6	Vdc
Forward Transconductance (V_{DS} = 3 Vdc, I_D = 20 Adc)		g_{FS}	15	55	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	4025	5635	pF
Output Capacitance		C_{oss}	—	1353	1894	
Reverse Transfer Capacitance		C_{rss}	—	307	430	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DS}= 15 Vdc, I_D = 75 Adc, V_{GS} = 5.0 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	24	48	ns
Rise Time		t_r	—	493	986	
Turn–Off Delay Time		$t_{d(off)}$	—	60	120	
Fall Time		t_f	—	149	300	
Gate Charge	(V_{DS} = 24 Vdc, I_D = 75 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	61	122	nC
		Q_1	—	14	28	
		Q_2	—	33	66	
		Q_3	—	27	54	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 75 Adc, V_{GS} = 0 Vdc) (I_S = 75 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	0.97 0.87	1.1 —	Vdc
Reverse Recovery Time	(I_S = 75 Adc, dI_S/dt = 100 A/μs)	t_{rr}	—	58	—	ns
		t_a	—	27	—	
		t_b	—	30	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.088	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

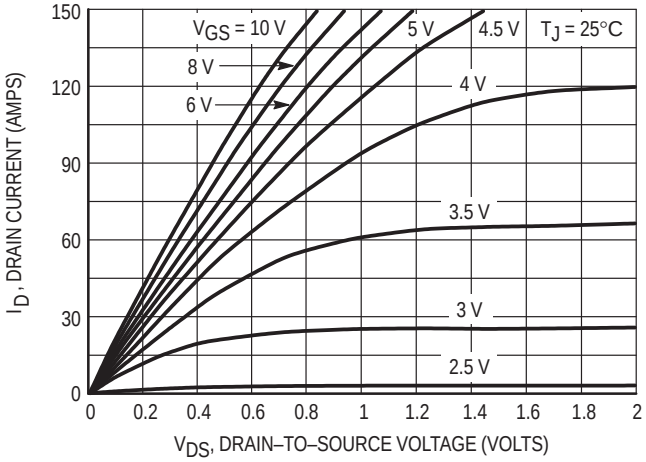


Figure 1. On–Region Characteristics

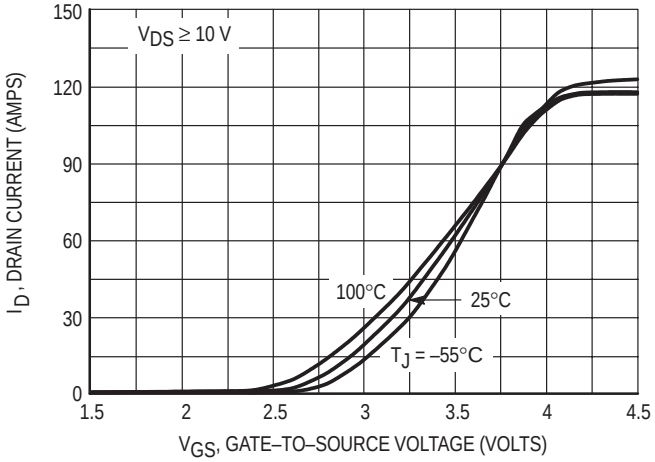


Figure 2. Transfer Characteristics

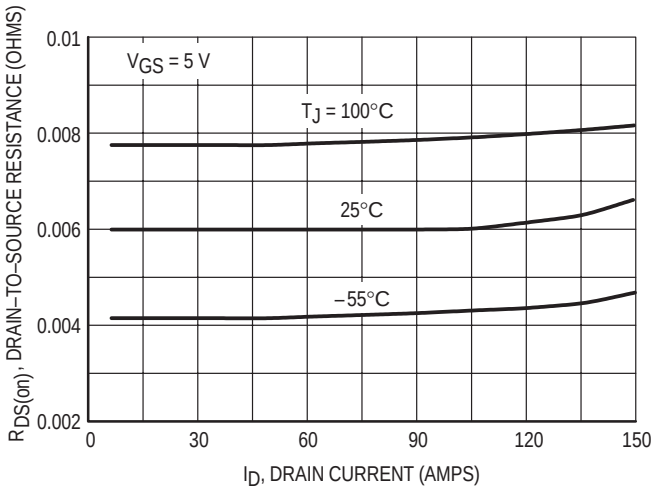


Figure 3. On–Resistance versus Drain Current and Temperature

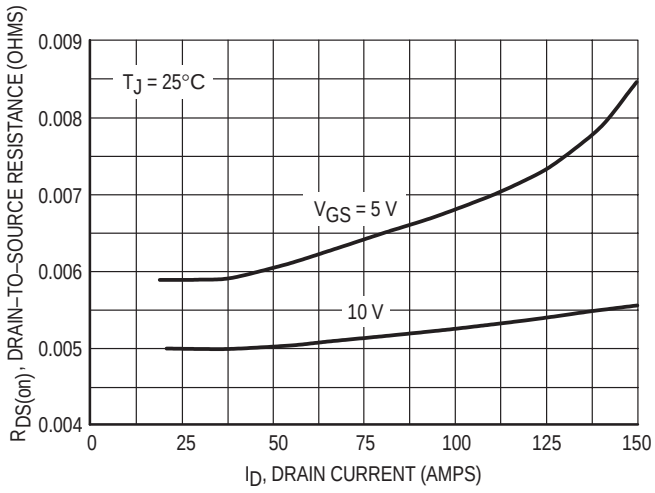


Figure 4. On–Resistance versus Drain Current and Gate Voltage

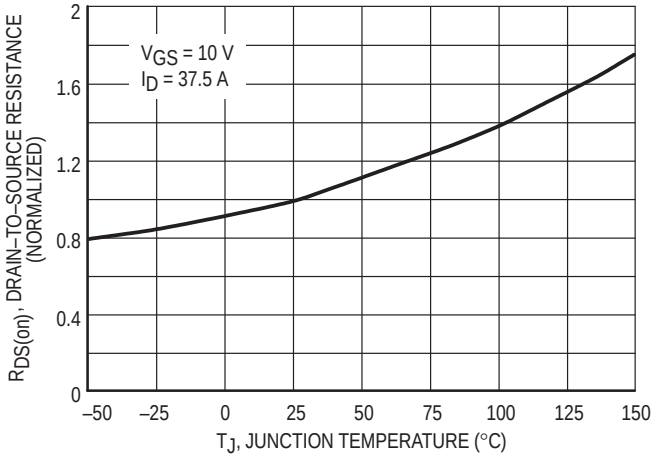


Figure 5. On–Resistance Variation with Temperature

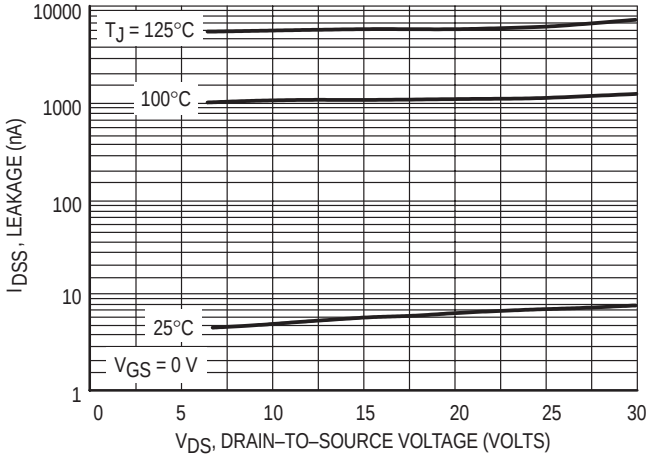


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

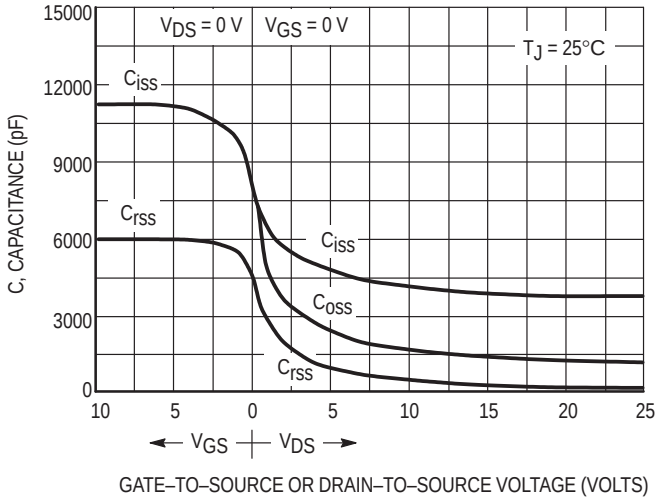


Figure 7. Capacitance Variation

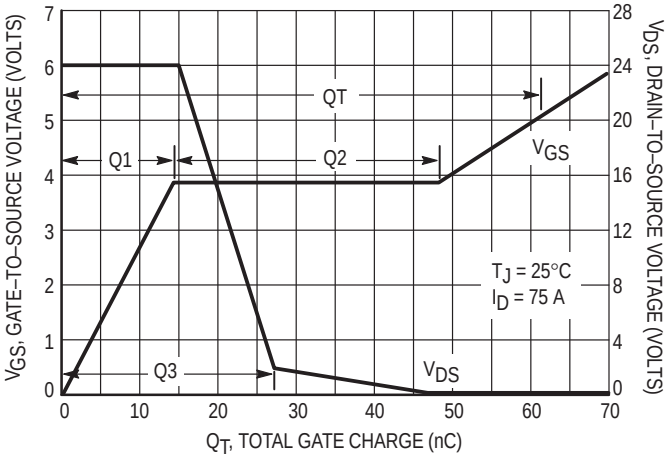


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

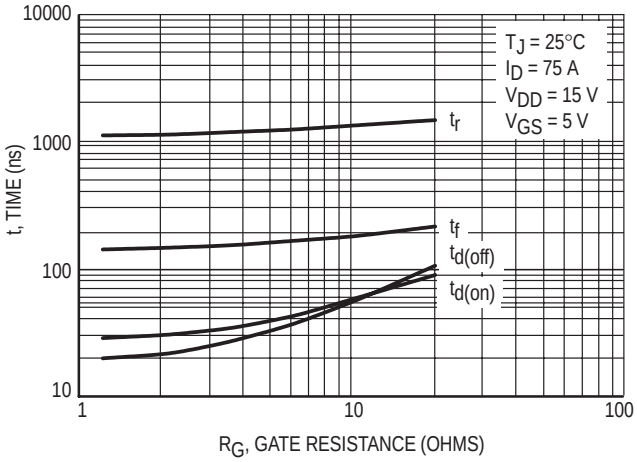


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

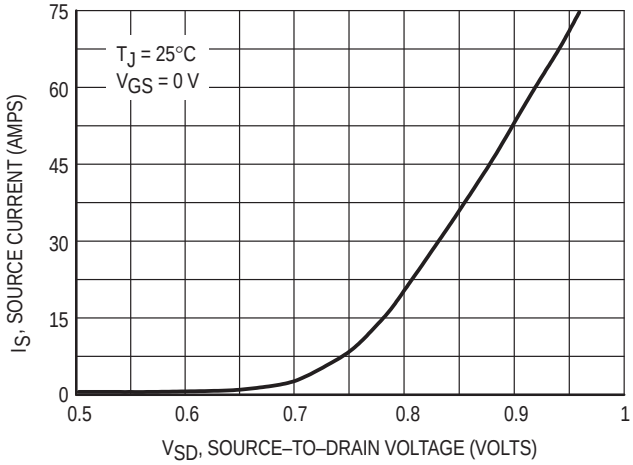


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

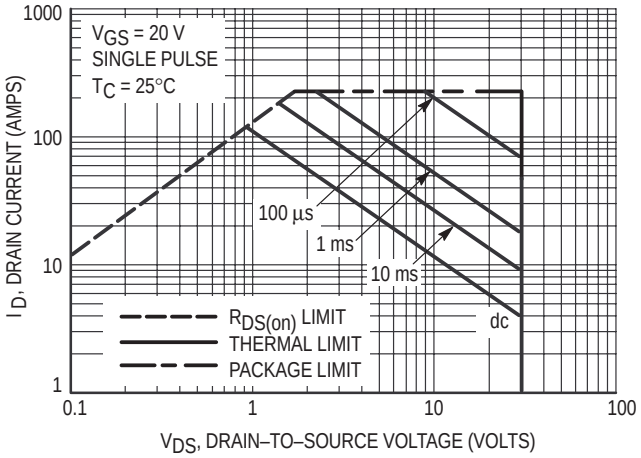


Figure 11. Maximum Rated Forward Biased Safe Operating Area

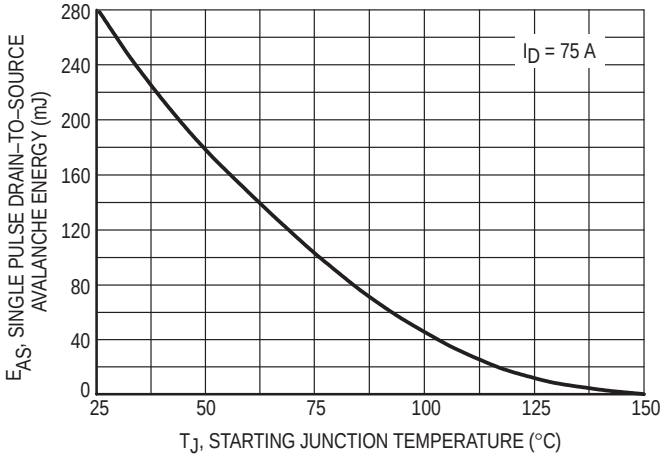


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

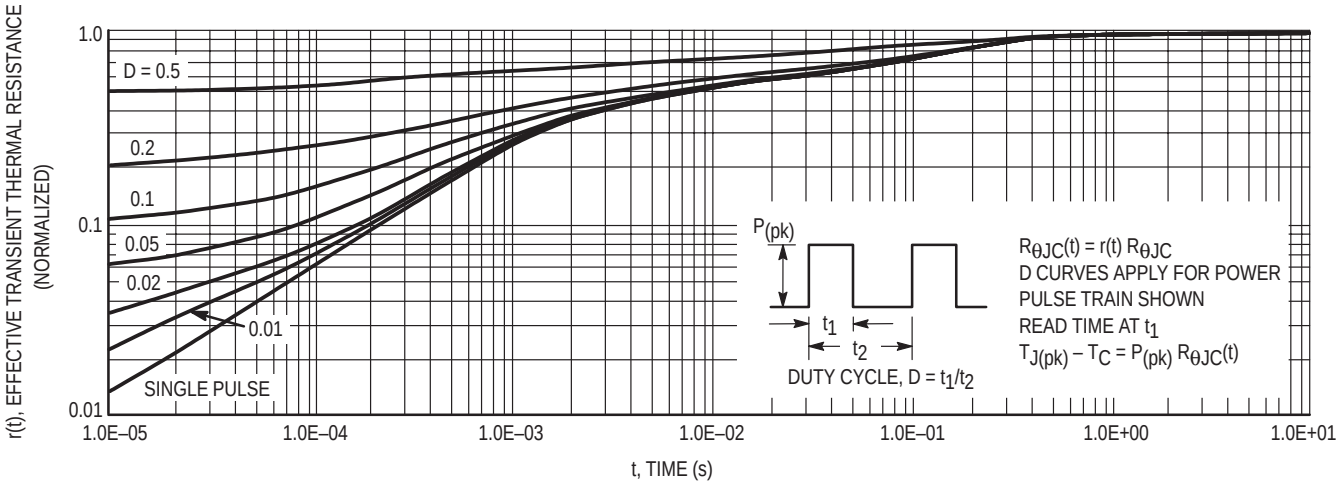


Figure 13. Thermal Response

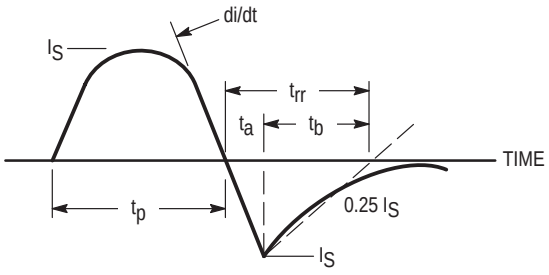


Figure 14. Diode Reverse Recovery Waveform

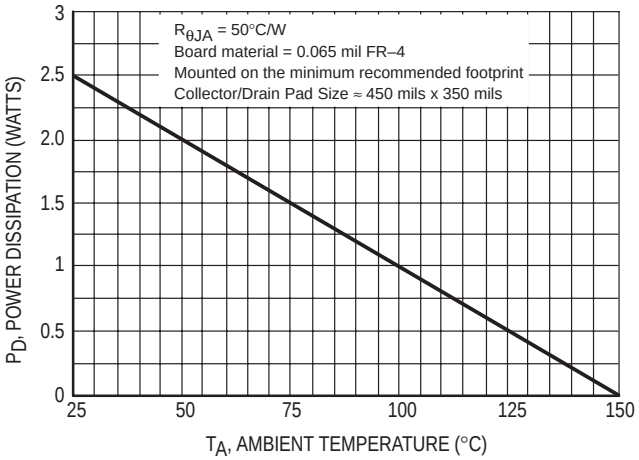


Figure 15. D²PAK Power Derating Curve

Designer's™ Data Sheet

HDTMOS E-FET™
High Energy Power FET
D²PAK for Surface Mount

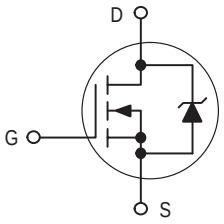
N–Channel Enhancement–Mode Silicon Gate

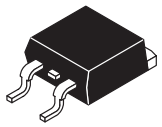
MTB75N05HD

Motorola Preferred Device

TMOS POWER FET
75 AMPERES
50 VOLTS
$R_{DS(on)}$ = 9.5 mΩ

The D²PAK package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced high–cell density HDTMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 418B–02, Style 2
D²PAK

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured — Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm 13–inch/800 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	50	Volts
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	75 65 225	Amps
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (minimum footprint, FR–4 board)	P_D	125 1.0 2.5	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 V, V_{GS} = 10 V, Peak I_L = 75 A, L = 0.177 mH, R_G = 25 Ω)	E_{AS}	500	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (minimum footprint, FR–4 board)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.0 62.5 50	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage ($C_{pk} \geq 2$)(2)		$V_{(BR)DSS}$				
(V_{GS} = 0, I_D = 250 μAdc)			50	—	—	Vdc
Temperature Coefficient (Positive)			—	54.9	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 50 V, V_{GS} = 0)			—	—	10	
(V_{DS} = 50 V, V_{GS} = 0, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current		I_{GSS}				nAdc
(V_{GS} = ± 20 Vdc, V_{DS} = 0)			—	—	100	
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($C_{pk} \geq 1.5$)(2)		$V_{GS(th)}$				
(V_{DS} = V_{GS}, I_D = 250 μAdc)			2.0	—	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	6.3	—	mV/°C
Static Drain–to–Source On–Resistance(3) ($C_{pk} \geq 3.0$)(2)		$R_{DS(on)}$				mΩ
(V_{GS} = 10 Vdc, I_D = 20 Adc)			—	7.0	9.5	
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc)(3)		$V_{DS(on)}$				Vdc
(I_D = 75 A)			—	0.63	—	
(I_D = 20 Adc, T_J = 125°C)			—	—	0.34	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 20 Adc)		g_{FS}	15	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz) ($C_{pk} \geq 2.0$)(2)	C_{iss}	—	2600	2900	pF
Output Capacitance	($C_{pk} \geq 2.0$)(2)	C_{oss}	—	1000	1100	
Transfer Capacitance	($C_{pk} \geq 2.0$)(2)	C_{rss}	—	230	275	
SWITCHING CHARACTERISTICS (4)						
Turn–On Delay Time	(V_{DD} = 25 V, I_D = 75 A, V_{GS} = 10 V, R_G = 9.1 Ω)	$t_{d(on)}$	—	15	30	ns
Rise Time		t_r	—	170	340	
Turn–Off Delay Time		$t_{d(off)}$	—	70	140	
Fall Time		t_f	—	100	200	
Gate Charge	(V_{DS} = 40 V, I_D = 75 A, V_{GS} = 10 V)	Q_T	—	71	100	nC
		Q_1	—	13	—	
		Q_2	—	33	—	
		Q_3	—	26	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 75 A, V_{GS} = 0) ($C_{pk} \geq 10$)(2)	V_{SD}		0.97	—	Vdc
	(I_S = 20 A, V_{GS} = 0)		—	0.80	1.00	
	(IS = 20 A, V_{GS} = 0, T_J = 125°C)		—	0.68	—	
Reverse Recovery Time	(I_S = 37.5 A, V_{GS} = 0, dI_S/dt = 100 A/μs)	t_{rr}	—	57	—	ns
		t_a	—	40	—	
		t_b	—	17	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.17	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance		L_S				
(Measured from the source lead 0.25″ from package to source bond pad)			—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Reflects Typical Values. C_{pk} = ABSOLUTE VALUE OF (SPEC – AVG) / 3 * SIGMA).
(3) For accurate measurements, good Kelvin contact required.
(4) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS(1)

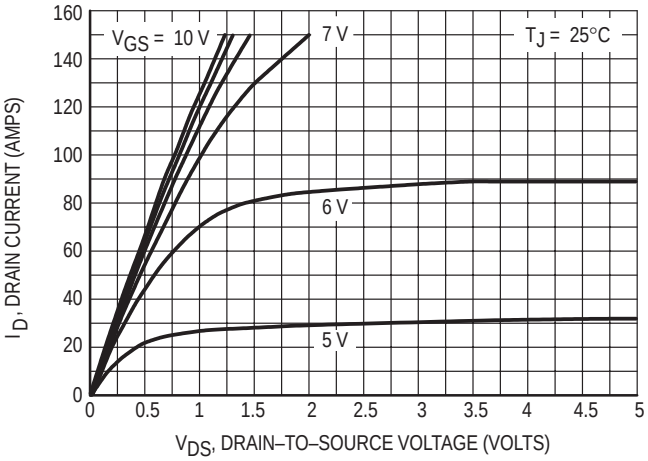


Figure 1. On–Region Characteristics

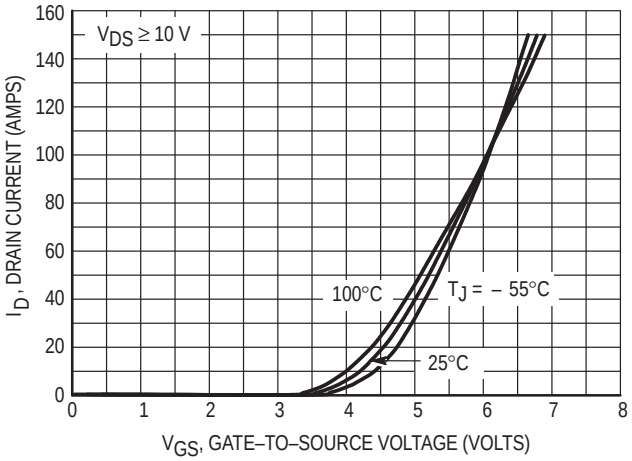


Figure 2. Transfer Characteristics

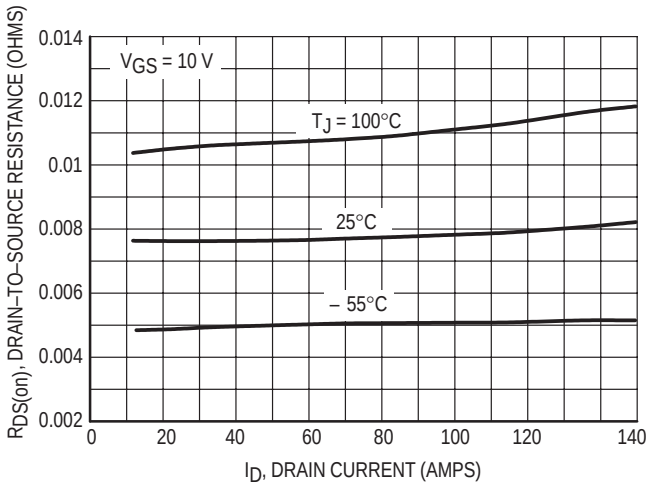


Figure 3. On–Resistance versus Drain Current and Temperature

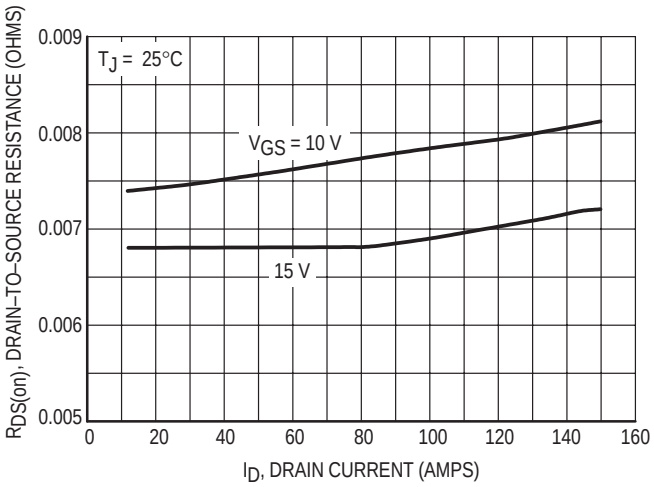


Figure 4. On–Resistance versus Drain Current and Gate Voltage

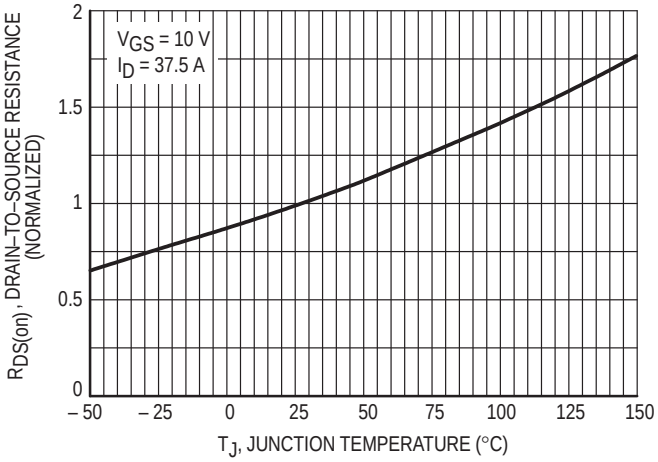


Figure 5. On–Resistance Variation with Temperature

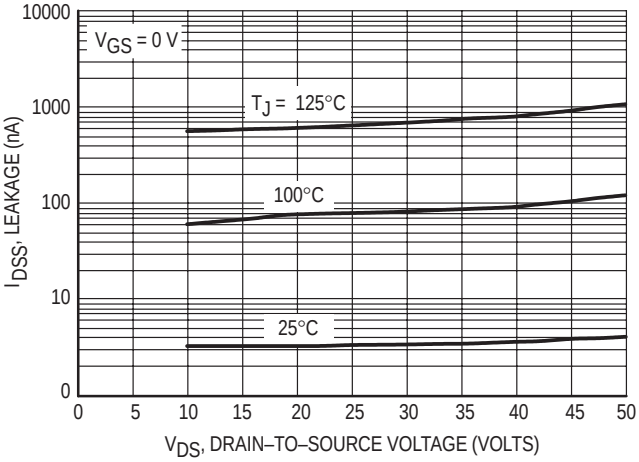


Figure 6. Drain–To–Source Leakage Current versus Voltage

(1)Pulse Tests: Pulse Width ≤ 250 μs, Duty Cycle ≤ 2%.

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in a RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board–mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

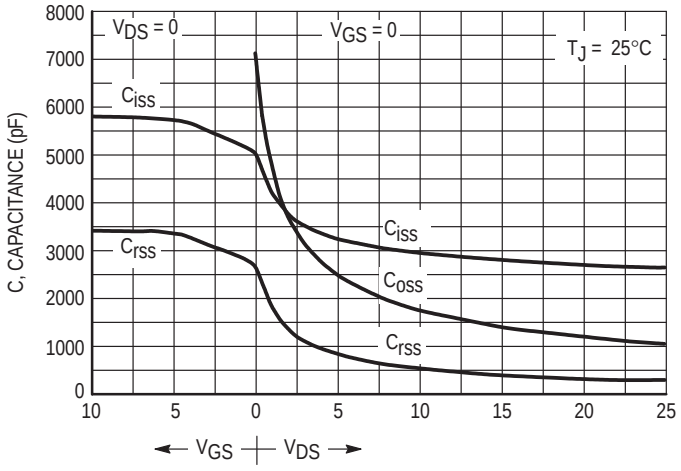


Figure 7. Capacitance Variation

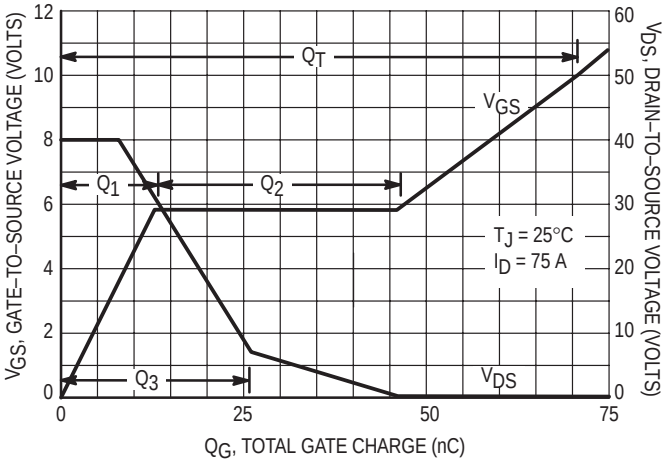


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

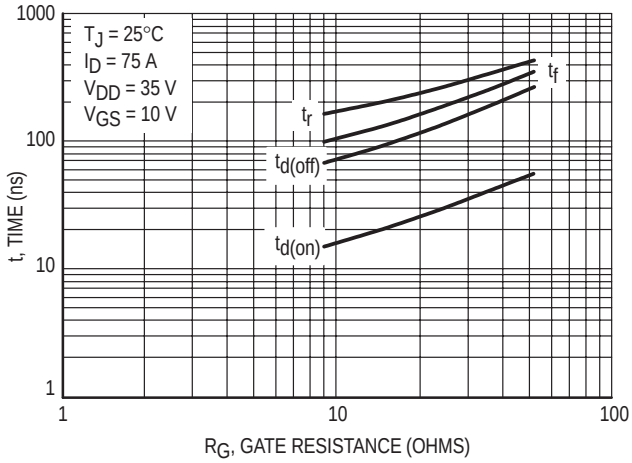


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

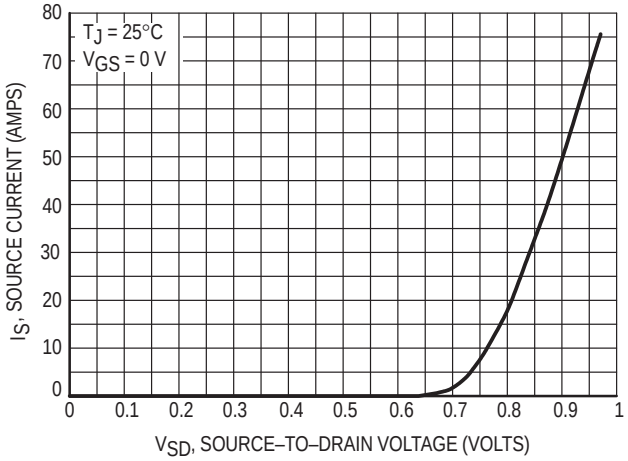


Figure 10. Diode Forward Voltage versus Current

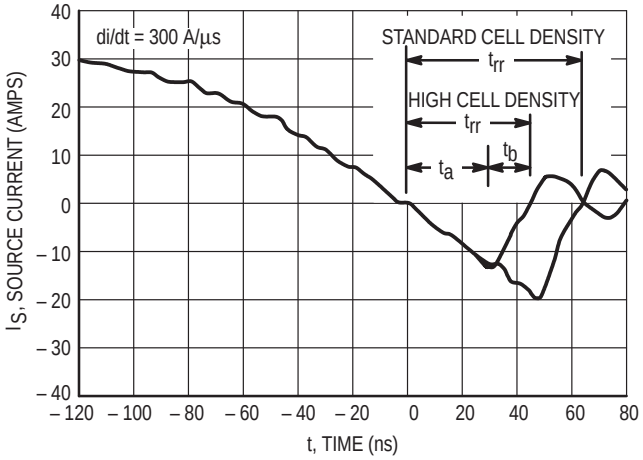


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

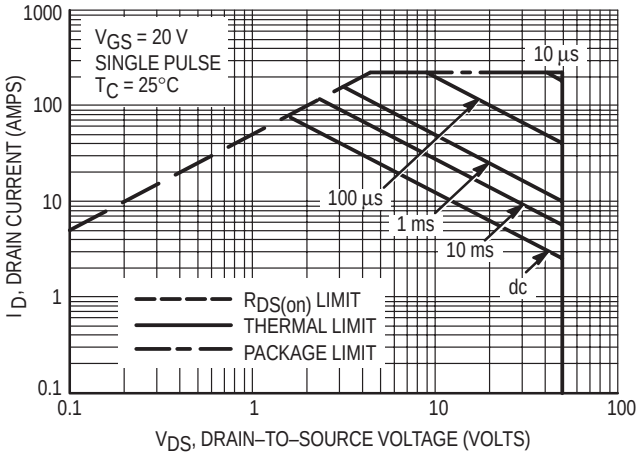


Figure 12. Maximum Rated Forward Biased Safe Operating Area

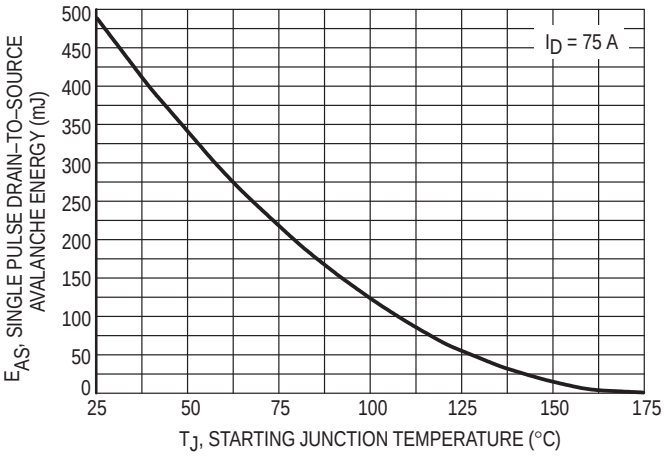


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

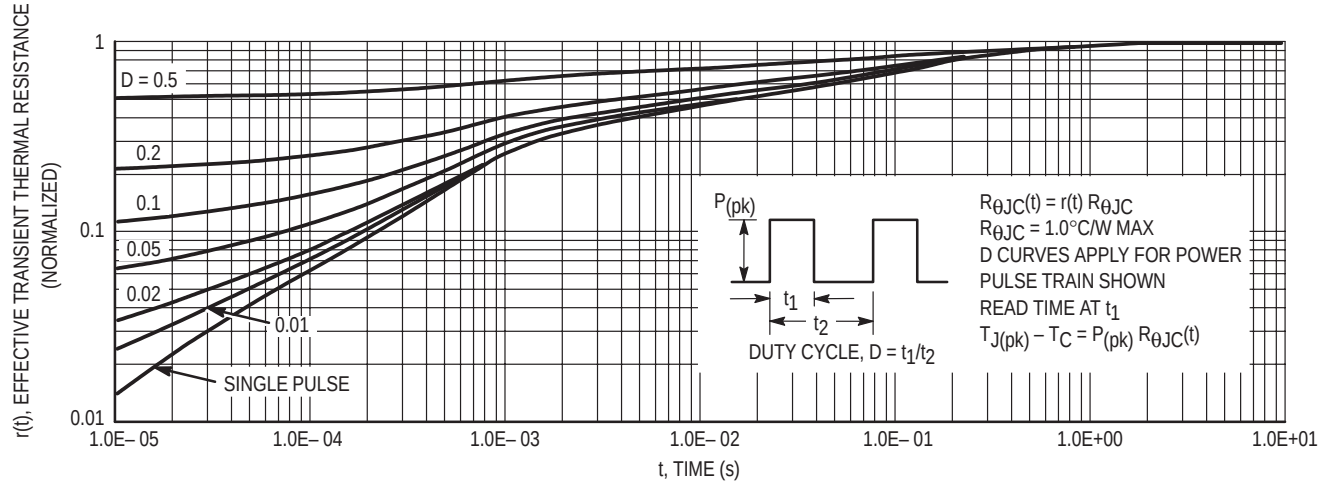


Figure 14. Thermal Response

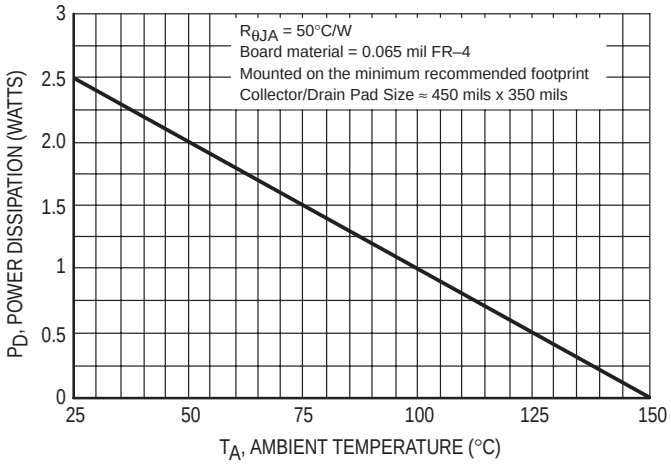


Figure 15. D^{2}PAK Power Derating Curve

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

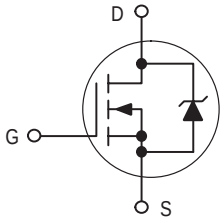
MTD1N50E

Motorola Preferred Device

TMOS POWER FET
1.0 AMPERE
500 VOLTS
$R_{DS(on)}$ = 5.0 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add –T4 Suffix to Part Number



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	500	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	1.0 0.8 3.0	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 μAdc)		$V_{(BR)DSS}$	500	—	—	Vdc
Temperature Coefficient (Positive)			—	480	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.2	4.0	Vdc
Temperature Coefficient (Negative)			—	6.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$R_{DS(on)}$	—	4.3	5.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 1.0 Adc)		$V_{DS(on)}$	—	4.5	6.0	Vdc
(I_D = 0.5 Adc, T_J = 125°C)			—	—	5.3	
Forward Transconductance (V_{DS} = Vdc, I_D = 0.5 Adc)		g_{FS}	0.5	0.9	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 10 Vdc, f = 1.0 MHz)	C_{iss}	—	215	315	pF
Output Capacitance		C_{oss}	—	30.2	42	
Reverse Transfer Capacitance		C_{rss}	—	6.7	12	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.0	20	ns
Rise Time		t_r	—	9.0	10	
Turn–Off Delay Time		$t_{d(off)}$	—	14	30	
Fall Time		t_f	—	17	30	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	7.4	9.0	nC
		Q_1	—	1.6	—	
		Q_2	—	3.8	—	
		Q_3	—	5.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.81	1.2	Vdc
	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.68	—	
Reverse Recovery Time (See Figure 14)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	141	—	ns
		t_a	—	82	—	
		t_b	—	58.5	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.65	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

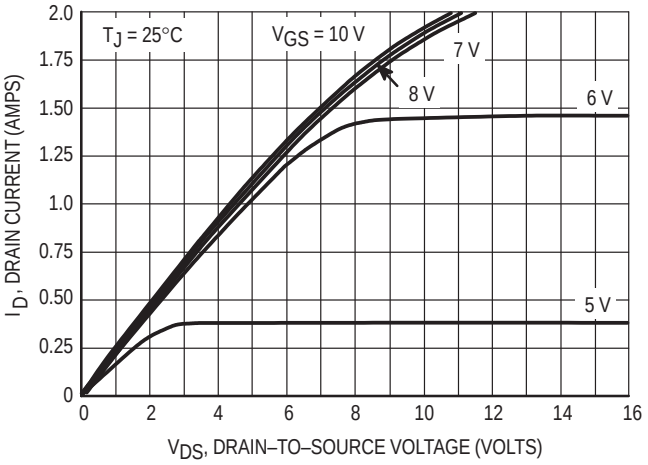


Figure 1. On–Region Characteristics

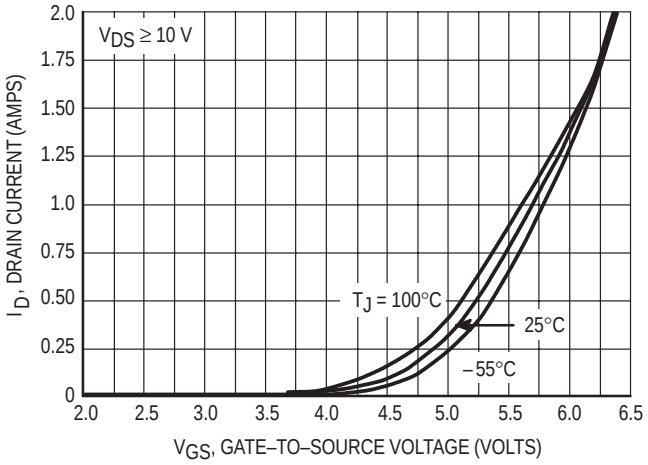


Figure 2. Transfer Characteristics

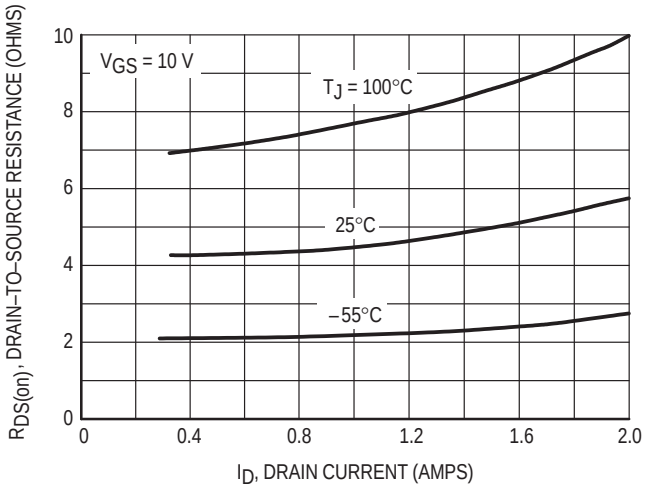


Figure 3. On–Resistance versus Drain Current and Temperature

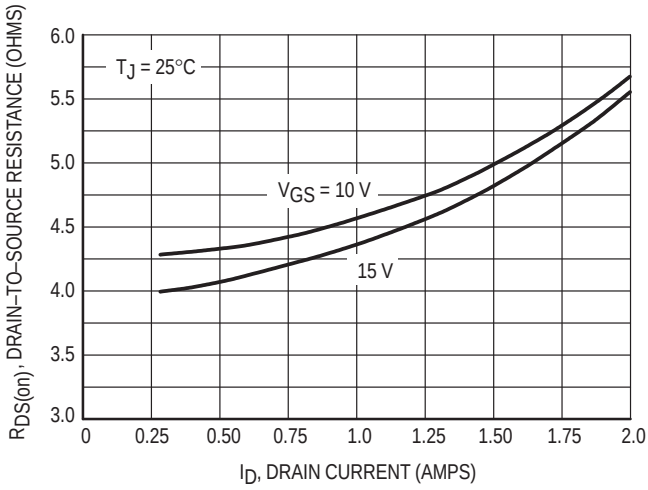


Figure 4. On–Resistance versus Drain Current and Gate Voltage

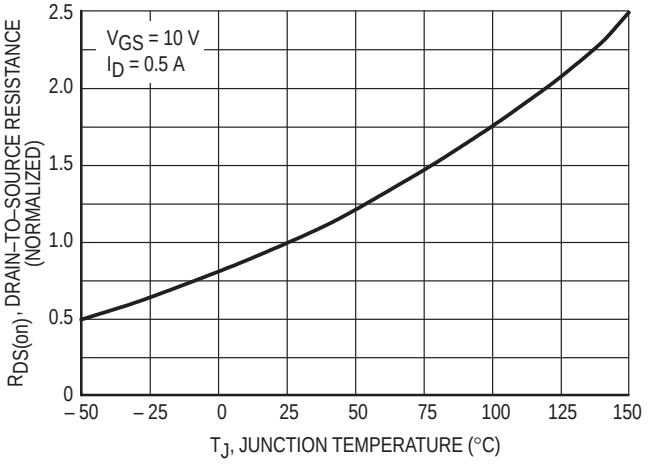


Figure 5. On–Resistance Variation with Temperature

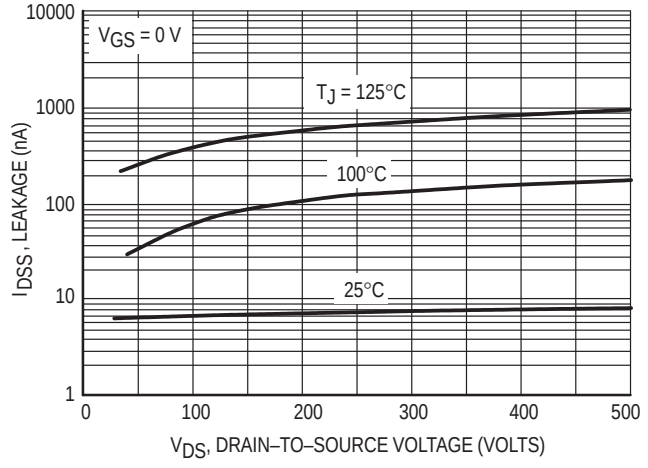


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

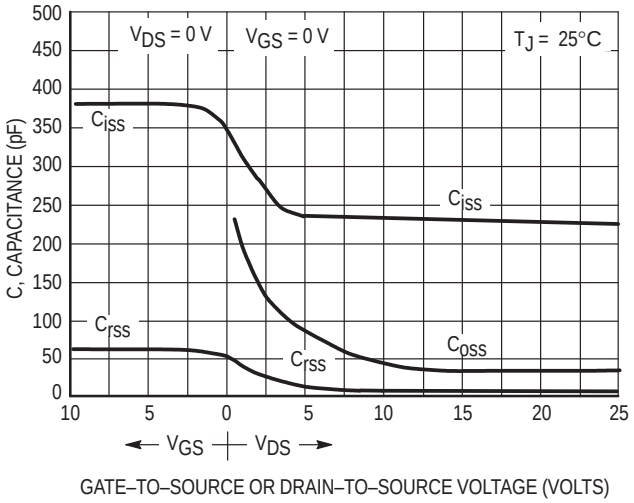


Figure 7a. Capacitance Variation

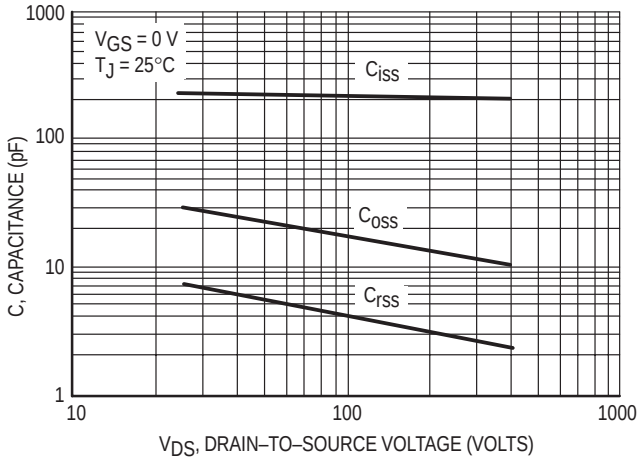


Figure 7b. High Voltage Capacitance Variation

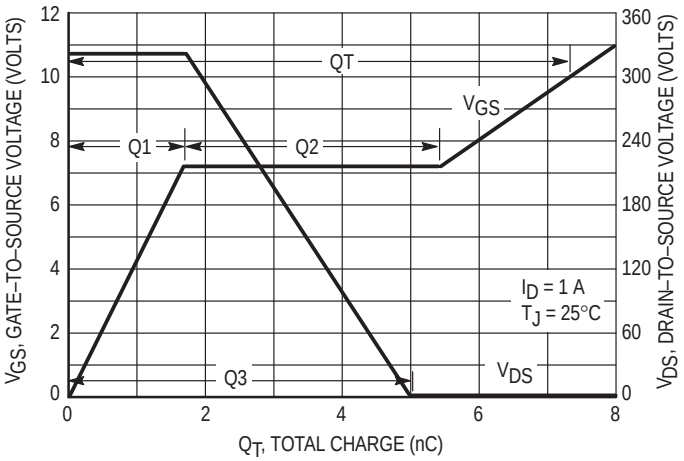


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

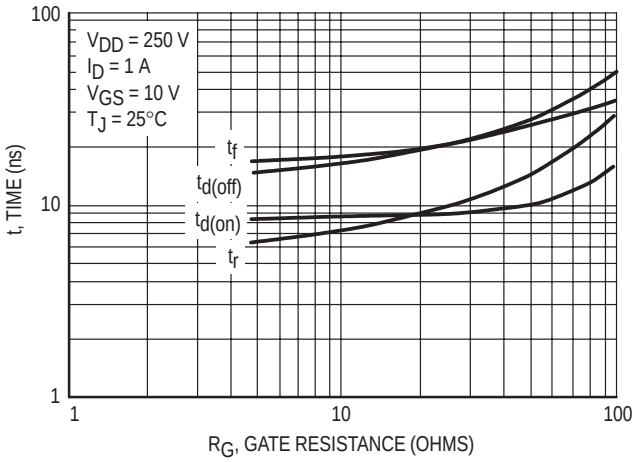


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

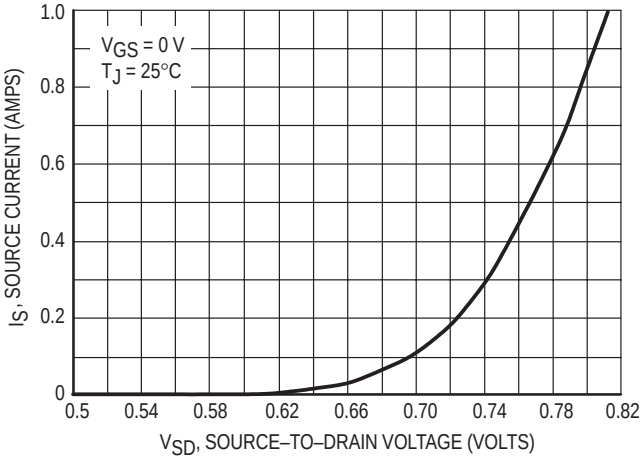


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

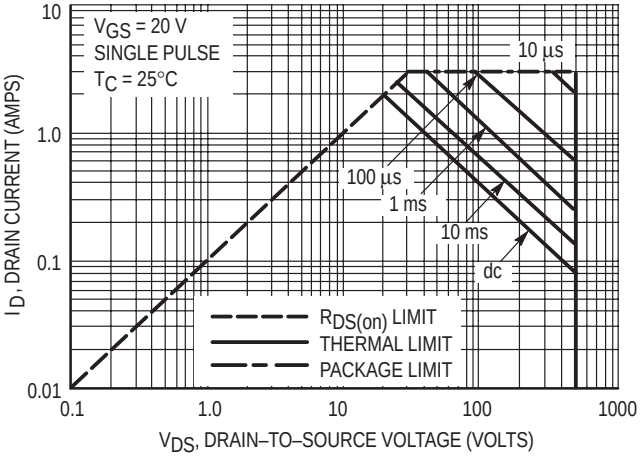


Figure 11. Maximum Rated Forward Biased Safe Operating Area

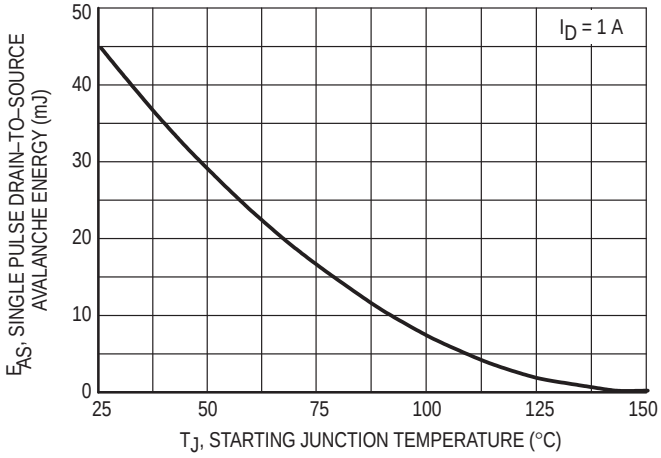


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

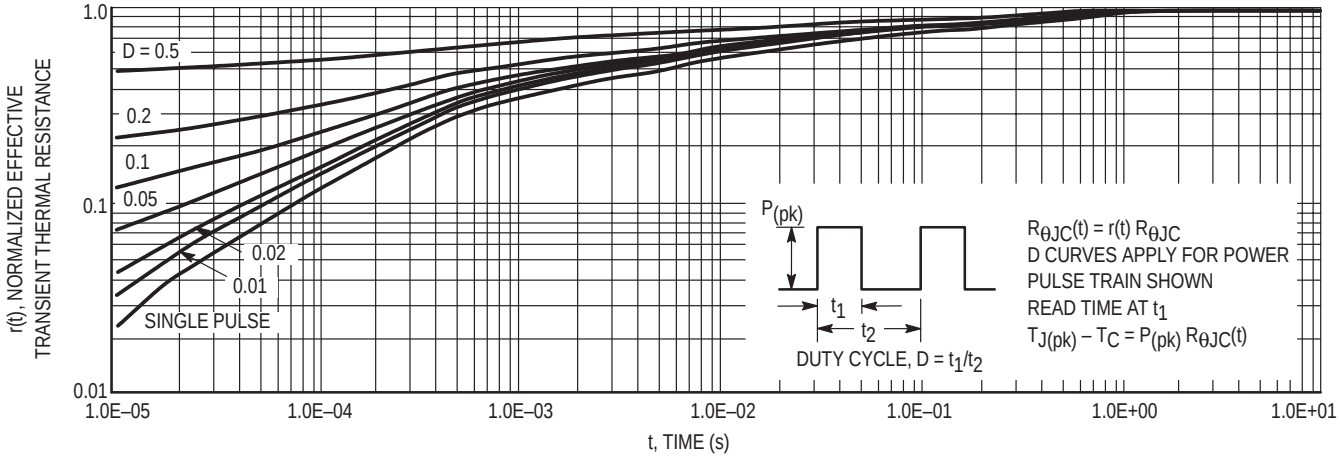


Figure 13. Thermal Response

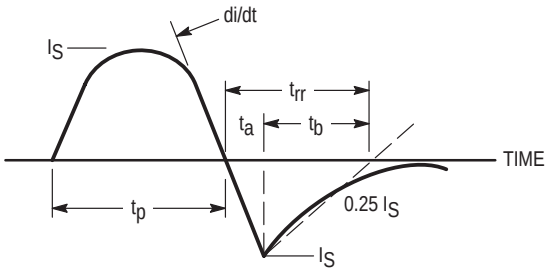


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

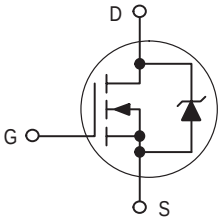
MTD1N60E

Motorola Preferred Device

TMOS POWER FET
1.0 AMPERE
600 VOLTS
$R_{DS(on)}$ = 8.0 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	600	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	1.0 0.8 3.0	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	720	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 600 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.2	4.0	Vdc
Temperature Coefficient (Negative)			—	6.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$R_{DS(on)}$	—	5.9	8.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 1.0 Adc)		$V_{DS(on)}$	—	—	9.6	Vdc
(I_D = 0.5 Adc, T_J = 125°C)			—	—	8.4	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 0.5 Adc)		g_{FS}	0.5	0.8	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	224	310	pF
Output Capacitance		C_{oss}	—	27	40	
Reverse Transfer Capacitance		C_{rss}	—	6.0	10	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 300 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.8	20	ns
Rise Time		t_r	—	6.8	14	
Turn–Off Delay Time		$t_{d(off)}$	—	15	30	
Fall Time		t_f	—	20	40	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	7.1	11	nC
		Q_1	—	1.7	—	
		Q_2	—	3.2	—	
		Q_3	—	3.9	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.82	1.4	Vdc
	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.7	—	
Reverse Recovery Time (See Figure 14)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	464	—	ns
		t_a	—	36	—	
		t_b	—	428	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.629	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

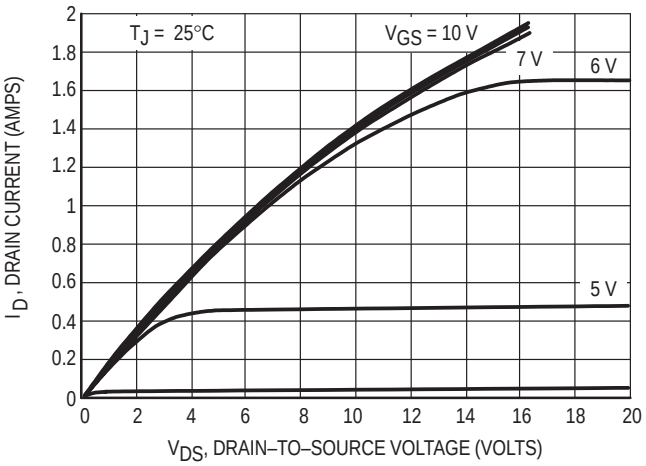


Figure 1. On–Region Characteristics

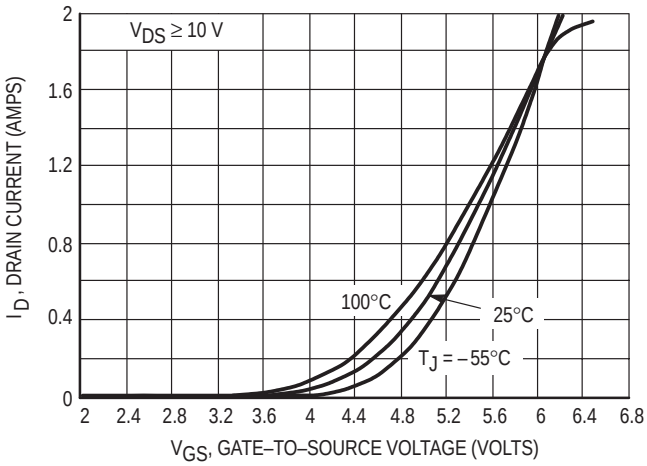


Figure 2. Transfer Characteristics

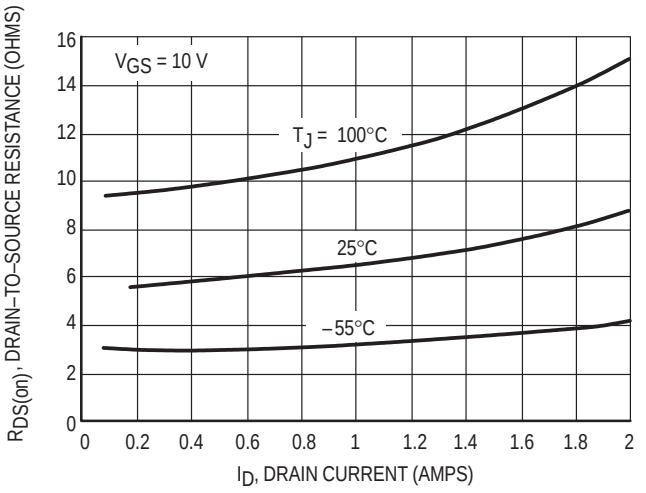


Figure 3. On–Resistance versus Drain Current and Temperature

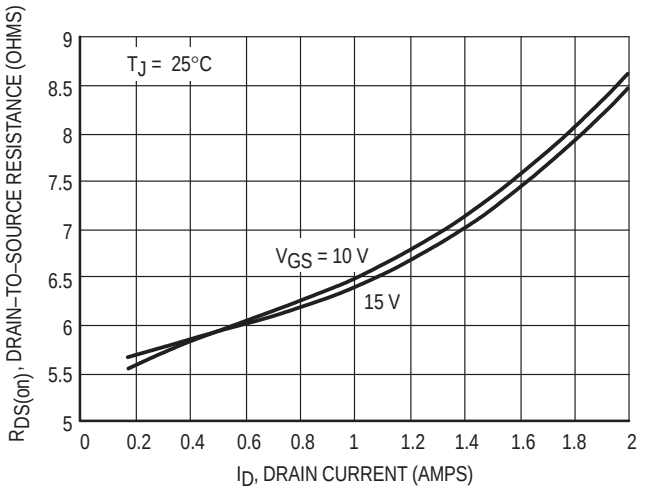


Figure 4. On–Resistance versus Drain Current and Gate Voltage

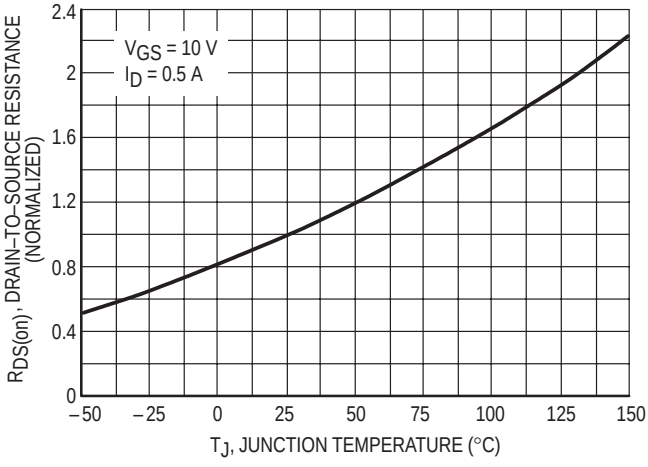
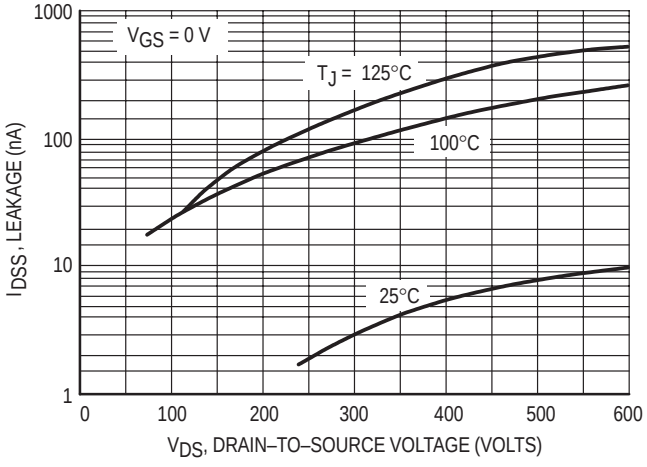


Figure 5. On–Resistance Variation with Temperature



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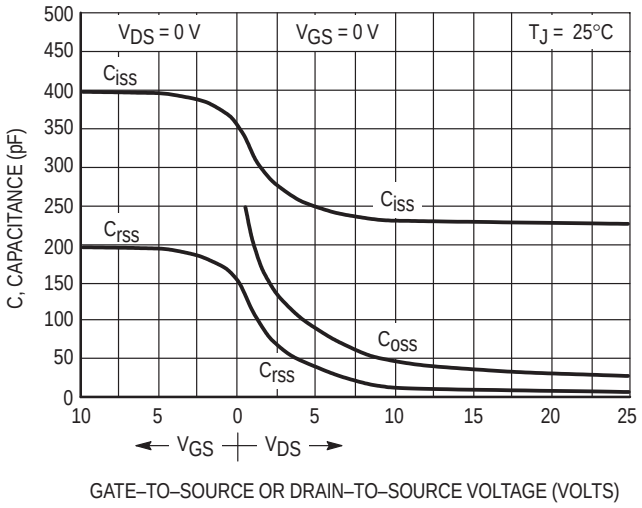

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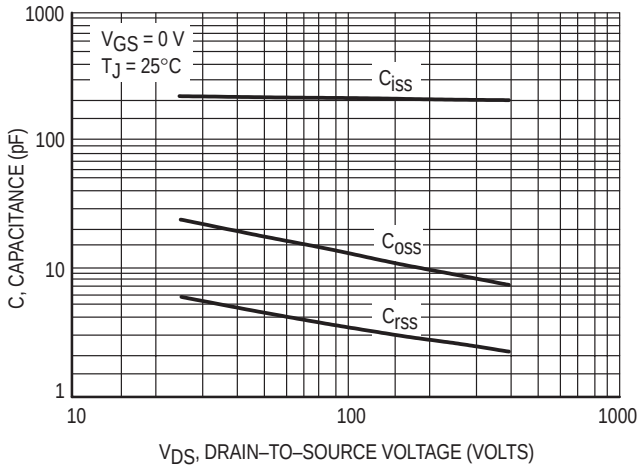
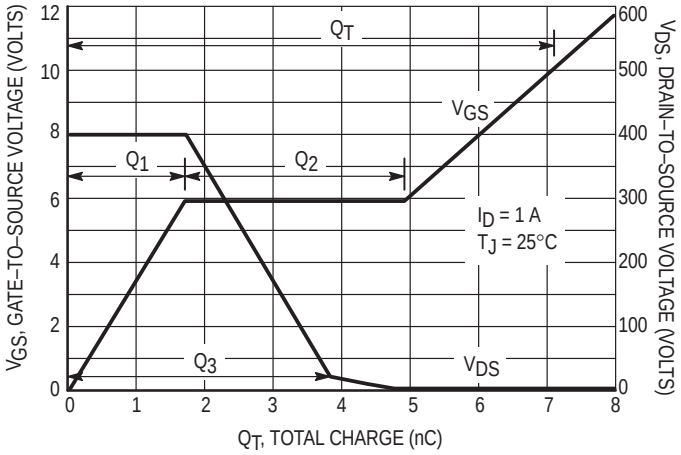


Figure 7b. High Voltage Capacitance Variation



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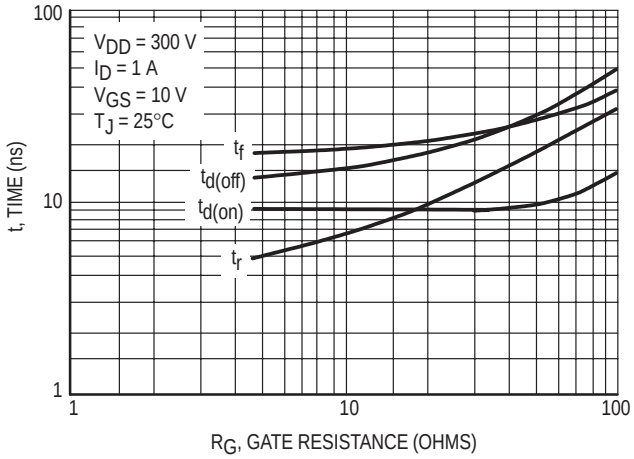

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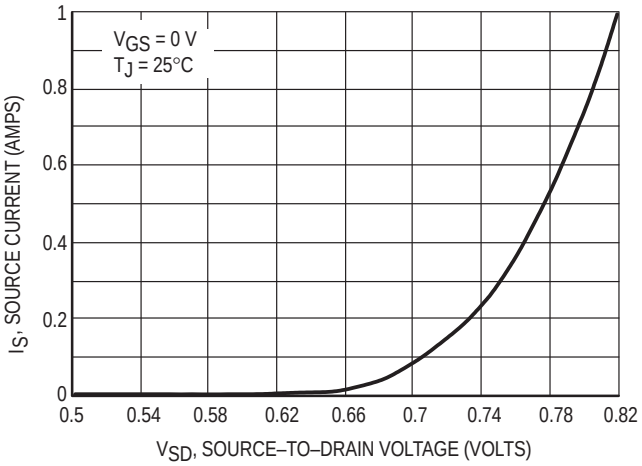
DRAIN–TO–SOURCE DIODE CHARACTERISTICS



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A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

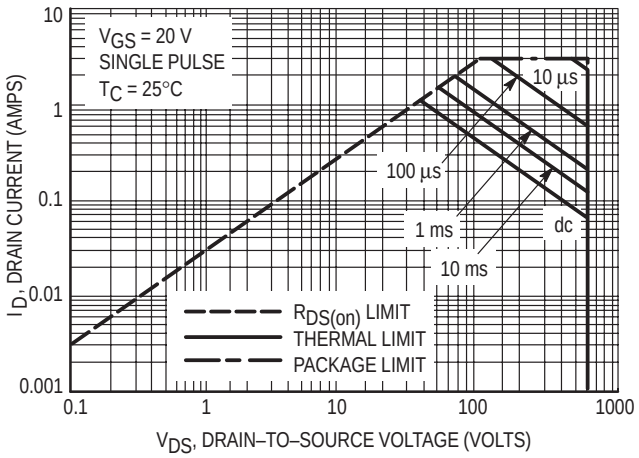


Figure 11. Maximum Rated Forward Biased Safe Operating Area

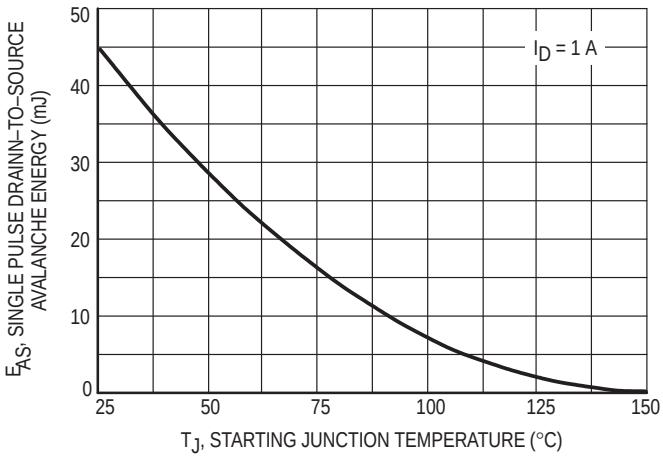


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

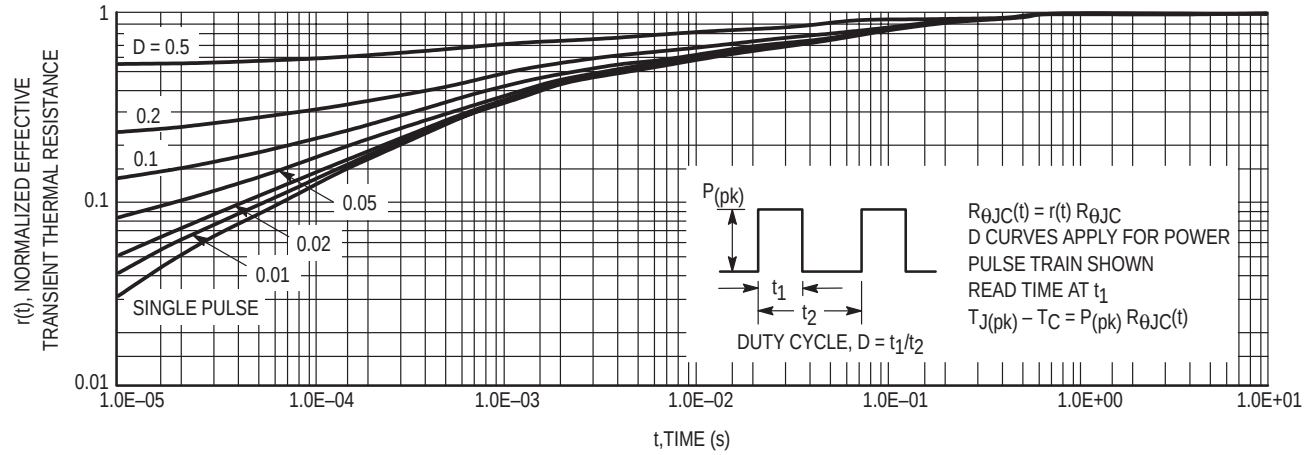


Figure 13. Thermal Response

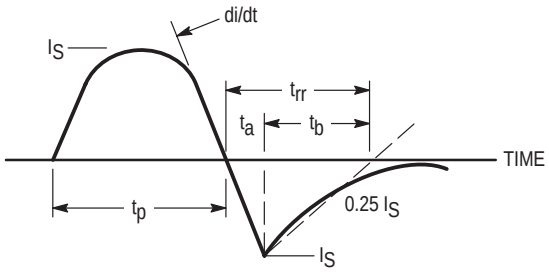


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

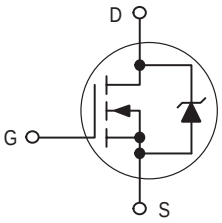
MTD1N80E

Motorola Preferred Device

TMOS POWER FET
1.0 AMPERES
800 VOLTS
$R_{DS(on)}$ = 12 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	800	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	800	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	1.0 0.8 3.0	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	48 0.38 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 2.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	 20	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.6 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.250 μAdc)	$V_{(BR)DSS}$	800	—	—	Vdc
Temperature Coefficient (Positive)		—	981	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 800 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
(V_{DS} = 800 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)	$V_{GS(th)}$	2.0	3.3	4.0	Vdc
Temperature Coefficient (Negative)		—	6.3	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)	$R_{DS(on)}$	—	10.3	12	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)	$V_{DS(on)}$	—	11	14.4	Vdc
(V_{GS} = 10 Vdc, I_D = 0.5 Adc, T_J = 125°C)		—	—	12.6	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 0.5 Adc)	g_{FS}	0.4	0.985	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	—	297	420	pF
Output Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{oss}	—	29	40	
Reverse Transfer Capacitance	C_{rss}	—	6.0	10	
SWITCHING CHARACTERISTICS (2)					
Turn–On Delay Time	$t_{d(on)}$	—	9.0	20	ns
Rise Time (V_{DD} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	t_r	—	10	20	
Turn–Off Delay Time	$t_{d(off)}$	—	20	40	
Fall Time	t_f	—	27	55	
Gate Charge	Q_T	—	9.6	20	nC
(V_{DS} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc)	Q_1	—	2.1	—	
	Q_2	—	4.2	—	
	Q_3	—	4.7	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (1) (I_S = 1.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.82	1.2	Vdc
(I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.7	—	
Reverse Recovery Time	t_{rr}	—	317	—	ns
(I_S = 1.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_a	—	56	—	
	t_b	—	261	—	
Reverse Recovery Stored Charge	Q_{RR}	—	0.93	—	μC
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)	L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

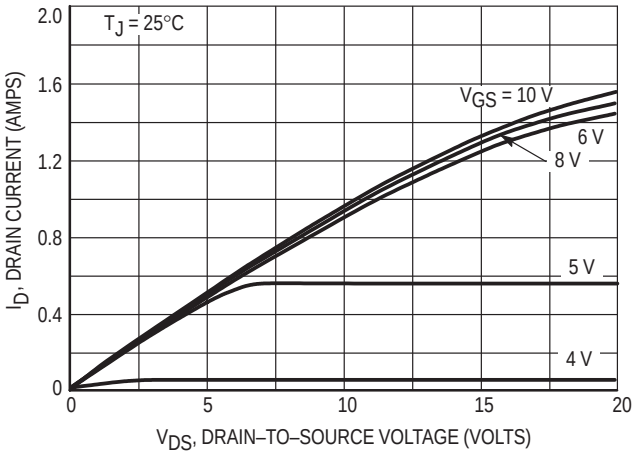


Figure 1. On–Region Characteristics

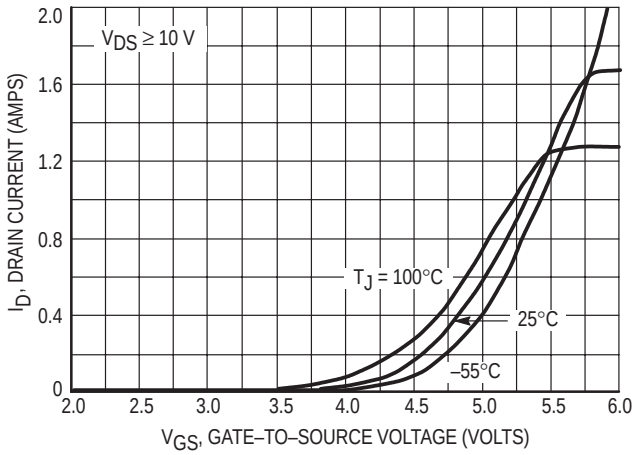


Figure 2. Transfer Characteristics

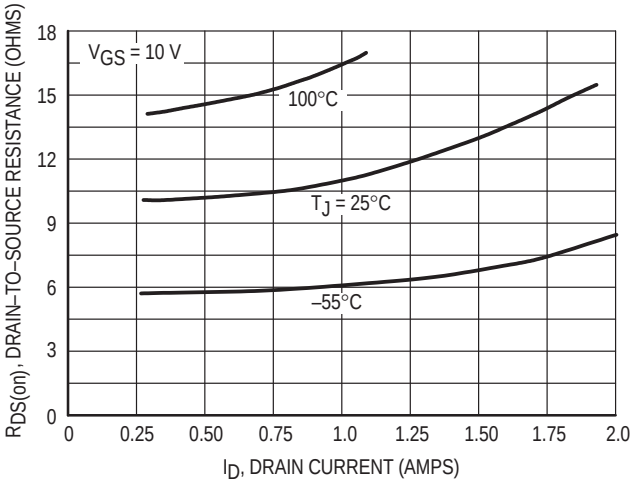


Figure 3. On–Resistance versus Drain Current and Temperature

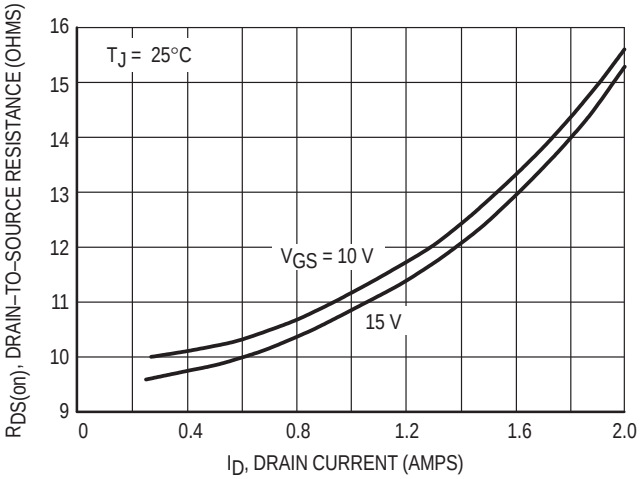


Figure 4. On–Resistance versus Drain Current and Gate Voltage

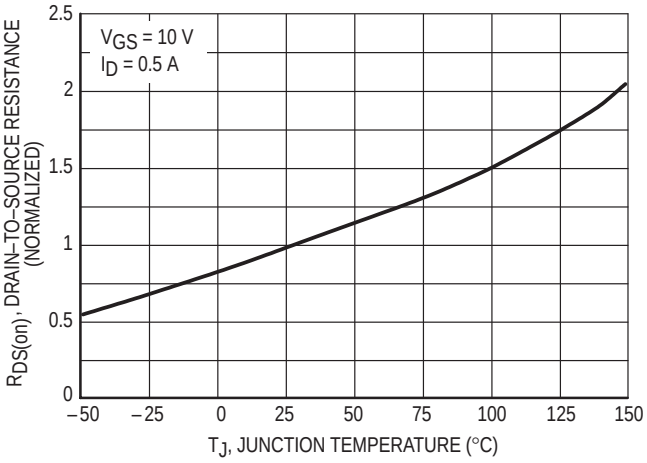


Figure 5. On–Resistance Variation with Temperature

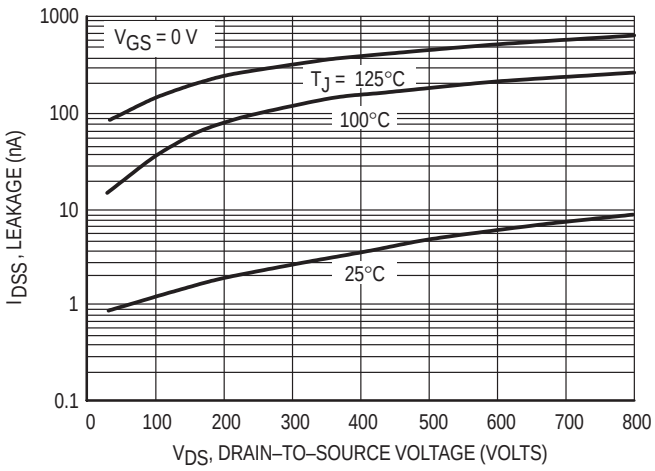


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

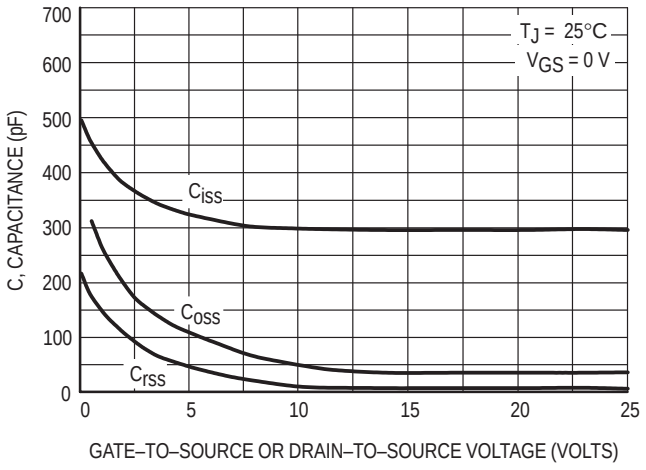


Figure 7a. Capacitance Variation

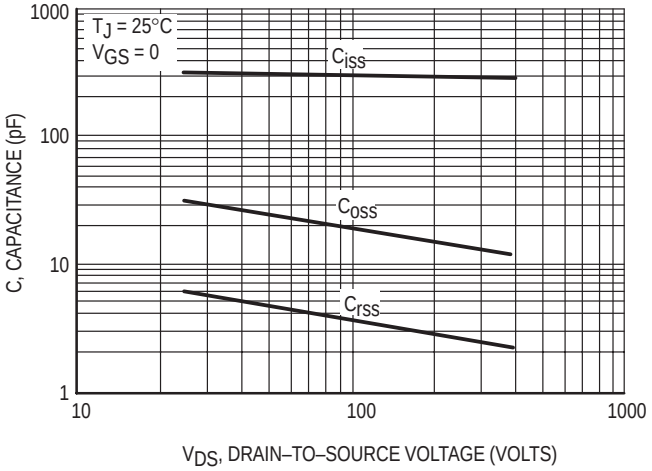


Figure 7b. High Voltage Capacitance Variation

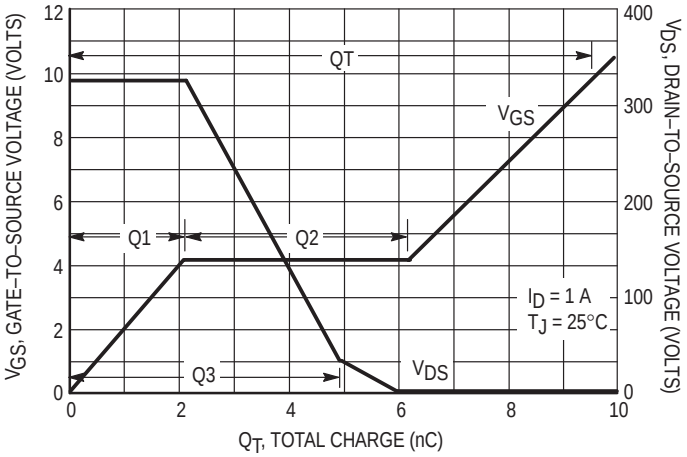


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

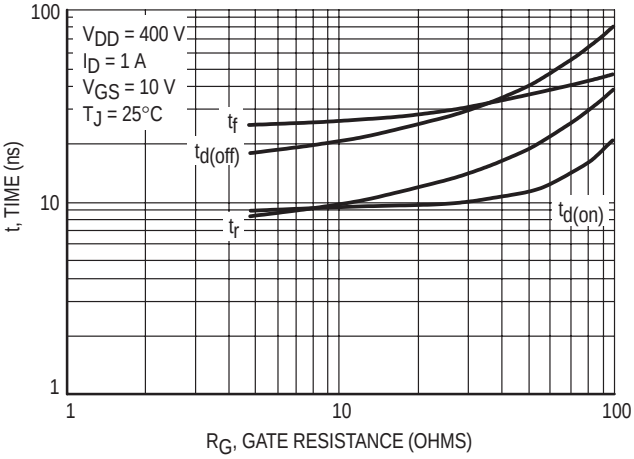


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

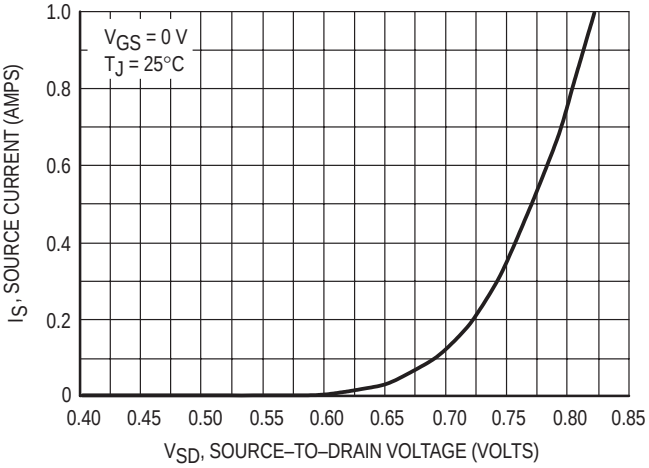


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

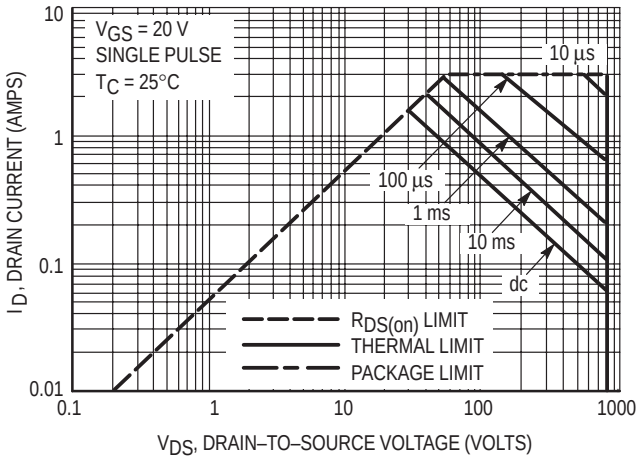


Figure 11. Maximum Rated Forward Biased Safe Operating Area

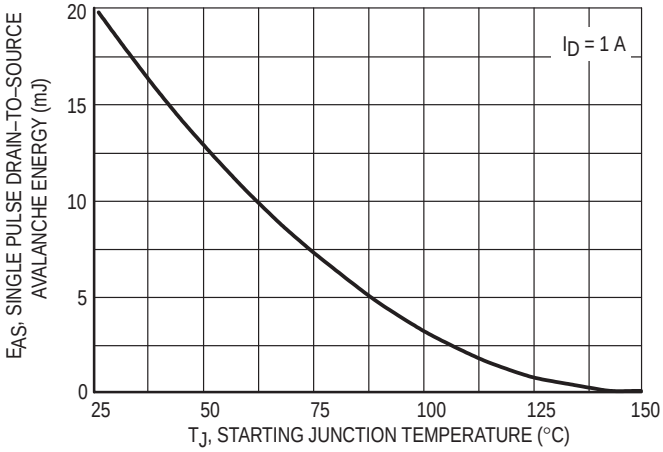


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

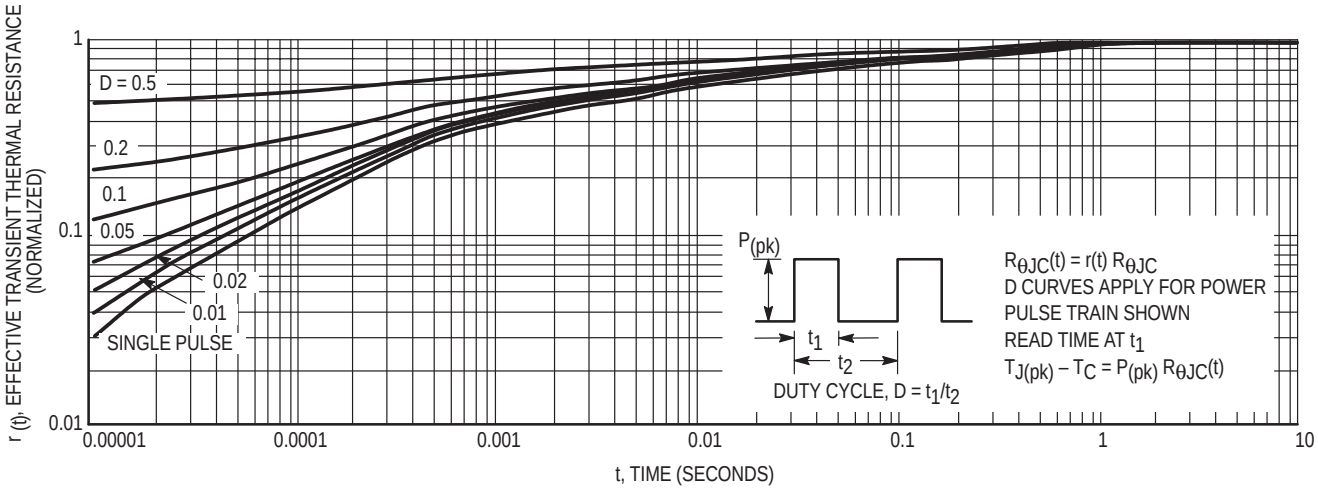


Figure 13. Thermal Response

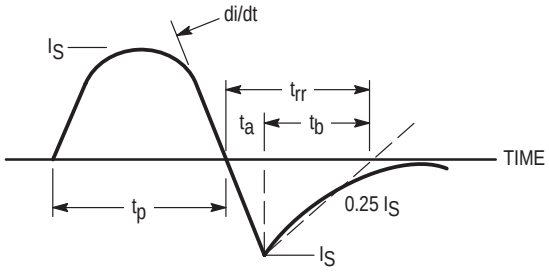


Figure 14. Diode Reverse Recovery Waveform

Product Preview

TMOS E-FET™
High Energy Power FET
P–Channel Enhancement–Mode Silicon Gate

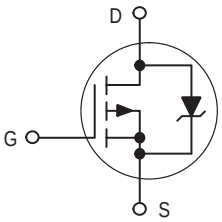
MTD1P50E

Motorola Preferred Device

TMOS POWER FET
1.0 AMPERES
500 VOLTS
15 Ω

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor–Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



CASE 369A–13, Style 2
DPAK Surface Mount

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	500	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–to–Source Voltage — Continuous — Single Pulse ($t_p \le 50$ μs)	V_{GS} V_{GSM}	±20 ±40	Vdc
Drain Current — Continuous @ T_C = 25°C — Continuous @ T_C = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	1.0 0.8 4.0	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_C = 25°C, when mounted to minimum recommended pad size	P_D	50 0.4 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.5 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	500 —	— TBD	— —	Vdc V/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.1 TBD	4.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$R_{DS(on)}$	—	12	15	Ohms
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 1.0 Adc) (I_D = 0.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	18 15.8	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 0.5 Adc)		g_{FS}	0.4	0.6	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	TBD	TBD	pF
Output Capacitance		C_{oss}	—	TBD	TBD	
Transfer Capacitance		C_{rss}	—	TBD	TBD	
SWITCHING CHARACTERISTICS*						
Turn–On Delay Time	(V_{DS} = 250 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	TBD	TBD	ns
Rise Time		t_r	—	TBD	TBD	
Turn–Off Delay Time		$t_{d(off)}$	—	TBD	TBD	
Fall Time		t_f	—	TBD	TBD	
Gate Charge	(V_{DS} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	TBD	TBD	nC
		Q_1	—	TBD	—	
		Q_2	—	TBD	—	
		Q_3	—	TBD	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 1.0 Adc, V_{GS} = 0 Vdc) (I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	2.0 TBD	3.5 —	Vdc
Reverse Recovery Time	(I_S = 1.0 Adc, dI_S/dt = 100 A/μs)	t_{rr}	—	TBD	—	ns
		t_a	—	TBD	—	
		t_b	—	TBD	—	
Reverse Recovery Stored Charge		Q_{RR}	—	TBD	—	μC

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

Designer's™ Data Sheet

TMOS E-FET™
High Energy Power FET
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

MTD2N40E

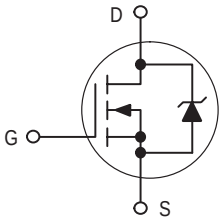
Motorola Preferred Device

TMOS POWER FET
2.0 AMPERES
400 VOLTS
$R_{DS(on)}$ = 3.5 OHM

CASE 369A–13, Style 2
DPAK

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche and switch efficiently. This new high energy device also offers a drain–to–soure diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add –T4 Suffix to Part Number
- Replaces MTD1N40E



MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	400	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous @ T_C = 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	2.0 1.5 6.0	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_C = 25°C, when mounted to minimum recommended pad size	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	400	—	—	Vdc
Temperature Coefficient (Positive)			—	451	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 400 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 400 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	2.0	3.2	4.0	Vdc
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	—	3.1	3.5	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 2.0 Adc)		$V_{DS(on)}$	—	7.3	8.4	Vdc
(I_D = 1.0 Adc, T_J = 125°C)			—	—	7.4	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.0 Adc)		g_{FS}	0.5	1.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	229	320	pF
Output Capacitance		C_{oss}	—	34	40	
Reverse Transfer Capacitance		C_{rss}	—	7.3	10	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 200 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.0	16	ns
Rise Time		t_r	—	8.4	14	
Turn–Off Delay Time		$t_{d(off)}$	—	12	26	
Fall Time		t_f	—	11	20	
Gate Charge	(V_{DS} = 320 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	8.6	12	nC
		Q_1	—	2.6	—	
		Q_2	—	3.2	—	
		Q_3	—	5.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.88	1.2	Vdc
	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.76	—	
Reverse Recovery Time	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	156	—	ns
		t_a	—	99	—	
		t_b	—	57	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.89	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

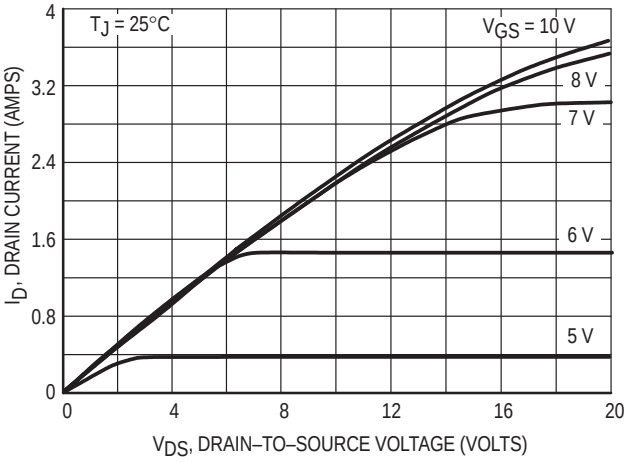


Figure 1. On–Region Characteristics

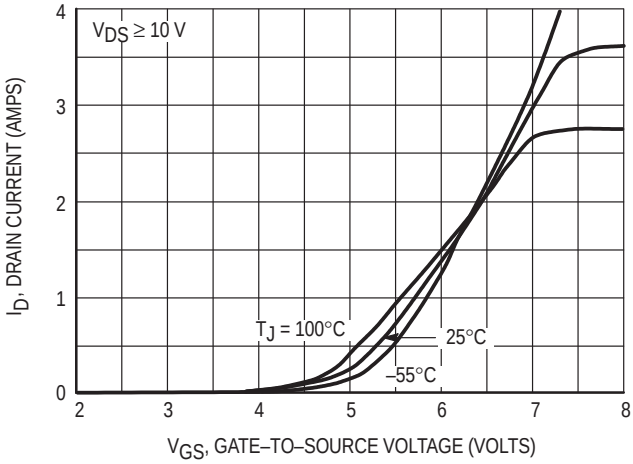


Figure 2. Transfer Characteristics

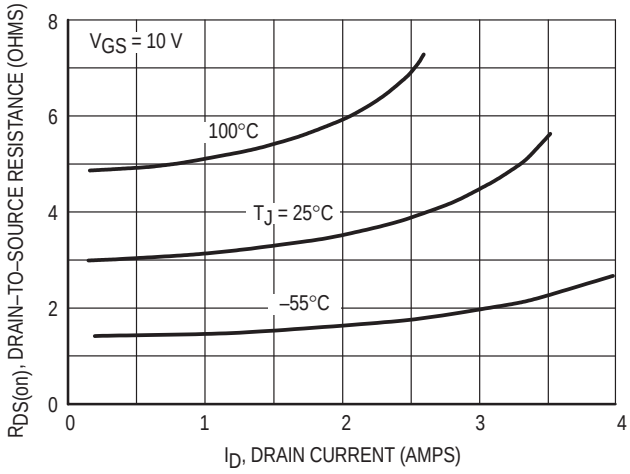


Figure 3. On–Resistance versus Drain Current and Temperature

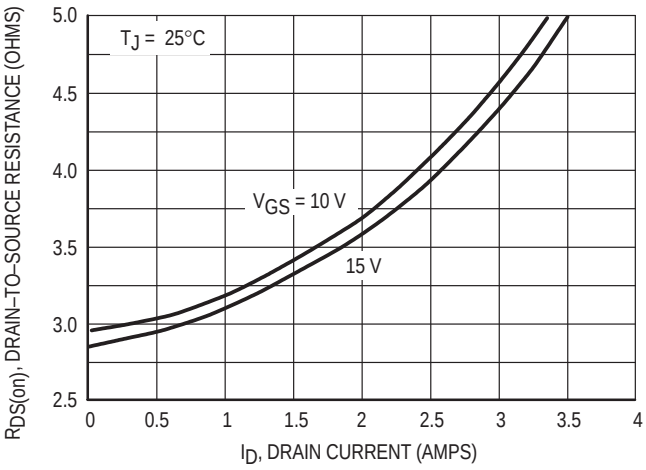


Figure 4. On–Resistance versus Drain Current and Gate Voltage

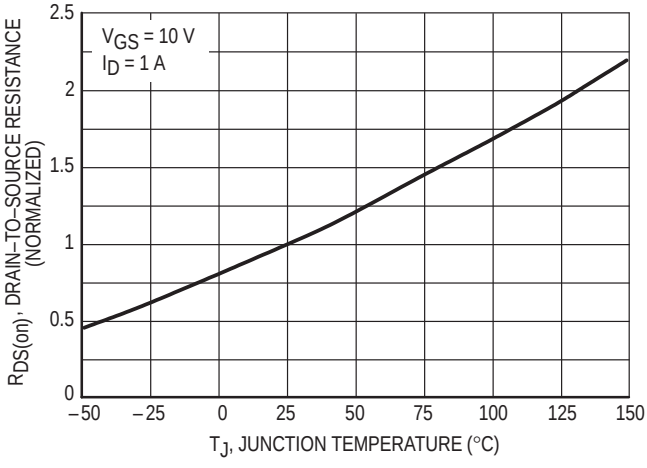


Figure 5. On–Resistance Variation with Temperature

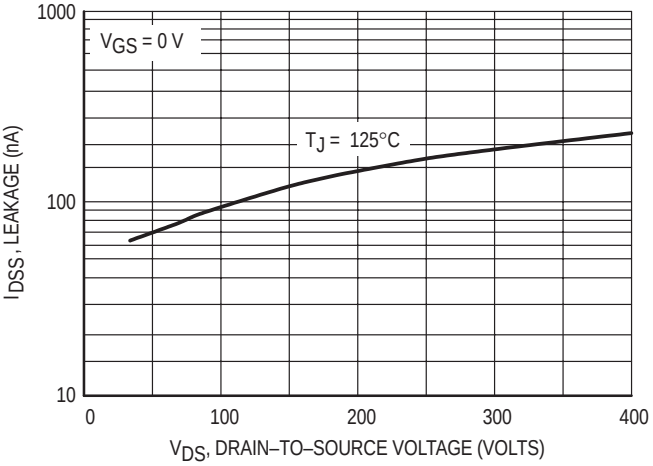


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

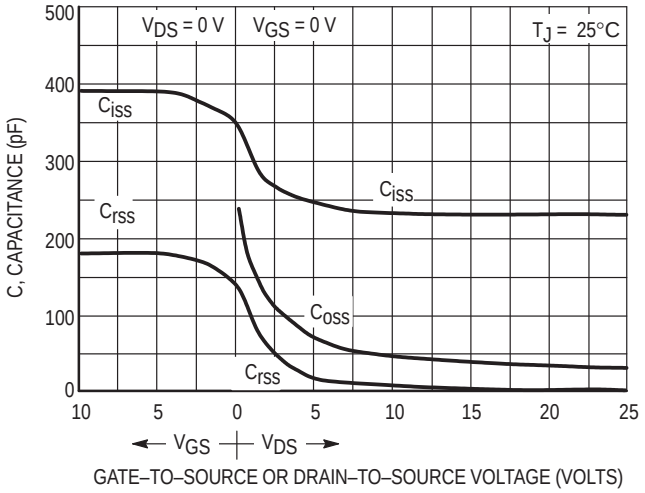


Figure 7a. Capacitance Variation

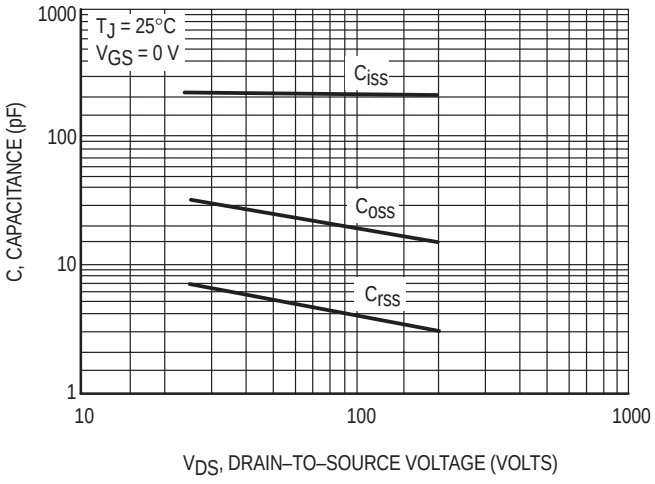


Figure 7b. High Voltage Capacitance Variation

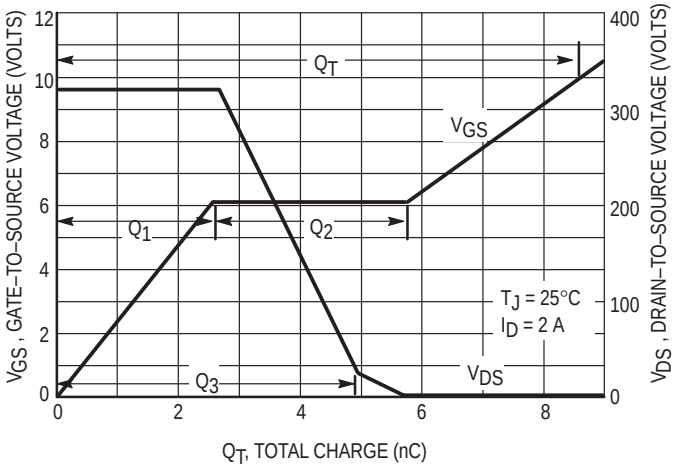


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

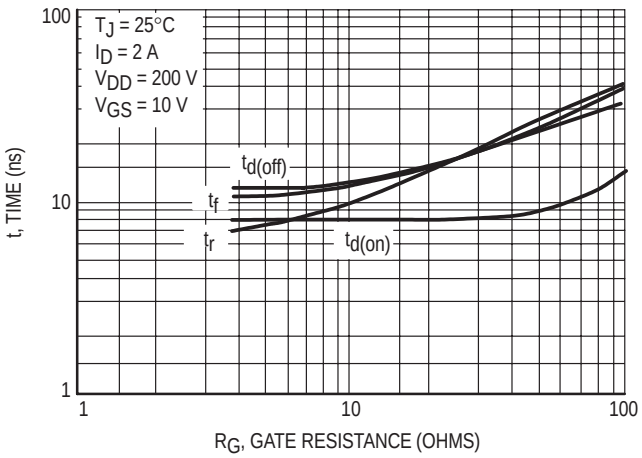


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

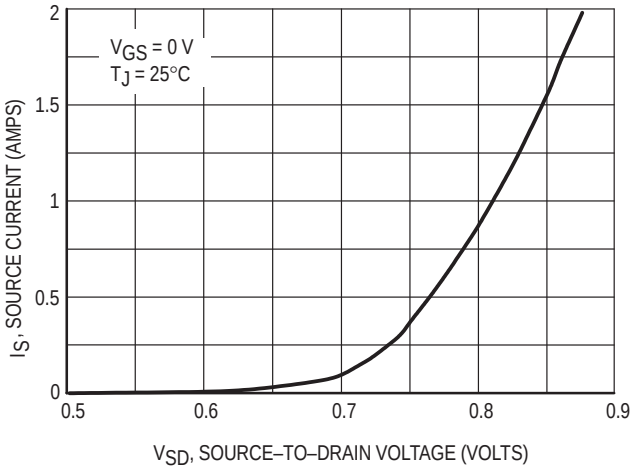


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

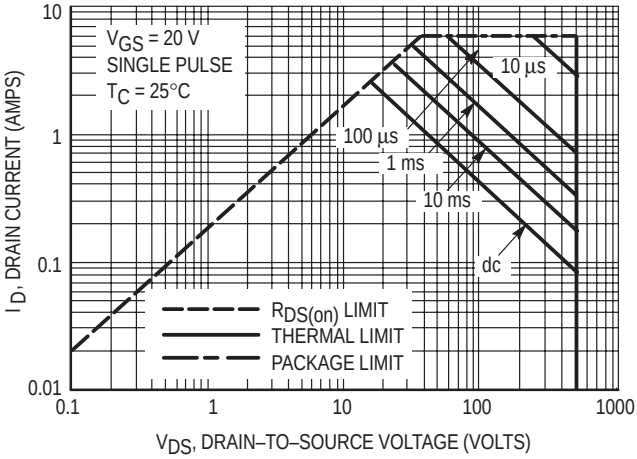


Figure 11. Maximum Rated Forward Biased Safe Operating Area

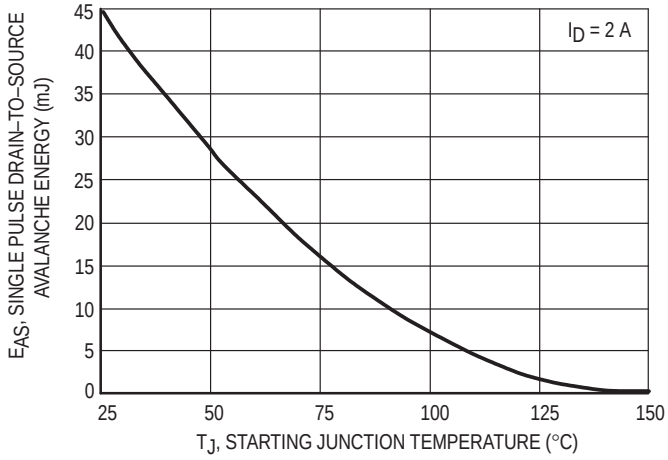


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

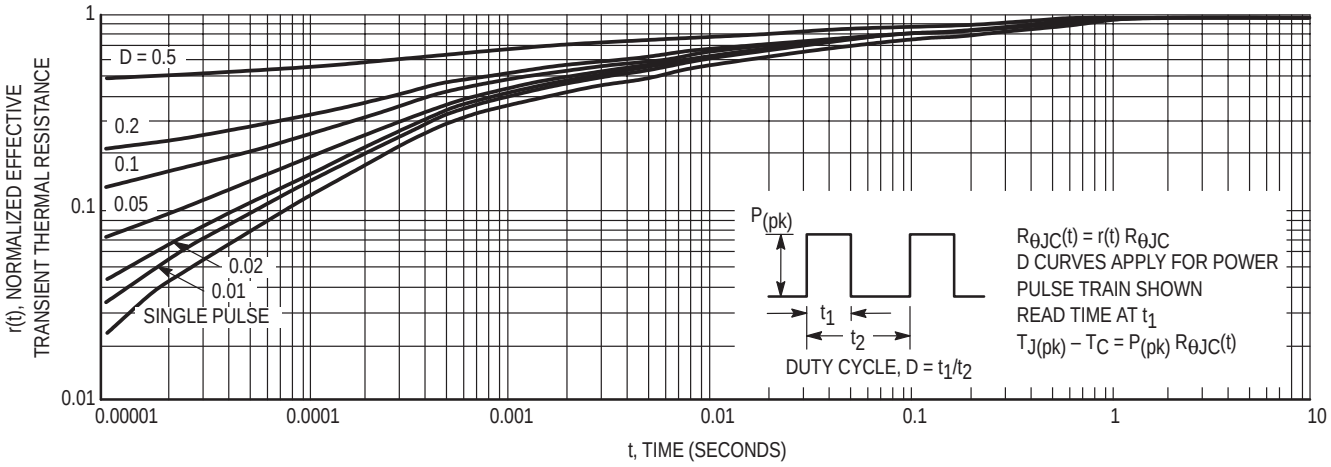


Figure 13. Thermal Response

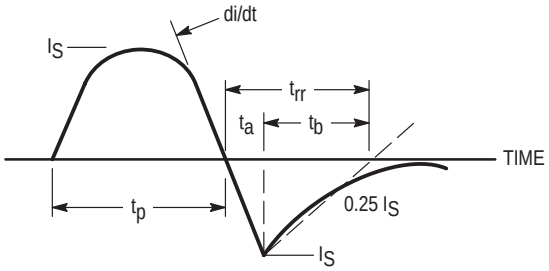


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

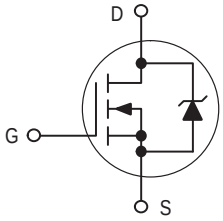
MTD2N50E

Motorola Preferred Device

TMOS POWER FET
2.0 AMPERES
500 VOLTS
$R_{DS(on)}$ = 3.6 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number
- Replaces MTD2N50



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	2.0 1.5 6.0	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 75 Vdc, V_{GS} = 10 Vdc, I_L = 2.0 Apk, L = 50 mH, R_G = 25 Ω)	E_{AS}	100	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	500 —	— 562	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	0.1 1.0	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	— 6.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	—	2.7	3.6	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 2.0 Adc) (I_D = 1.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	6.0 —	8.64 6.48	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.0 Adc)		g_{FS}	1.2	1.6	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	323	450	pF
Output Capacitance		C_{oss}	—	45	63	
Reverse Transfer Capacitance		C_{rss}	—	9.0	20	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.0	20	ns
Rise Time		t_r	—	6.0	20	
Turn–Off Delay Time		$t_{d(off)}$	—	16	30	
Fall Time		t_f	—	10	20	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	11	15	nC
		Q_1	—	2.0	—	
		Q_2	—	5.4	—	
		Q_3	—	5.1	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.8 0.69	1.6 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	334	—	ns
		t_a	—	62	—	
		t_b	—	272	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.99	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

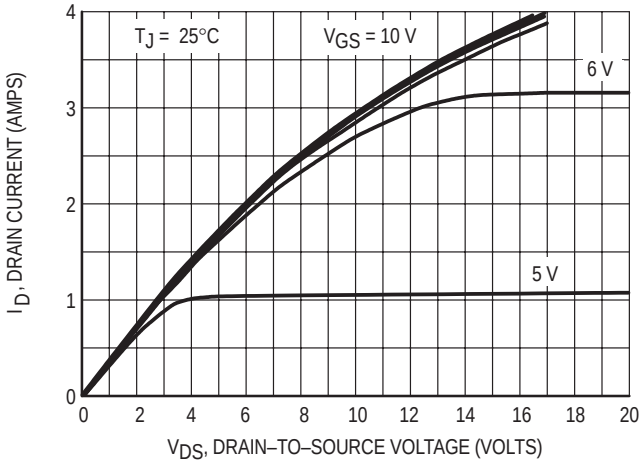


Figure 1. On–Region Characteristics

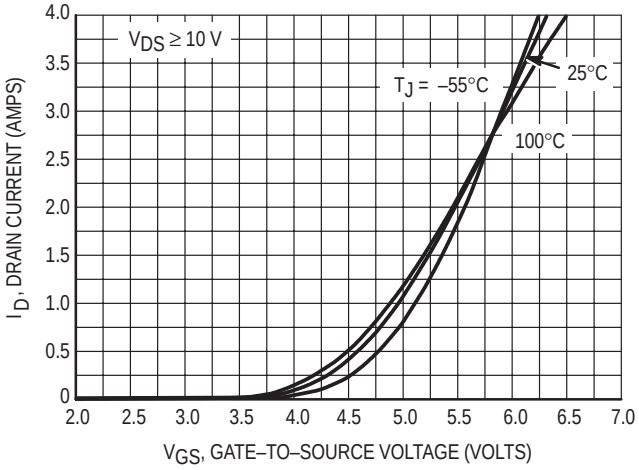


Figure 2. Transfer Characteristics

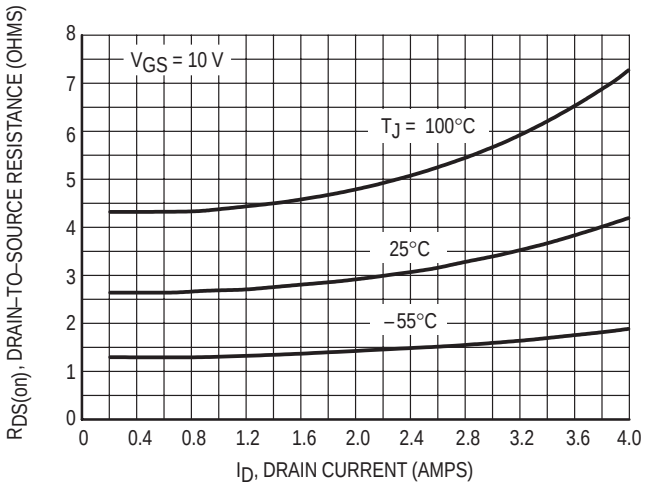


Figure 3. On–Resistance versus Drain Current and Temperature

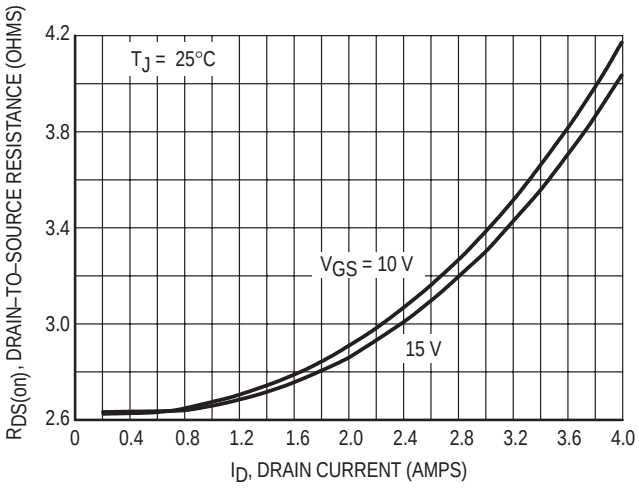


Figure 4. On–Resistance versus Drain Current and Gate Voltage

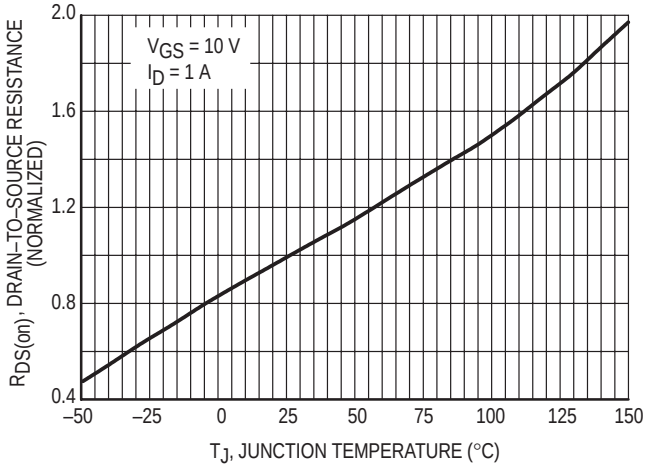


Figure 5. On–Resistance Variation with Temperature

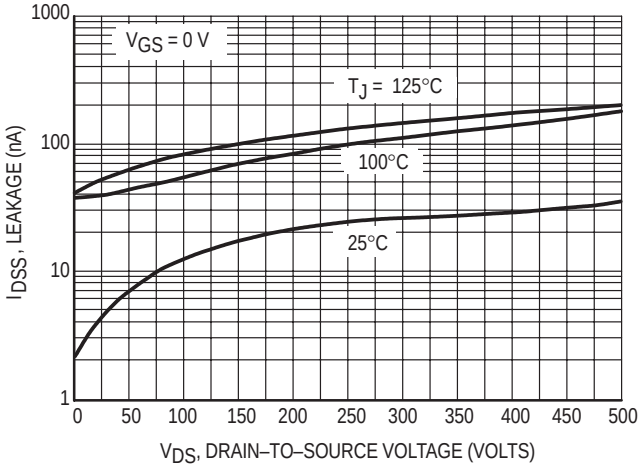


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

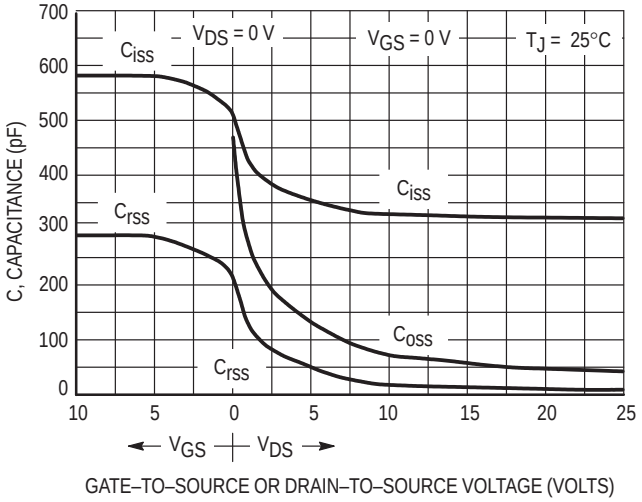


Figure 7a. Capacitance Variation

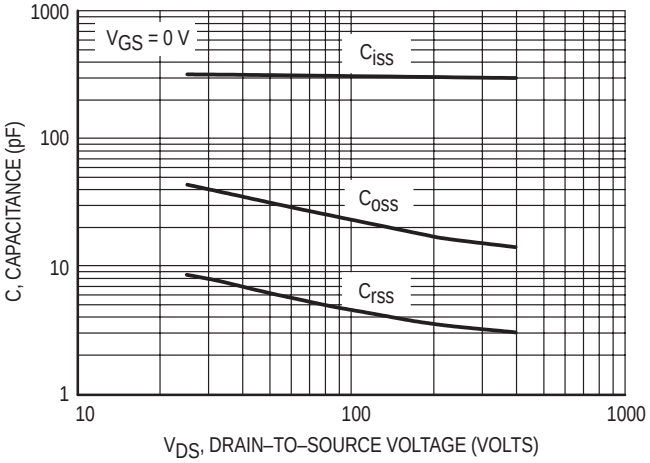


Figure 7b. High Voltage Capacitance Variation

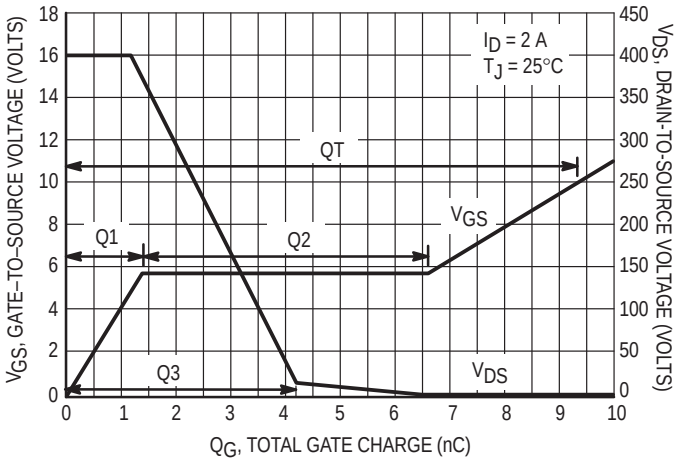


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

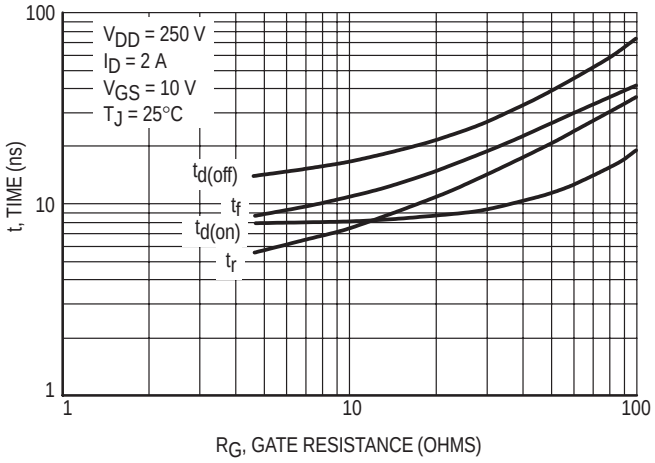


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

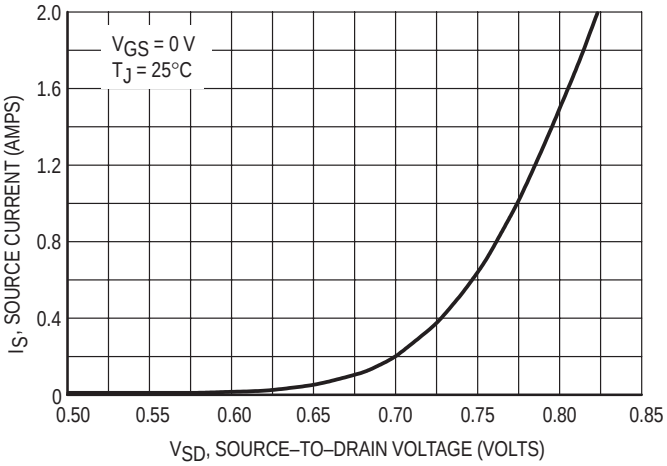


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

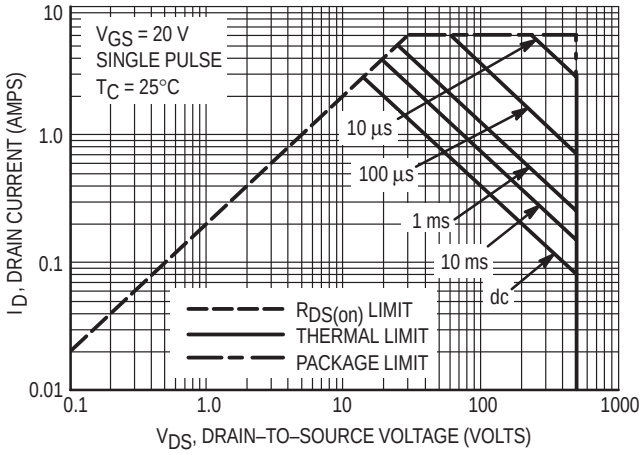


Figure 11. Maximum Rated Forward Biased Safe Operating Area

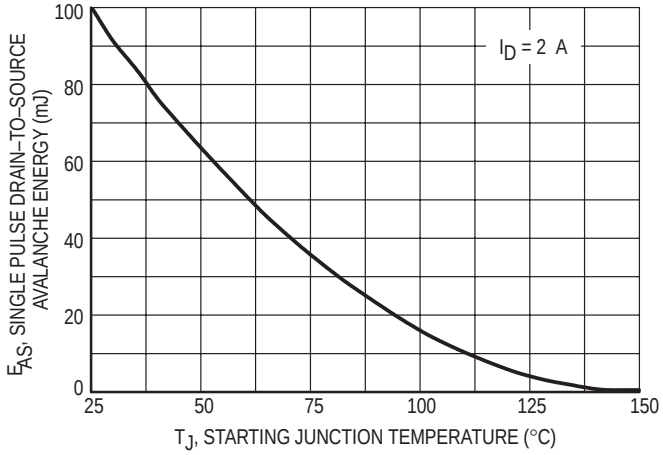


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

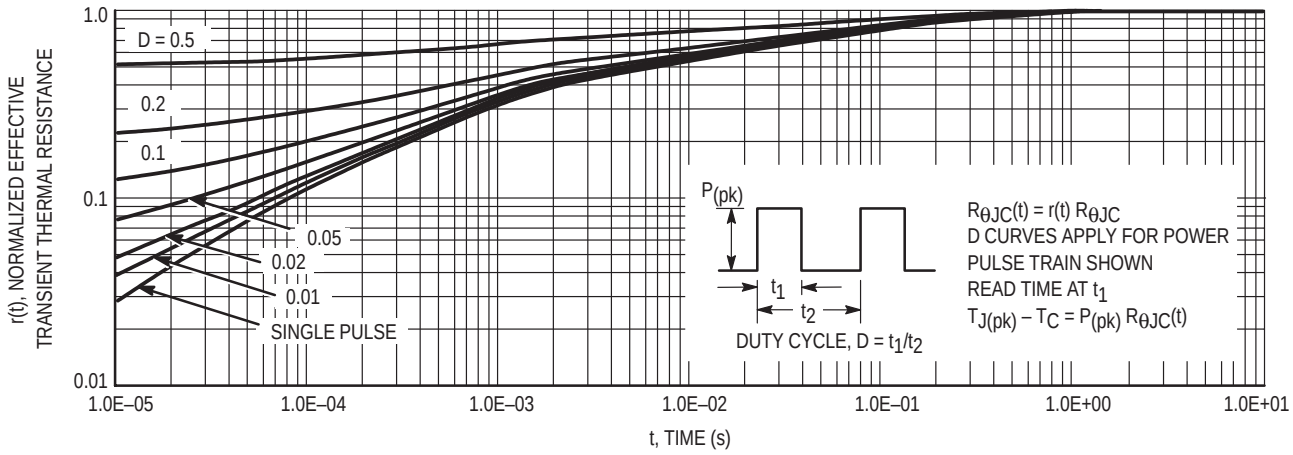


Figure 13. Thermal Response

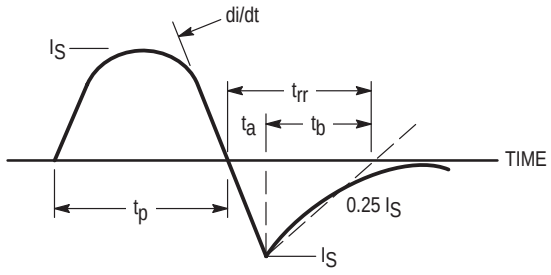


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

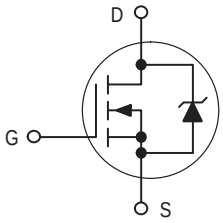
MTD3N25E

Motorola Preferred Device

TMOS POWER FET
3 AMPERES
250 VOLTS
$R_{DS(on)}$ = 1.4 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	250	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	250	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	3.0 2.0 9.0	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	250 —	— 367	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 250 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 250 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	— 6.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$R_{DS(on)}$	—	1.1	1.4	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 3.0 Adc) (I_D = 1.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	5.04 4.41	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.5 Adc)		g_{FS}	1.0	1.8	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	307	430	pF
Output Capacitance		C_{oss}	—	57	75	
Reverse Transfer Capacitance		C_{rss}	—	14	25	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 125 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	7.0	15	ns
Rise Time		t_r	—	5.0	15	
Turn–Off Delay Time		$t_{d(off)}$	—	15	30	
Fall Time		t_f	—	6.0	15	
Gate Charge (See Figure 8)	(V_{DS} = 200 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	9.8	15	nC
		Q_1	—	2.1	—	
		Q_2	—	4.2	—	
		Q_3	—	3.8	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.9 0.728	1.6 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	153	—	ns
		t_a	—	64	—	
		t_b	—	89	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.51	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

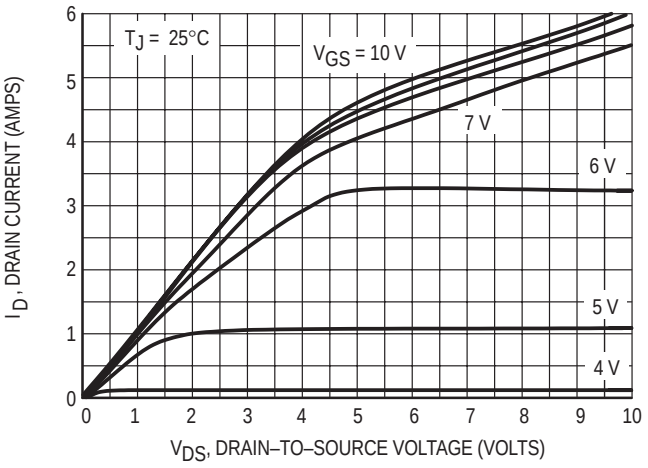
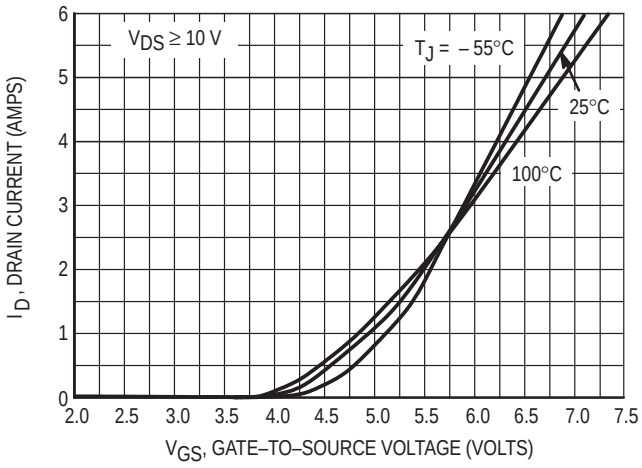


Figure 1. On–Region Characteristics



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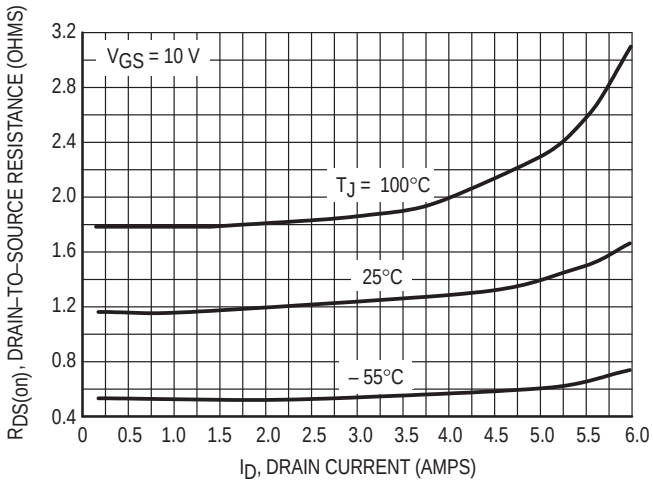

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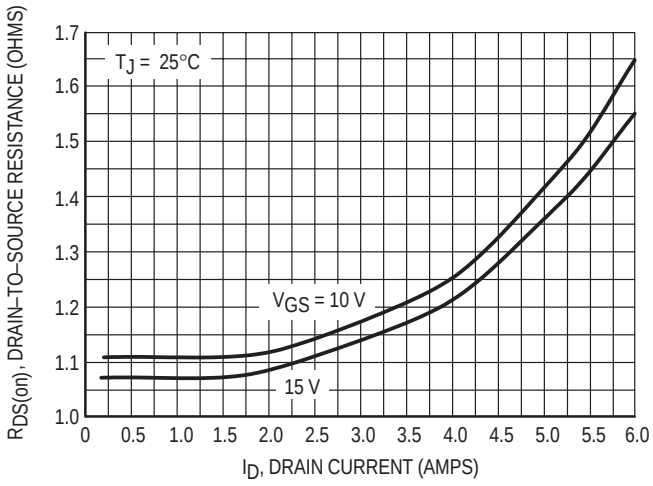


Figure 4. On–Resistance versus Drain Current and Gate Voltage

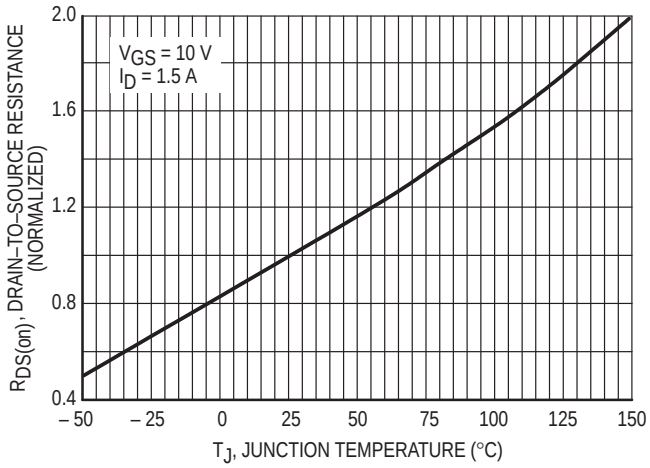
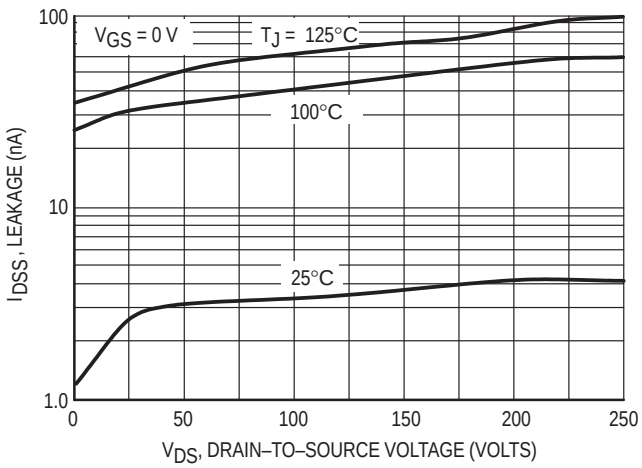


Figure 5. On–Resistance Variation with Temperature



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$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

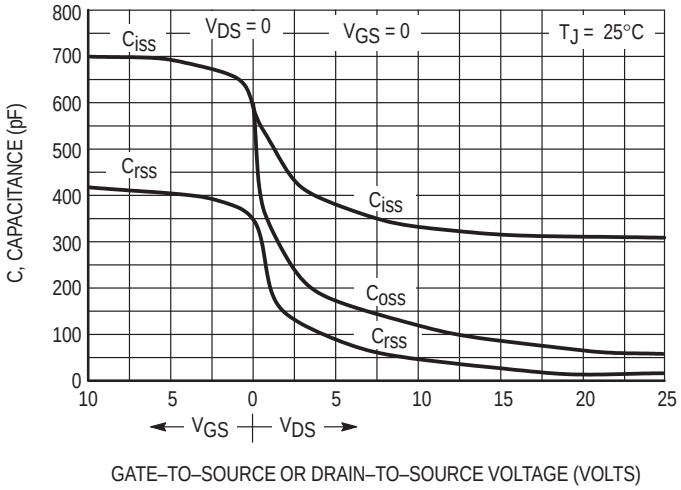


Figure 7. Capacitance Variation

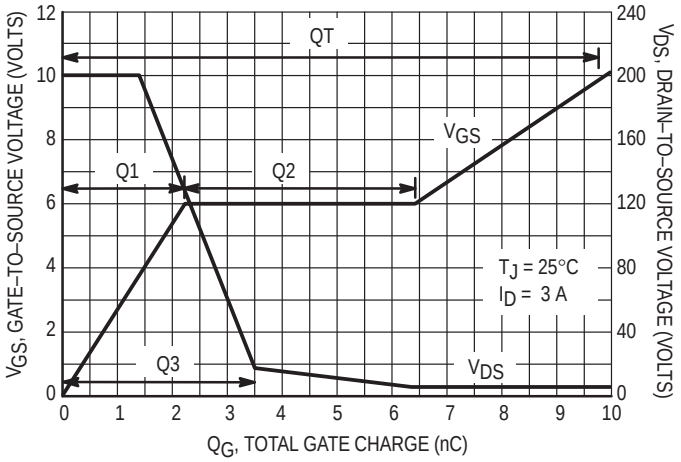


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Ttotal Charge

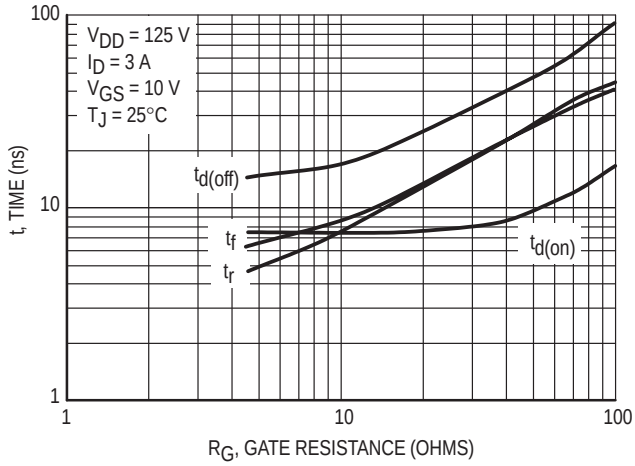


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

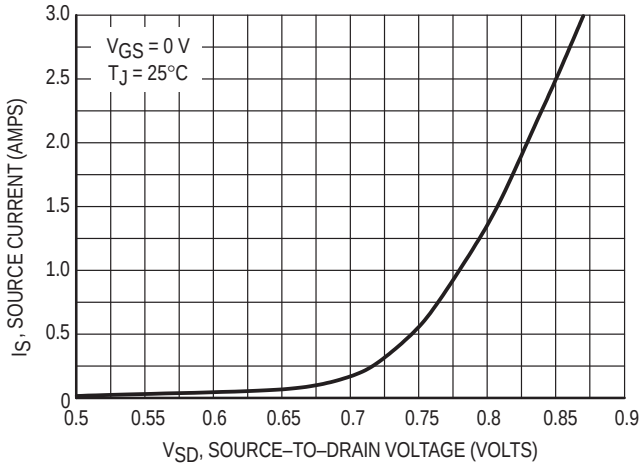


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

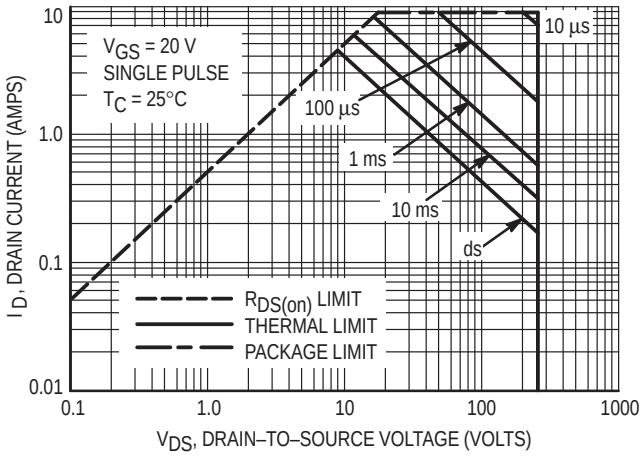


Figure 11. Maximum Rated Forward Biased Safe Operating Area

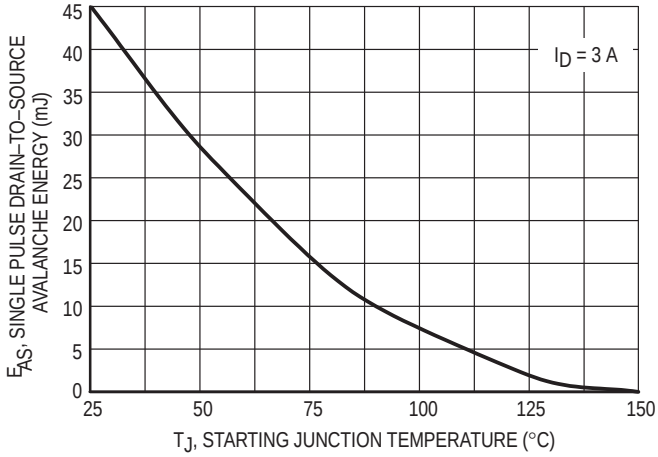


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

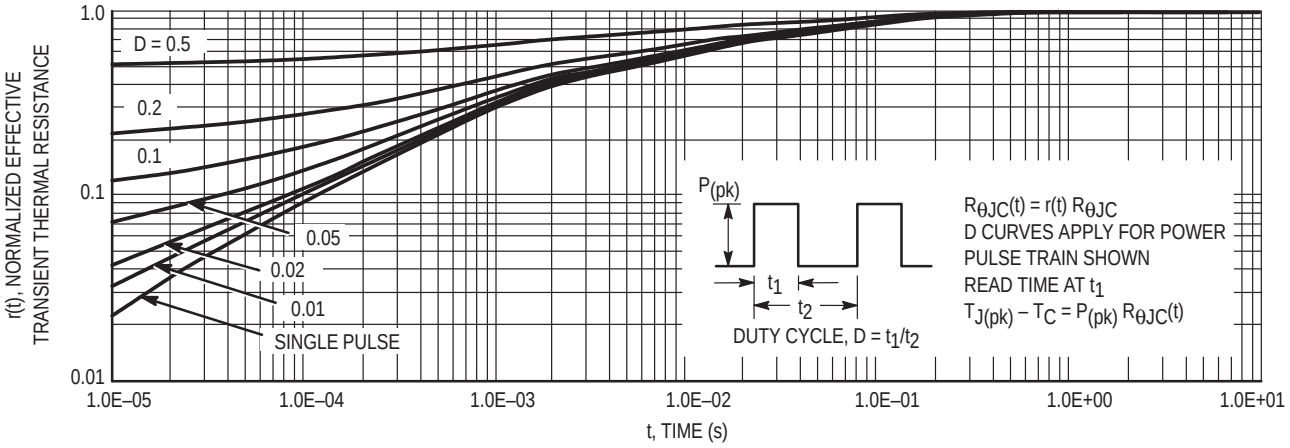


Figure 13. Thermal Response

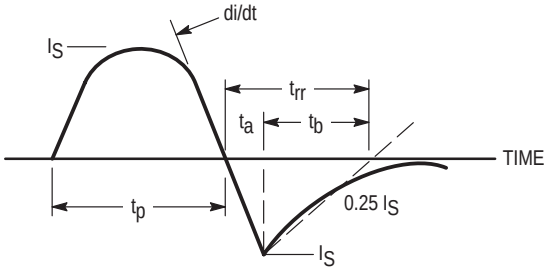


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

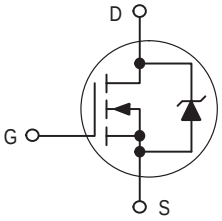
MTD4N20E

Motorola Preferred Device

TMOS POWER FET
4.0 AMPERES
200 VOLTS
$R_{DS(on)}$ = 1.2 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add –T4 Suffix to Part Number



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	200	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	Vdc
Gate–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	4.0 2.6 12	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, I_L = 4.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	80	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 μAdc)		$V_{(BR)DSS}$	200	—	—	Vdc
Temperature Coefficient (Positive)			—	263	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc)		$R_{DS(on)}$	—	0.98	1.2	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 4.0 Adc)		$V_{DS(on)}$	—	3.5	5.8	Vdc
(I_D = 2.0 Adc, T_J = 125°C)			—	—	5.0	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.0 Adc)		g_{FS}	1.5	2.1	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	311	430	pF
Output Capacitance		C_{oss}	—	66	80	
Reverse Transfer Capacitance		C_{rss}	—	11	20	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 100 Vdc, I_D = 4.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	10	17	ns
Rise Time		t_r	—	4.0	26	
Turn–Off Delay Time		$t_{d(off)}$	—	15	29	
Fall Time		t_f	—	6.0	18	
Gate Charge (See Figure 8)	(V_{DS} = 160 Vdc, I_D = 4.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	9.2	14	nC
		Q_1	—	2.4	—	
		Q_2	—	4.1	—	
		Q_3	—	5.6	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.92		Vdc
	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.82	—	
Reverse Recovery Time (See Figure 14)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	123	—	ns
		t_a	—	82	—	
		t_b	—	41	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.58	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

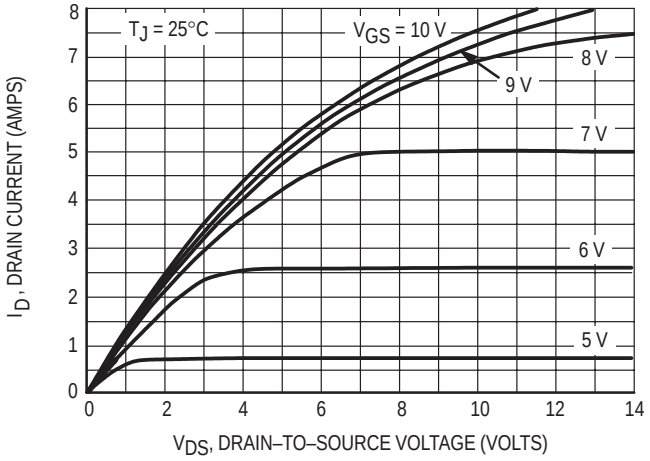


Figure 1. On–Region Characteristics

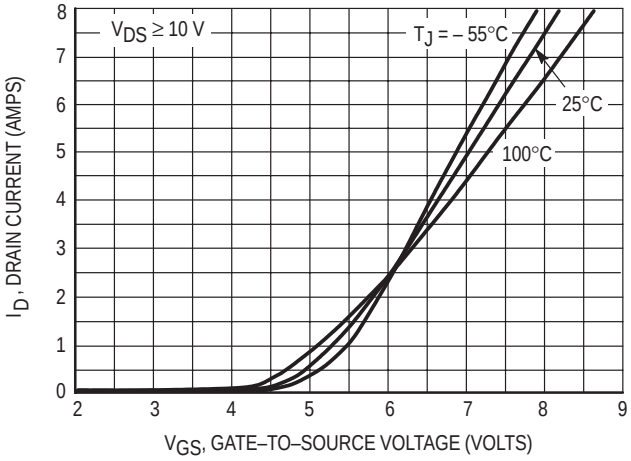


Figure 2. Transfer Characteristics

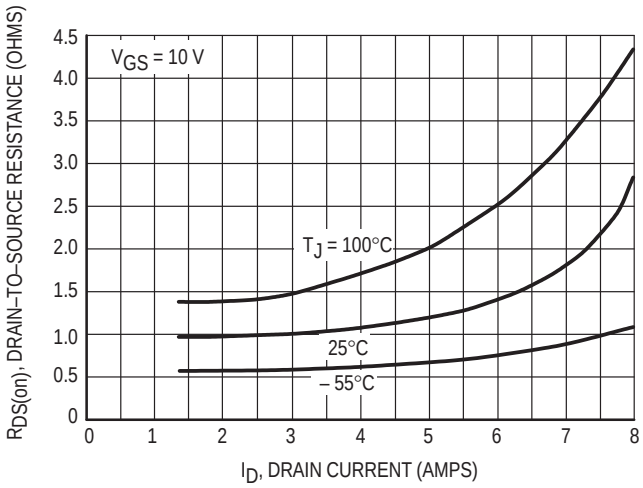


Figure 3. On–Resistance versus Drain Current and Temperature

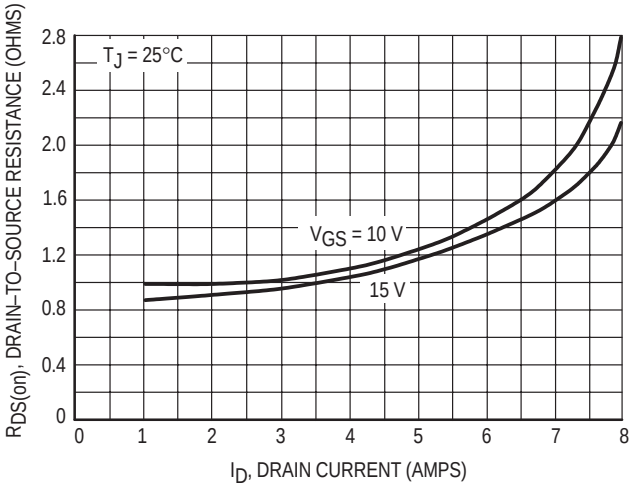


Figure 4. On–Resistance versus Drain Current and Gate Voltage

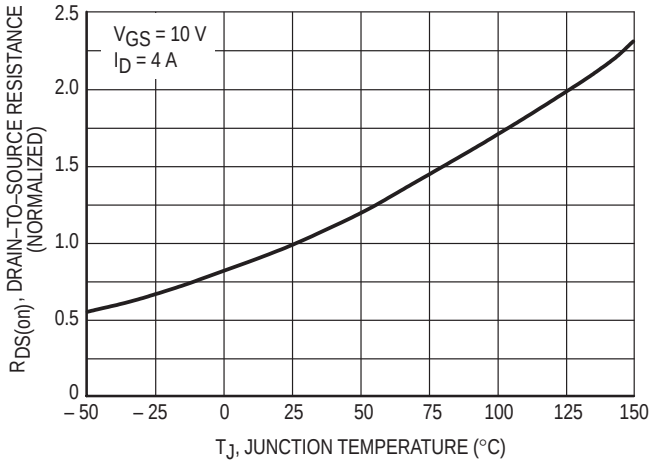


Figure 5. On–Resistance Variation with Temperature

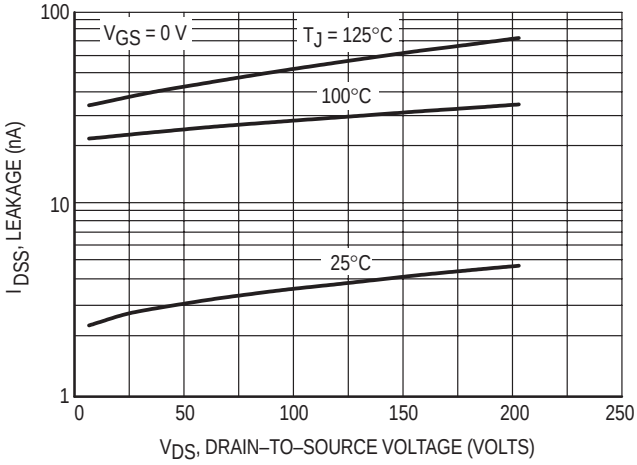


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

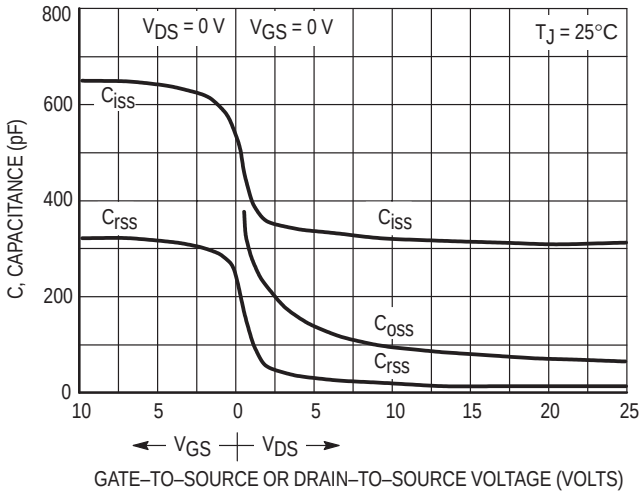
$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.



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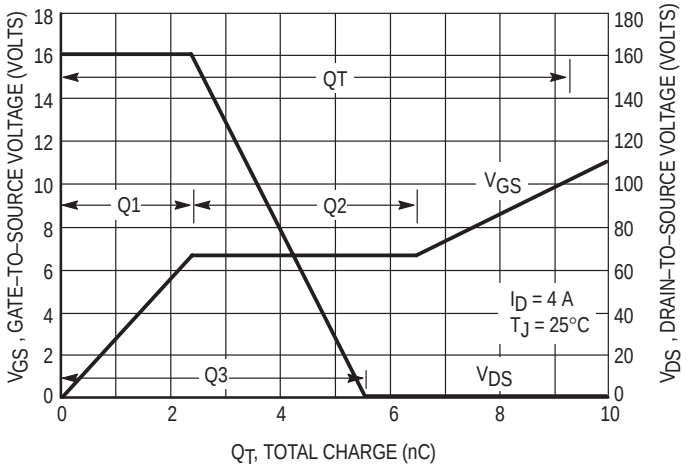

Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

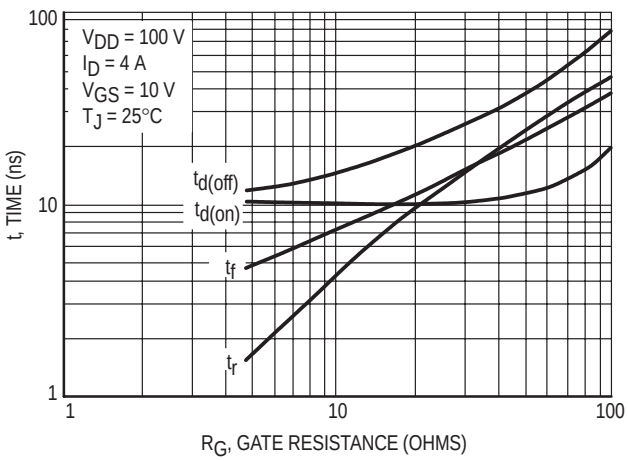

Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

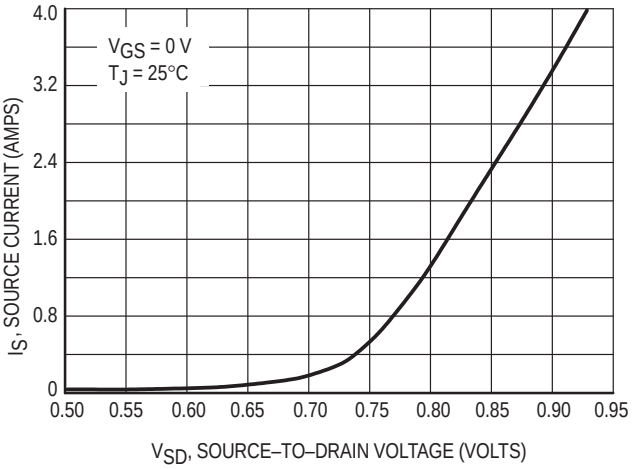

Figure 10. Diode Forward Voltage versus Current

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SAFE OPERATING AREA

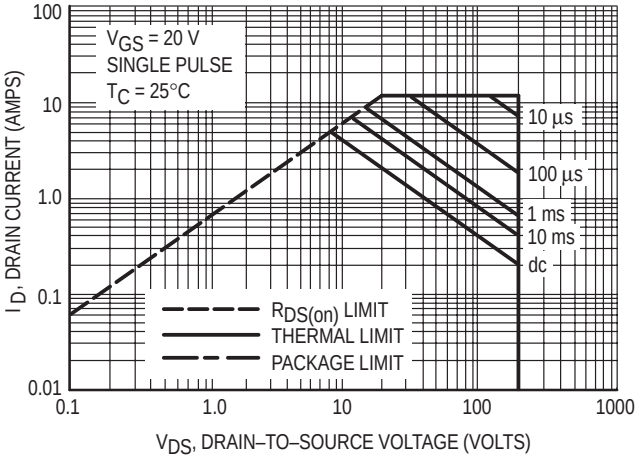
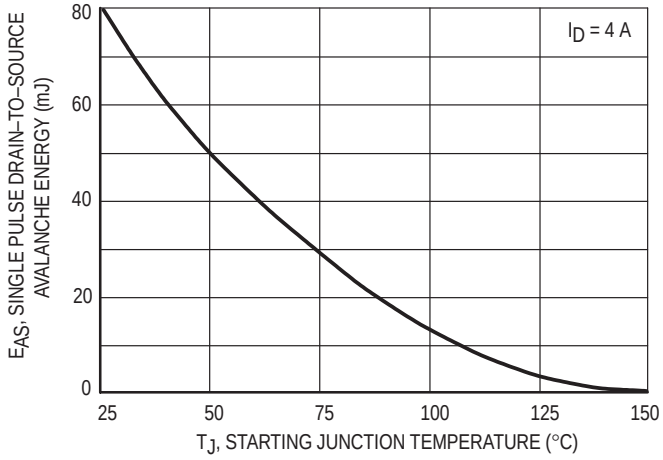


Figure 11. Maximum Rated Forward Biased Safe Operating Area



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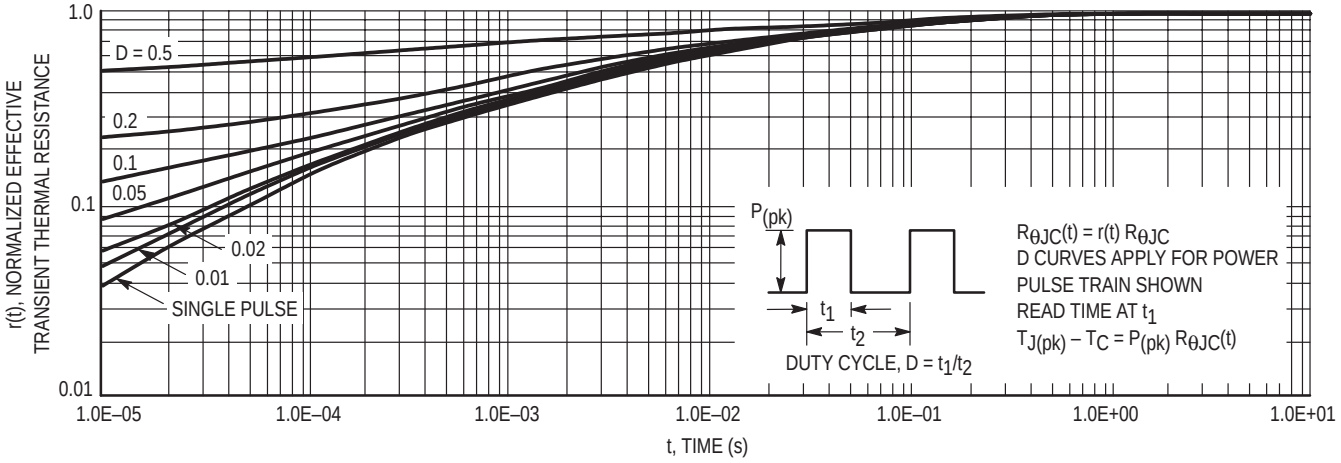

Figure 13. Thermal Response

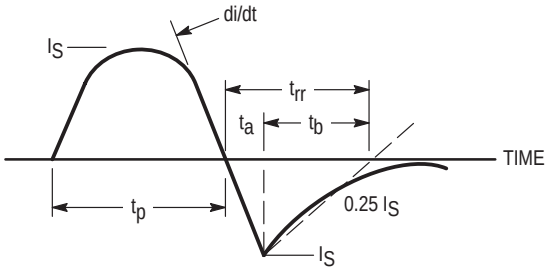

Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

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Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

MTD5N25E

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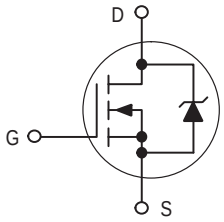
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add –T4 Suffix to Part Number

TMOS®



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	250	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	250	Vdc
Gate–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	5.0 3.2 15	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	50 0.4 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, I_L = 7.5 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	84	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.50 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 μAdc)		$V_{(BR)DSS}$	250	—	—	Vdc
Temperature Coefficient (Positive)			—	326	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 250 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 250 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	6.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$R_{DS(on)}$	—	0.81	1.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 5.0 Adc)		$V_{DS(on)}$	—	3.4	6.0	Vdc
(I_D = 2.5 Adc, T_J = 125°C)			—	—	5.3	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.5 Adc)		g_{FS}	1.5	2.6	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	369	520	pF
Output Capacitance		C_{oss}	—	66	90	
Reverse Transfer Capacitance		C_{rss}	—	14	30	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 125 Vdc, I_D = 5.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	9	10	ns
Rise Time		t_r	—	18	40	
Turn–Off Delay Time		$t_{d(off)}$	—	21	40	
Fall Time		t_f	—	18	40	
Gate Charge (See Figure 8)	(V_{DS} = 200 Vdc, I_D = 5.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	13.2	15	nC
		Q_1	—	2.9	—	
		Q_2	—	6.2	—	
		Q_3	—	5.9	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 5.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.93	1.6	Vdc
	(I_S = 5.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.82	—	
Reverse Recovery Time (See Figure 14)	(I_S = 5.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	147	—	ns
		t_a	—	100	—	
		t_b	—	47	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.847	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

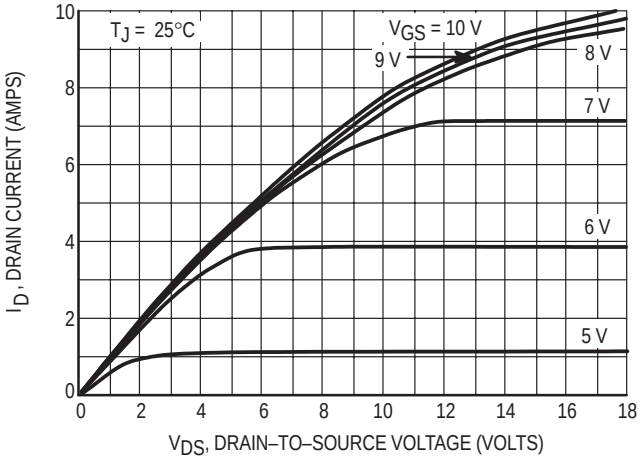


Figure 1. On–Region Characteristics

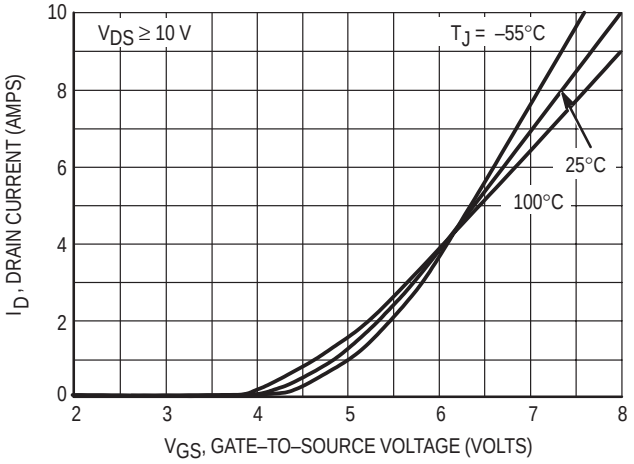


Figure 2. Transfer Characteristics

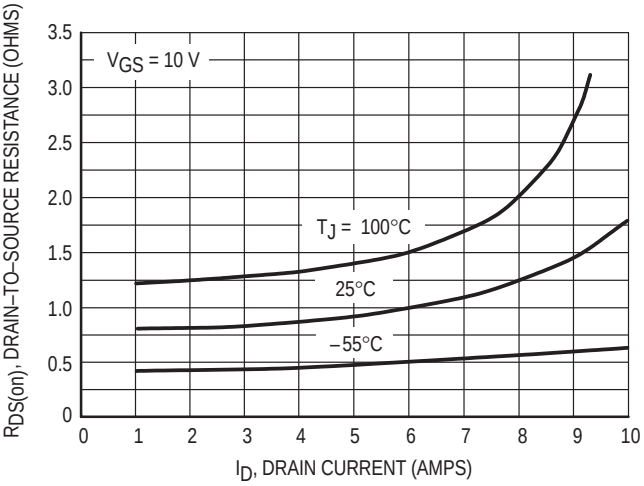


Figure 3. On–Resistance versus Drain Current and Temperature

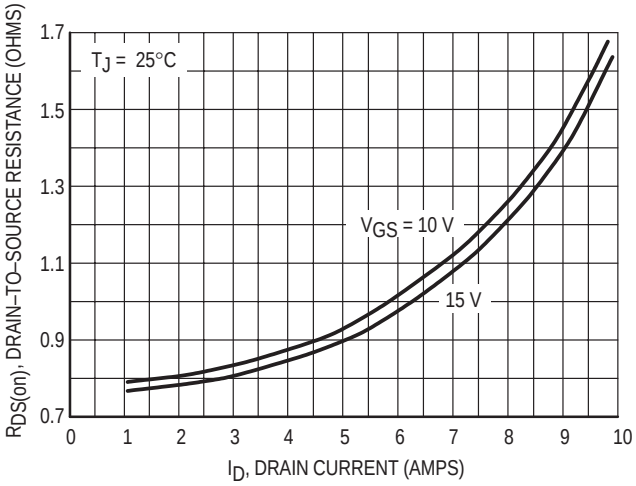


Figure 4. On–Resistance versus Drain Current and Gate Voltage

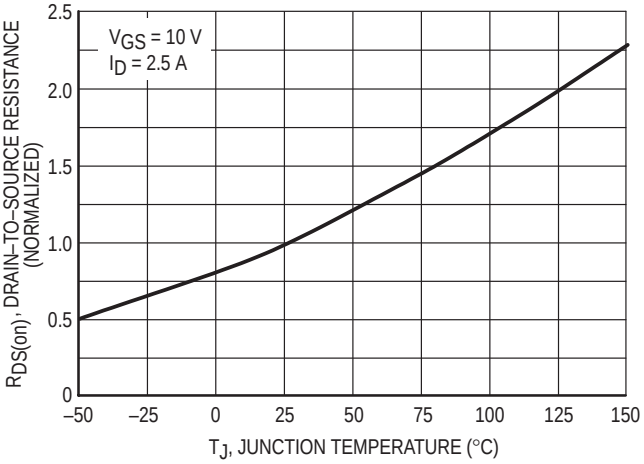


Figure 5. On–Resistance Variation with Temperature

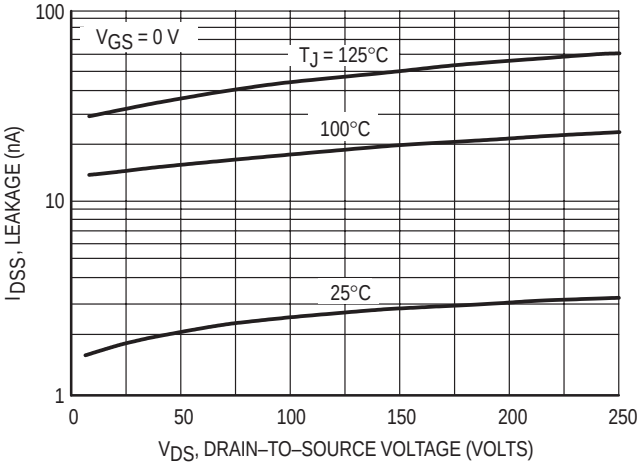


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

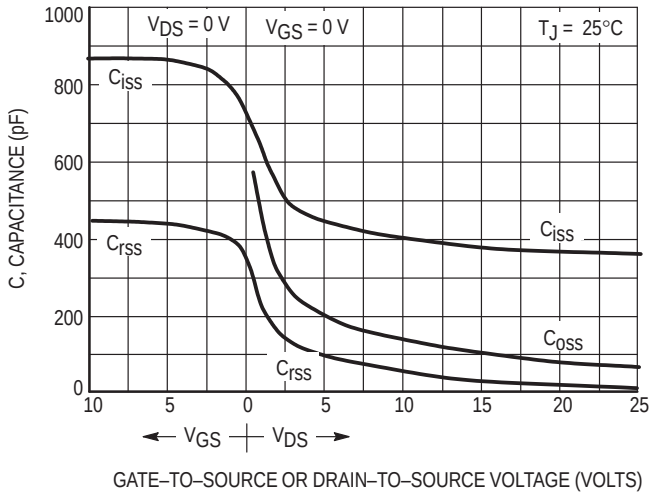


Figure 7. Capacitance Variation

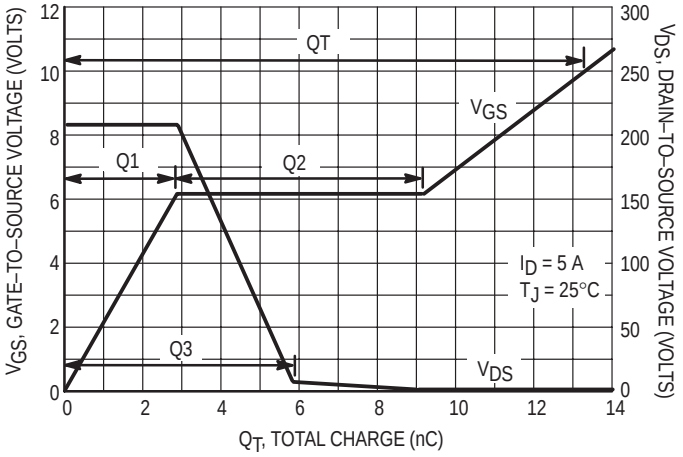


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

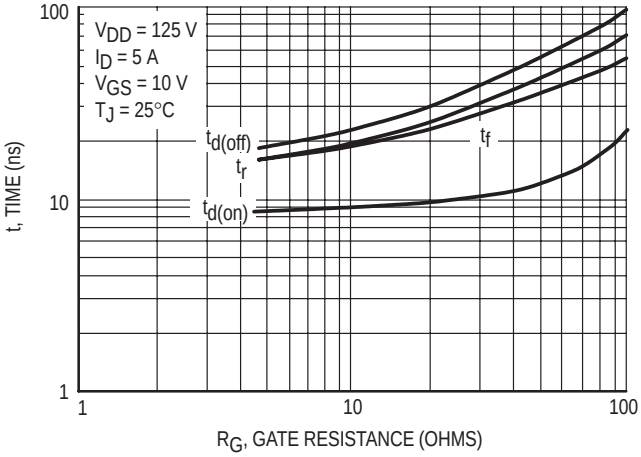


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

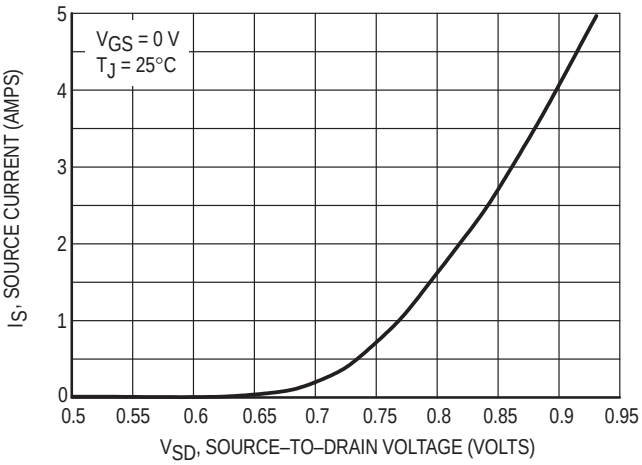


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (TC) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (IDM) nor rated voltage (VDSS) is exceeded and the transition time (tr,tf) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed (TJ(MAX) – TC)/(RθJC).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (IDM), the energy rating is specified at rated continuous current (ID), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous ID can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

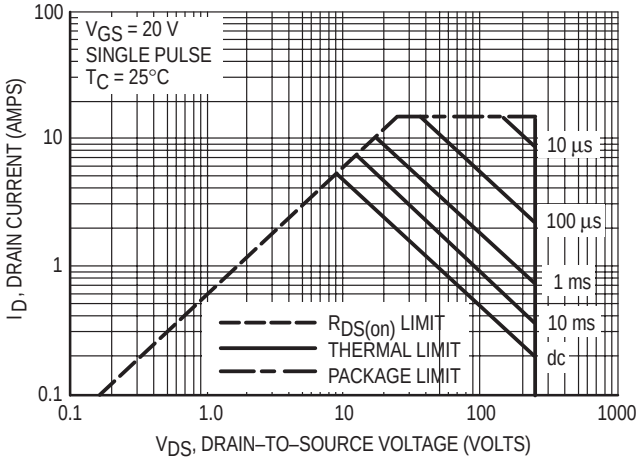


Figure 11. Maximum Rated Forward Biased Safe Operating Area

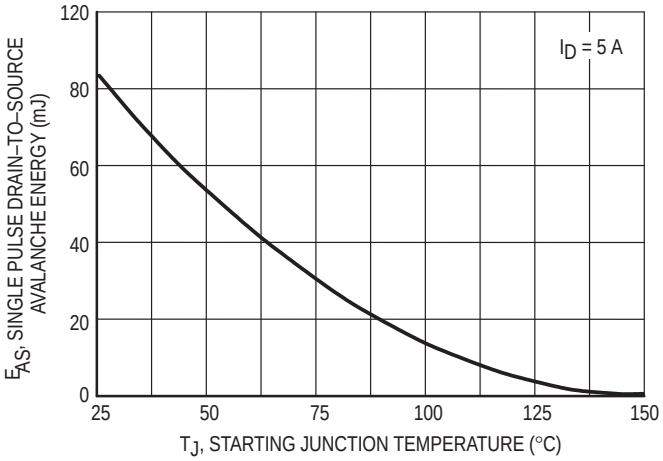


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

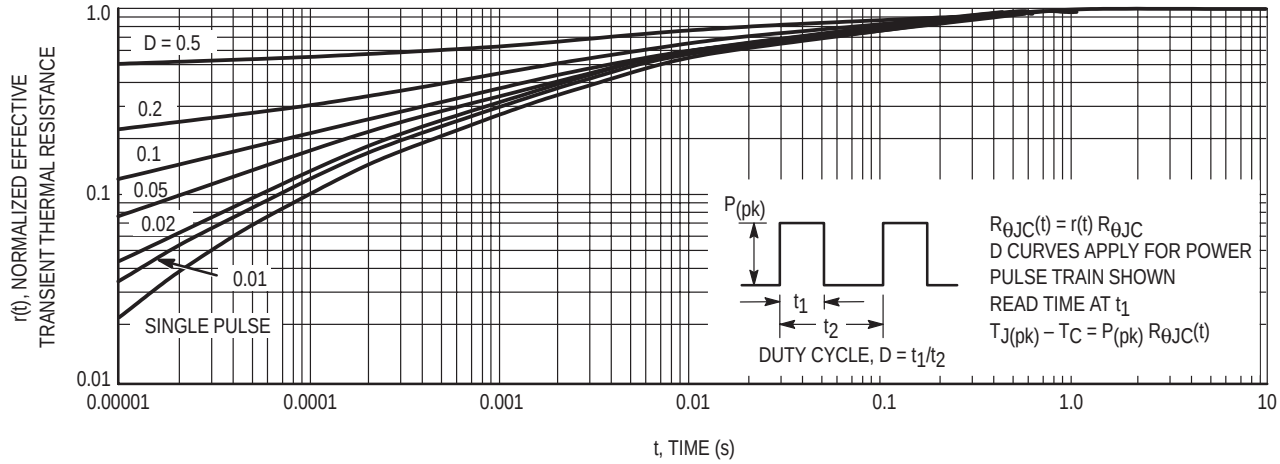


Figure 13. Thermal Response

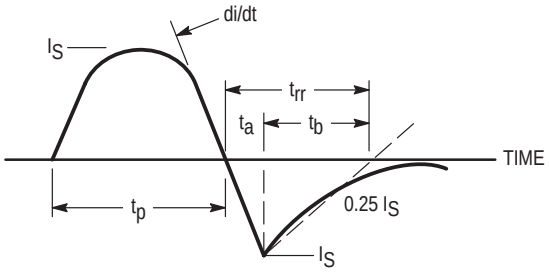


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

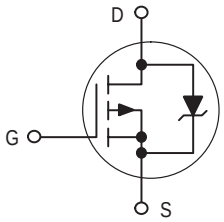
TMOS V ™
Power Field Effect Transistor
DPAK for Surface Mount
P–Channel Enhancement–Mode Silicon Gate

MTD5P06V

Motorola Preferred Device

TMOS POWER FET
5 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.450 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.



CASE 369A–13, Style 2
DPAK Surface Mount

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add –T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	5 4 18	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	40 0.27 2.1	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, PEAK I_L = 5 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	125	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.75 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	61.2	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.8	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	4.7	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$R_{DS(on)}$	—	0.34	0.45	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 5 Adc)		$V_{DS(on)}$	—	—	2.7	Vdc
(V_{GS} = 10 Vdc, I_D = 2.5 Adc, T_J = 150°C)			—	—	2.6	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.5 Adc)		g_{FS}	1.5	3.6	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	367	510	pF
Output Capacitance		C_{oss}	—	140	200	
Transfer Capacitance		C_{rss}	—	29	60	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 5 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	11	20	ns
Rise Time		t_r	—	26	50	
Turn–Off Delay Time		$t_{d(off)}$	—	17	30	
Fall Time		t_f	—	19	40	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 5 Adc, V_{GS} = 10 Vdc)	Q_T	—	12	20	nC
		Q_1	—	3.0	—	
		Q_2	—	5.0	—	
		Q_3	—	5.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 5 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.72	3.5	Vdc
	(I_S = 5 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	1.34	—	
Reverse Recovery Time	(I_S = 5 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	97	—	ns
		t_a	—	73	—	
		t_b	—	24	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.42	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

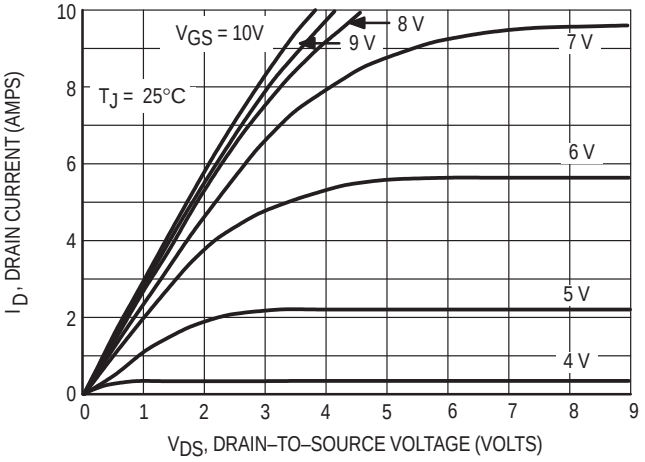


Figure 1. On–Region Characteristics

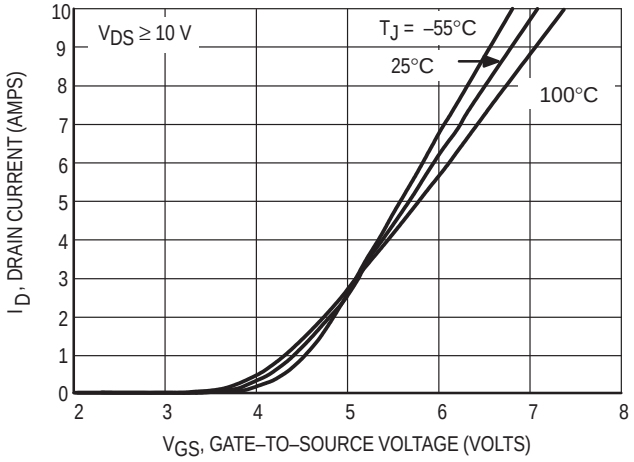


Figure 2. Transfer Characteristics

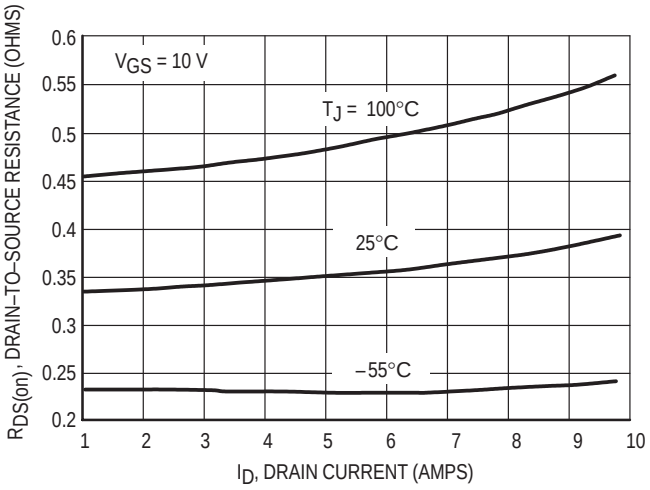


Figure 3. On–Resistance versus Drain Current and Temperature

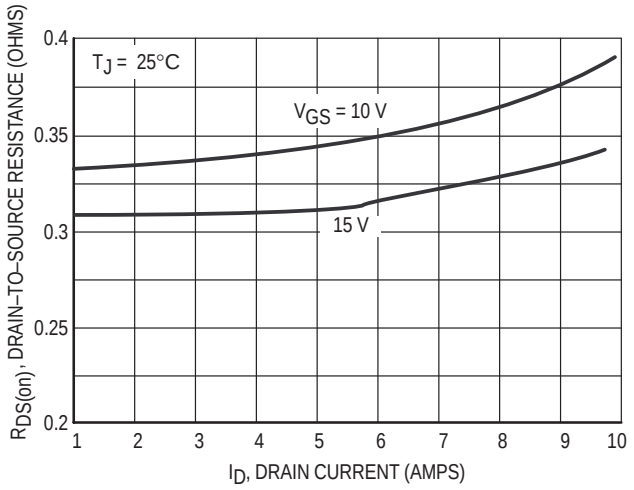


Figure 4. On–Resistance versus Drain Current and Gate Voltage

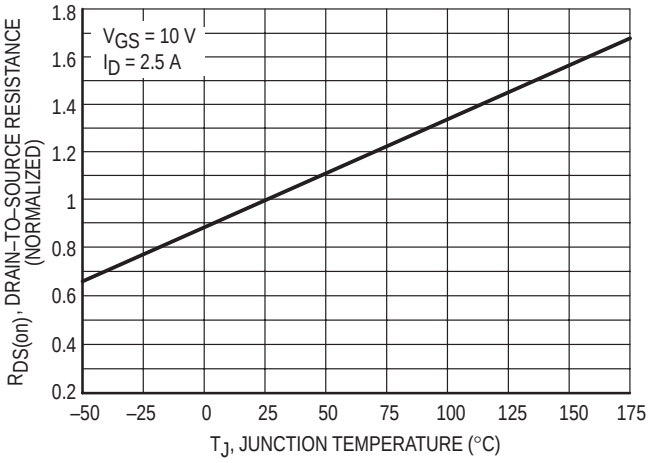


Figure 5. On–Resistance Variation with Temperature

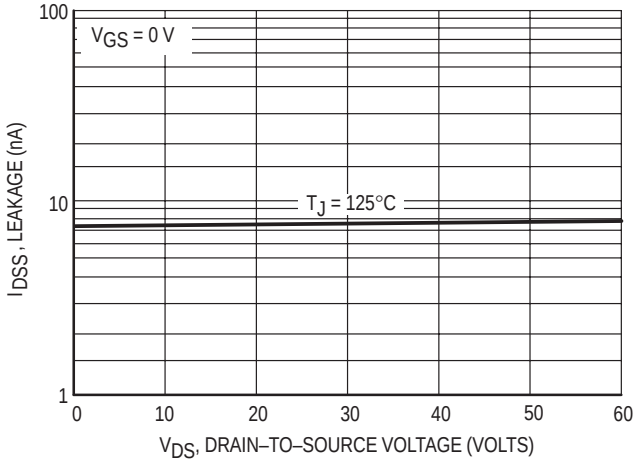


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

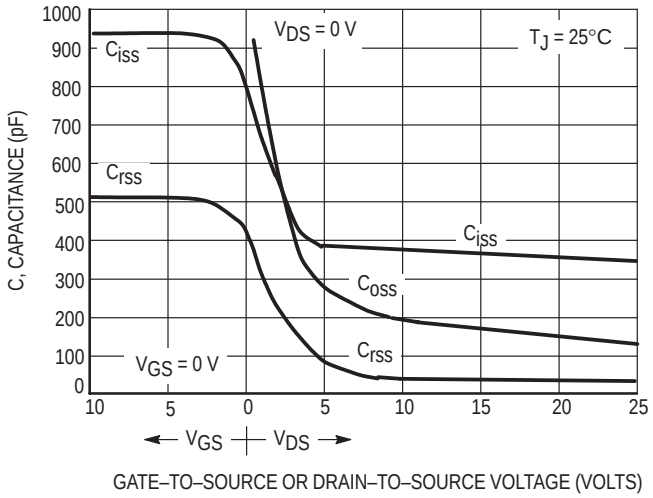


Figure 7. Capacitance Variation

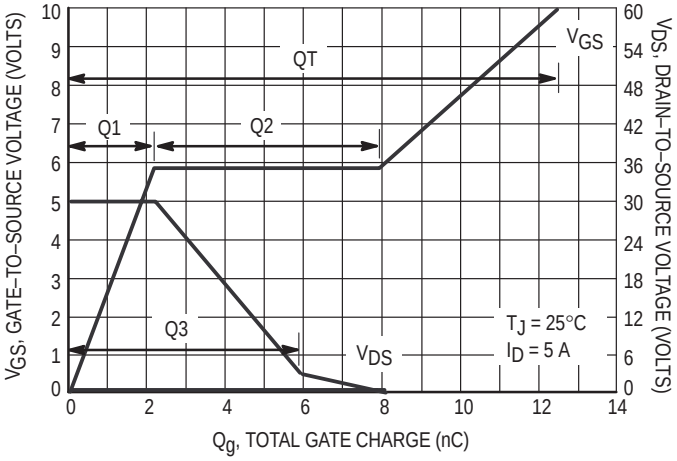


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

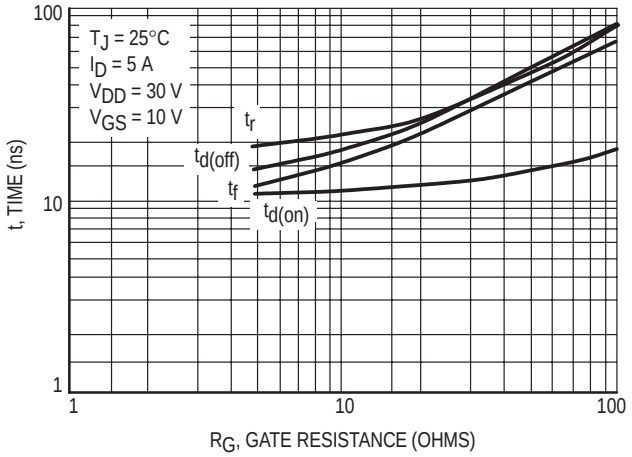


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

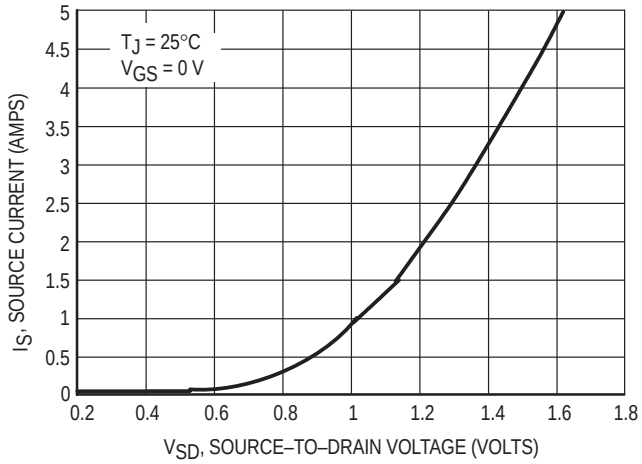


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

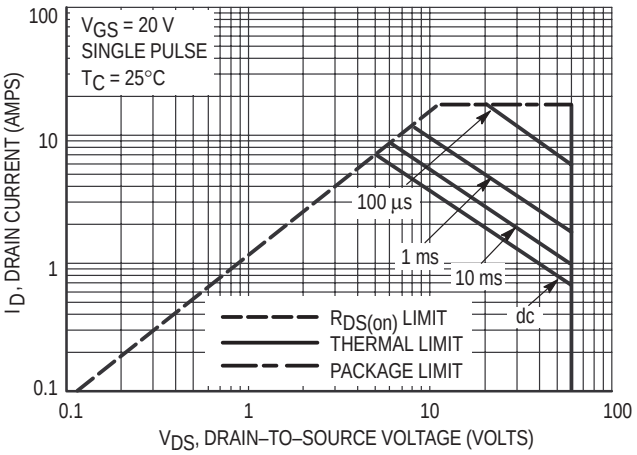


Figure 11. Maximum Rated Forward Biased Safe Operating Area

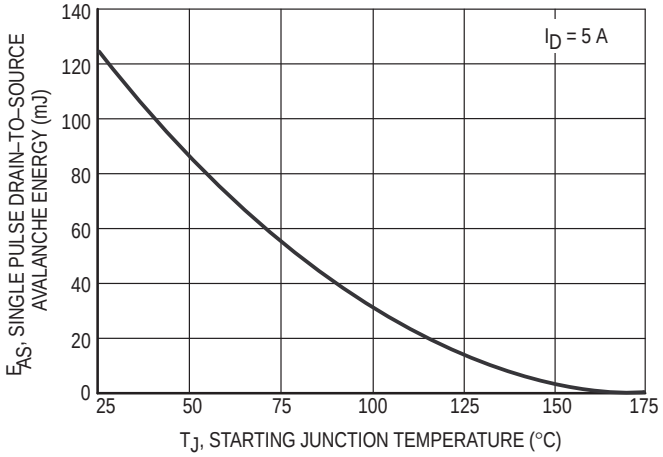


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

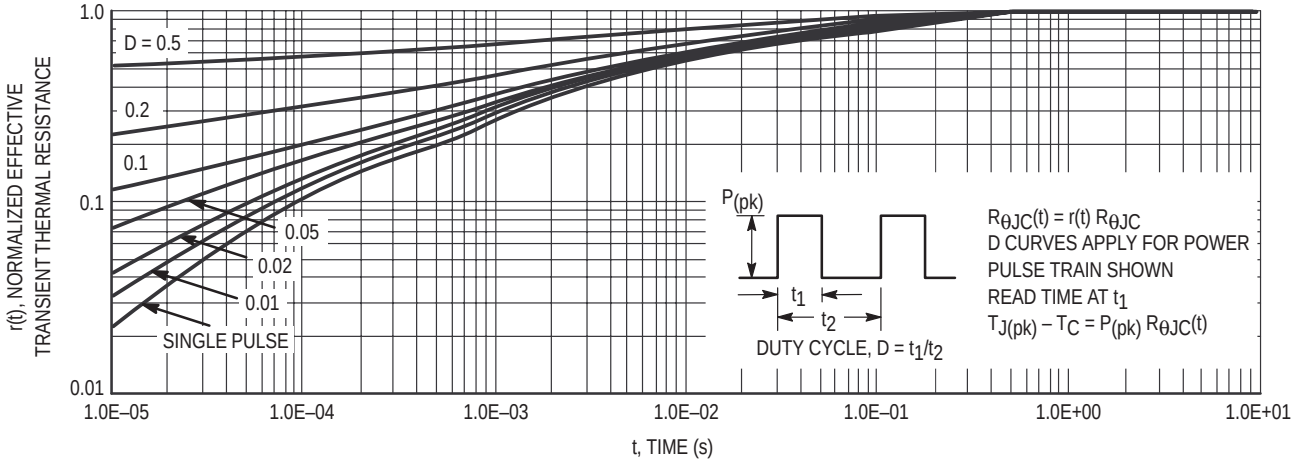


Figure 13. Thermal Response

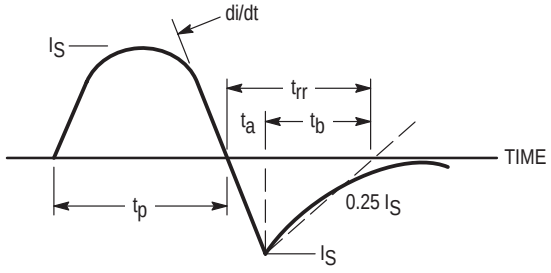


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

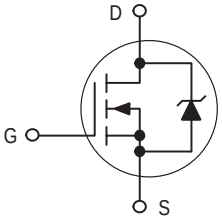
MTD6N10E

Motorola Preferred Device

TMOS POWER FET
6.0 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.400 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number
- Replaces MTD5N10



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	100	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	6.0 4.5 18	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 6.0 Apk, L = 3.0 mH, R_G =25 Ω)	E_{AS}	50	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	100	—	—	Vdc
Temperature Coefficient (Positive)			—	124	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.2	4.0	Vdc
Temperature Coefficient (Negative)			—	4.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	—	0.29	0.4	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 6.0 Adc)		$V_{DS(on)}$	—	1.75	2.9	Vdc
(I_D = 3.0 Adc, T_J = 125°C)			—	—	2.5	
Forward Transconductance (V_{DS} = 13 Vdc, I_D = 3.0 Adc)		g_{FS}	1.5	2.4	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	310	420	pF
Output Capacitance		C_{oss}	—	120	210	
Reverse Transfer Capacitance		C_{rss}	—	25	50	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 50 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.0	15	ns
Rise Time		t_r	—	31	49	
Turn–Off Delay Time		$t_{d(off)}$	—	13	31	
Fall Time		t_f	—	12	27	
Gate Charge (See Figure 8)	(V_{DS} = 80 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	10	14	nC
		Q_1	—	3.3	—	
		Q_2	—	4.3	—	
		Q_3	—	5.5	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.98	2.0	Vdc
	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.9	—	
Reverse Recovery Time (See Figure 14)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	86.7	—	ns
		t_a	—	64	—	
		t_b	—	22.7	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.327	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

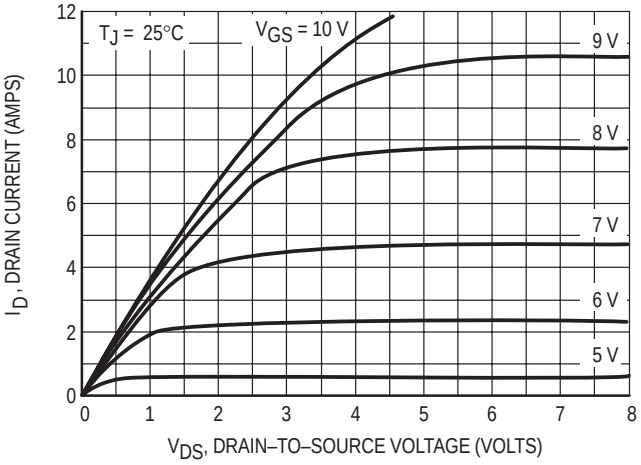
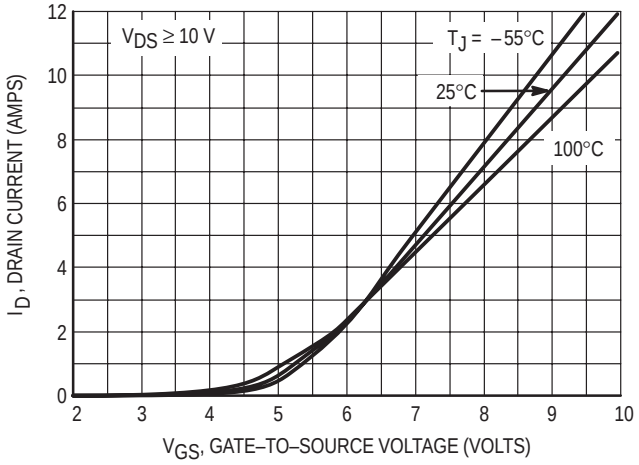


Figure 1. On–Region Characteristics



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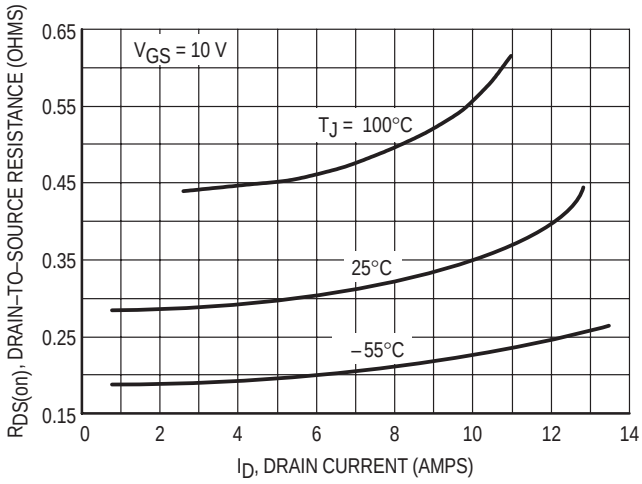

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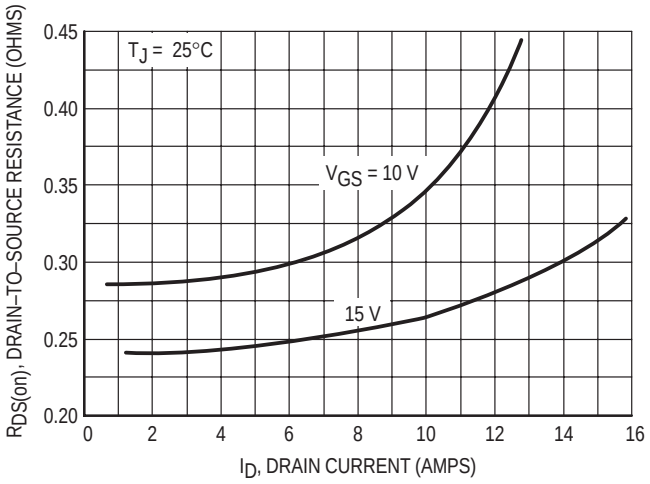

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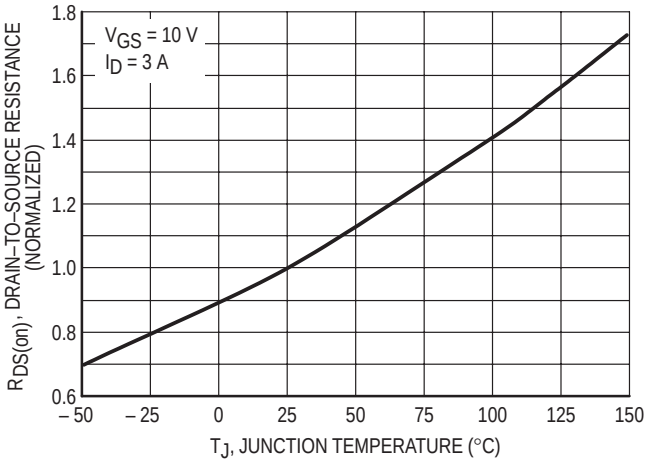
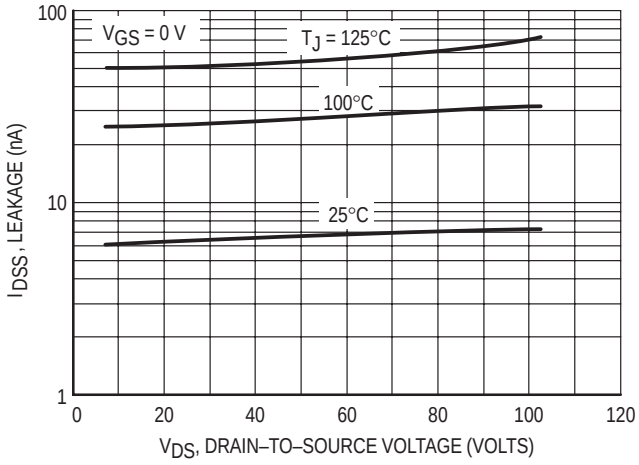


Figure 5. On–Resistance Variation with Temperature



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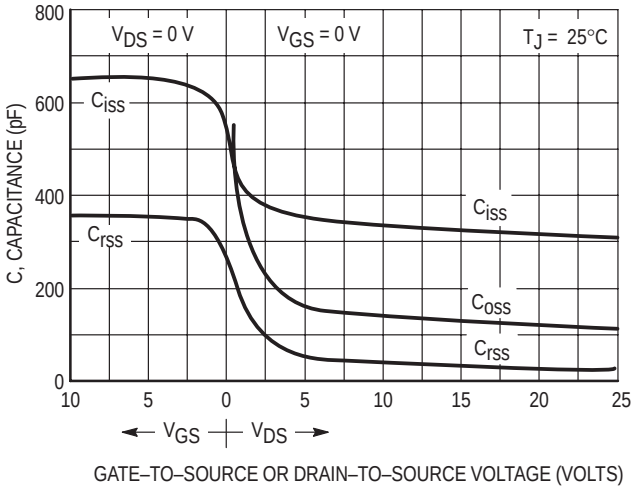

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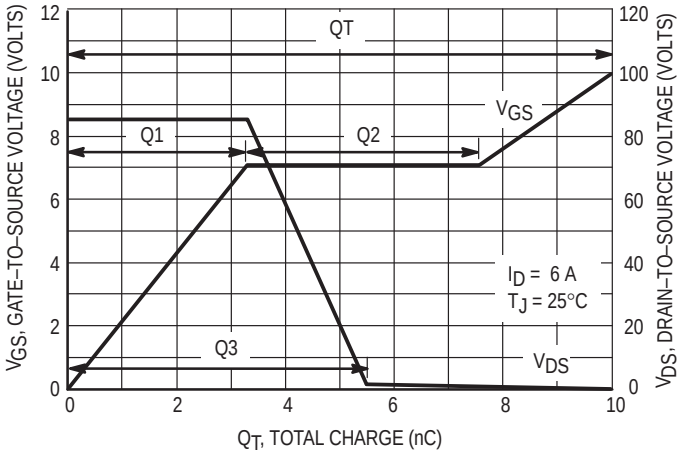

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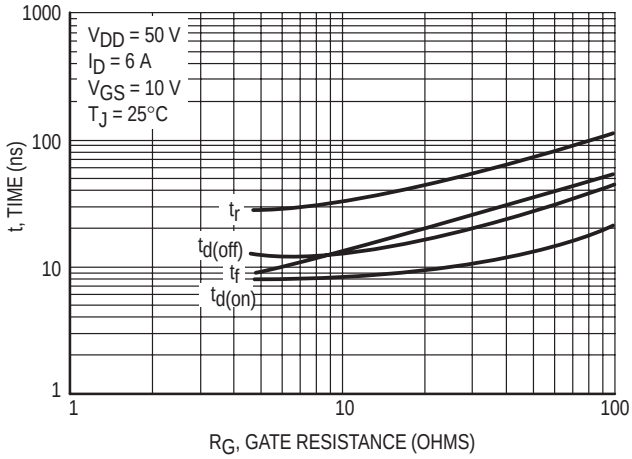

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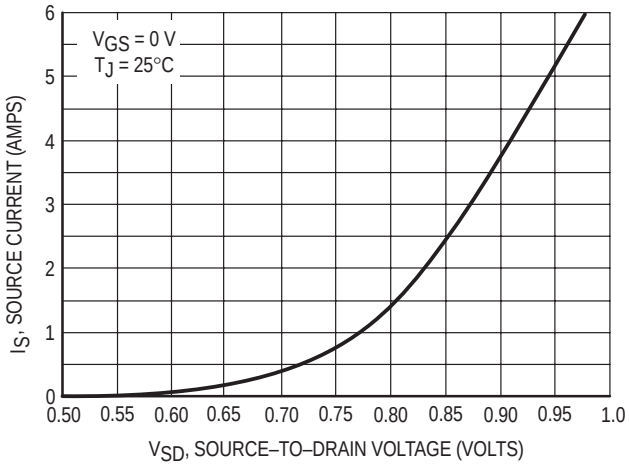
DRAIN–TO–SOURCE DIODE CHARACTERISTICS



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SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

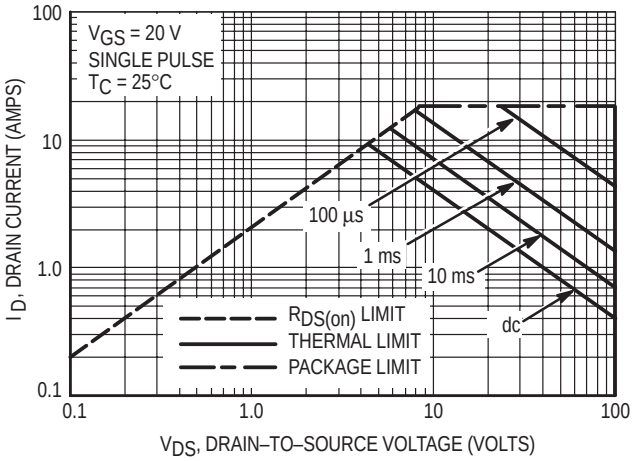


Figure 11. Maximum Rated Forward Biased Safe Operating Area

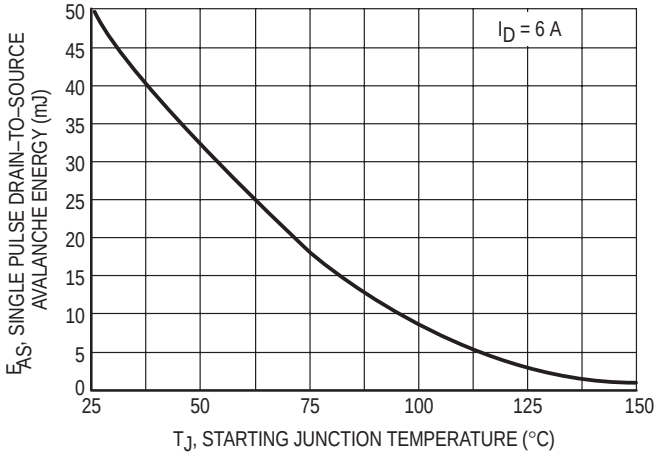


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

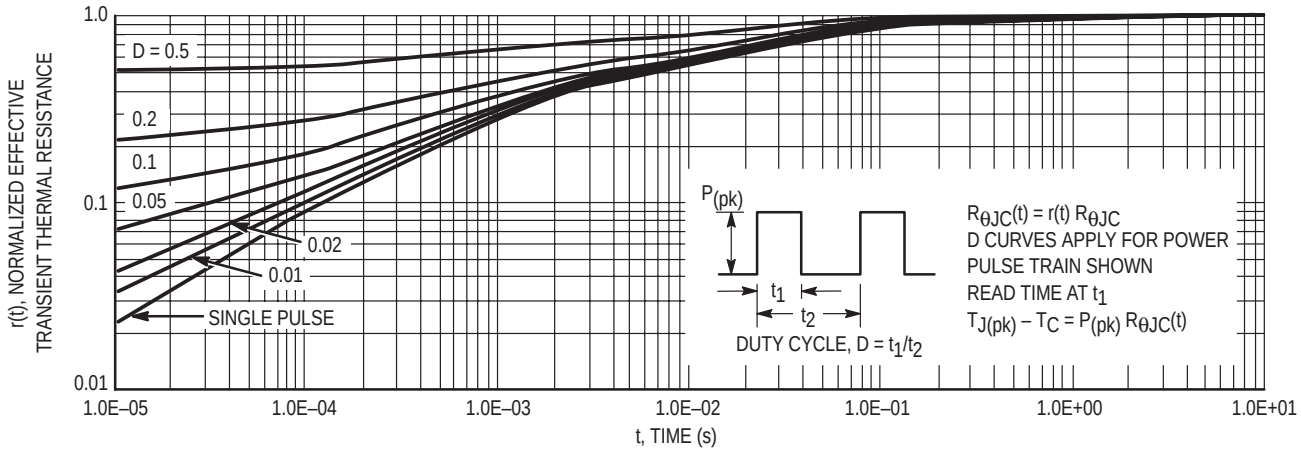


Figure 13. Thermal Response

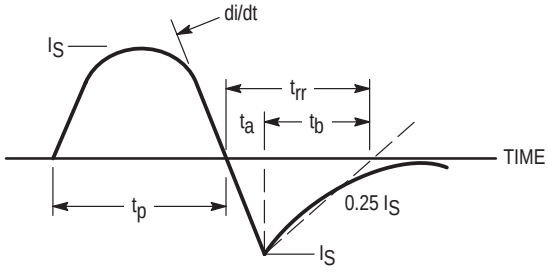


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

Power Field Effect Transistor DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

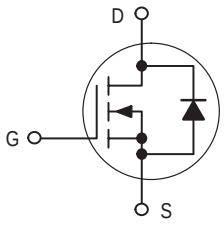
MTD6N15

TMOS POWER FET
6.0 AMPERES
150 VOLTS
$R_{DS(on)}$ = 0.3 OHM

This TMOS Power FET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $R_{DS(on)}$ — 0.3 Ω Max
- Rugged — SOA is Power Dissipation Limited
- Source–to–Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 4.0 V Max
- Surface Mount Package on 16 mm Tape

TMOS®



CASE 369A–13, Style 2
DPAK (TO–252)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	150	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	150	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \leq 50$ μs)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	6.0 20	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	1.25 0.01	Watts W/°C
Total Power Dissipation @ T_A = 25°C (1) Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	6.25 100 71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)	$V_{(BR)DSS}$	150	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0 Vdc) T_J = 125°C	I_{DSS}	— —	10 100	μAdc

(1) These ratings are applicable when surface mounted on the minimum pad size recommended. (continued)

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS — continued (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS — continued					
Gate–Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate–Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mAdc) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	—	0.3	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 6.0 Adc) (I_D = 3.0 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 1.8 1.5	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 3.0 Adc)		g_{FS}	2.5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz) See Figure 11	C_{iss}	—	1200	pF
Output Capacitance		C_{oss}	—	500	
Reverse Transfer Capacitance		C_{rss}	—	120	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn–On Delay Time	(V_{DD} = 25 Vdc, I_D = 3.0 Adc, R_G = 50 Ω) See Figures 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	180	
Turn–Off Delay Time		$t_{d(off)}$	—	200	
Fall Time		t_f	—	100	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 Vdc) See Figure 12	Q_g	15 (Typ)	30	nC
Gate–Source Charge		Q_{gs}	8.0 (Typ)	—	
Gate–Drain Charge		Q_{gd}	7.0 (Typ)	—	
SOURCE–DRAIN DIODE CHARACTERISTICS*					
Forward On–Voltage	(I_S = 6.0 Adc, di/dt = 25 A/μs V_{GS} = 0 Vdc,)	V_{SD}	1.3 (Typ)	2.0	Vdc
Forward Turn–On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	325 (Typ)	—	ns

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

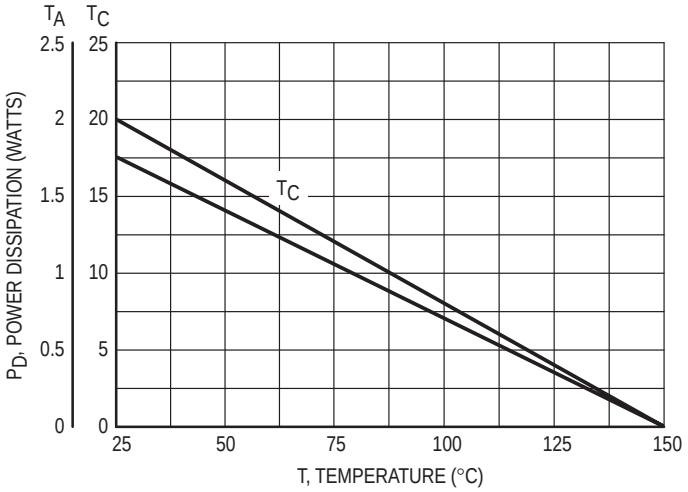


Figure 1. Power Derating

TYPICAL ELECTRICAL CHARACTERISTICS

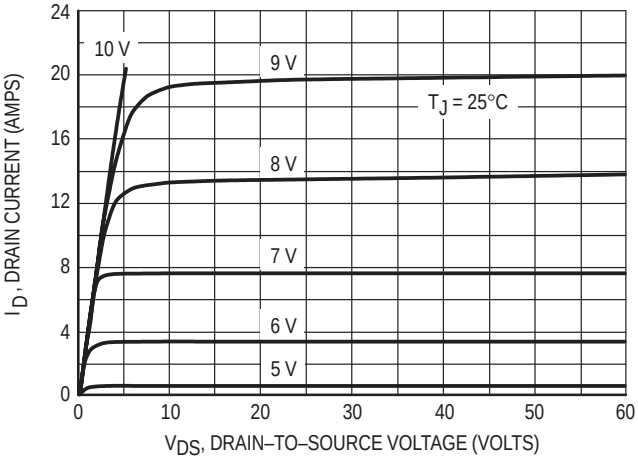


Figure 2. On–Region Characteristics

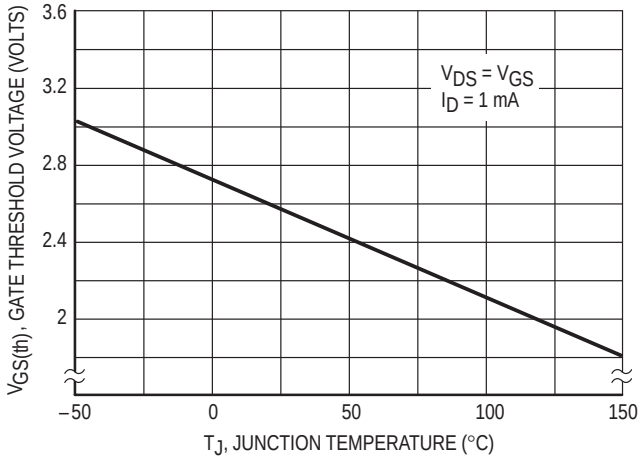


Figure 3. Gate–Threshold Voltage Variation With Temperature

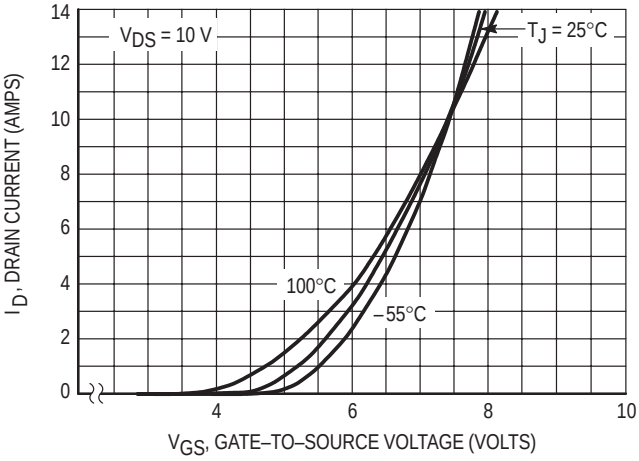


Figure 4. Transfer Characteristics

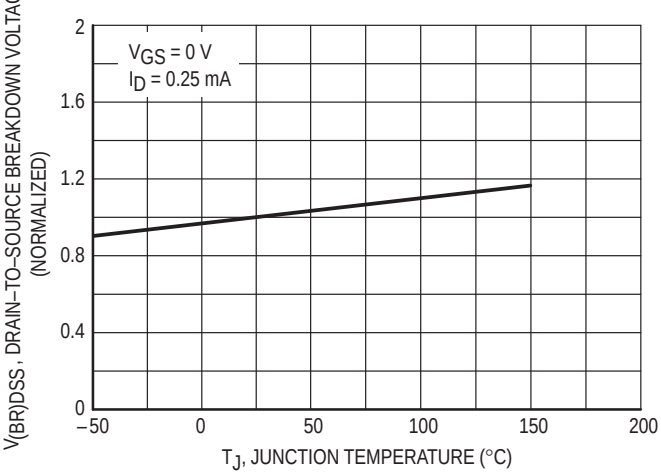


Figure 5. Breakdown Voltage Variation With Temperature

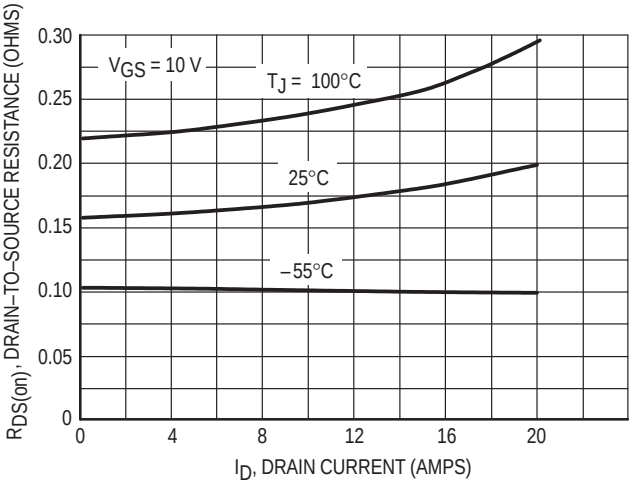


Figure 6. On–Resistance versus Drain Current

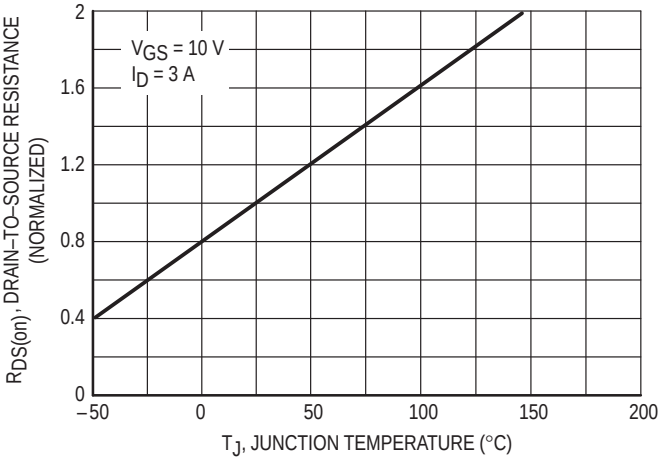


Figure 7. On–Resistance Variation With Temperature

SAFE OPERATING AREA

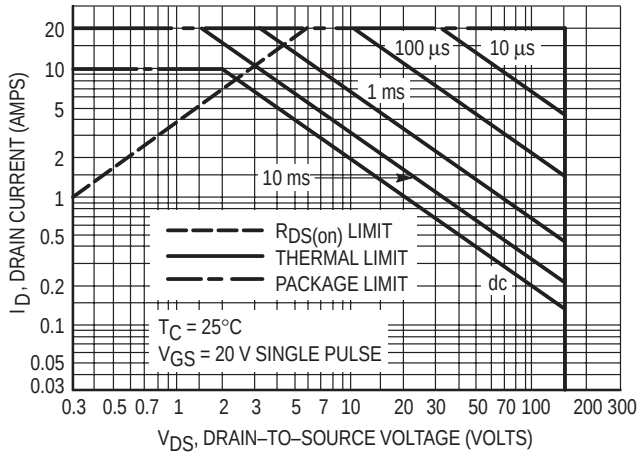


Figure 8. Maximum Rated Forward Biased Safe Operating Area

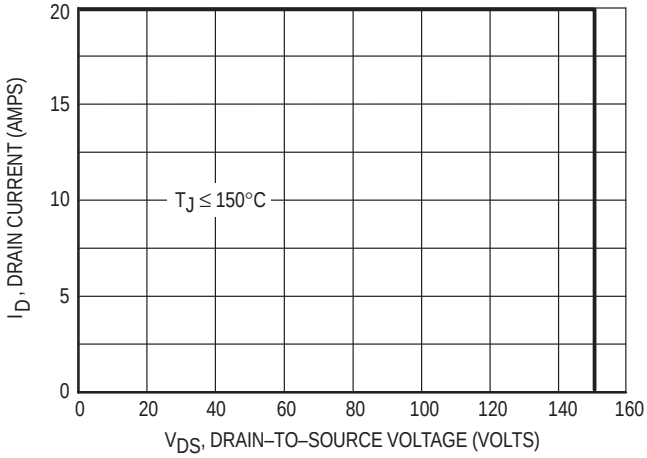


Figure 9. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

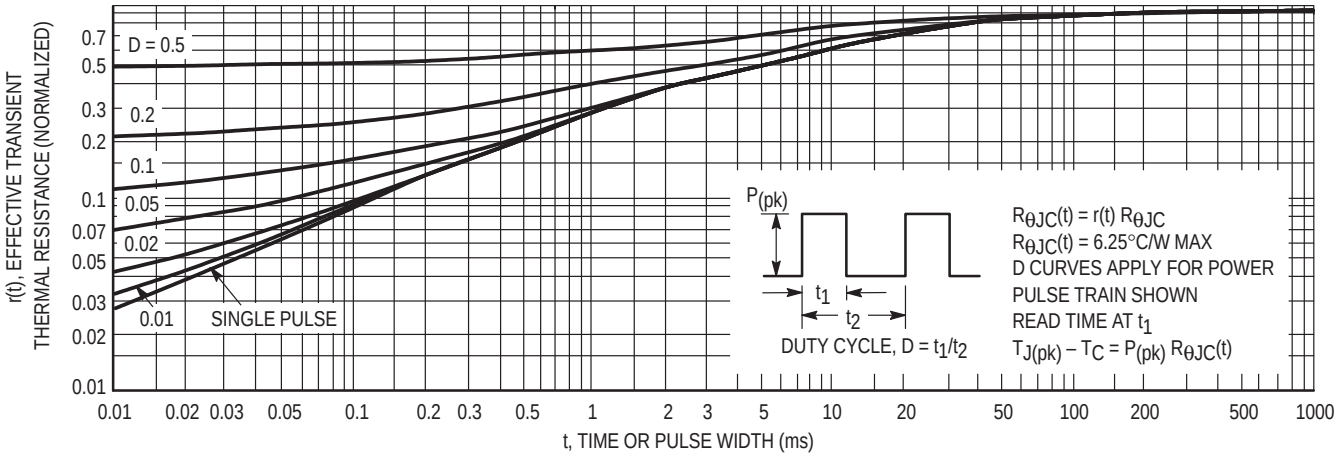


Figure 10. Thermal Response

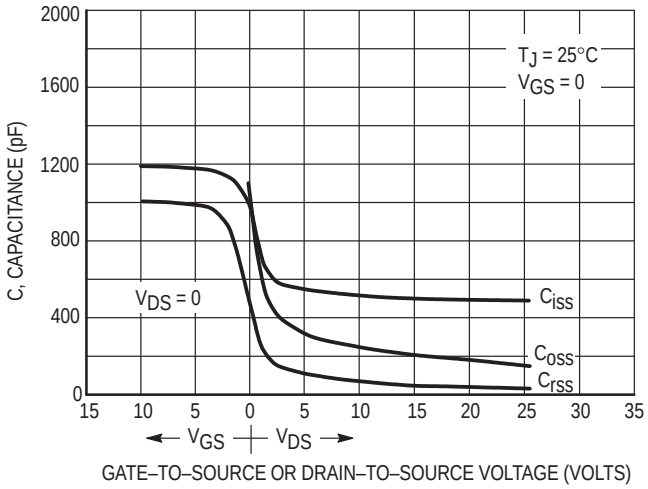


Figure 11. Capacitance Variation

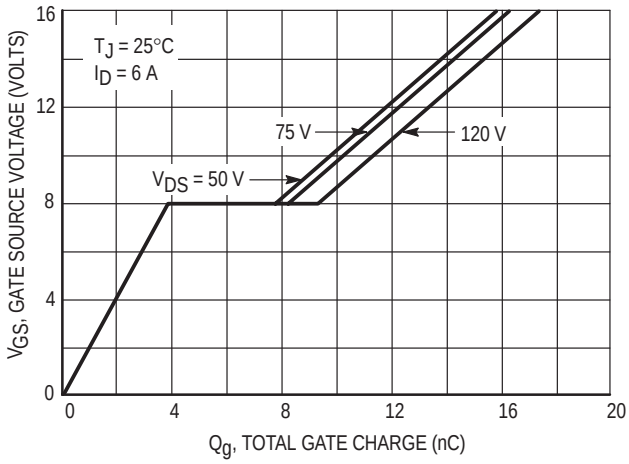


Figure 12. Gate Charge versus Gate–To–Source Voltage

RESISTIVE SWITCHING

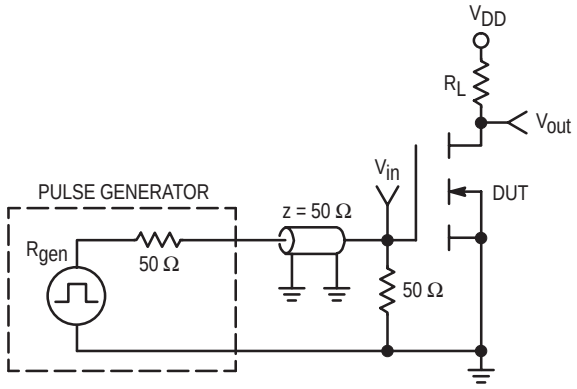


Figure 13. Switching Test Circuit

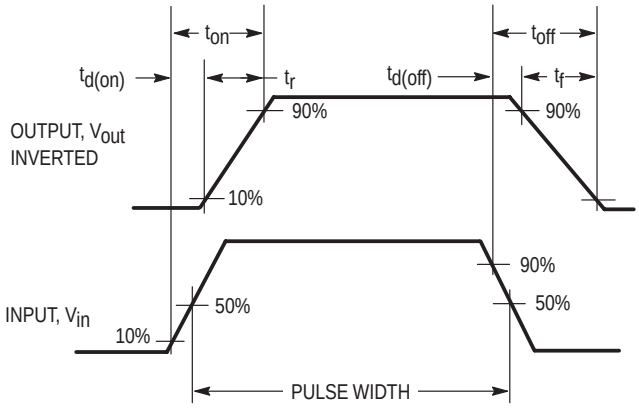


Figure 14. Switching Waveforms

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

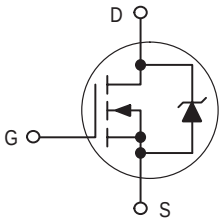
MTD6N20E

Motorola Preferred Device

TMOS POWER FET
6.0 AMPERES
200 VOLTS
$R_{DS(on)}$ = 0.7 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add –T4 Suffix to Part Number



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	200	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	6.0 3.8 18	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	50 0.4 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, I_L = 6.0 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	54	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.50 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	200 —	— 689	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 7.1	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	—	0.46	0.700	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 6.0 Adc) (I_D = 3.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	2.9 —	5.0 4.4	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 3.0 Adc)		g_{FS}	1.5	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	342	480	pF
Output Capacitance		C_{oss}	—	92	130	
Reverse Transfer Capacitance		C_{rss}	—	27	55	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 100 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.8	17.6	ns
Rise Time		t_r	—	29	58	
Turn–Off Delay Time		$t_{d(off)}$	—	22	44	
Fall Time		t_f	—	20	40.8	
Gate Charge (See Figure 8)	(V_{DS} = 160 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	13.7	21	nC
		Q_1	—	2.7	—	
		Q_2	—	7.1	—	
		Q_3	—	5.9	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc) (I_S = 6.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.99 0.9	1.2 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	138	—	ns
		t_a	—	93	—	
		t_b	—	45	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.74	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

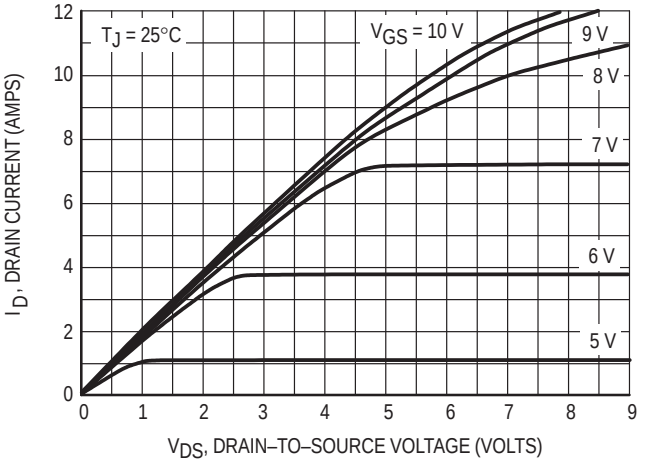


Figure 1. On–Region Characteristics

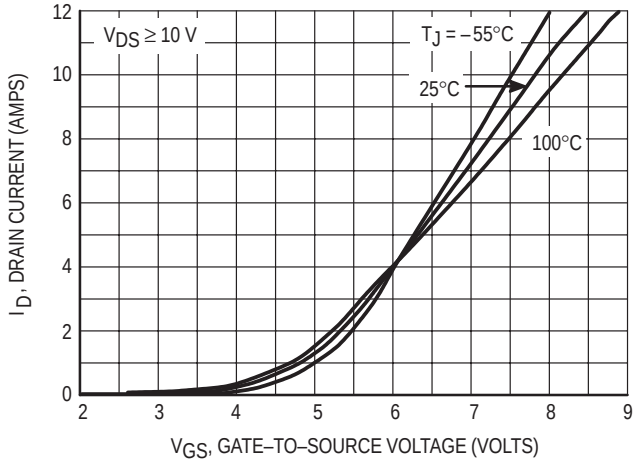


Figure 2. Transfer Characteristics

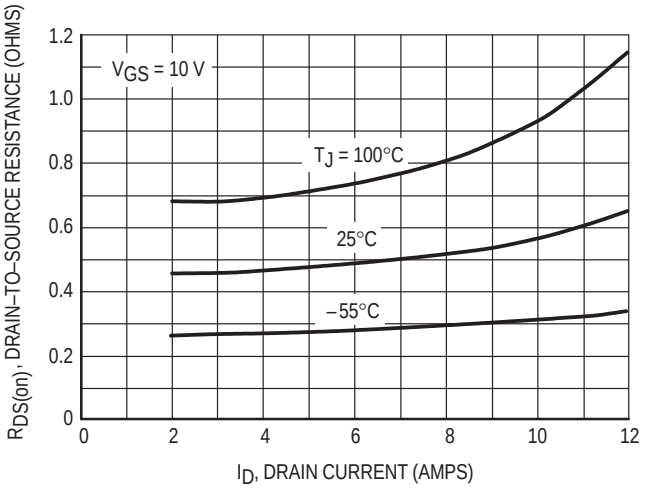


Figure 3. On–Resistance versus Drain Current and Temperature

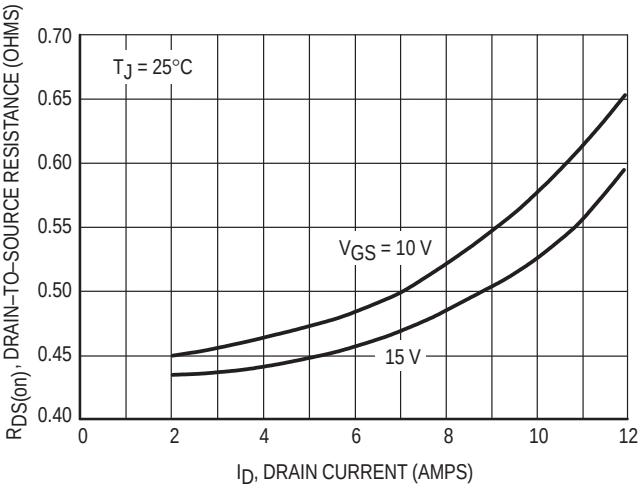


Figure 4. On–Resistance versus Drain Current and Gate Voltage

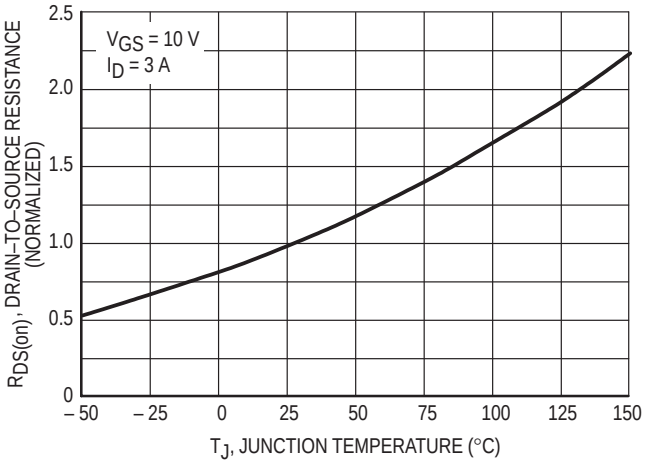


Figure 5. On–Resistance Variation with Temperature

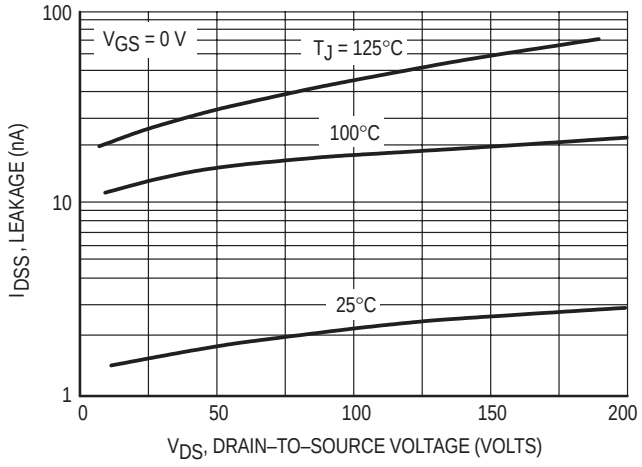


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

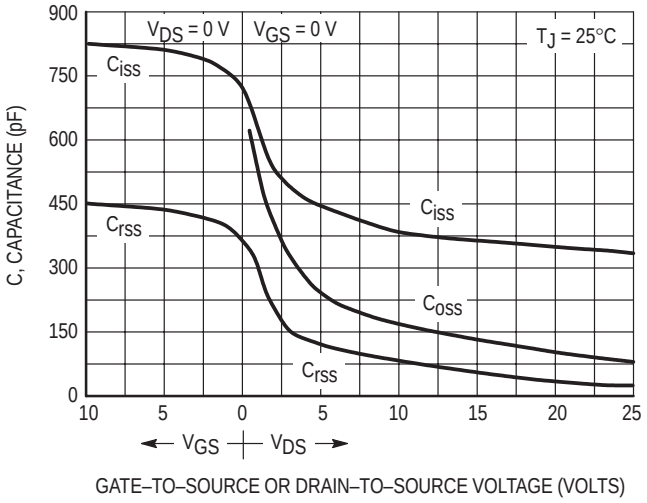


Figure 7. Capacitance Variation

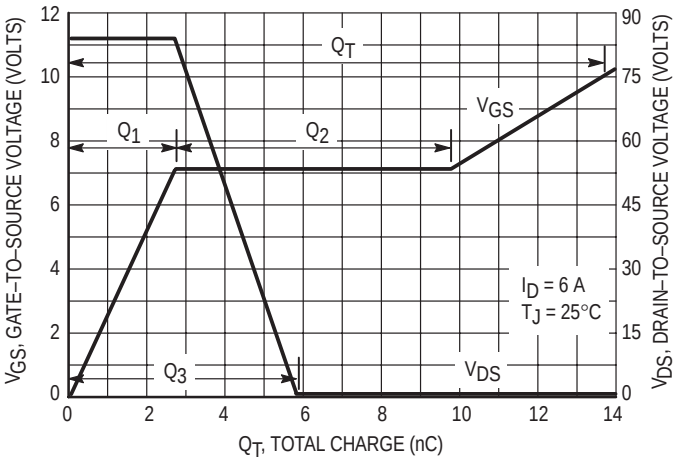


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

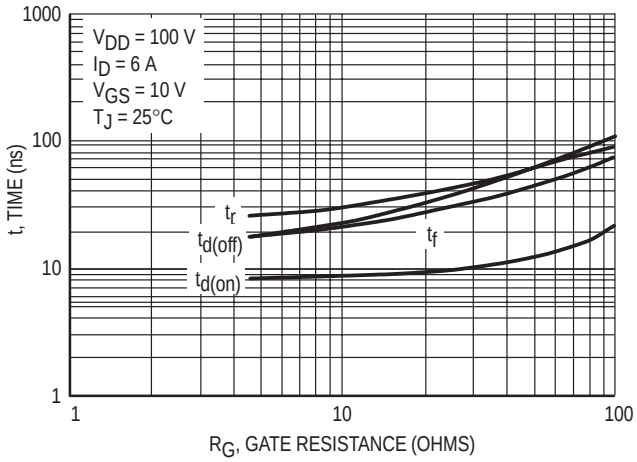


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

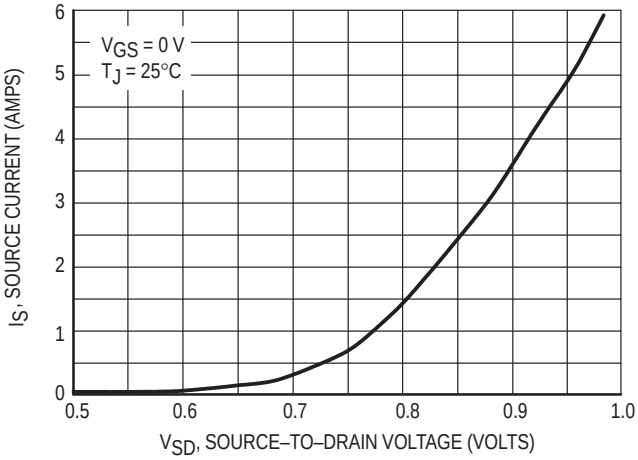


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

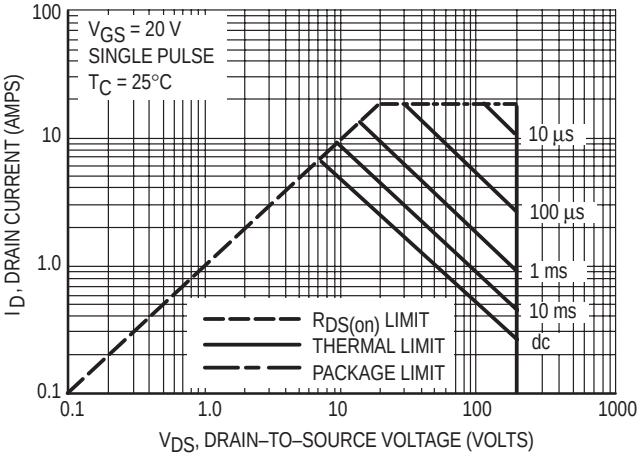


Figure 11. Maximum Rated Forward Biased Safe Operating Area

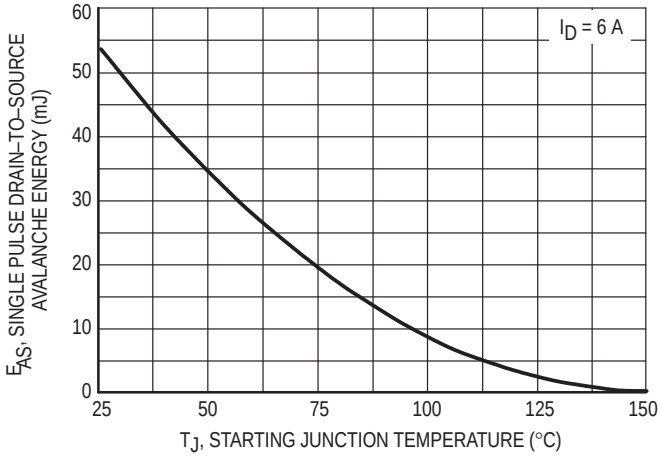


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

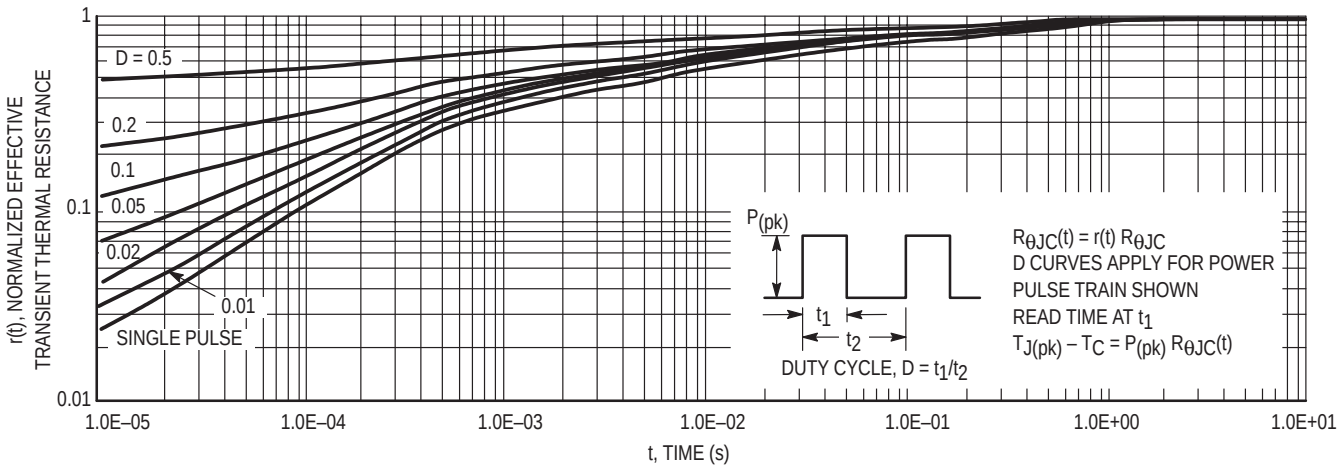


Figure 13. Thermal Response

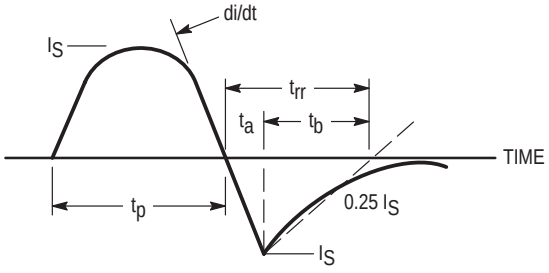


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
DPAK for Surface Mount

P–Channel Enhancement–Mode Silicon Gate

MTD6P10E

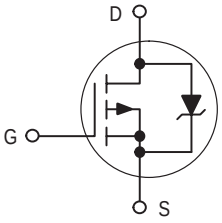
Motorola Preferred Device

TMOS POWER FET
6.0 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.66 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add –T4 Suffix to Part Number

CASE 369A–13, Style 2
DPAK



MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	100	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	6.0 3.9 18	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	50 0.4 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 6.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	180	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.50 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.250 μAdc)		$V_{(BR)DSS}$	100	—	—	Vdc
Temperature Coefficient (Positive)			—	124	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.9	4.0	Vdc
Temperature Coefficient (Negative)			—	4.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	—	0.56	0.66	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 6.0 Adc)		$V_{DS(on)}$	—	3.6	4.8	Vdc
(I_D = 3.0 Adc, T_J = 125°C)			—	—	4.2	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 3.0 Adc)		g_{FS}	1.5	3.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	550	840	pF
Output Capacitance		C_{oss}	—	154	240	
Reverse Transfer Capacitance		C_{rss}	—	27	56	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 50 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	12	25	ns
Rise Time		t_r	—	29	60	
Turn–Off Delay Time		$t_{d(off)}$	—	18	40	
Fall Time		t_f	—	9	20	
Gate Charge (See Figure 8)	(V_{DS} = 80 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	15.3	22	nC
		Q_1	—	4.1	—	
		Q_2	—	7.1	—	
		Q_3	—	6.8	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.8	5.0	Vdc
	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.5	—	
Reverse Recovery Time (See Figure 14)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	112	—	ns
		t_a	—	92	—	
		t_b	—	20	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.603	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

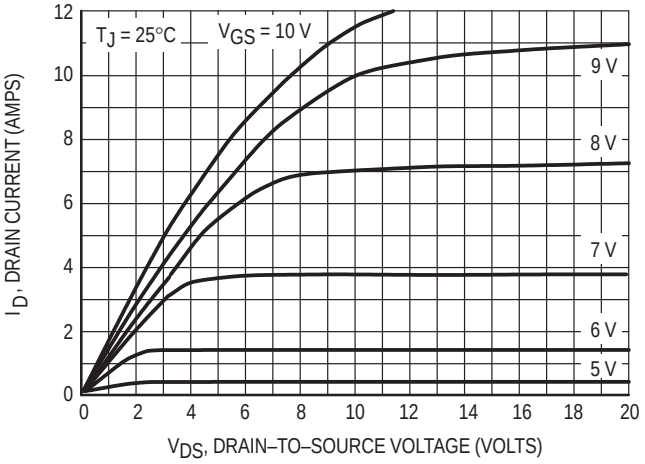


Figure 1. On–Region Characteristics

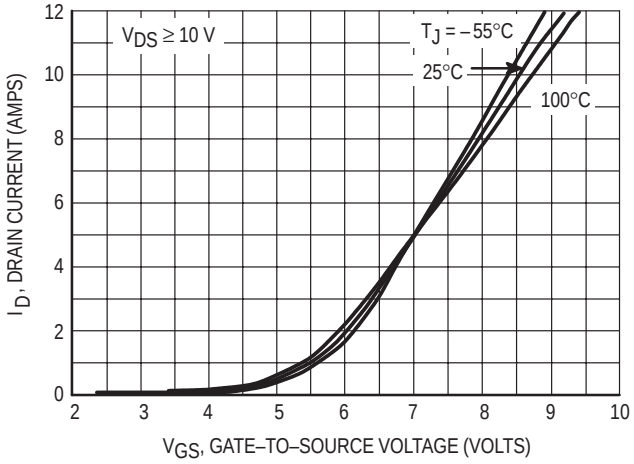
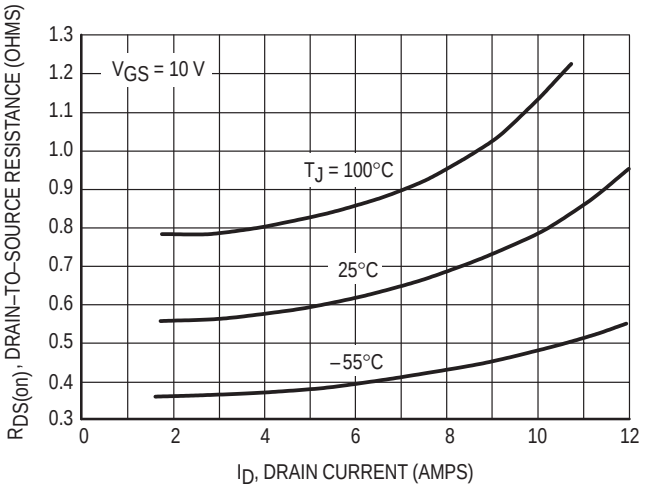


Figure 2. Transfer Characteristics



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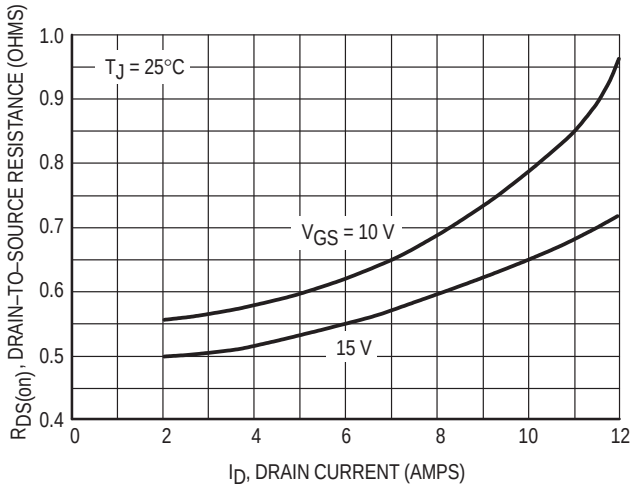

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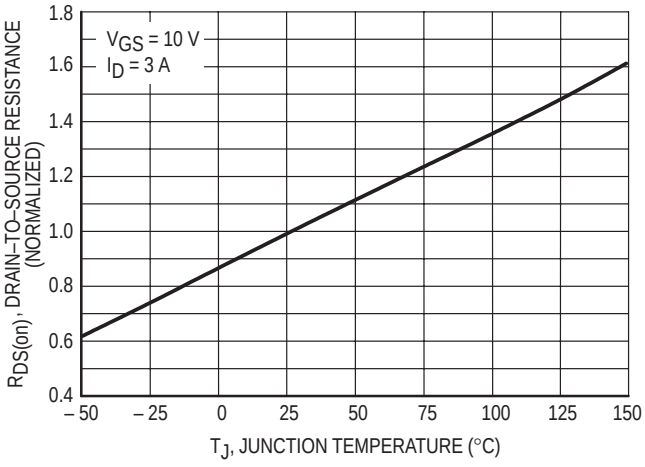
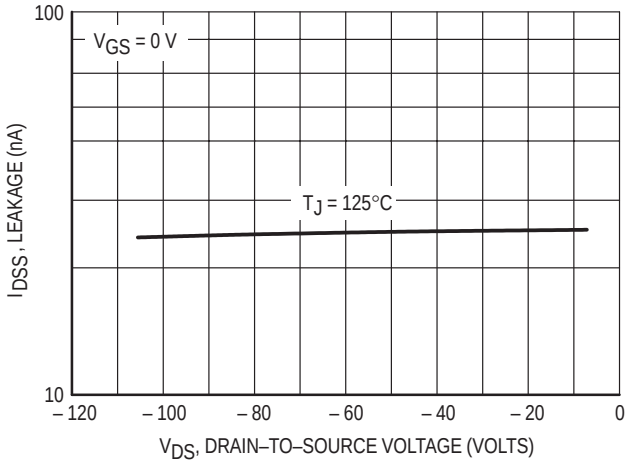


Figure 5. On–Resistance Variation with Temperature



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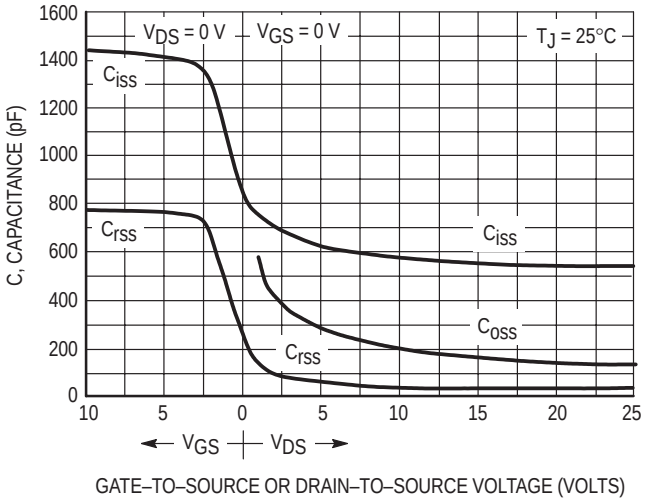

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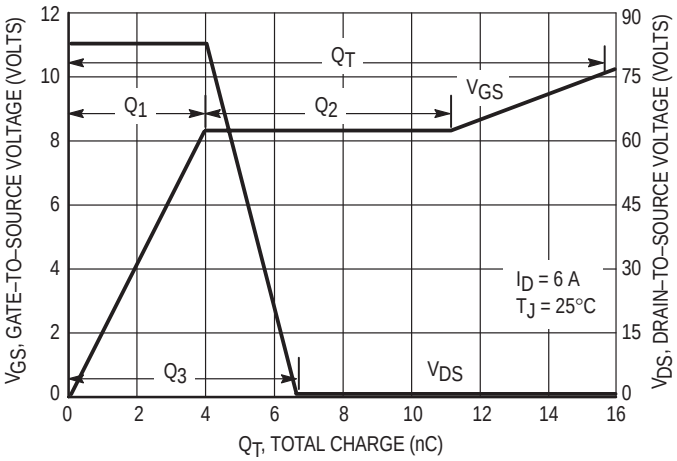

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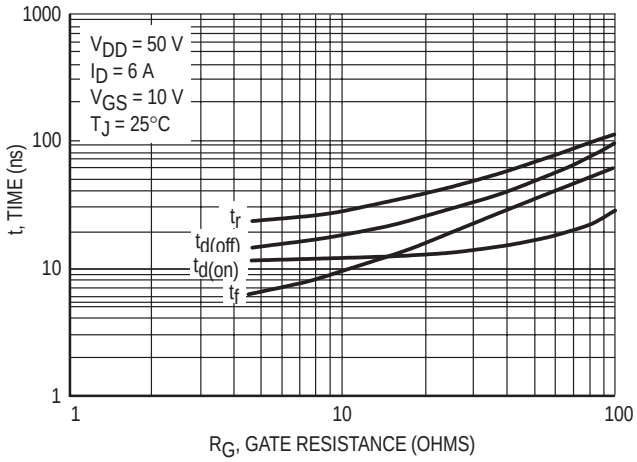
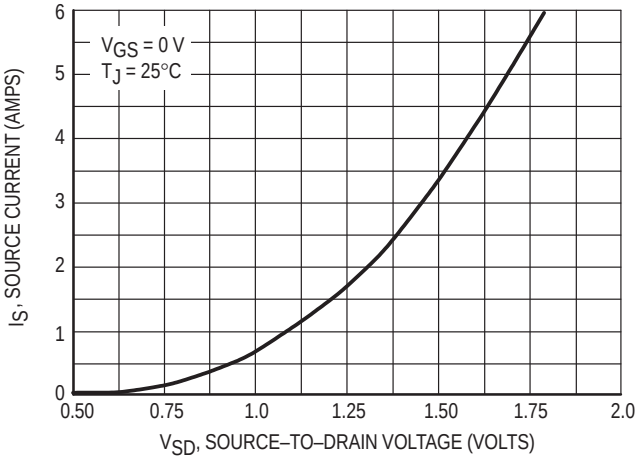


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS



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Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

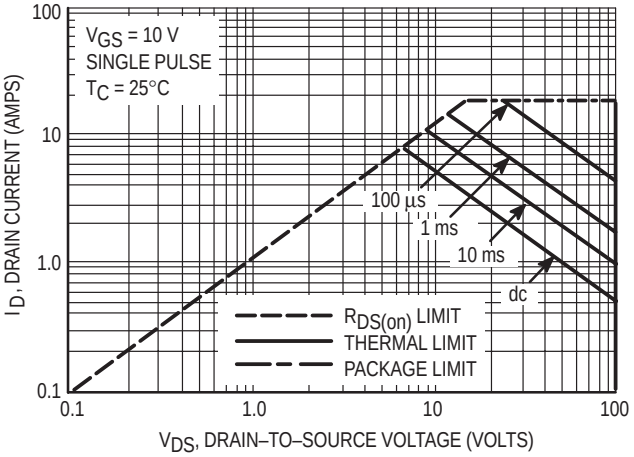


Figure 11. Maximum Rated Forward Biased Safe Operating Area

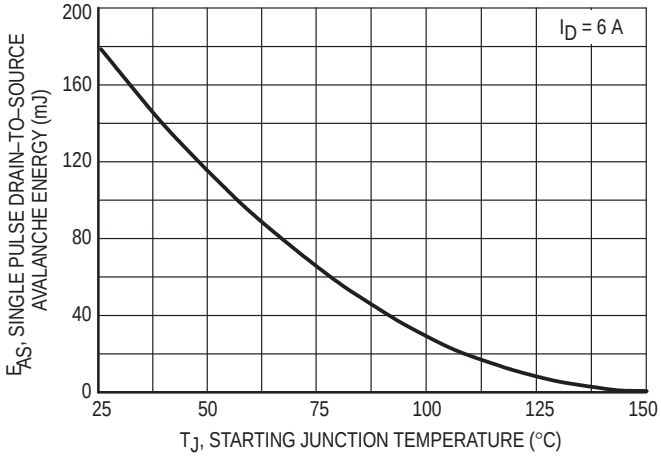


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

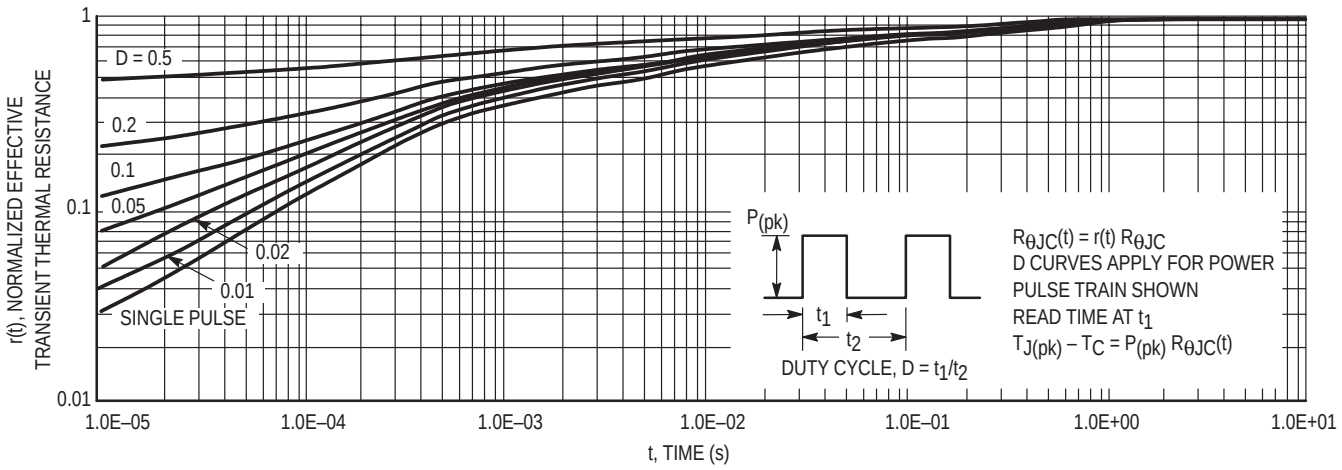


Figure 13. Thermal Response

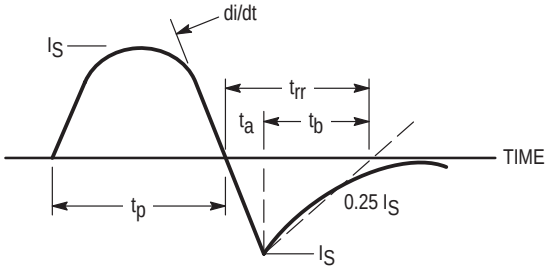


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

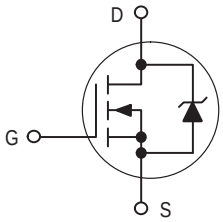
MTD9N10E

Motorola Preferred Device

TMOS POWER FET
9.0 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.25 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number
- Replaces MTD6N10



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	100	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 30	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	9.0 5.0 27	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 9.0 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	40	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	100 —	— 103	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	— 6.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 4.5 Adc)		$R_{DS(on)}$	—	0.17	0.25	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 9.0 Adc) (I_D = 4.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	2.43 2.40	Vdc
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 4.5 Adc)		g_{FS}	4.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	610	1200	pF
Output Capacitance		C_{oss}	—	176	400	
Reverse Transfer Capacitance		C_{rss}	—	14	30	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 50 Vdc, I_D = 9.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.8	20	ns
Rise Time		t_r	—	28	60	
Turn–Off Delay Time		$t_{d(off)}$	—	16	30	
Fall Time		t_f	—	4.8	10	
Gate Charge (See Figure 8)	(V_{DS} = 80 Vdc, I_D = 9.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	14	21	nC
		Q_1	—	5.2	—	
		Q_2	—	3.2	—	
		Q_3	—	6.6	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 9.0 Adc, V_{GS} = 0 Vdc) (I_S = 9.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.98 0.9	1.8 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 9.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	91	—	ns
		t_a	—	71	—	
		t_b	—	20	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.4	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

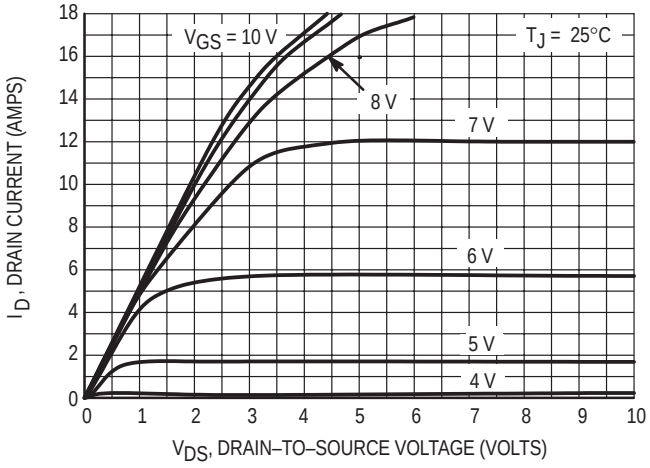


Figure 1. On–Region Characteristics

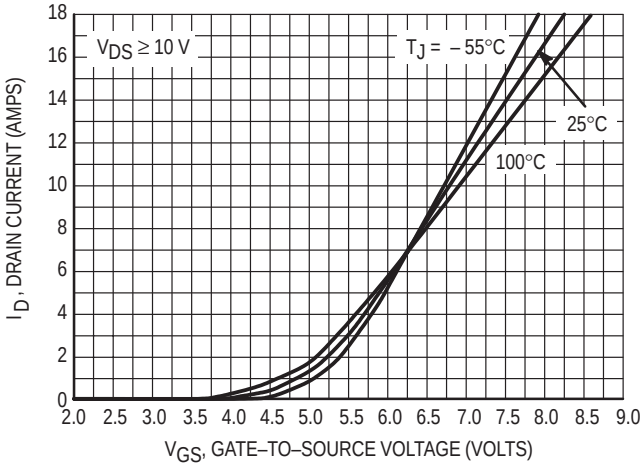


Figure 2. Transfer Characteristics

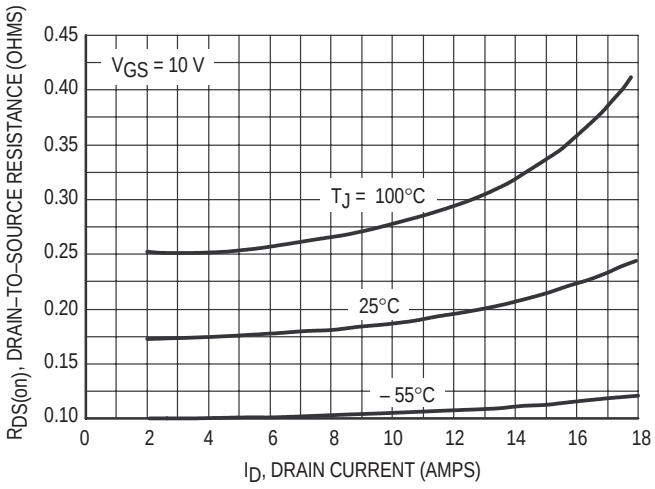


Figure 3. On–Resistance versus Drain Current and Temperature

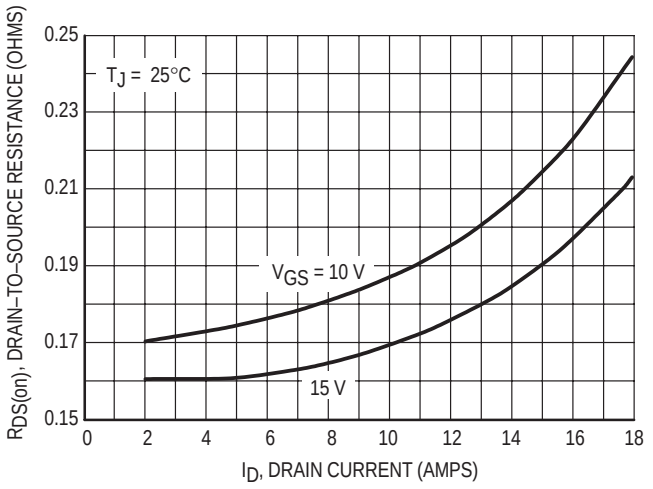


Figure 4. On–Resistance versus Drain Current and Gate Voltage

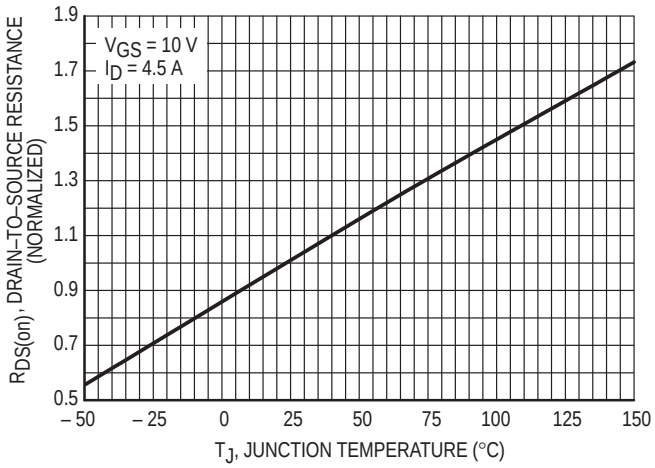


Figure 5. On–Resistance Variation with Temperature

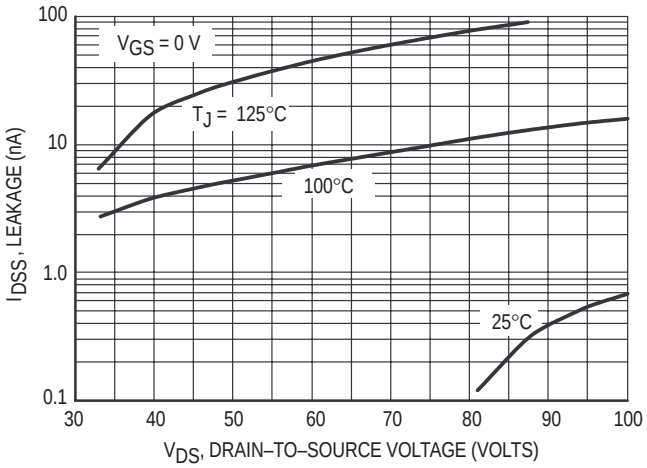


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

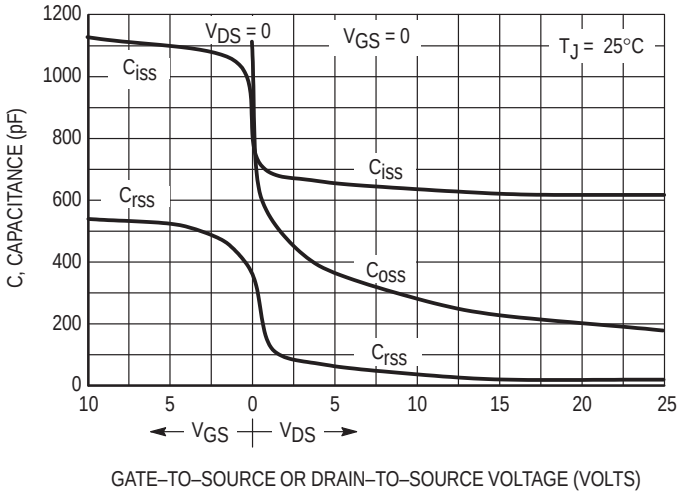


Figure 7. Capacitance Variation

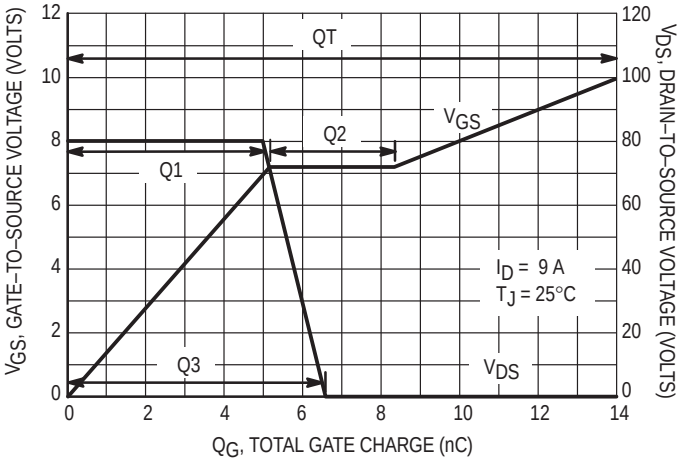


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

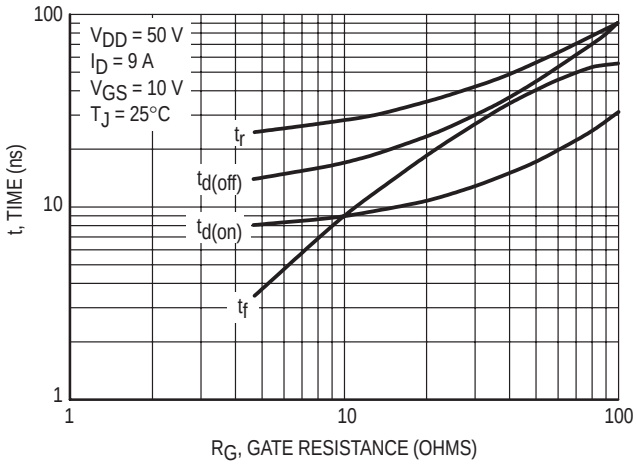


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

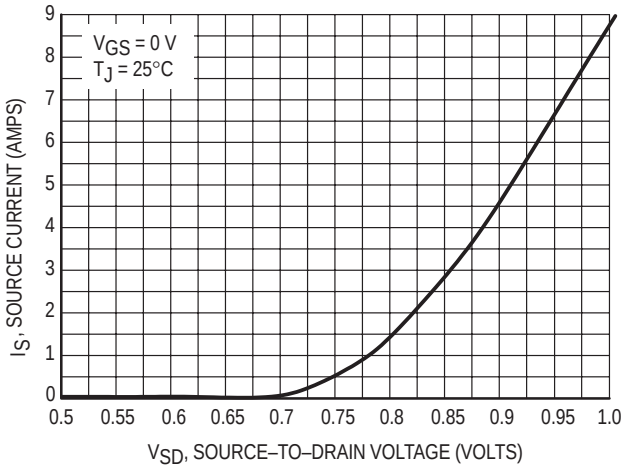


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

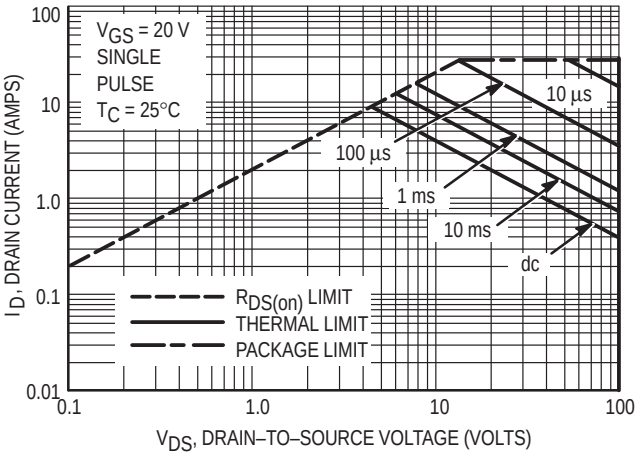


Figure 11. Maximum Rated Forward Biased Safe Operating Area

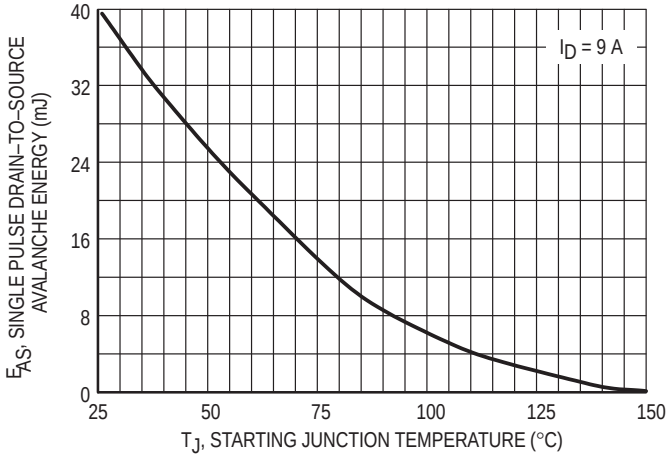


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

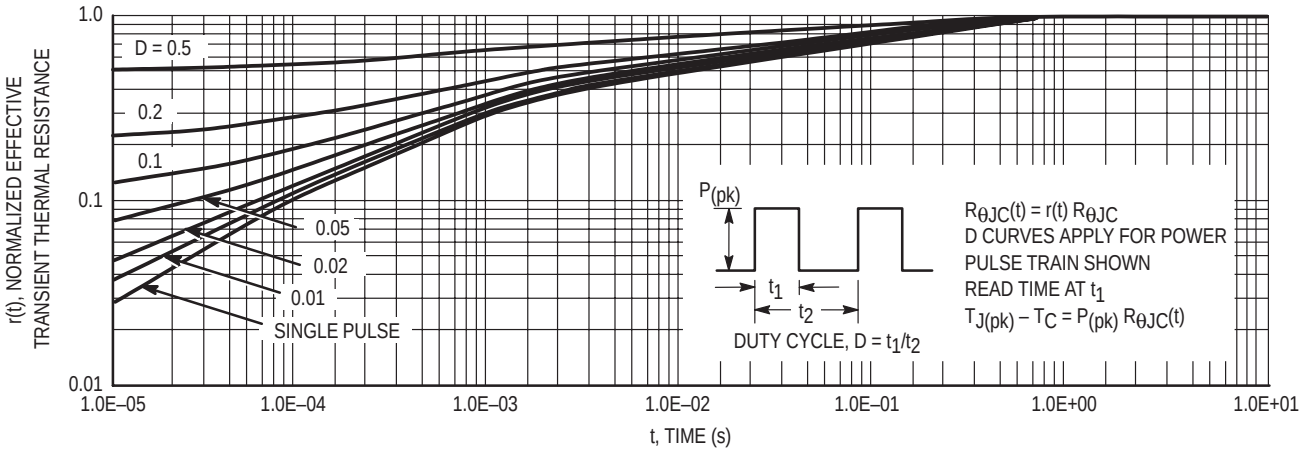


Figure 13. Thermal Response

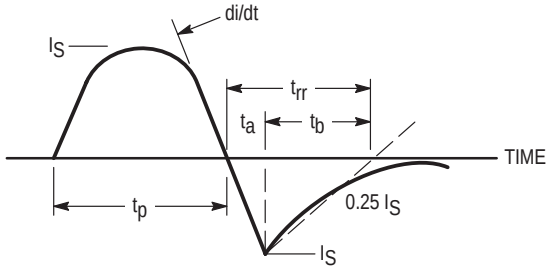


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

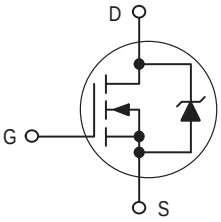
MTD10N10EL

Motorola Preferred Device

TMOS POWER FET
10 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.22 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number



CASE 369A–13, Style 2
DPAK Surface Mount

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	100	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±15 ±20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	10 6.0 35	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 10 Apk, L = 1.0 mH, R_G =25 Ω)	E_{AS}	 50	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	100	—	—	Vdc
Temperature Coefficient (Positive)			—	115	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.45	2.0	Vdc
Threshold Temperature Coefficient (Negative)			—	4.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 5.0 Adc)		$R_{DS(on)}$	—	0.17	0.22	Ohm
Drain–to–Source On–Voltage (V_{GS} = 5.0 Vdc, I_D = 10 Adc)		$V_{DS(on)}$	—	1.85	2.6	Vdc
(V_{GS} = 5.0 Vdc, I_D = 5.0 Adc, T_J = 125°C)			—	—	2.3	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 5.0 Adc)		g_{FS}	2.5	7.9	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	741	1040	pF
Output Capacitance		C_{oss}	—	175	250	
Reverse Transfer Capacitance		C_{rss}	—	18.9	40	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 50 Vdc, I_D = 10 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	11	20	ns
Rise Time		t_r	—	74	150	
Turn–Off Delay Time		$t_{d(off)}$	—	17	30	
Fall Time		t_f	—	38	80	
Gate Charge (See Figure 8)	(V_{DS} = 80 Vdc, I_D = 10 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	9.3	15	nC
		Q_1	—	2.56	—	
		Q_2	—	4.4	—	
		Q_3	—	4.66	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 10 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.98	1.6	Vdc
	(I_S = 10 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.898	—	
Reverse Recovery Time (See Figure 14)	(I_S = 10 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	124.7	—	ns
		t_a	—	86	—	
		t_b	—	38.7	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.539	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

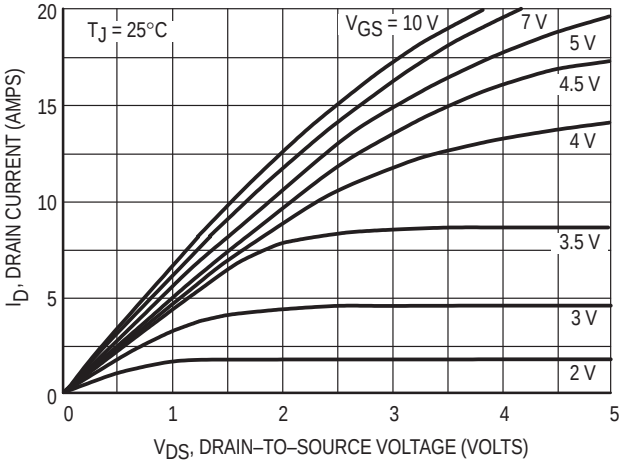


Figure 1. On–Region Characteristics

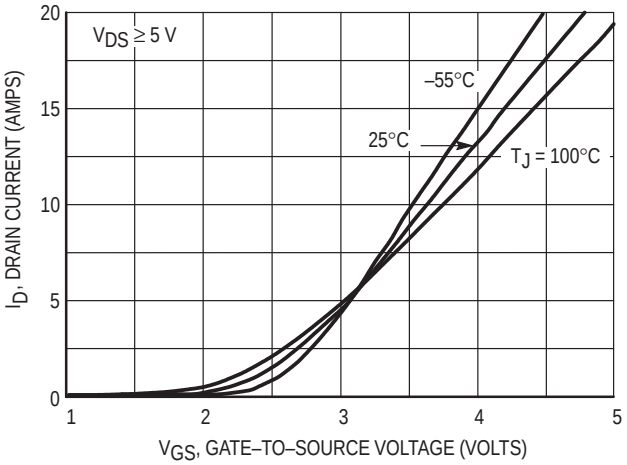


Figure 2. Transfer Characteristics

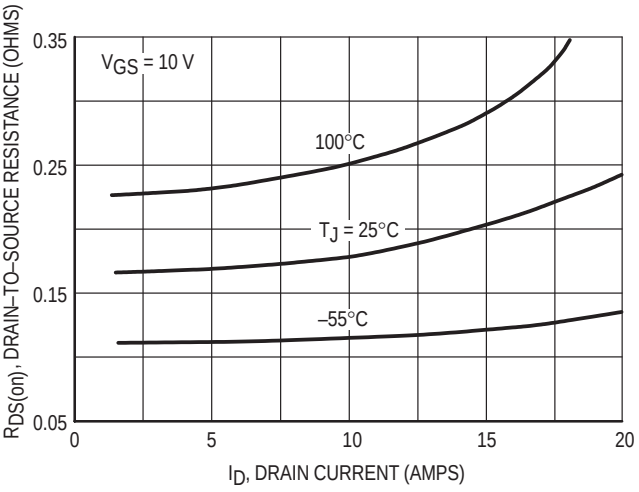


Figure 3. On–Resistance versus Drain Current and Temperature

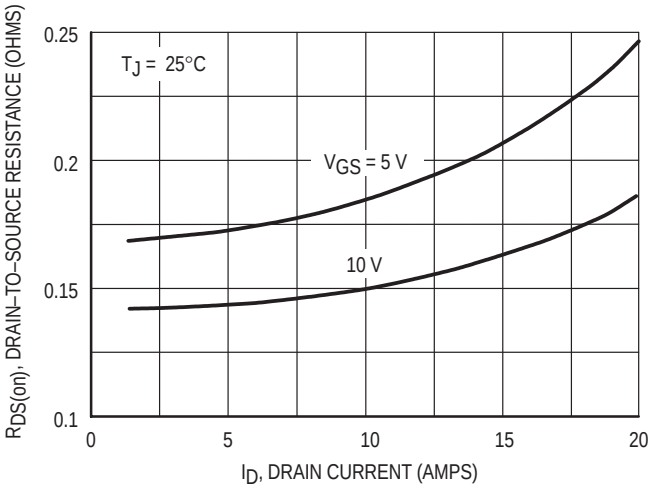


Figure 4. On–Resistance versus Drain Current and Gate Voltage

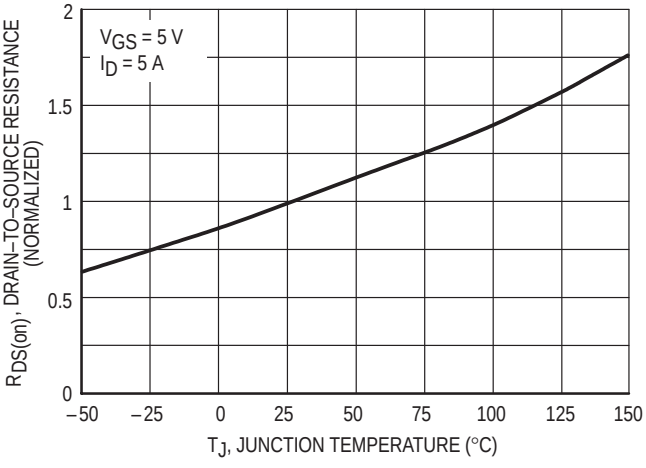


Figure 5. On–Resistance Variation with Temperature

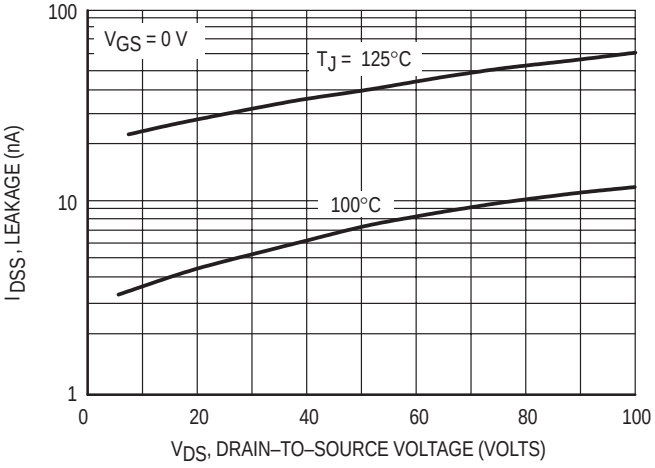


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

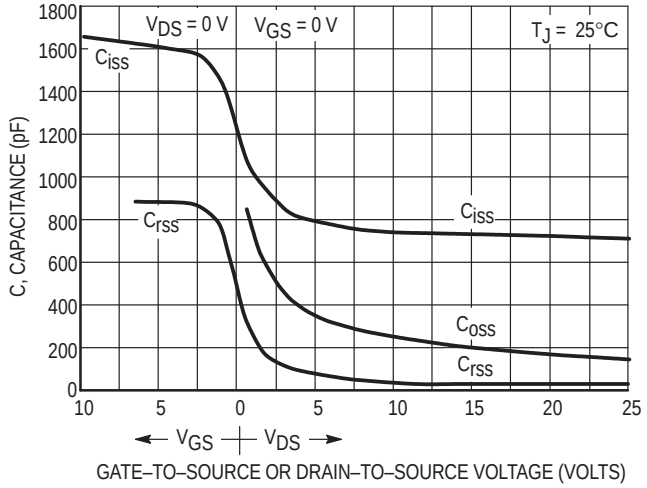


Figure 7. Capacitance Variation

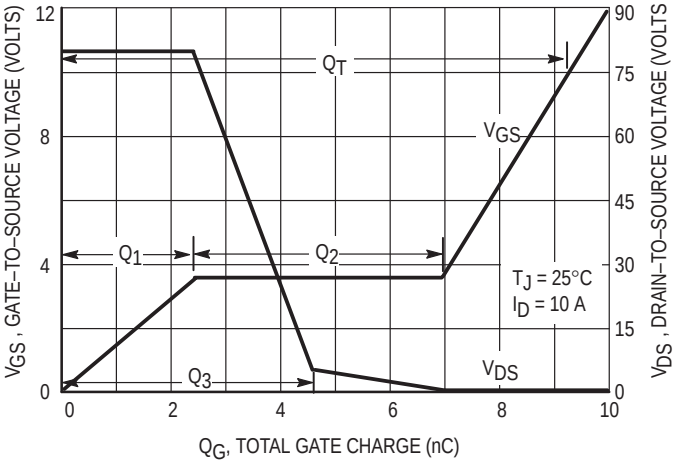


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

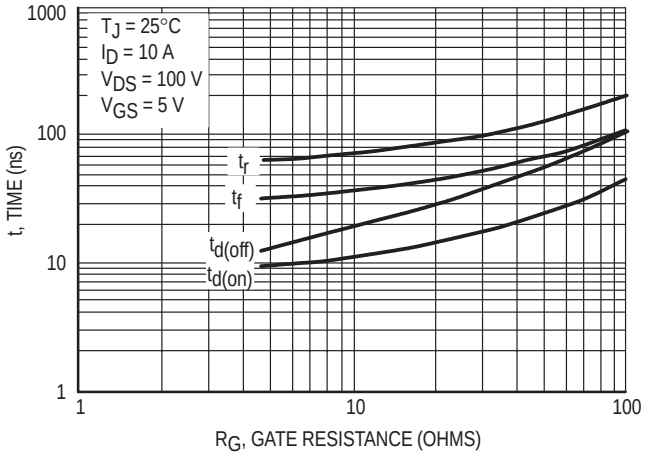


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

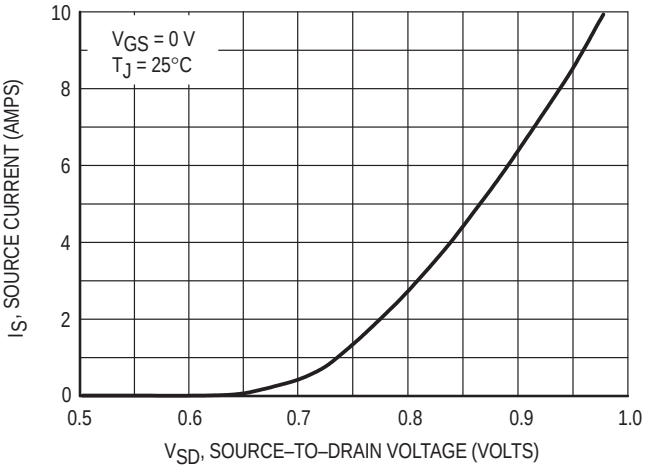


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

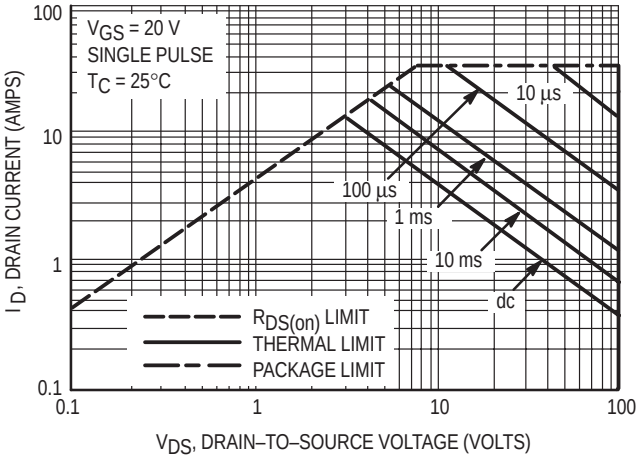


Figure 11. Maximum Rated Forward Biased Safe Operating Area

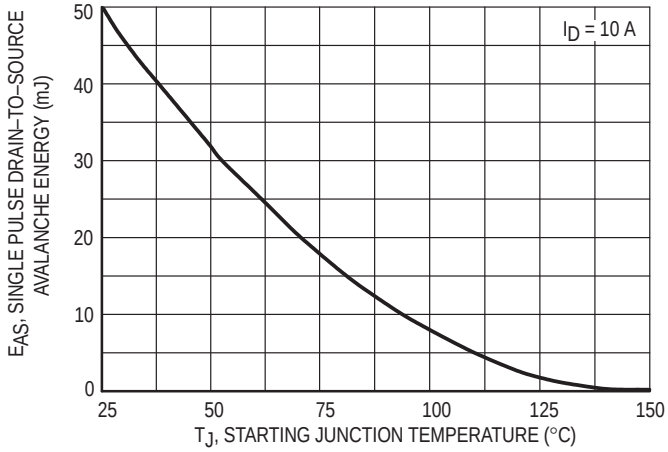


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

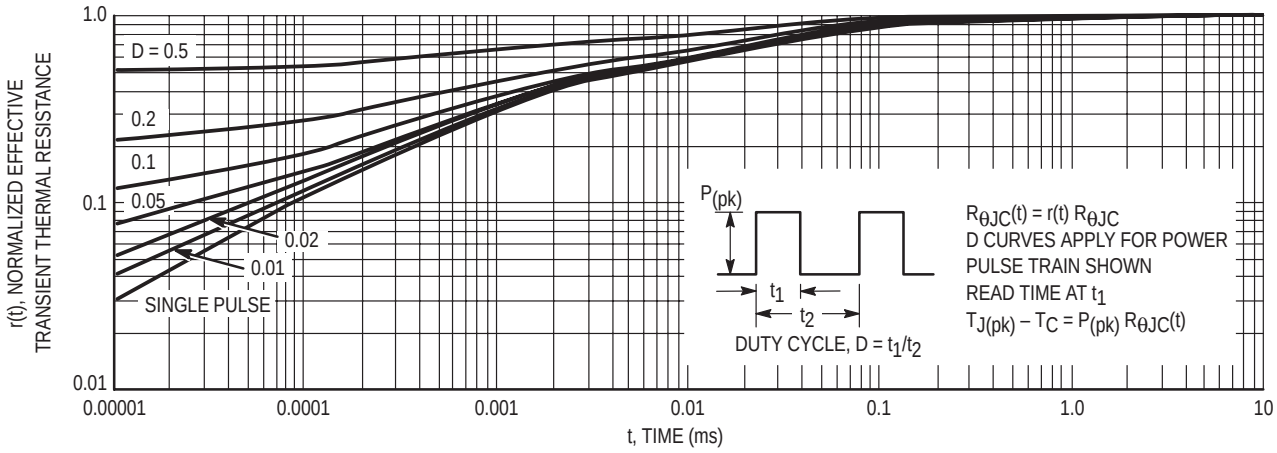


Figure 13. Thermal Response

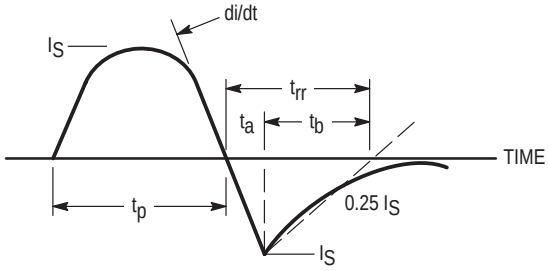


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
High Energy Power FET
DPAK for Surface Mount or Insertion Mount

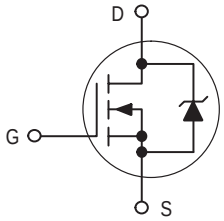
N–Channel Enhancement–Mode Silicon Gate

MTD12N06EZL

TMOS POWER FET
12 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.180 OHM

This advanced TMOS power FET is designed to withstand high energy in the avalanche and mode and switch efficiently. This new high energy device also offers a gate–to–source zener diode designed for 4 kV ESD protection (human body model).

- ESD Protected
- 4 kV Human Body Model
- 400 V Machine Model
- Avalanche Energy Capability
- Internal Source–To–Drain Diode Designed to Replace External Zener Transient Suppressor–Absorbs High Energy in the Avalanche Mode



CASE 369A–13, Style 2
DPAK Surface Mount

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive (t_p ±50 ms)	V_{GS} V_{GSM}	±15 ±20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	12 7.1 36	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	45 0.36 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 12 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	72	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.78 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

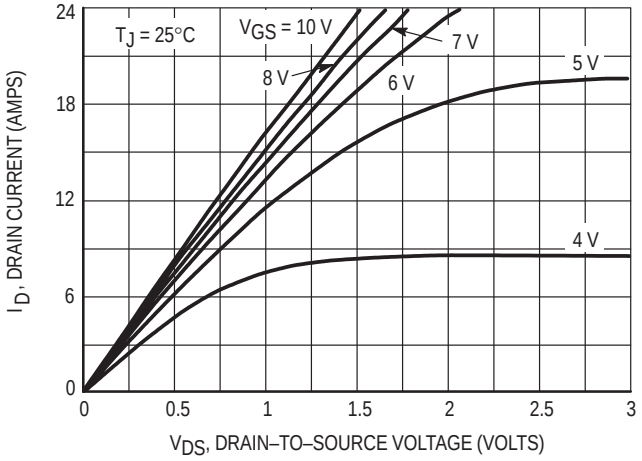
Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	0.06	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Source Breakdown Voltage (V_{DS} = 0 V, I_G = 10 mA)			18	—	—	Vdc
Gate–Body Leakage Current		I_{GSS}				
(V_{GS} = ±10 Vdc, V_{DS} = 0 V, T_J = 25°C)			—	—	500	nAdc
(V_{GS} = ±10 Vdc, V_{DS} = 0 V, T_J = 150°C)			—	—	100	μAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Temperature Coefficient (Negative)			—	4.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	—	—	0.18	Ohm
Drain–Source On–Voltage (V_{GS} = 5.0 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 12 Adc)			—	—	2.6	
(I_D = 6.0 Adc, T_J = 125°C)			—	—	2.3	
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 6.0 Adc)		g_{FS}	3.0	6.8	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	430	600	pF
Output Capacitance		C_{oss}	—	224	310	
Reverse Transfer Capacitance		C_{rss}	—	51	100	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DS} = 30 Vdc, I_D = 12 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	70	90	ns
Rise Time		t_r	—	436	540	
Turn–Off Delay Time		$t_{d(off)}$	—	158	380	
Fall Time		t_f	—	186	340	
Gate Charge (See Figures 8 & 9)	(V_{DS} = 48 Vdc, I_D = 12 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	10.6	40	nC
		Q_1	—	1.4	—	
		Q_2	—	5.9	—	
		Q_3	—	6.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 12 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.1	1.4	Vdc
	(I_S = 12 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.05	—	
Reverse Recovery Time (See Figure 14)	(I_S = 12 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	325	—	ns
		t_a	—	124	—	
		t_b	—	201	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.013	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS



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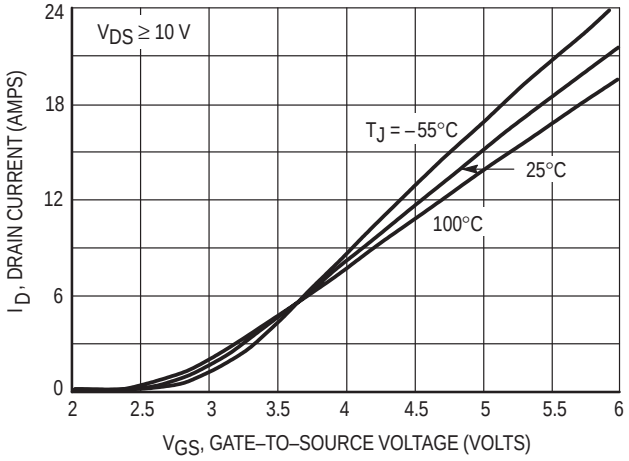

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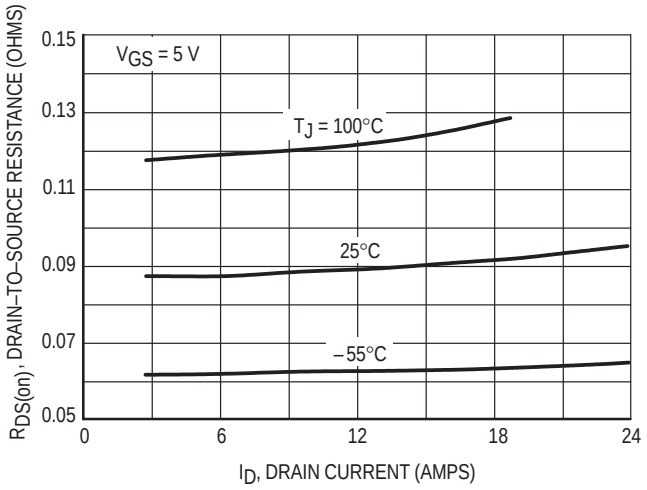

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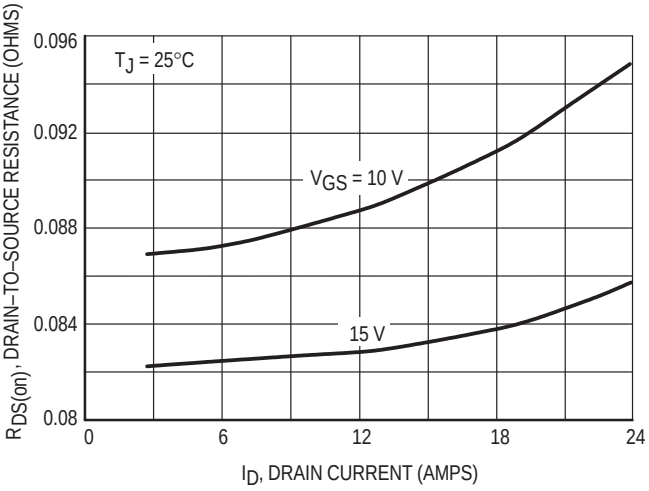

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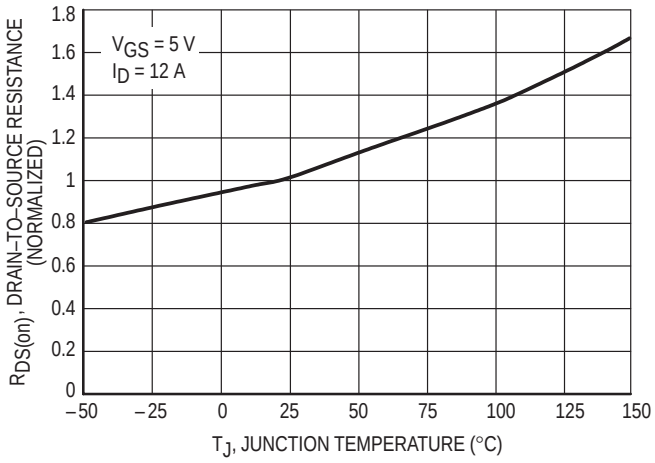

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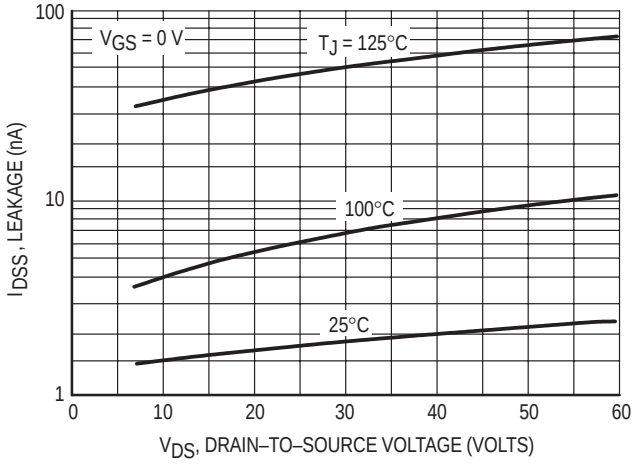

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$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

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$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

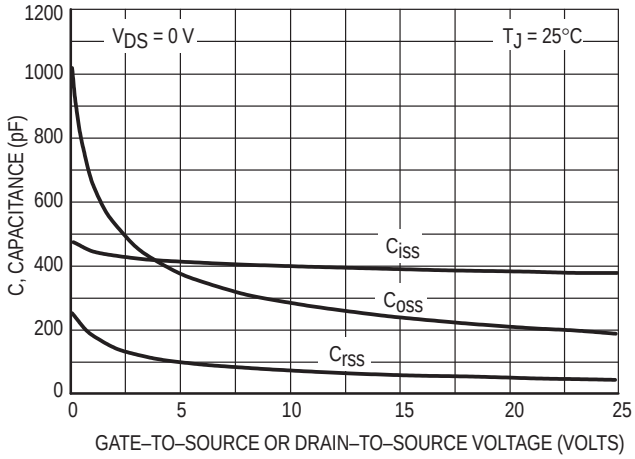


Figure 7. Capacitance Variation

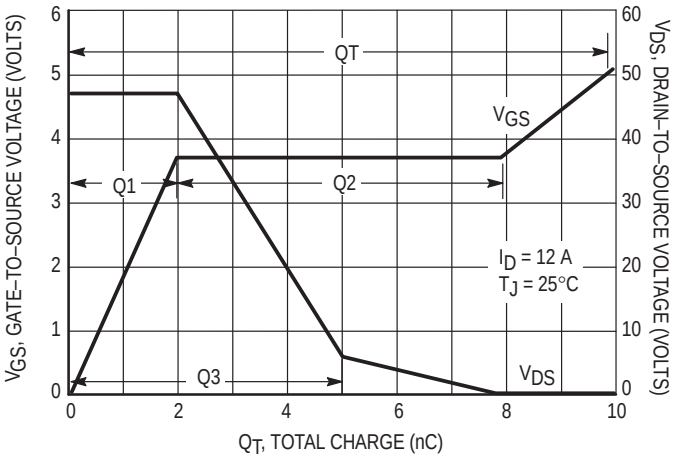


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

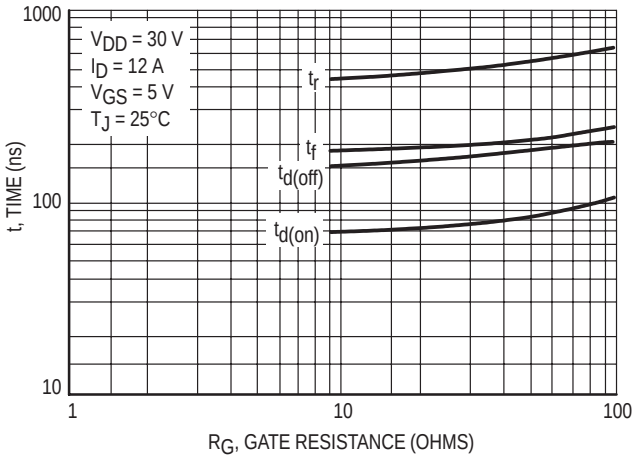


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

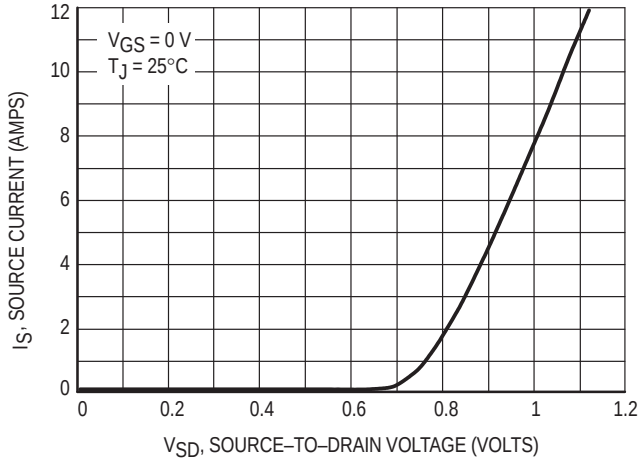


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

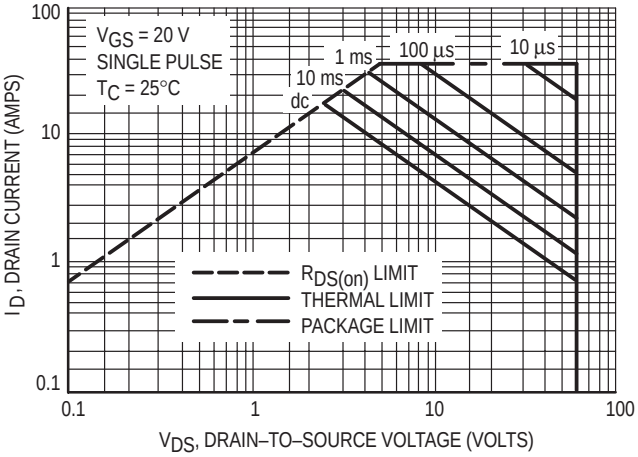


Figure 11. Maximum Rated Forward Biased Safe Operating Area

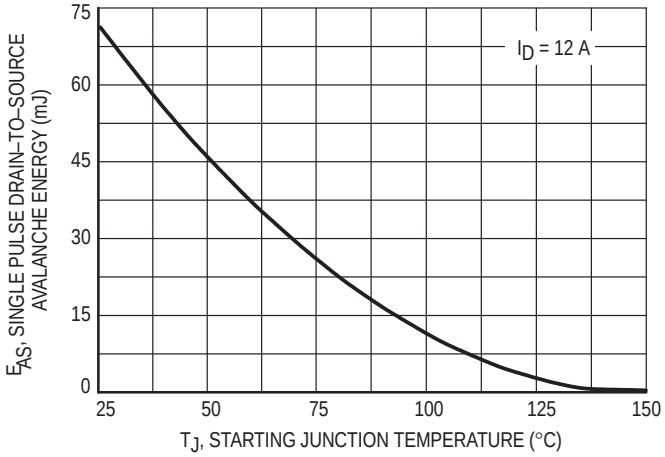


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

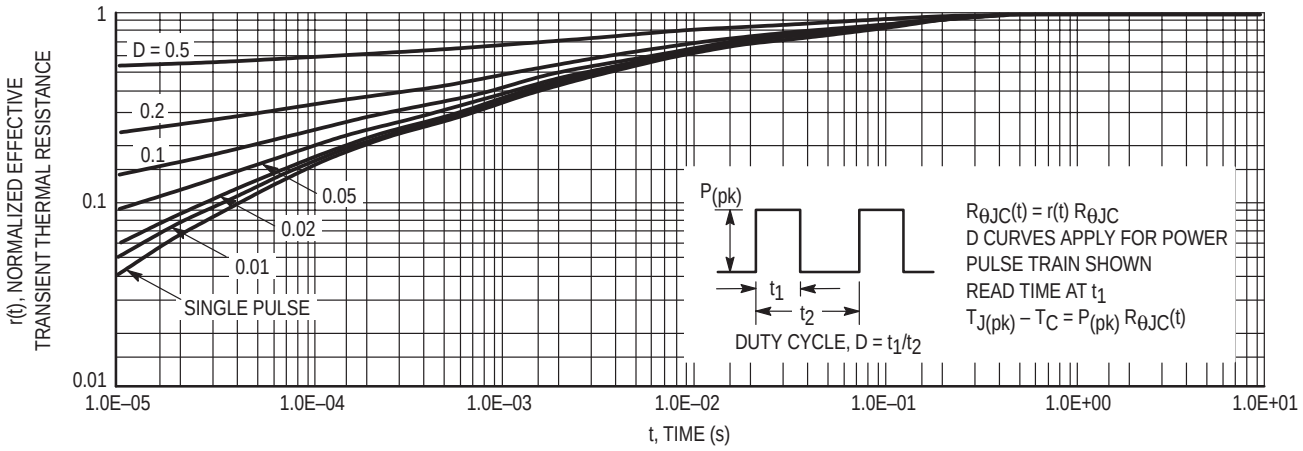


Figure 13. Thermal Response

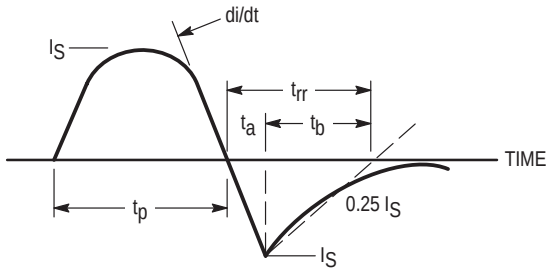


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

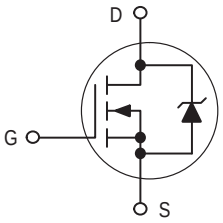
TMOS V
Power Field Effect Transistor
DPAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

MTD15N06V

Motorola Preferred Device

TMOS POWER FET
15 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.12 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.



CASE 369A–13, Style 2
DPAK Surface Mount

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Single Pulse ($t_p \le 50$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	15 8.7 45	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	55 0.36 2.1	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 15 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	113	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.73 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	60 —	— 67	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	2.7 5.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$R_{DS(on)}$	—	0.08	0.12	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 15 Adc) (I_D = 7.5 Adc, T_J = 150°C)		$V_{DS(on)}$	— —	2.0 —	2.2 1.9	Vdc
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 7.5 Adc)		g_{FS}	4.0	6.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	469	660	pF
Output Capacitance		C_{oss}	—	148	200	
Reverse Transfer Capacitance		C_{rss}	—	35	60	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 15 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	7.6	20	ns
Rise Time		t_r	—	51	100	
Turn–Off Delay Time		$t_{d(off)}$	—	18	40	
Fall Time		t_f	—	33	70	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 15 Adc, V_{GS} = 10 Vdc)	Q_T	—	14.4	20	nC
		Q_1	—	2.8	—	
		Q_2	—	6.4	—	
		Q_3	—	6.1	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 15 Adc, V_{GS} = 0 Vdc) (I_S = 15 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	— —	1.05 1.5	1.6 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 15 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	59.3	—	ns
		t_a	—	46	—	
		t_b	—	13.3	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.165	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

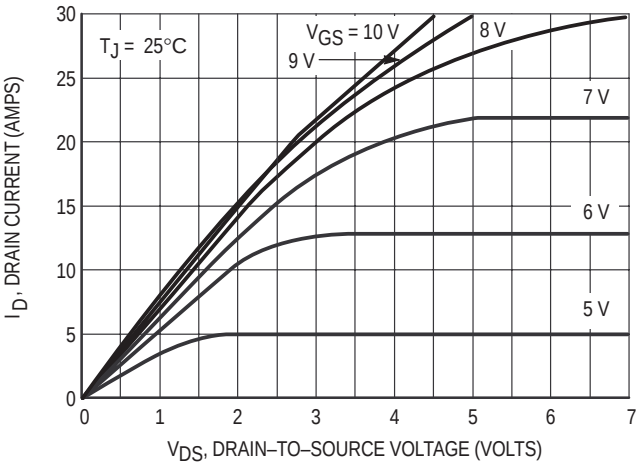


Figure 1. On–Region Characteristics

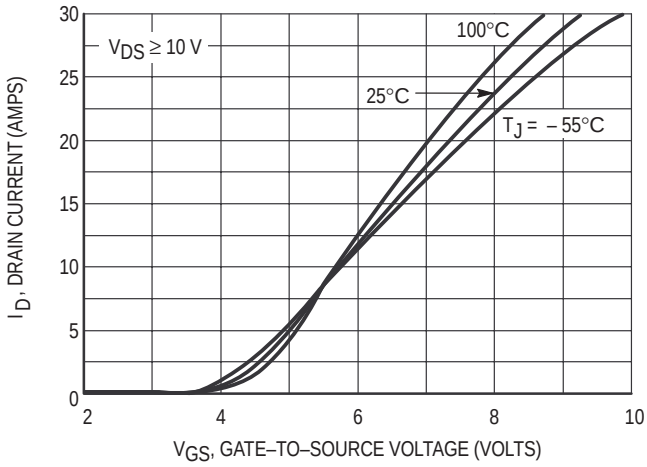


Figure 2. Transfer Characteristics

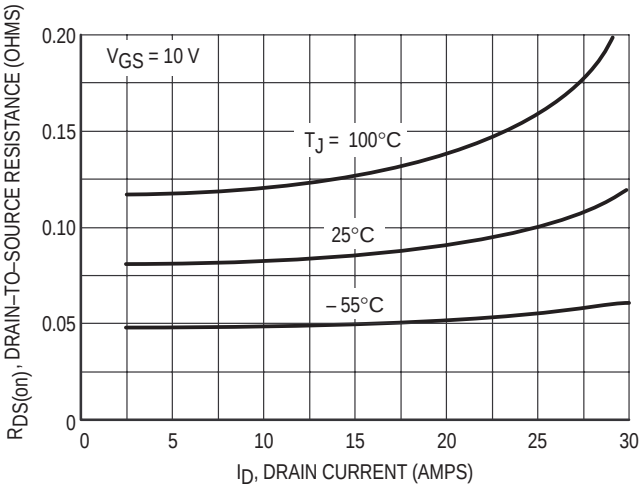


Figure 3. On–Resistance versus Drain Current and Temperature

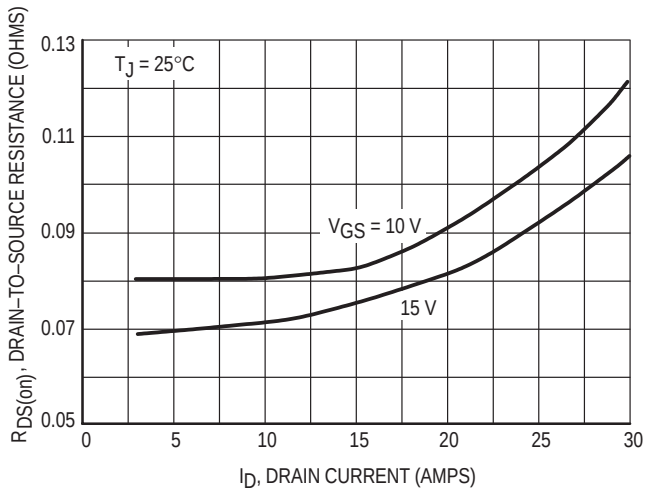


Figure 4. On–Resistance versus Drain Current and Gate Voltage

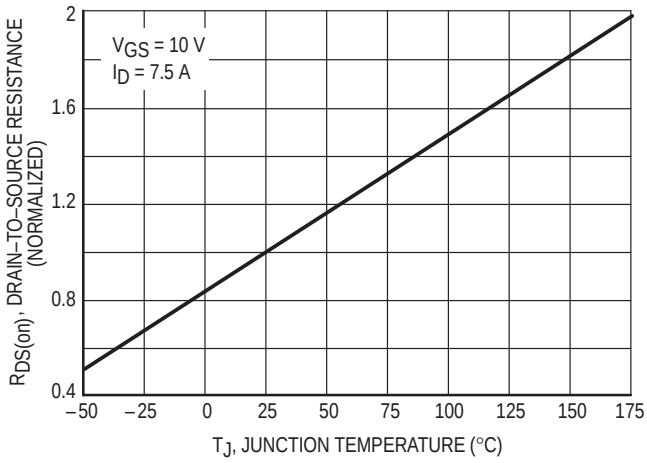


Figure 5. On–Resistance Variation with Temperature

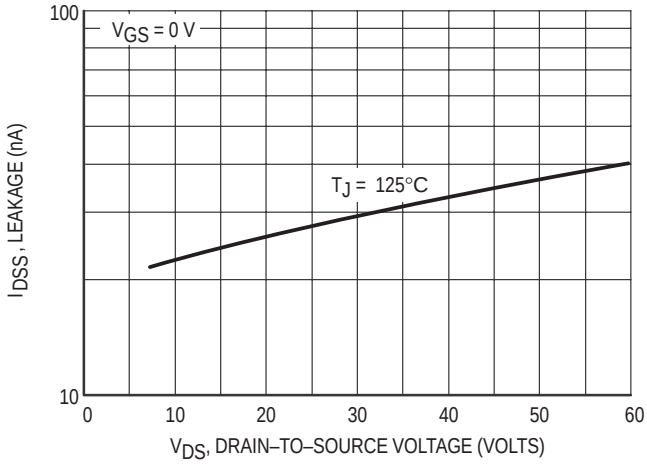


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

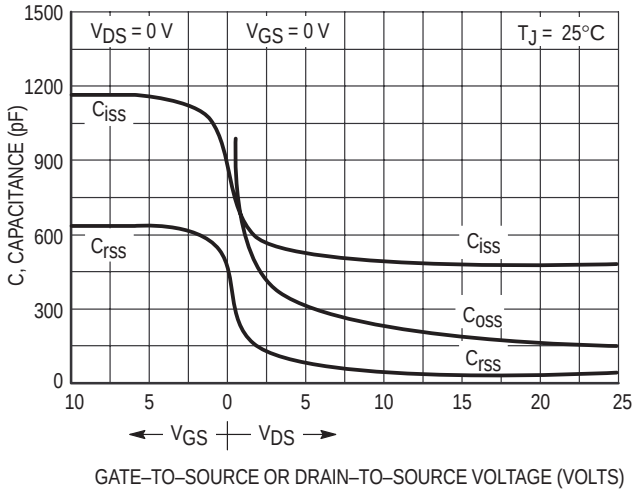
$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.



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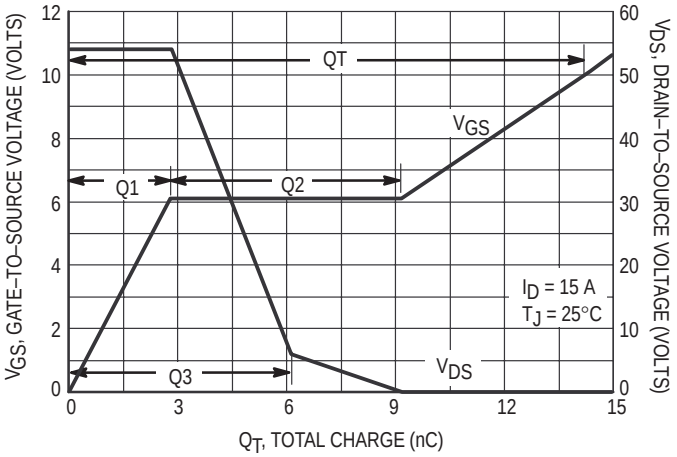
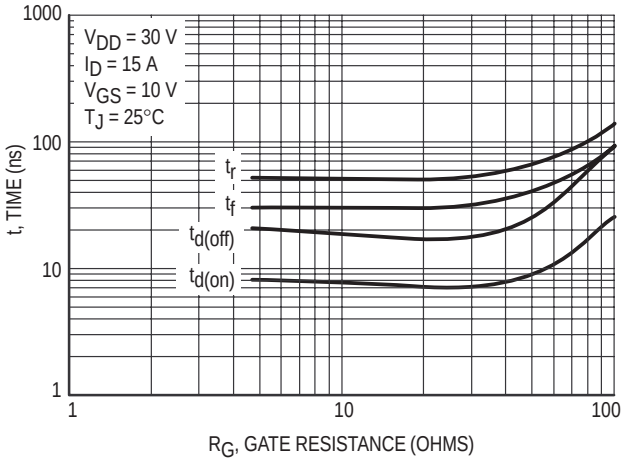


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge



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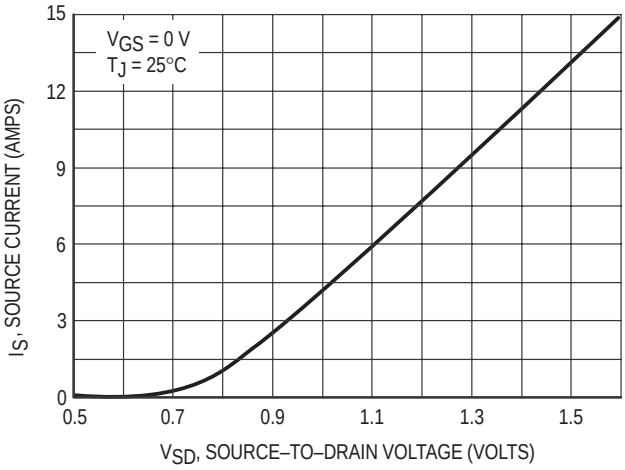
DRAIN–TO–SOURCE DIODE CHARACTERISTICS



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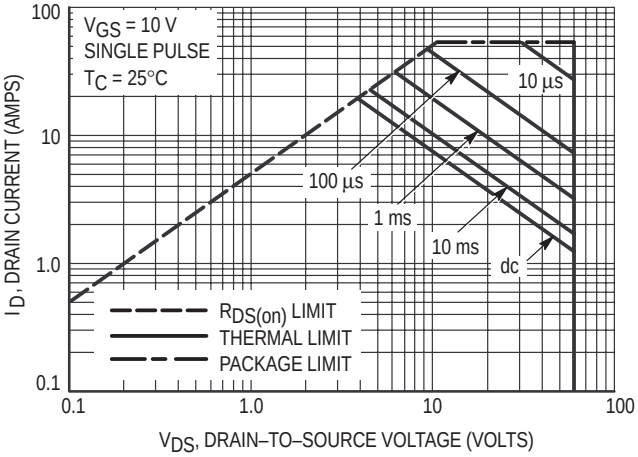

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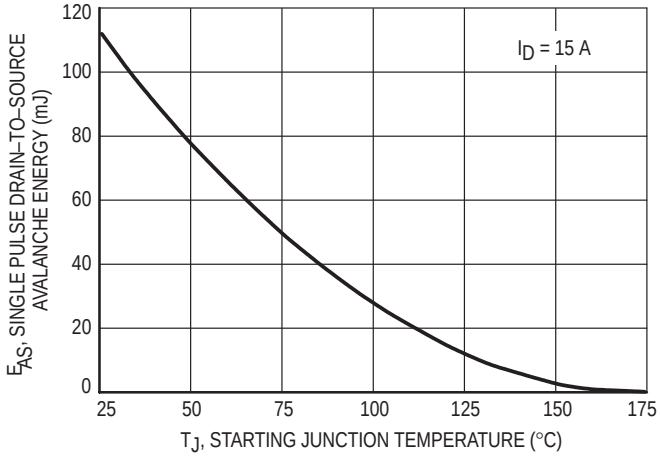

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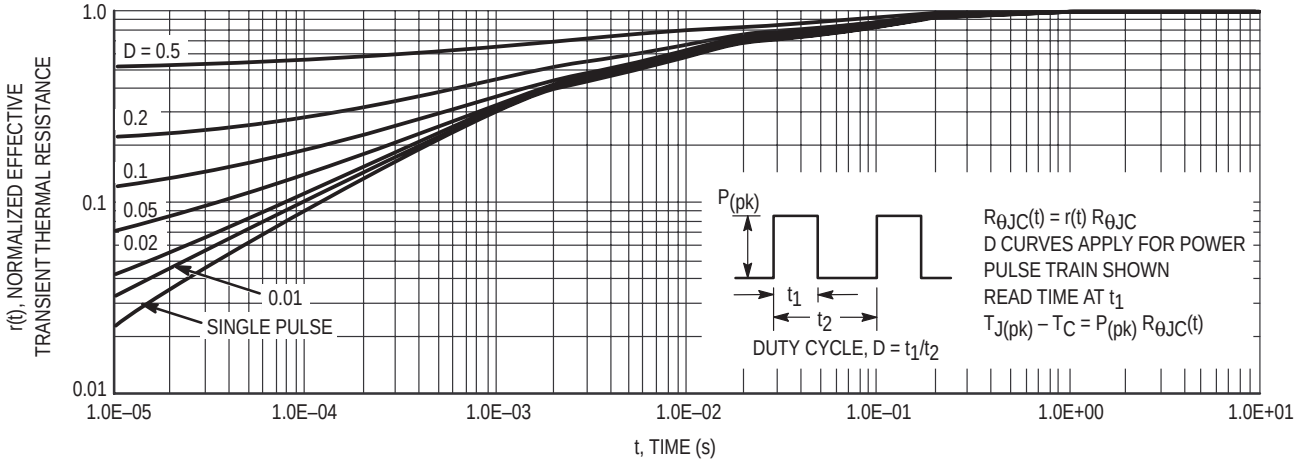

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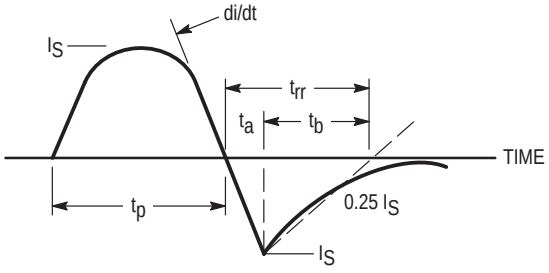

Figure 14. Diode Reverse Recovery Waveform

Product Preview

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Power Field Effect Transistor
DPAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

MTD15N06VL

TMOS POWER FET
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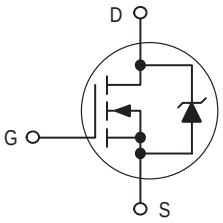
TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.



CASE 369A–13, Style 2
DPAK Surface Mount

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 25	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	15 12 53	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ 25°C(1)	P_D	60 0.4 2.1	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 15 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	113	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient(1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.5 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 7.5 Adc)		$R_{DS(on)}$	—	0.075	0.085	Ohm
Drain–to–Source On–Voltage (V_{GS} = 5.0 Vdc, I_D = 15 Adc)		$V_{DS(on)}$	—	—	1.5	Vdc
(V_{GS} = 5.0 Vdc, I_D = 7.5 Adc, T_J = 150°C)			—	—	1.3	
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 7.5 Adc)		g_{FS}	8.0	10	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	630	880	pF
Output Capacitance		C_{oss}	—	270	380	
Reverse Transfer Capacitance		C_{rss}	—	56	110	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 15 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	26	50	ns
Rise Time		t_r	—	105	210	
Turn–Off Delay Time		$t_{d(off)}$	—	80	160	
Fall Time		t_f	—	70	140	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 15 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	12	20	nC
		Q_1	—	3.0	—	
		Q_2	—	8.0	—	
		Q_3	—	10	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 15 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.6	Vdc
	(I_S = 15 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.9	—	
Reverse Recovery Time	(I_S = 15 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	100	—	ns
		t_a	—	55	—	
		t_b	—	45	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.345	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

Designer's™ Data Sheet

HDTMOS E-FET™
High Density Power FET
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

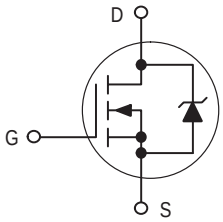
MTD20N03HDL

Motorola Preferred Device

TMOS POWER FET
LOGIC LEVEL
20 AMPERES
30 VOLTS
$R_{DS(on)}$ = 0.035 OHM

This advanced HDTMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	30	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±15 ± 20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	20 16 60	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_C = 25°C, when mounted with the minimum recommended pad size	P_D	74 0.6 1.75	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 20 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	200	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.67 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage ($C_{pk} \geq 2.0$) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			30	—	—	
Temperature Coefficient (Positive)			—	43	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 30 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current		I_{GSS}				nAdc
(V_{GS} = ±15 Vdc, V_{DS} = 0 Vdc)			—	—	100	
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($C_{pk} \geq 2.0$) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			1.0	1.5	2.0	
Threshold Temperature Coefficient (Negative)			—	5.0	—	mV/°C
Static Drain–to–Source On–Resistance ($C_{pk} \geq 2.0$) (3)		$R_{DS(on)}$				Ohm
(V_{GS} = 4.0 Vdc, I_D = 10 Adc)			—	0.034	0.040	
(V_{GS} = 5.0 Vdc, I_D = 10 Adc)				0.030	0.035	
Drain–to–Source On–Voltage (V_{GS} = 5.0 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 20 Adc)			—	0.55	0.8	
(I_D = 10 Adc, T_J = 125°C)			—	—	0.7	
Forward Transconductance		g_{FS}				mhos
(V_{DS} = 5.0 Vdc, I_D = 10 Adc)			10	13	—	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	880	1260	pF
Output Capacitance		C_{oss}	—	300	420	
Transfer Capacitance		C_{rss}	—	80	112	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 20 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	13	15.8	ns
Rise Time		t_r	—	212	238	
Turn–Off Delay Time		$t_{d(off)}$	—	37	30	
Fall Time		t_f	—	84	96	
Gate Charge (See Figure 8)	(V_{DS} = 24 Vdc, I_D = 20 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	13.4	18.9	nC
		Q_1	—	3.0	—	
		Q_2	—	7.3	—	
		Q_3	—	6.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage ($C_{pk} \geq 2.0$) (3)	(I_S = 20 Adc, V_{GS} = 0 Vdc)	V_{SD}				Vdc
	(I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.95	1.1	
			—	0.87	—	
Reverse Recovery Time (See Figure 15)	(I_S = 20 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	33	—	ns
		t_a	—	23	—	
		t_b	—	10	—	
Reverse Recovery Stored Charge		Q_{RR}	—	33	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. C_{pk} = Absolute Value of Spec (Spec–AVG/3.516 μA).

TYPICAL ELECTRICAL CHARACTERISTICS

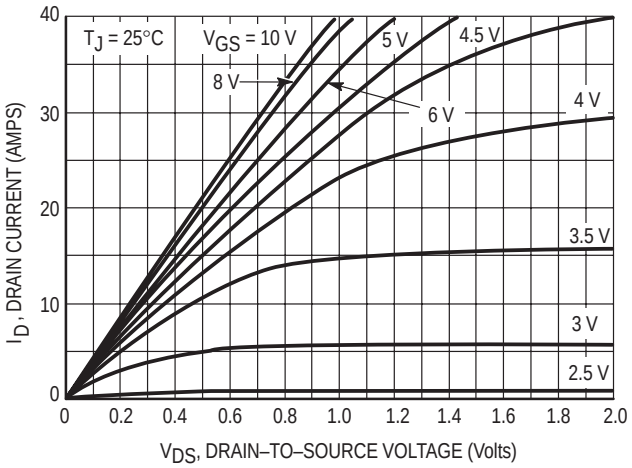


Figure 1. On–Region Characteristics

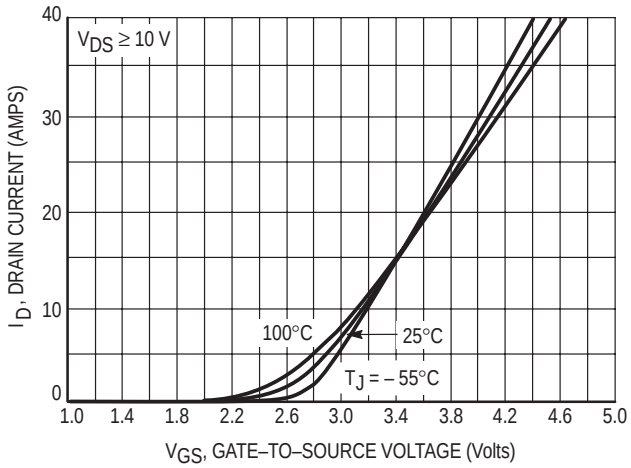


Figure 2. Transfer Characteristics

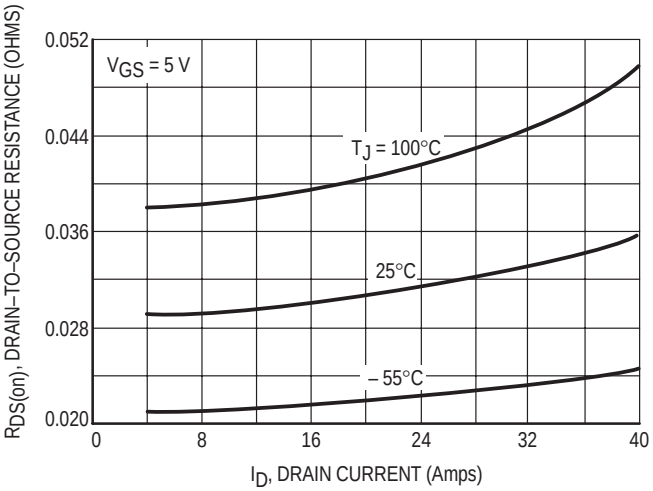


Figure 3. On–Resistance versus Drain Current and Temperature

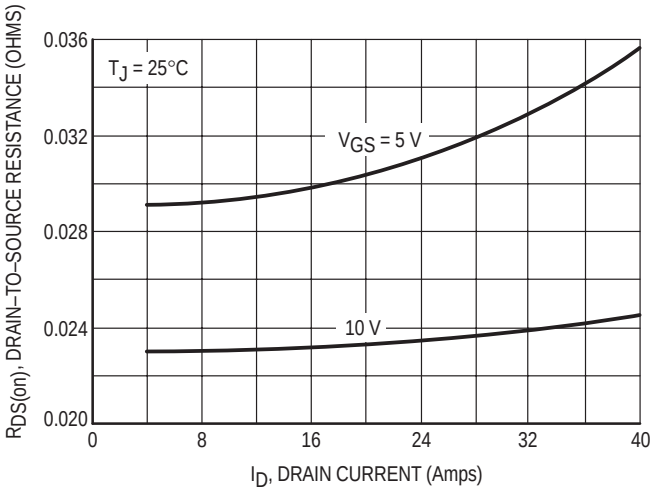


Figure 4. On–Resistance versus Drain Current and Gate Voltage

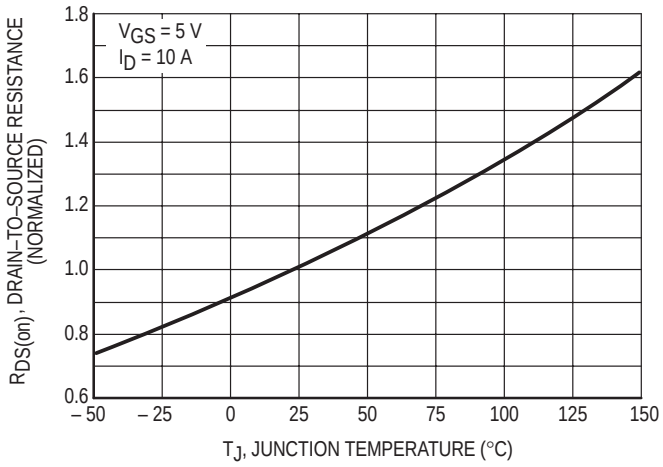


Figure 5. On–Resistance Variation with Temperature

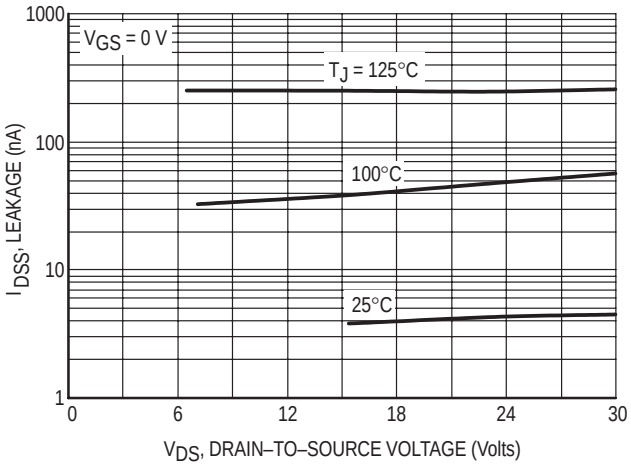


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

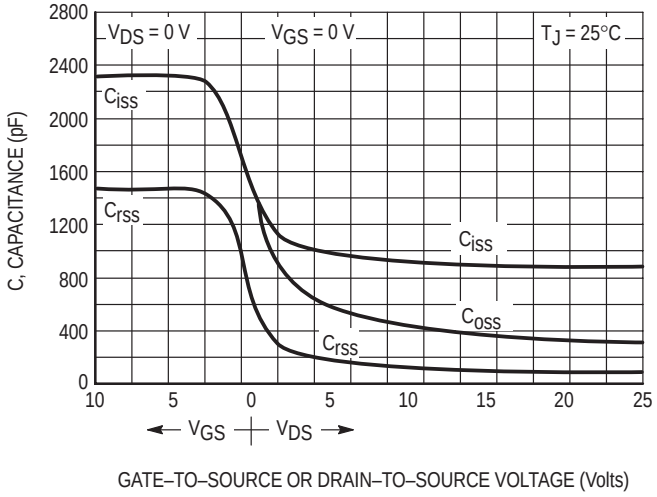


Figure 7. Capacitance Variation

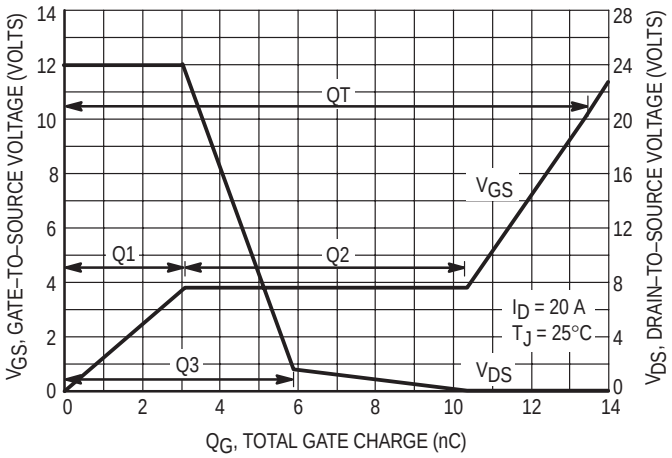


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

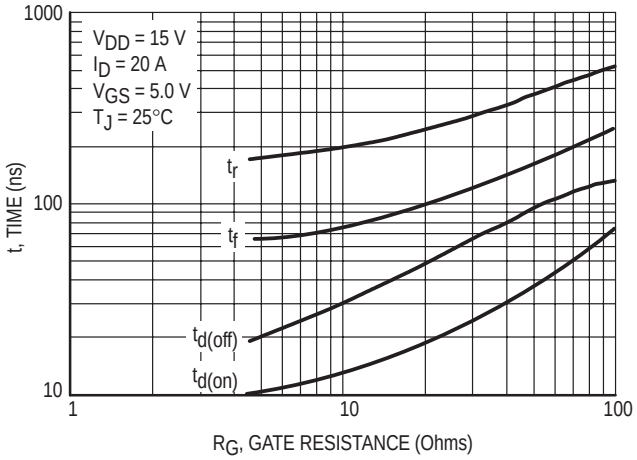


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

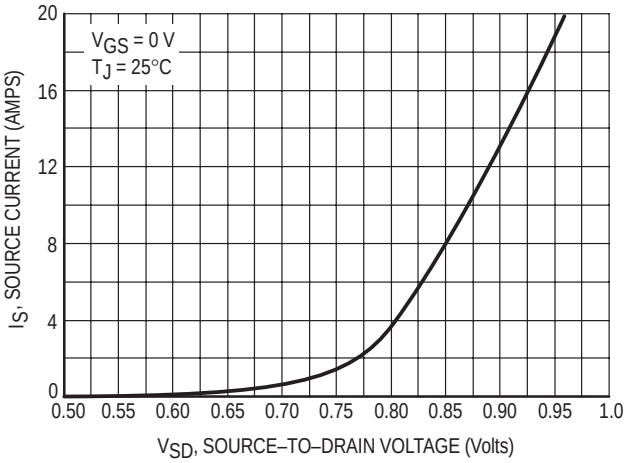


Figure 10. Diode Forward Voltage versus Current

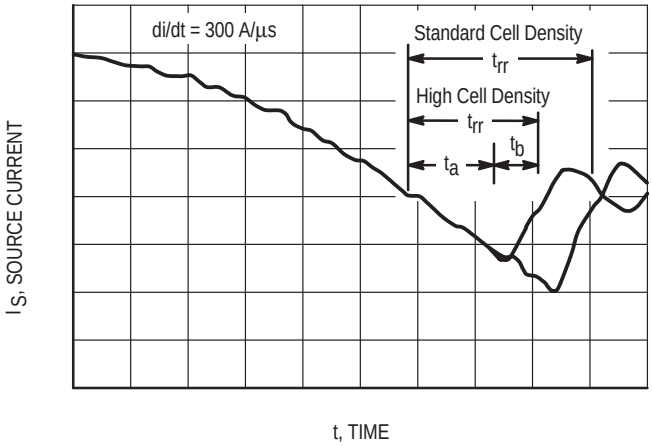


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

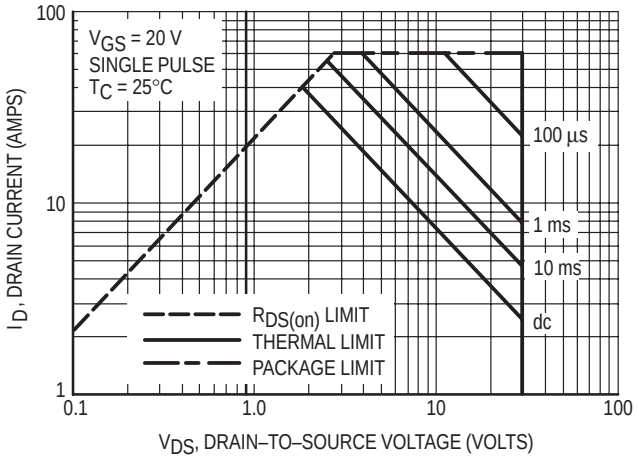


Figure 12. Maximum Rated Forward Biased Safe Operating Area

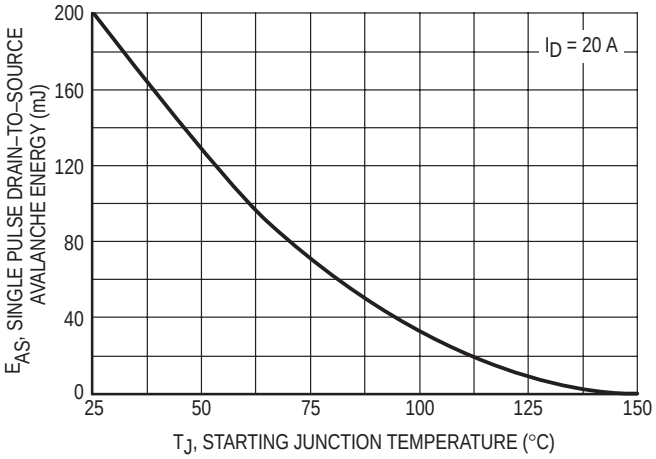


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

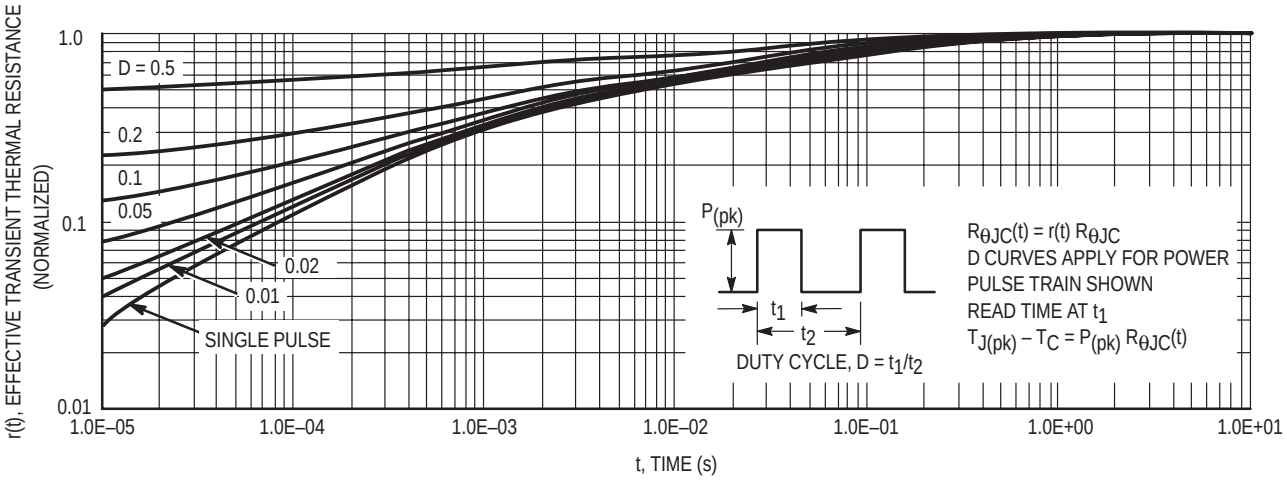


Figure 14. Thermal Response

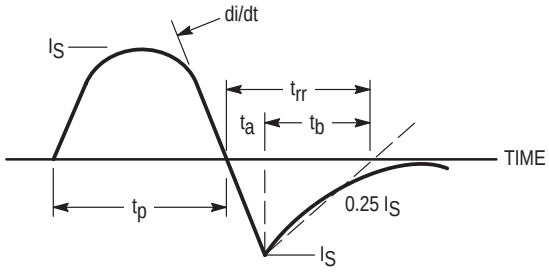


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

HDTMOS E-FET™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

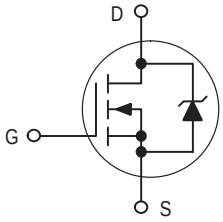
MTD20N06HD

Motorola Preferred Device

TMOS POWER FET
20 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.045 OHM

This advanced HDTMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 30	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	20 16 60	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 20 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	60	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage ($C_{pk} \geq 2.0$) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			60	—	—	
Temperature Coefficient (Positive)			—	54	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($C_{pk} \geq 2.0$) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			2.0	—	4.0	
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance ($C_{pk} \geq 2.0$) (3)		$R_{DS(on)}$				Ohm
(V_{GS} = 10 Vdc, I_D = 10 Adc)			—	0.035	0.045	
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 20 Adc)			—	—	1.2	
(I_D = 10 Adc, T_J = 125°C)			—	—	1.1	
Forward Transconductance (V_{DS} = 4.0 Vdc, I_D = 10 Adc)		g_{FS}	5.0	6.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	607	840	pF
Output Capacitance		C_{oss}	—	218	290	
Transfer Capacitance		C_{rss}	—	55	110	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	9.2	18	ns
Rise Time		t_r	—	61.2	122	
Turn–Off Delay Time		$t_{d(off)}$	—	19	38	
Fall Time		t_f	—	36	72	
Gate Charge (See Figure 7)	(V_{DS} = 48 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc)	Q_T	—	17	24	nC
		Q_1	—	3.4	—	
		Q_2	—	7.75	—	
		Q_3	—	7.46	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 20 Adc, V_{GS} = 0 Vdc)	V_{SD}		0.95	1.0	Vdc
($C_{pk} \geq 8.0$) (3)	(I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.88	—	
Reverse Recovery Time (See Figure 14)	(I_S = 20 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	35.7	—	ns
		t_a	—	24	—	
		t_b	—	11.7	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.055	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. C_{pk} = Absolute Value of Spec (Spec–AVG/3.516 μA).

TYPICAL ELECTRICAL CHARACTERISTICS

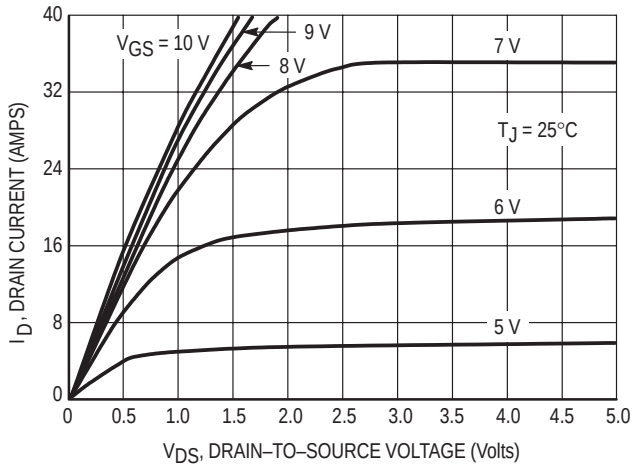


Figure 1. On–Region Characteristics

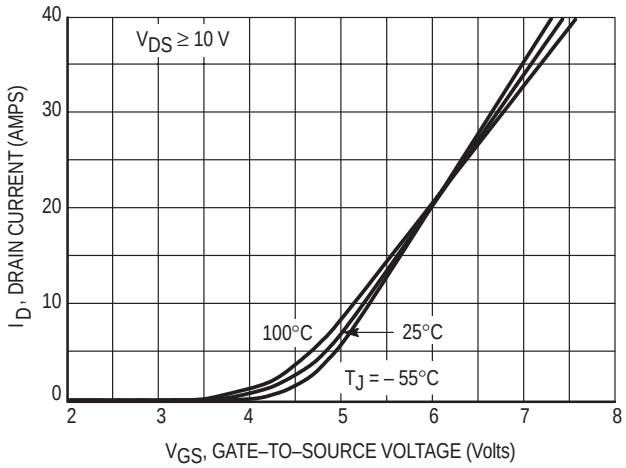


Figure 2. Transfer Characteristics

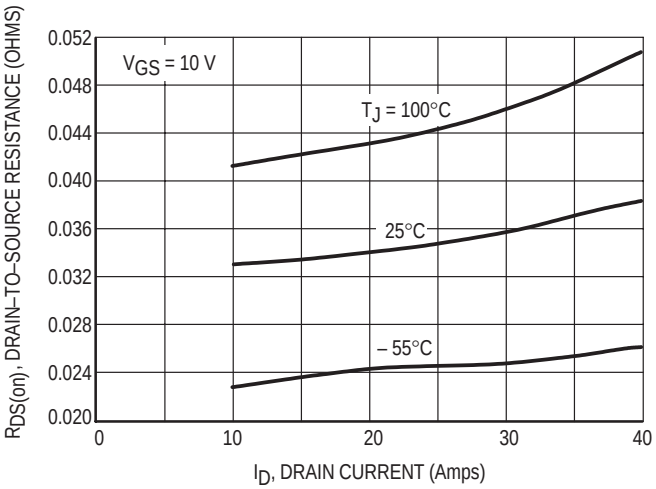


Figure 3. On–Resistance versus Drain Current and Temperature

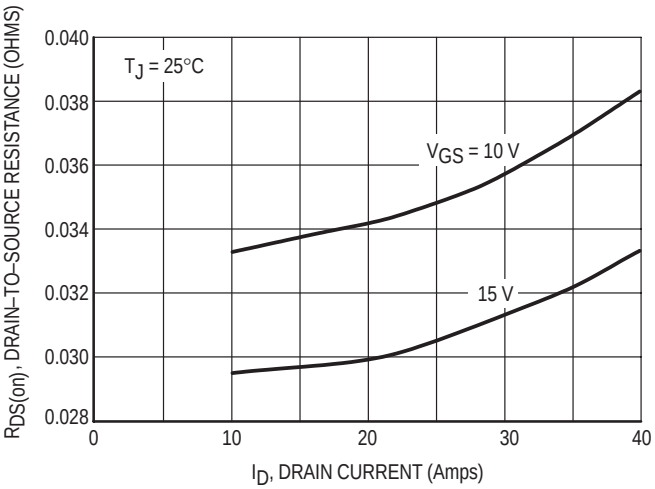


Figure 4. On–Resistance versus Drain Current and Gate Voltage

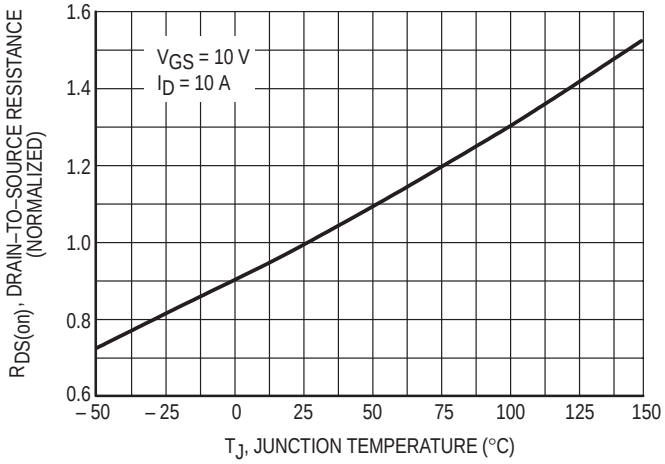


Figure 5. On–Resistance Variation with Temperature

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 8) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

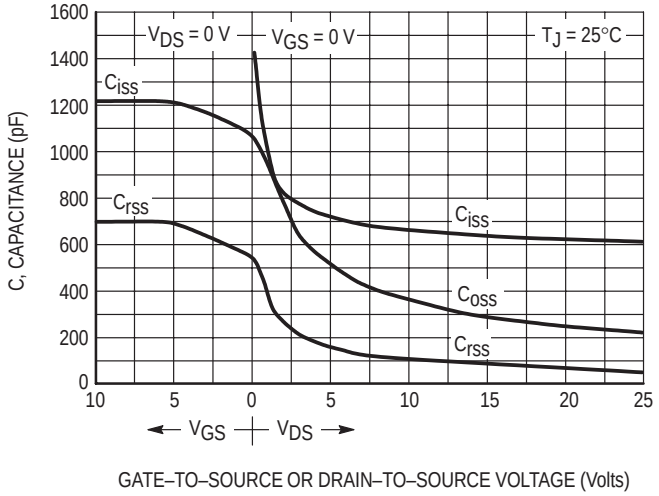


Figure 6. Capacitance Variation

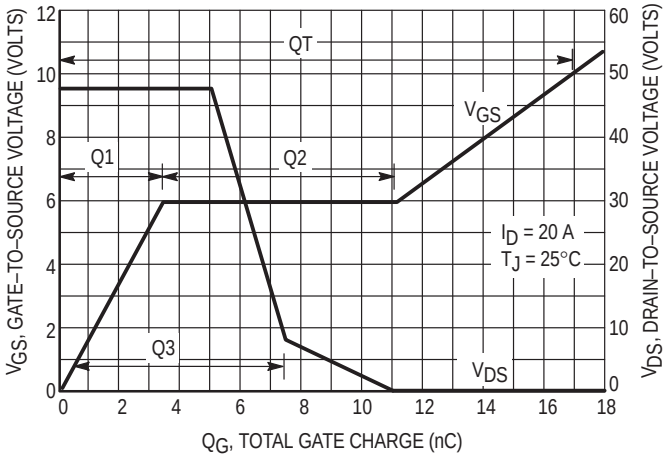


Figure 7. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

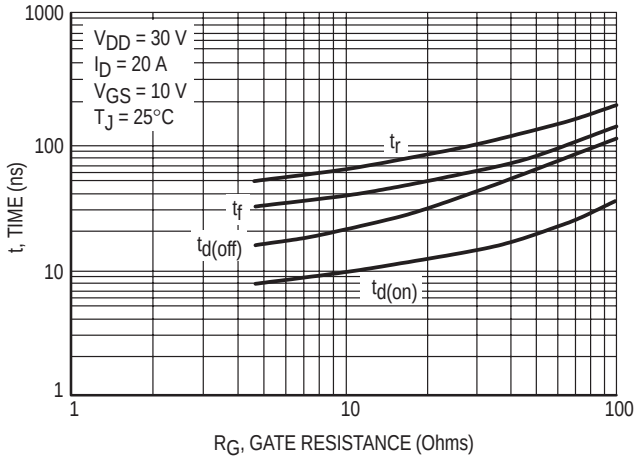


Figure 8. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 10. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

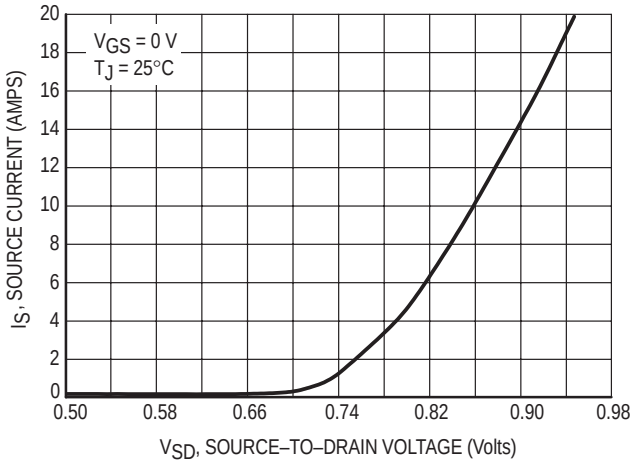


Figure 9. Diode Forward Voltage versus Current

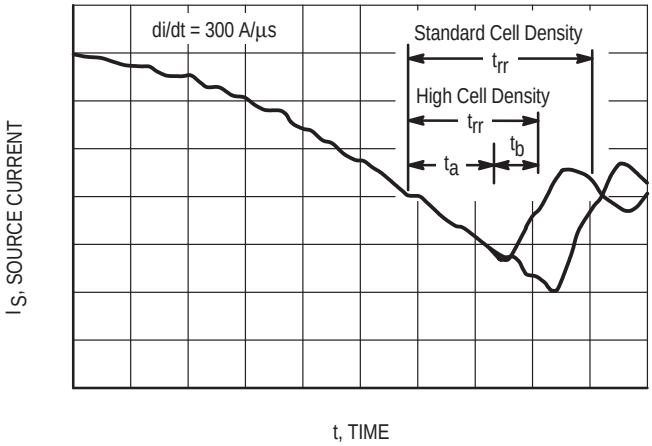


Figure 10. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

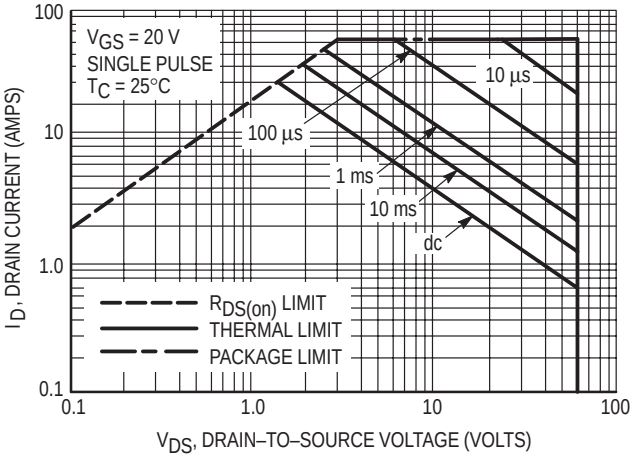


Figure 11. Maximum Rated Forward Biased Safe Operating Area

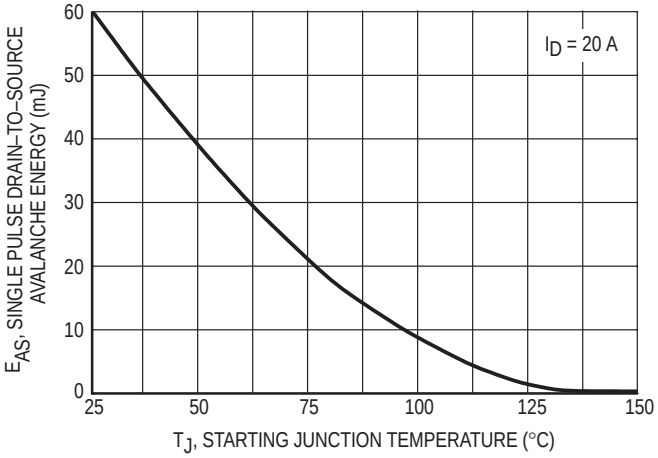


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

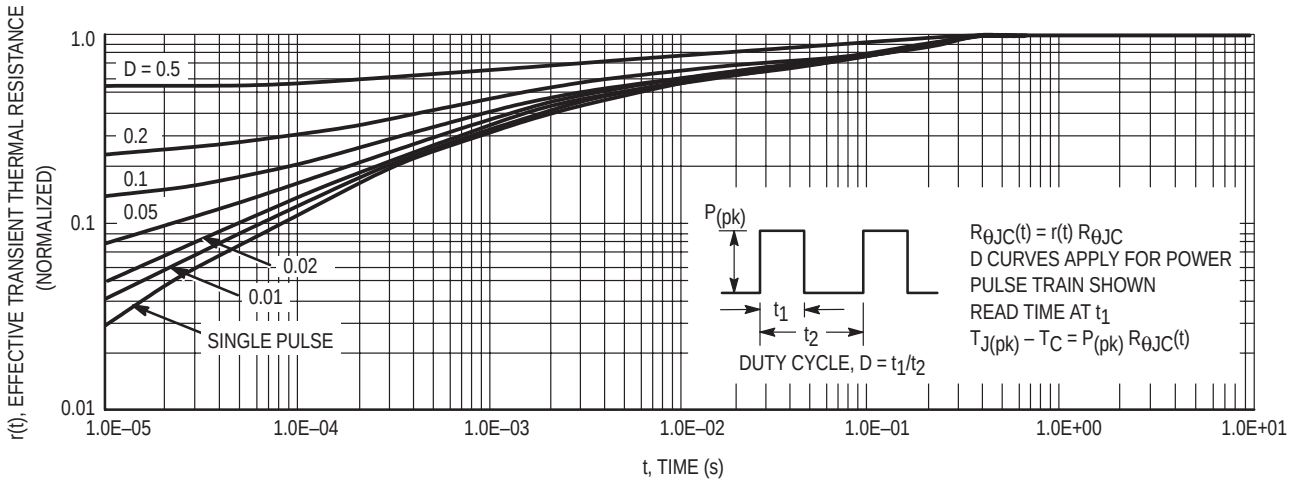


Figure 13. Thermal Response

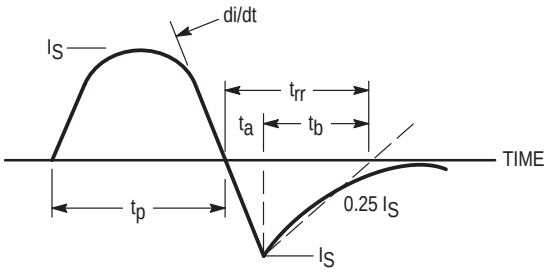


Figure 14. Diode Reverse Recovery Waveform

Advance Information

HDTMOS E-FET™ High Density Power FET DPAK for Surface Mount or Insertion Mount

N–Channel Enhancement–Mode Silicon Gate

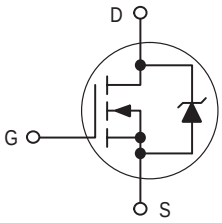
MTD20N06HDL

Motorola Preferred Device

TMOS POWER FET
LOGIC LEVEL
20 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.045 OHM

This advanced high–cell density HDTMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low–voltage, high–speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits, and inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched, and to offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number
- Available in Insertion Mount, Add –1 or 1 to Part Number



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 20	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	20 12 60	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_C = 25°C (1)	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 20 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	 200	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR–4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	25	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Threshold Temperature Coefficient (Negative)			—	6.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 4.0 Vdc, I_D = 10 Adc)		$R_{DS(on)}$	—	0.045	0.070	Ohm
(V_{GS} = 5.0 Vdc, I_D = 10 Adc)			—	0.037	0.045	
Drain–Source On–Voltage (V_{GS} = 5.0 Vdc) (I_D = 20 Adc)		$V_{DS(on)}$	—	0.76	1.2	Vdc
(I_D = 10 Adc, T_J = 125°C)			—	—	1.1	
Forward Transconductance (V_{DS} = 4.0 Vdc, I_D = 10 Adc)		g_{FS}	6.0	12	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	863	1232	pF
Output Capacitance		C_{oss}	—	216	300	
Reverse Transfer Capacitance		C_{rss}	—	53	73	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DS} = 30 Vdc, I_D = 20 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	11	15	ns
Rise Time		t_r	—	151	190	
Turn–Off Delay Time		$t_{d(off)}$	—	34	35	
Fall Time		t_f	—	75	98	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 20 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	14.6	22	nC
		Q_1	—	3.25	—	
		Q_2	—	7.75	—	
		Q_3	—	7.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 20 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.95	1.1	Vdc
	(I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.88	—	
Reverse Recovery Time	(I_S = 20 Adc, dI_S/dt = 100 A/μs)	t_{rr}	—	22	—	ns
		t_a	—	12	—	
		t_b	—	34	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.049	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

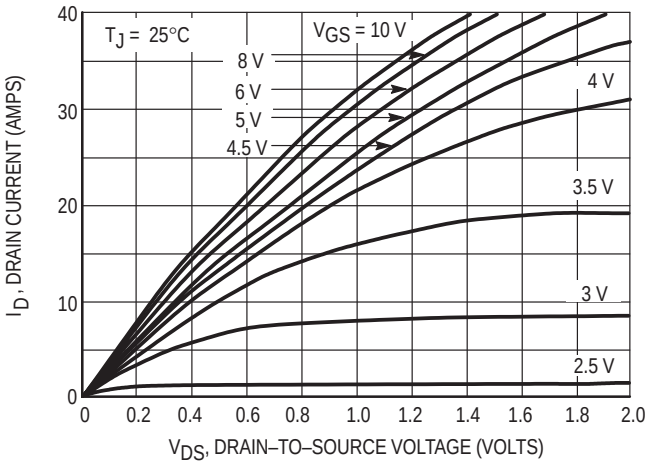


Figure 1. On–Region Characteristics

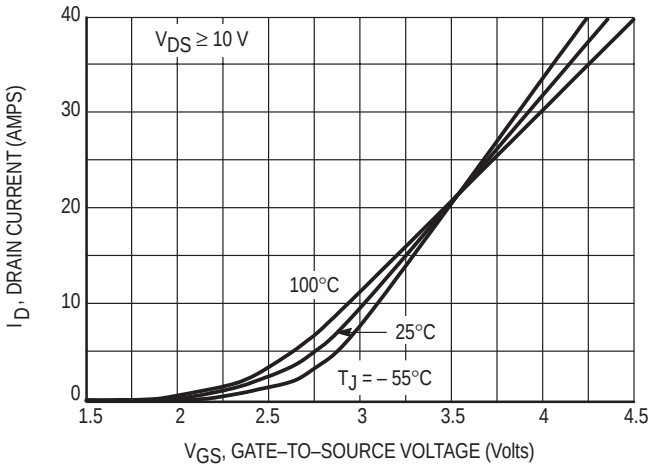


Figure 2. Transfer Characteristics

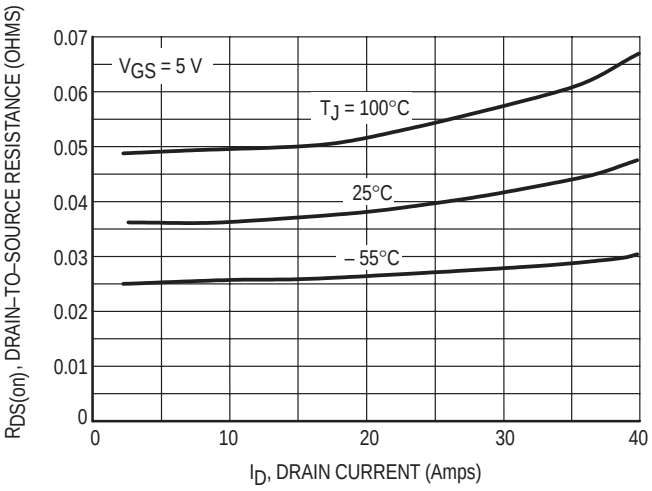


Figure 3. On–Resistance versus Drain Current and Temperature

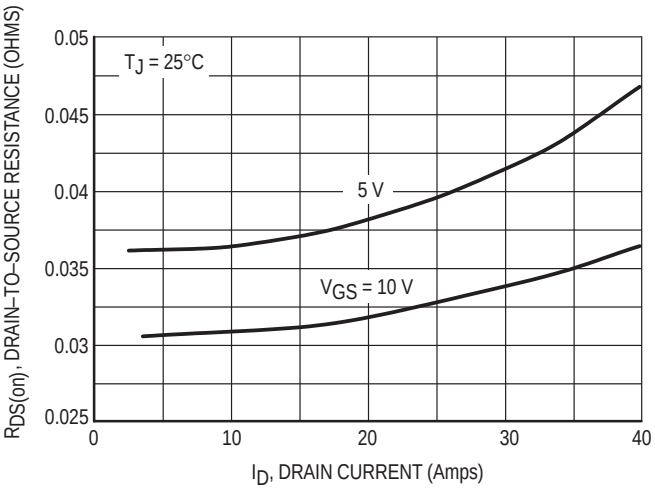


Figure 4. On–Resistance versus Drain Current and Gate Voltage

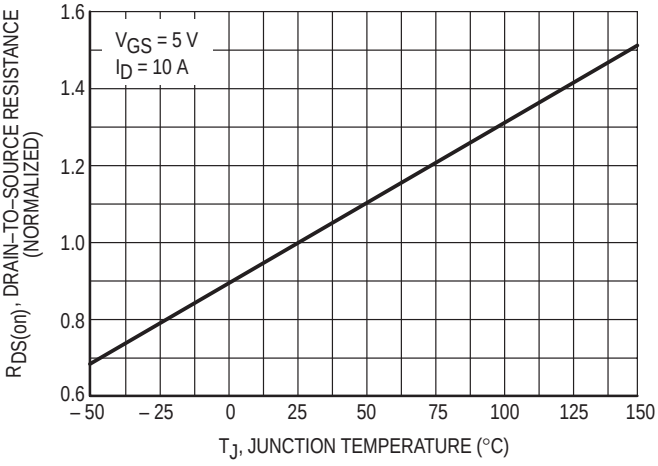


Figure 5. On–Resistance Variation with Temperature

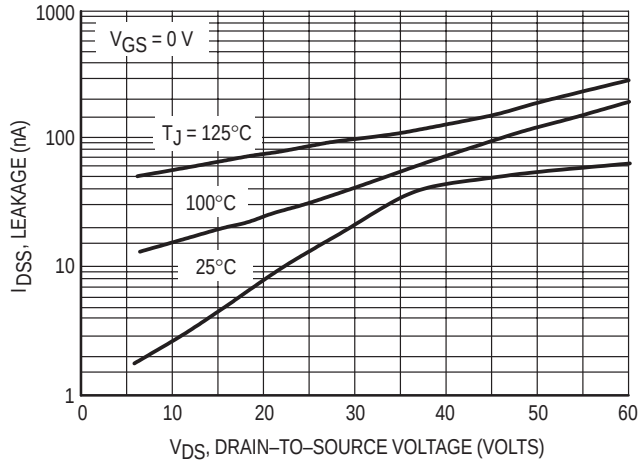


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 8) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

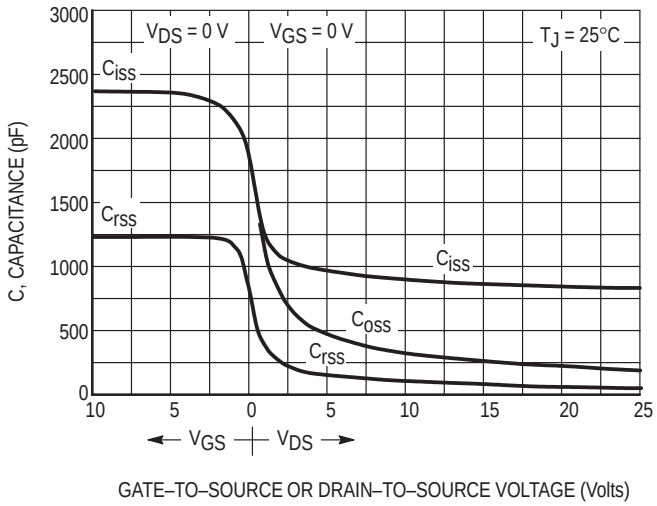


Figure 7. Capacitance Variation

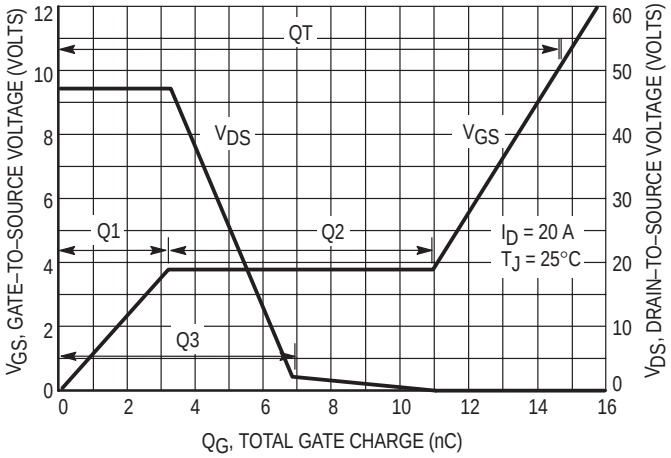


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

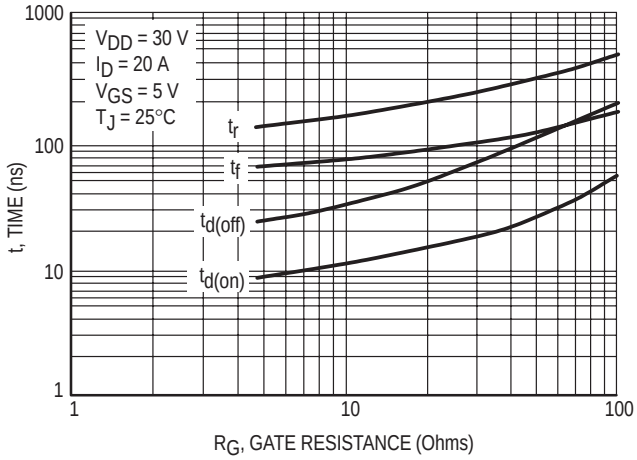


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 10. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

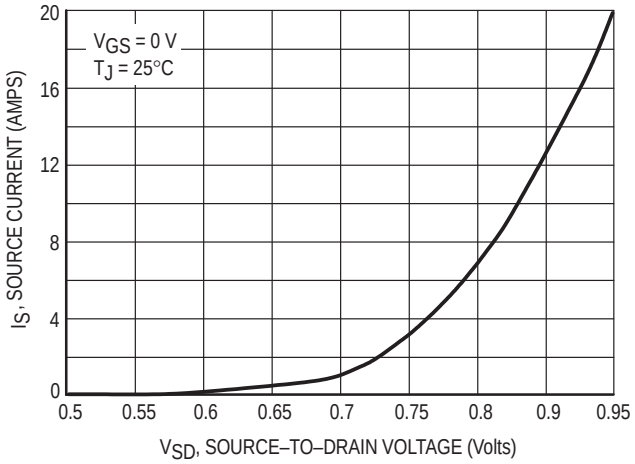


Figure 10. Diode Forward Voltage versus Current

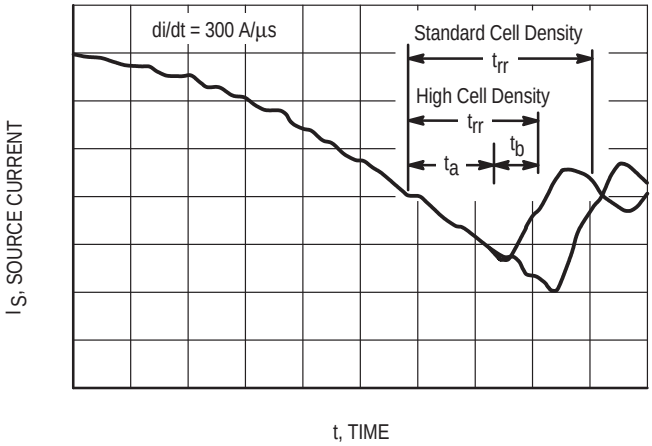


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

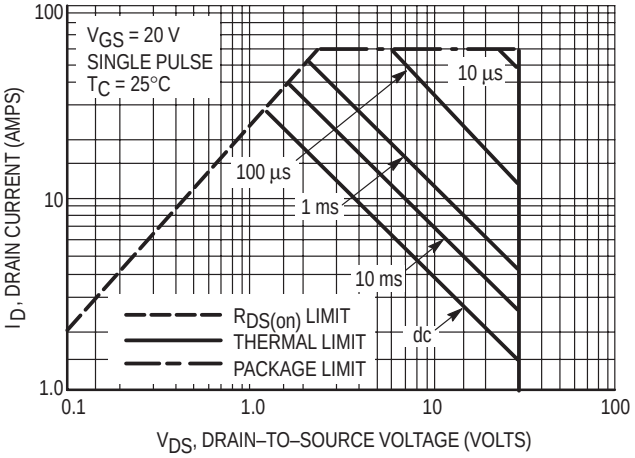


Figure 12. Maximum Rated Forward Biased Safe Operating Area

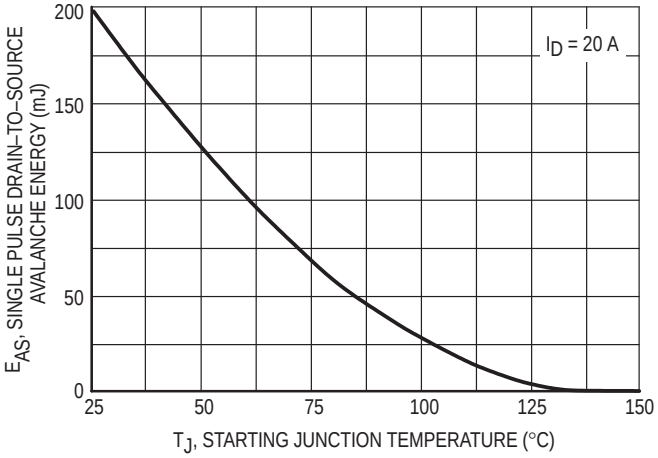


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

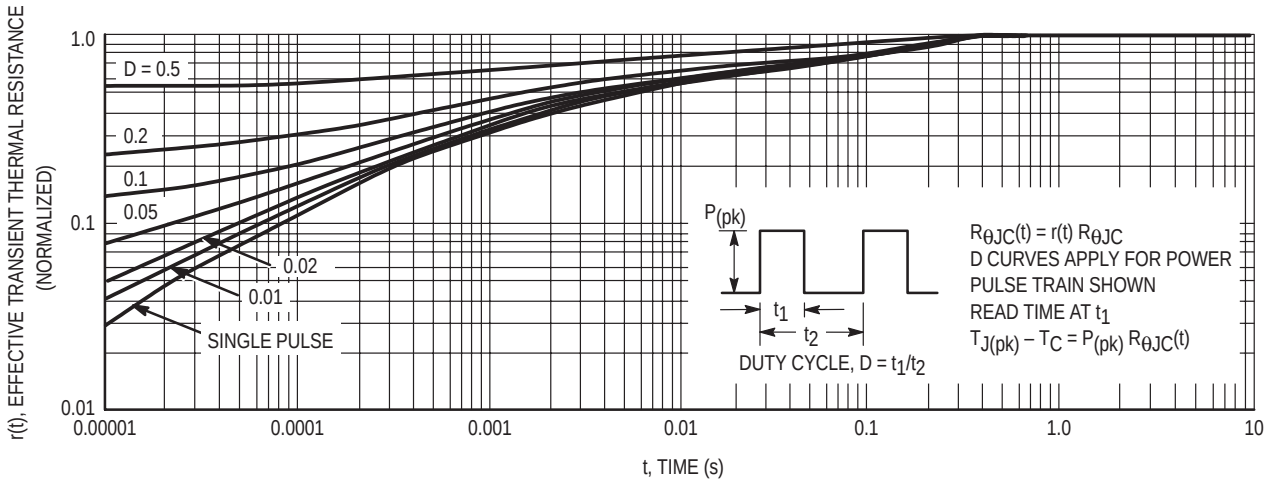


Figure 14. Thermal Response

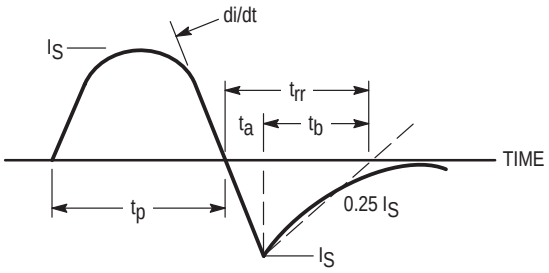


Figure 15. Diode Reverse Recovery Waveform

Product Preview

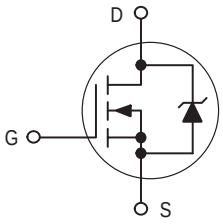
TMOS V™
Power Field Effect Transistor
DPAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

MTD20N06V

TMOS POWER FET
20 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.085 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.



CASE 369A–13, Style 2
DPAK Surface Mount

New Features of TMOS V

- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS

- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	20 13 70	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ 25°C(1)	P_D	60 0.4 2.1	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 20 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	200	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient(1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.5 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.8	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$R_{DS(on)}$	—	0.065	0.085	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 10 Adc)		$V_{DS(on)}$	—	—	2.0	Vdc
(V_{GS} = 10 Vdc, I_D = 10 Adc, T_J = 150°C)			—	—	1.9	
Forward Transconductance (V_{DS} = 6.0 Vdc, I_D = 10 Adc)		g_{FS}	6.0	8.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	590	830	pF
Output Capacitance		C_{oss}	—	180	250	
Reverse Transfer Capacitance		C_{rss}	—	40	80	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.7	20	ns
Rise Time		t_r	—	77	150	
Turn–Off Delay Time		$t_{d(off)}$	—	26	50	
Fall Time		t_f	—	46	90	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc)	Q_T	—	28	40	nC
		Q_1	—	4.0	—	
		Q_2	—	9.0	—	
		Q_3	—	8.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 20 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.6	Vdc
	(I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.96	—	
Reverse Recovery Time	(I_S = 20 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	60	—	ns
		t_a	—	52	—	
		t_b	—	8.0	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.172	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

Designer's™ Data Sheet

HDTMOS E-FET ™
High Density Power FET
DPAK for Surface Mount

P–Channel Enhancement–Mode Silicon Gate

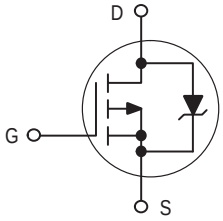
MTD20P03HDL

Motorola Preferred Device

TMOS POWER FET
LOGIC LEVEL
19 AMPERES
30 VOLTS
$R_{DS(on)}$ = 0.099 OHM

This advanced HDTMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	30	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±15 ± 20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	19 12 57	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_C = 25°C, when mounted with the minimum recommended pad size	P_D	75 0.6 1.75	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 19 Apk, L = 1.1 mH, R_G = 25 Ω)	E_{AS}	200	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.67 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage ($C_{pk} \geq 2.0$) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			30	—	—	
Temperature Coefficient (Positive)			—	15	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 30 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current		I_{GSS}				nAdc
(V_{GS} = ±15 Vdc, V_{DS} = 0 Vdc)			—	—	100	
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($C_{pk} \geq 2.0$) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			1.0	1.5	2.0	
Threshold Temperature Coefficient (Negative)			—	4.0	—	mV/°C
Static Drain–to–Source On–Resistance ($C_{pk} \geq 2.0$) (3)		$R_{DS(on)}$				mΩ
(V_{GS} = 4.0 Vdc, I_D = 10 Adc)			—	120	—	
(V_{GS} = 5.0 Vdc, I_D = 9.5 Adc)				90	99	
Drain–to–Source On–Voltage (V_{GS} = 5.0 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 19 Adc)			—	0.94	2.2	
(I_D = 9.5 Adc, T_J = 125°C)			—	—	1.9	
Forward Transconductance		g_{FS}				mhos
(V_{DS} = 8.0 Vdc, I_D = 9.5 Adc)			5.0	6.0	—	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	770	1064	pF
Output Capacitance		C_{oss}	—	360	504	
Transfer Capacitance		C_{rss}	—	130	182	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 19 Adc, V_{GS} = 5.0 Vdc, R_G = 1.3 Ω)	$t_{d(on)}$	—	18	25.2	ns
Rise Time		t_r	—	178	246.4	
Turn–Off Delay Time		$t_{d(off)}$	—	21	26.6	
Fall Time		t_f	—	72	98	
Gate Charge (See Figure 8)	(V_{DS} = 24 Vdc, I_D =19 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	15	22.4	nC
		Q_1	—	3.0	—	
		Q_2	—	11	—	
		Q_3	—	8.2	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage ($C_{pk} \geq 2.0$) (3)	(I_S = 19 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	3.1	3.4	Vdc
	(I_S = 19 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	2.56	—	
Reverse Recovery Time (See Figure 15)	(I_S = 19 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	78	—	ns
		t_a	—	50	—	
		t_b	—	28	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.209	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. C_{pk} = Absolute Value of Spec (Spec–AVG/3.516 μA).

TYPICAL ELECTRICAL CHARACTERISTICS

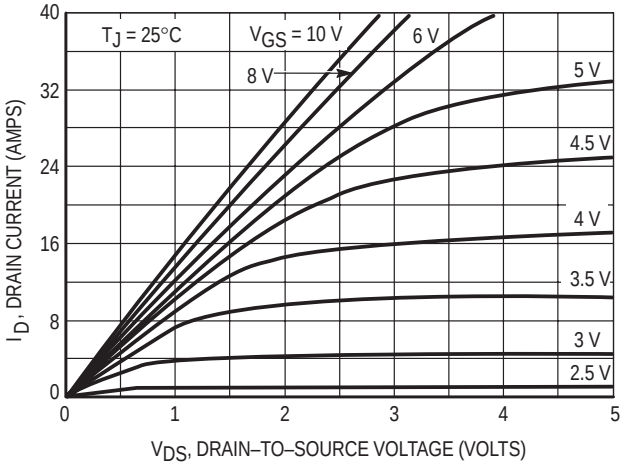


Figure 1. On–Region Characteristics

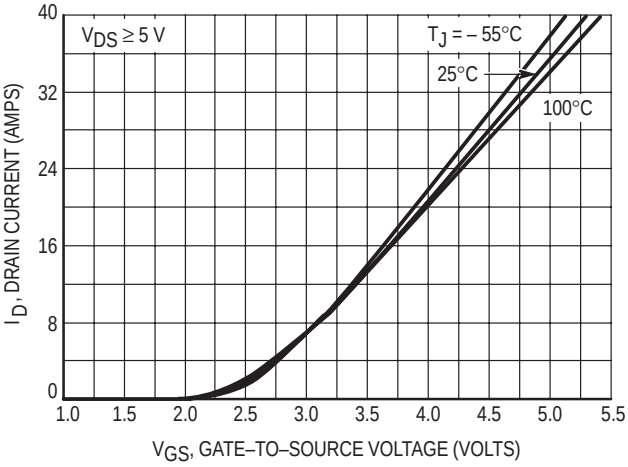


Figure 2. Transfer Characteristics

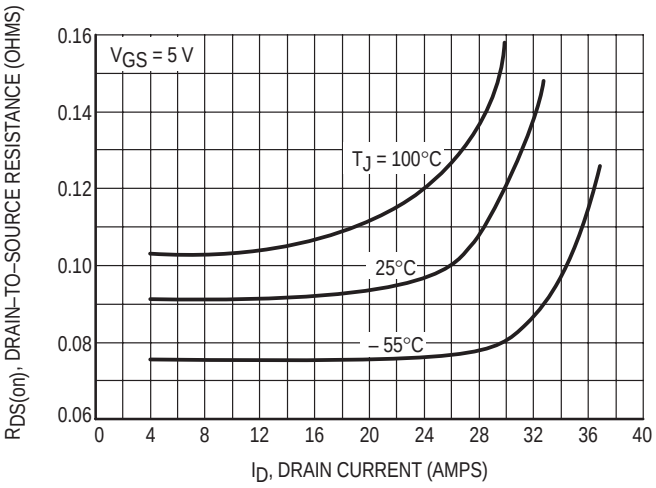


Figure 3. On–Resistance versus Drain Current and Temperature

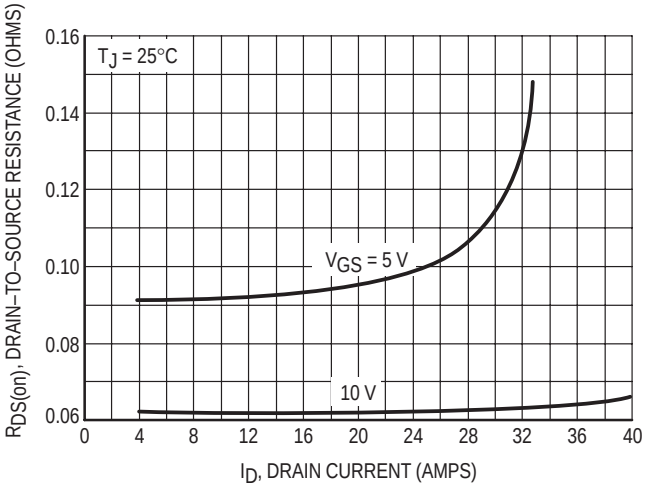


Figure 4. On–Resistance versus Drain Current and Gate Voltage

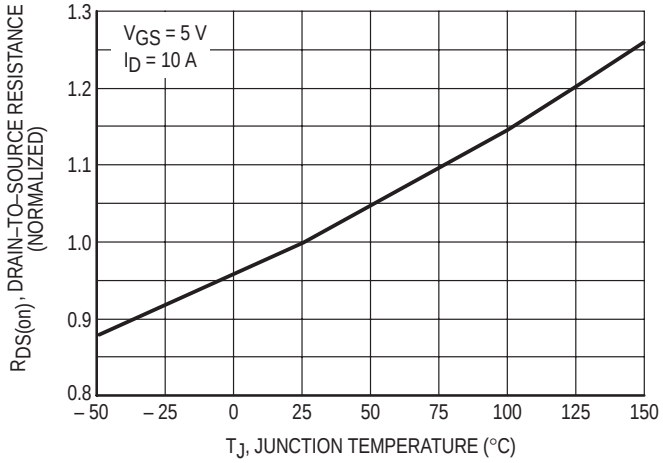


Figure 5. On–Resistance Variation with Temperature

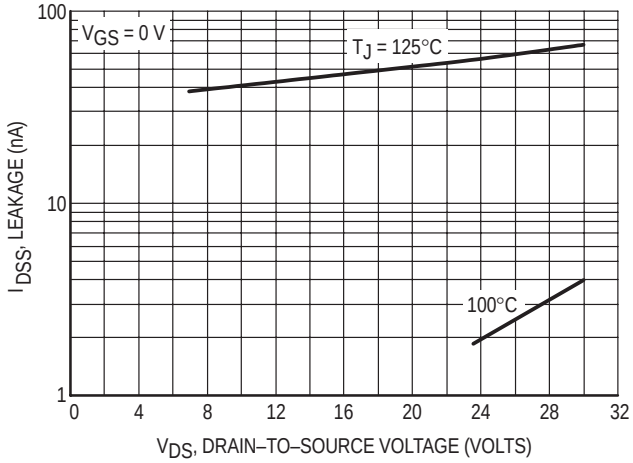


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

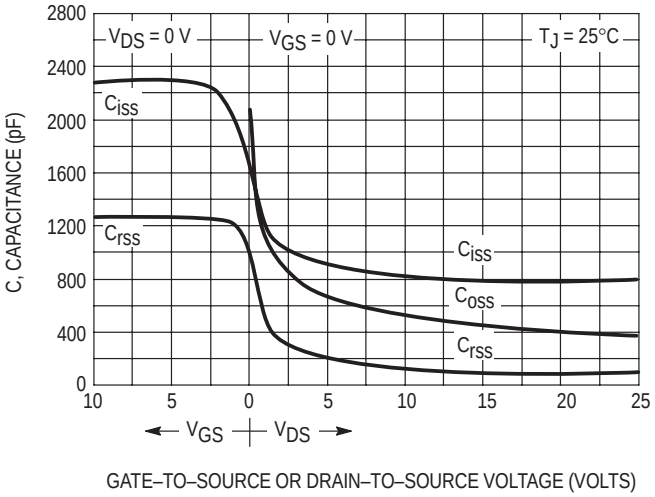


Figure 7. Capacitance Variation

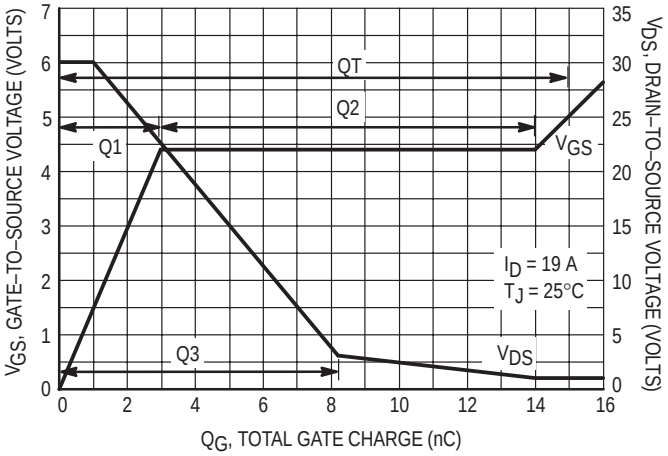


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

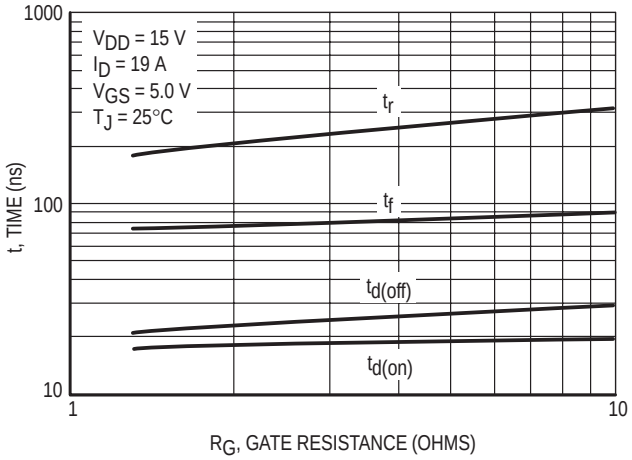


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

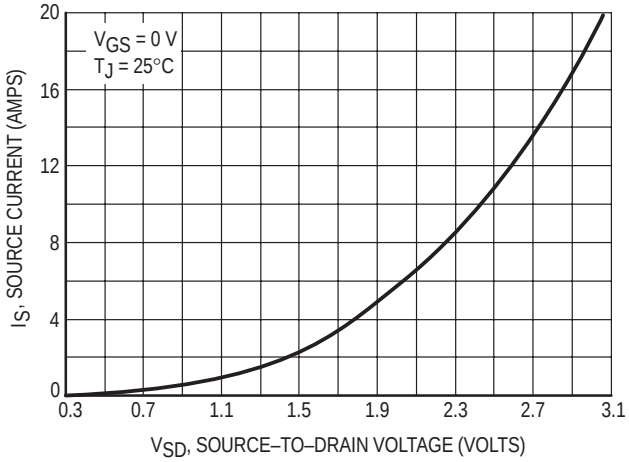


Figure 10. Diode Forward Voltage versus Current

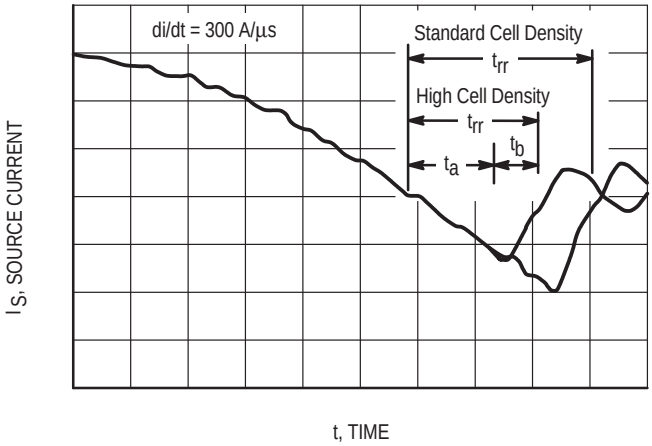


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

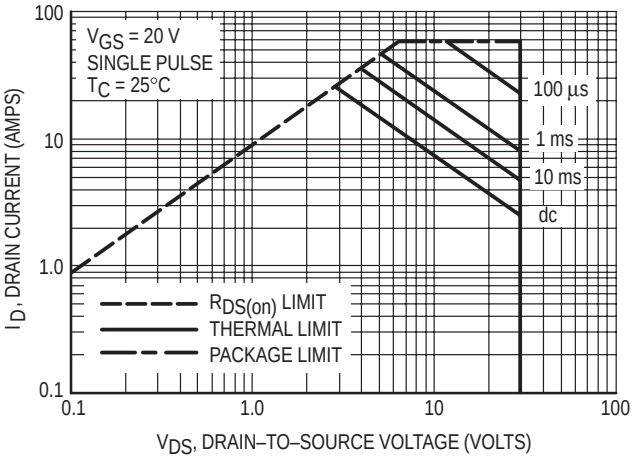


Figure 12. Maximum Rated Forward Biased Safe Operating Area

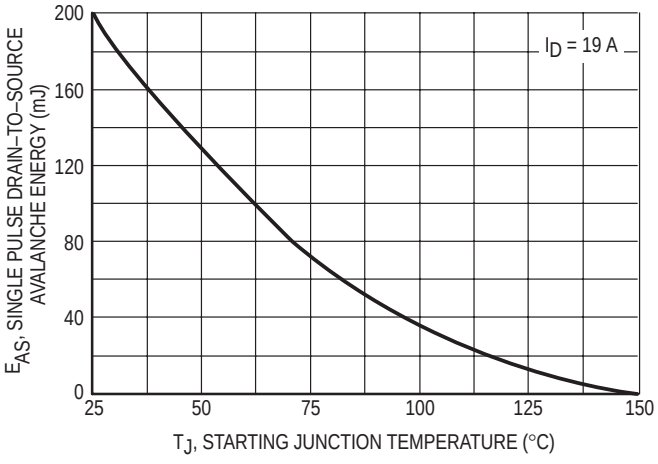


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

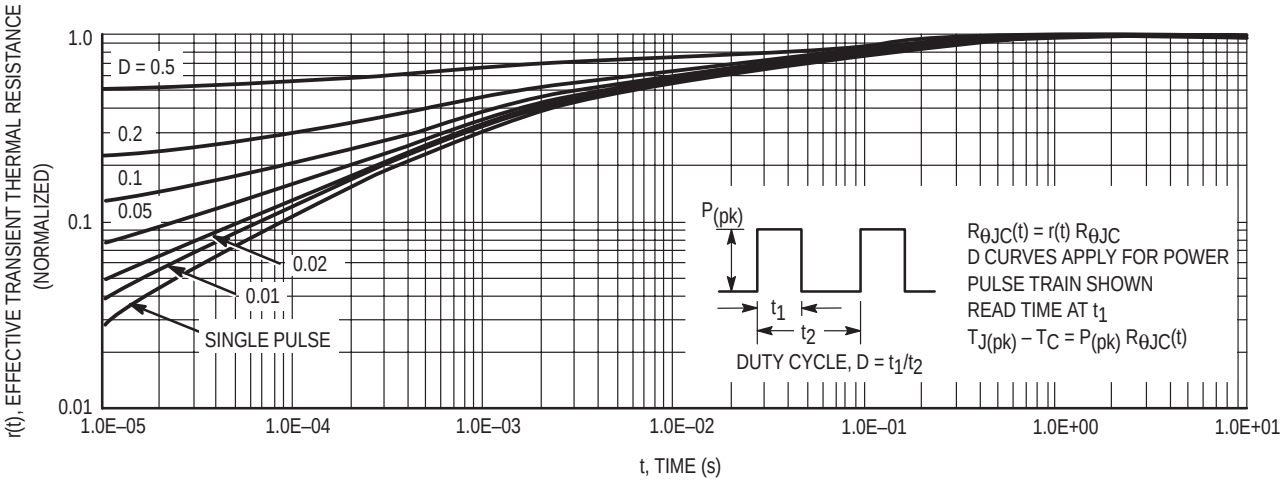


Figure 14. Thermal Response

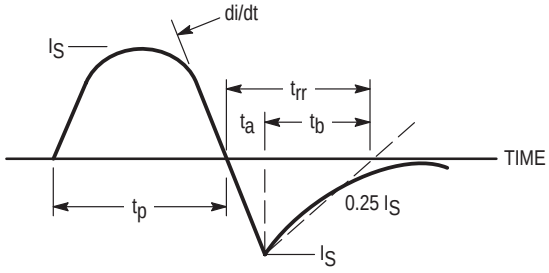


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

HDTMOS E-FET™
High Density Power FET
DPAK for Surface Mount

P–Channel Enhancement–Mode Silicon Gate

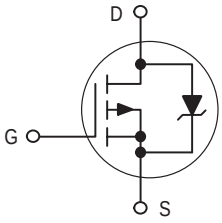
MTD20P06HDL

Motorola Preferred Device

TMOS POWER FET
LOGIC LEVEL
15 AMPERES
60 VOLTS
$R_{DS(on)}$ = 175 MΩ

This advanced high–cell density HDTMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low–voltage, high–speed switching applications in power supplies, converters and PWM motor controls, and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched, and to offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$, High–Cell Density, HDTMOS
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Surface Mount Package Available in 16 mm, 13–inch/2500 Unit, Tape & Reel, Add T4 Suffix to Part Number



CASE 369A–13, Style 2
DPAK

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	15 9.0 45	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_C = 25°C (1)	P_D	72 0.58 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 15 Apk, L = 2.7 mH, R_G = 25 Ω)	E_{AS}	300	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.73 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	81.3	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	1.0	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	10	
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.7	2.0	Vdc
Temperature Coefficient (Negative)			—	3.9	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 7.5 Adc)		$R_{DS(on)}$	—	143	175	mΩ
Drain–Source On–Voltage (V_{GS} = 5.0 Vdc) (I_D = 15 Adc)		$V_{DS(on)}$	—	2.3	3.0	Vdc
(I_D = 7.5 Adc, T_J = 125°C)			—	1.6	2.0	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 7.5 Adc)		g_{FS}	9.0	11	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	850	1190	pF
Output Capacitance		C_{oss}	—	210	290	
Reverse Transfer Capacitance		C_{rss}	—	66	130	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DS} = 30 Vdc, I_D = 15 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	19	38	ns
Rise Time		t_r	—	175	350	
Turn–Off Delay Time		$t_{d(off)}$	—	41	82	
Fall Time		t_f	—	68	136	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 15 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	20.6	29	nC
		Q_1	—	3.7	—	
		Q_2	—	7.6	—	
		Q_3	—	8.4	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 15 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	2.5	3.0	Vdc
	(I_S = 15 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.9	—	
Reverse Recovery Time	(I_S = 15 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	64	—	ns
		t_a	—	50	—	
		t_b	—	14	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.177	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

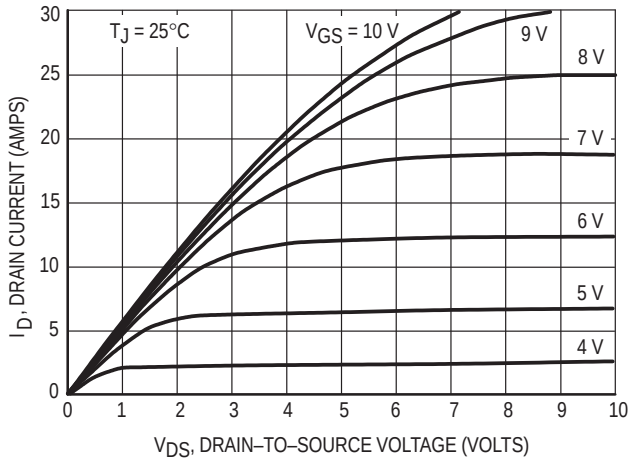


Figure 1. On–Region Characteristics

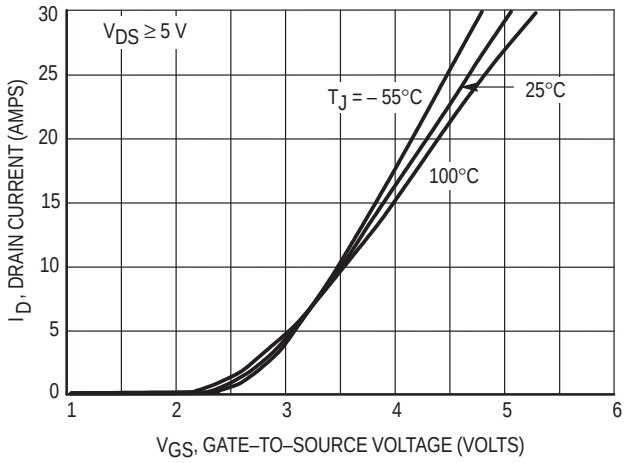


Figure 2. Transfer Characteristics

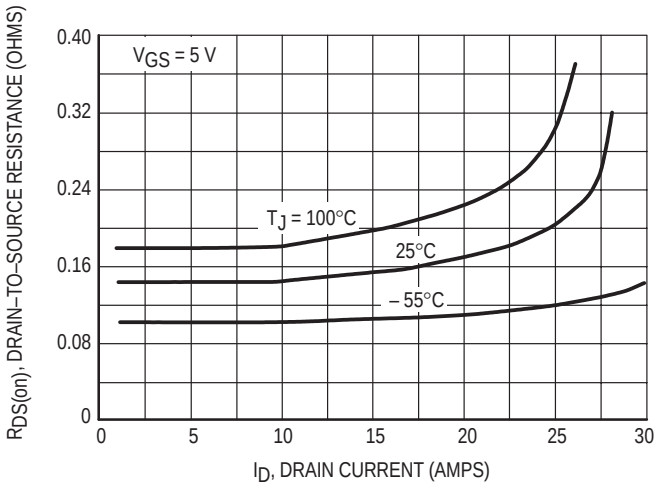


Figure 3. On–Resistance versus Drain Current and Temperature

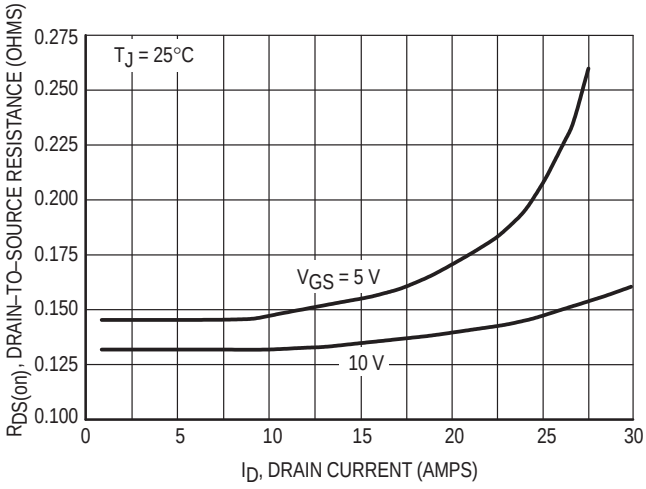


Figure 4. On–Resistance versus Drain Current and Gate Voltage

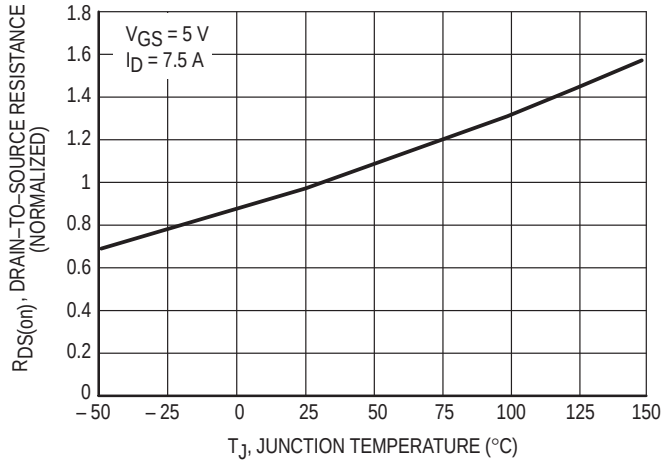


Figure 5. On–Resistance Variation with Temperature

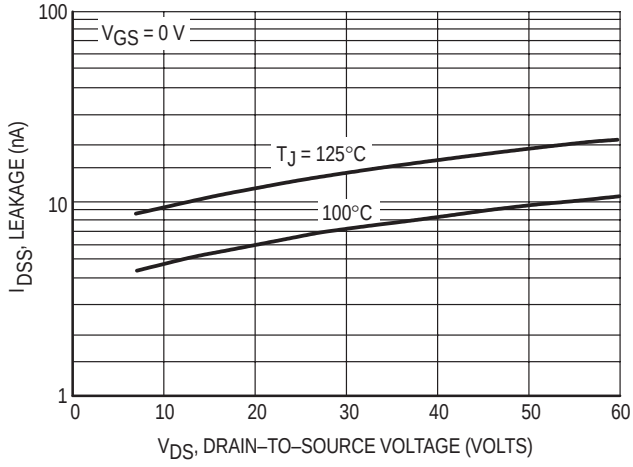


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

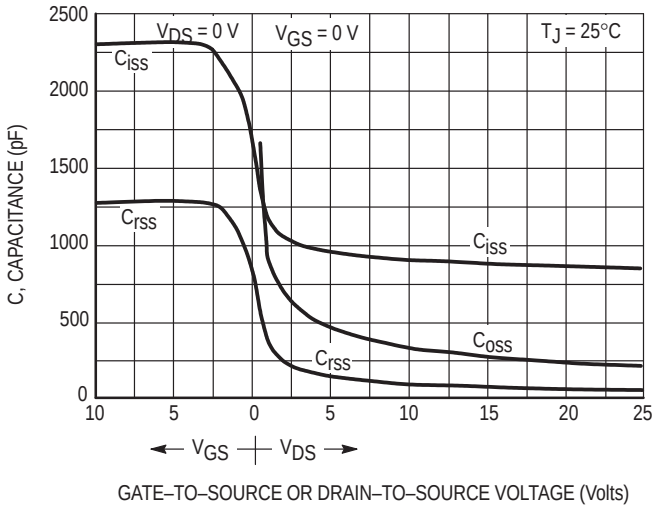


Figure 7. Capacitance Variation

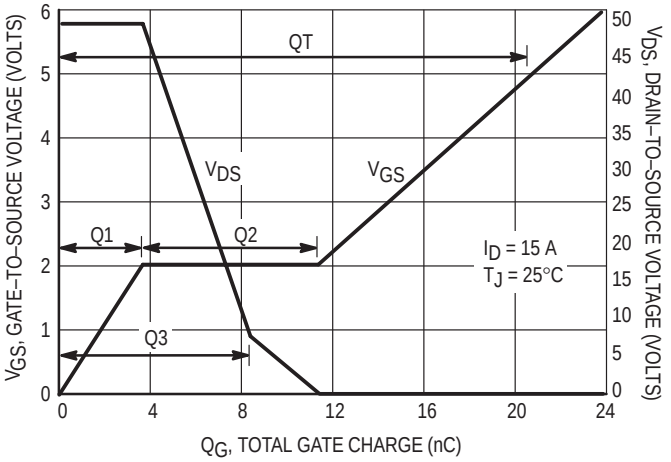


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

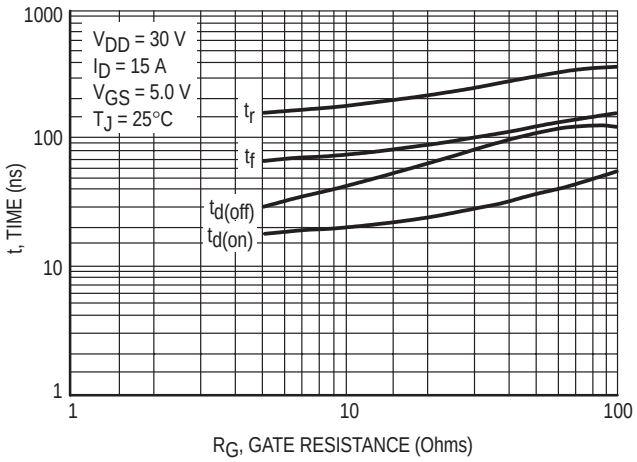


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

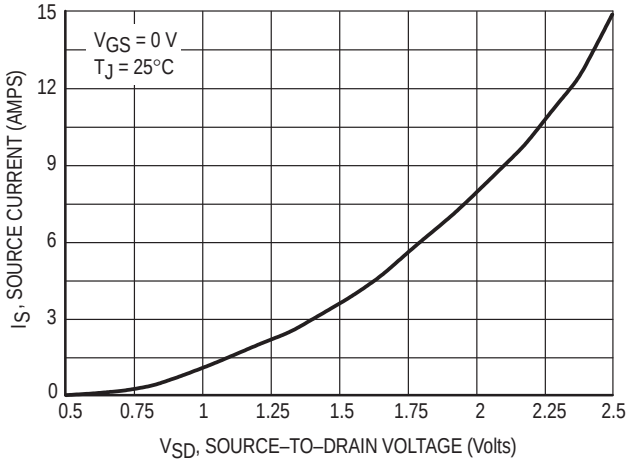


Figure 10. Diode Forward Voltage versus Current

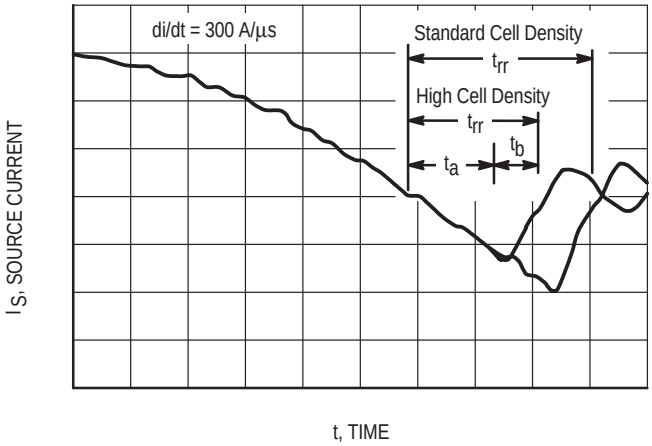


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

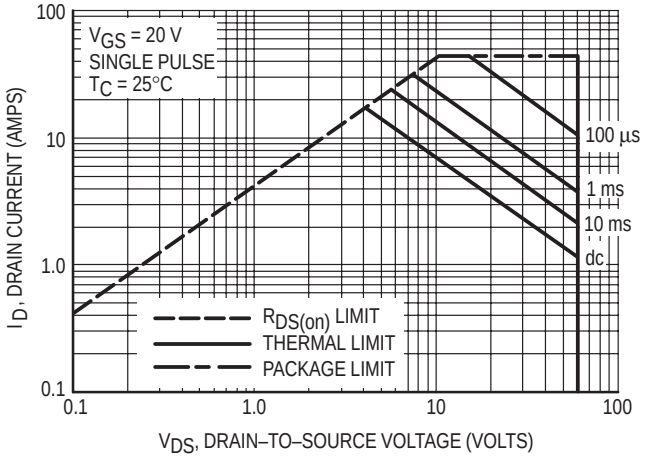


Figure 12. Maximum Rated Forward Biased Safe Operating Area

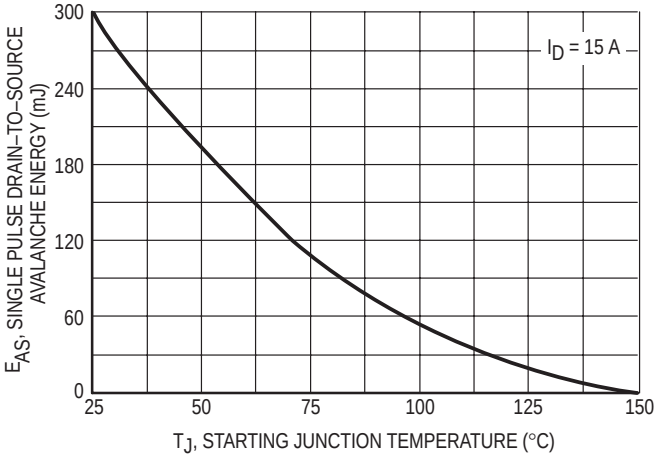


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

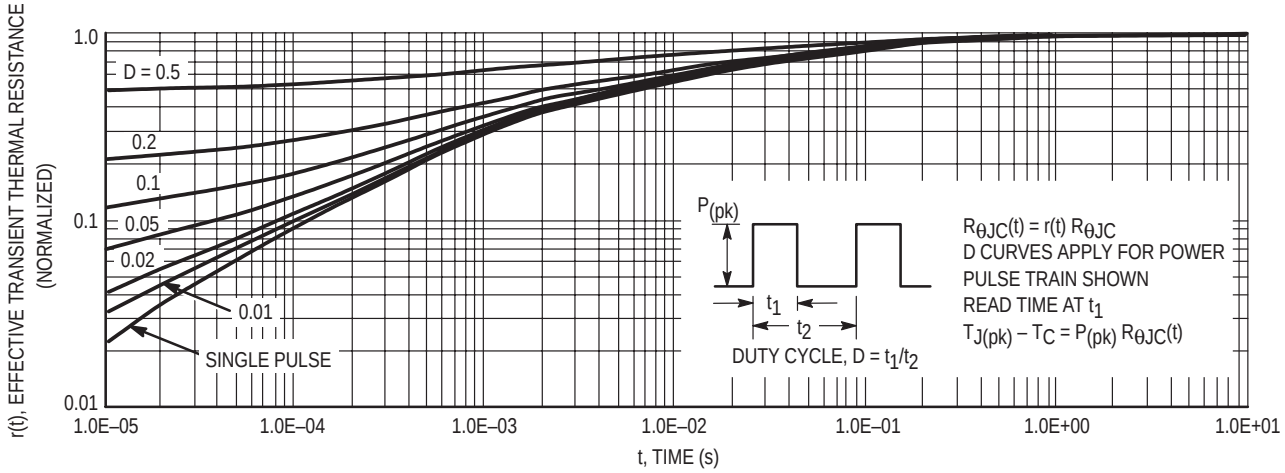


Figure 14. Thermal Response

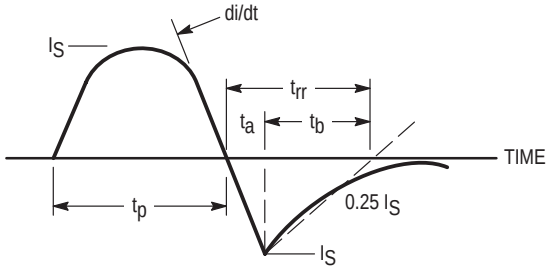


Figure 15. Diode Reverse Recovery Waveform

Product Preview

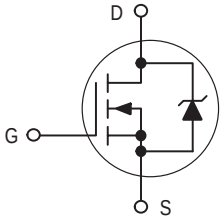
TMOS V™
Power Field Effect Transistor
DPAK for Surface Mount

P–Channel Enhancement–Mode Silicon Gate

MTD2955V

TMOS POWER FET
12 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.200 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.



CASE 369A–13, Style 2
DPAK Surface Mount

New Features of TMOS V

- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS

- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 25	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	12 8.0 42	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ 25°C(1)	P_D	60 0.4 2.1	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 12 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	216	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient(1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.5 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.8	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	—	0.185	0.200	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 12 Adc)		$V_{DS(on)}$	—	—	2.9	Vdc
(V_{GS} = 10 Vdc, I_D = 6.0 Adc, T_J = 150°C)			—	—	2.8	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 6.0 Adc)		g_{FS}	3.0	5.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	500	700	pF
Output Capacitance		C_{oss}	—	200	280	
Reverse Transfer Capacitance		C_{rss}	—	40	80	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 12 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	11	20	ns
Rise Time		t_r	—	38	80	
Turn–Off Delay Time		$t_{d(off)}$	—	18	40	
Fall Time		t_f	—	26	50	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 12 Adc, V_{GS} = 10 Vdc)	Q_T	—	15	20	nC
		Q_1	—	4.0	—	
		Q_2	—	7.0	—	
		Q_3	—	6.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 12 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.8	3.0	Vdc
	(I_S = 12 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	TBD	—	
Reverse Recovery Time	(I_S = 12 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	114	—	ns
		t_a	—	86	—	
		t_b	—	28	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.553	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

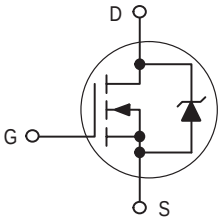
Designer's™ Data Sheet

TMOS V
Power Field Effect Transistor
DPAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

MTD3055V

Motorola Preferred Device

TMOS POWER FET
12 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.15 OHM



CASE 369A–13, Style 2
DPAK

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

New Features of TMOS V
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- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage – Continuous – Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current – Continuous @ 25°C – Continuous @ 100°C – Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	12 7.3 37	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	48 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 12 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	72	mJ
Thermal Resistance – Junction to Case – Junction to Ambient – Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

E–FET, Designer's and TMOS V are trademarks of Motorola, Inc. TMOS is a registered trademark of Motorola, Inc.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	60 –	– 65	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	– –	– –	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	–	–	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 –	2.7 5.4	4.0 –	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	–	0.10	0.15	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 12 Adc) (I_D = 6.0 Adc, T_J = 150°C)		$V_{DS(on)}$	– –	1.3 –	2.2 1.9	Vdc
Forward Transconductance (V_{DS} = 7.0 Vdc, I_D = 6.0 Adc)		g_{FS}	4.0	5.0	–	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	410	500	pF
Output Capacitance		C_{oss}	–	130	180	
Reverse Transfer Capacitance		C_{rss}	–	25	50	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 12 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	–	7.0	10	ns
Rise Time		t_r	–	34	60	
Turn–Off Delay Time		$t_{d(off)}$	–	17	30	
Fall Time		t_f	–	18	50	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 12 Adc, V_{GS} = 10 Vdc)	Q_T	–	12.2	17	nC
		Q_1	–	3.2	–	
		Q_2	–	5.2	–	
		Q_3	–	5.5	–	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 12 Adc, V_{GS} = 0 Vdc) (I_S = 12 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	– –	1.0 0.91	1.6 –	Vdc
Reverse Recovery Time (See Figure 15)	(I_S = 12 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	–	56	–	ns
		t_a	–	40	–	
		t_b	–	16	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.128	–	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	–	4.5	–	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	–	7.5	–	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

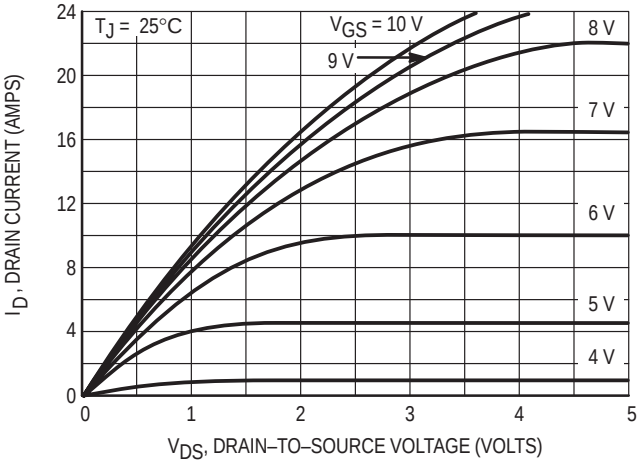


Figure 1. On–Region Characteristics

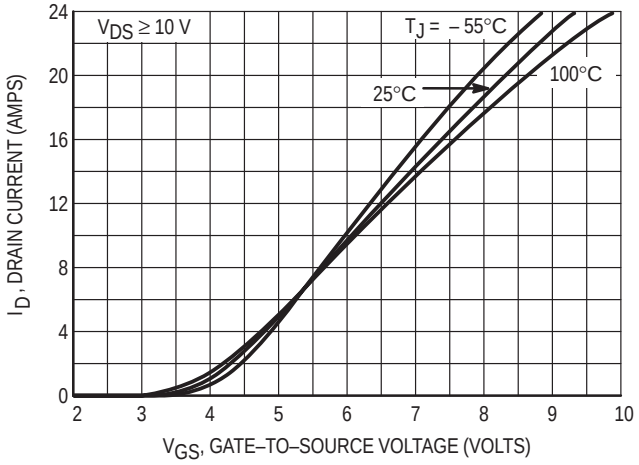


Figure 2. Transfer Characteristics

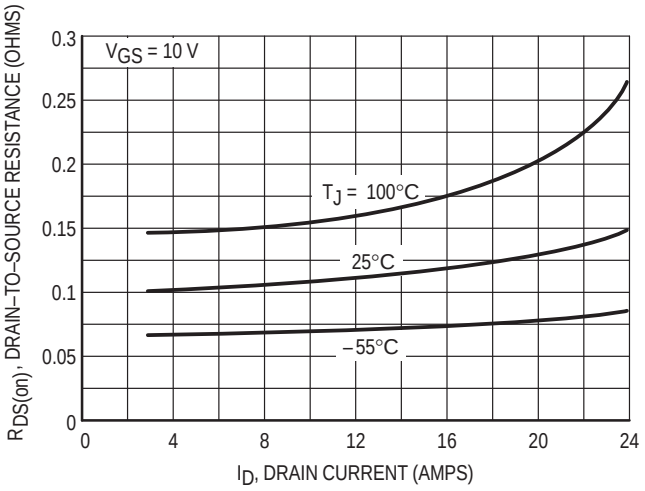


Figure 3. On–Resistance versus Drain Current and Temperature

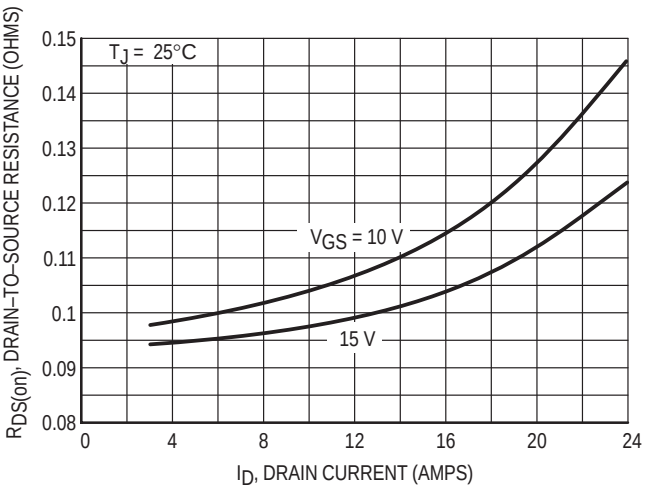


Figure 4. On–Resistance versus Drain Current and Gate Voltage

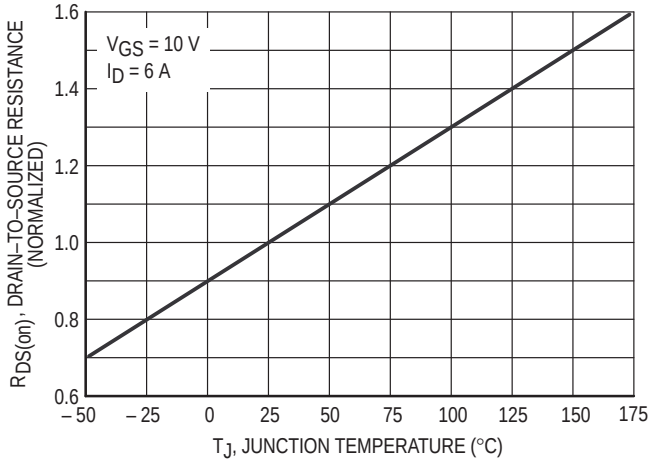


Figure 5. On–Resistance Variation with Temperature

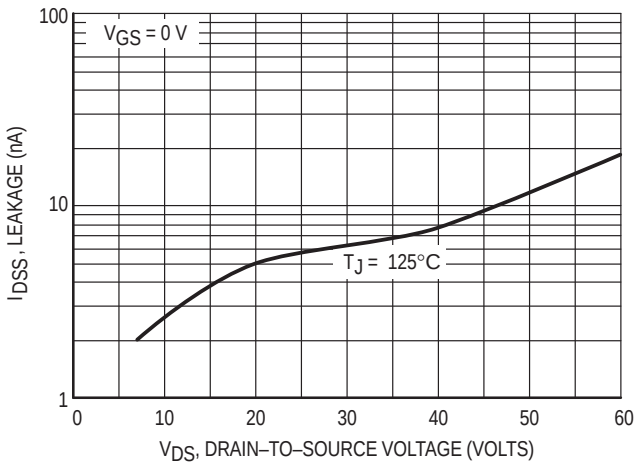


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

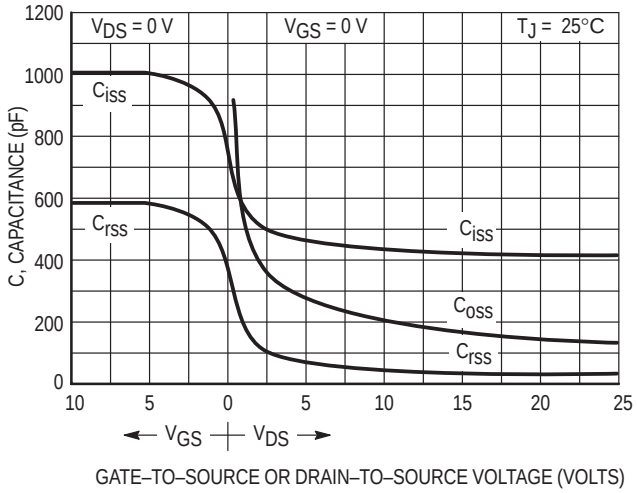


Figure 7. Capacitance Variation

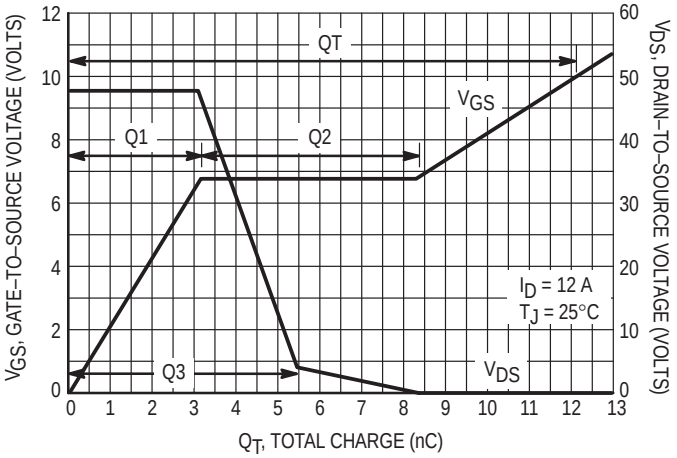


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

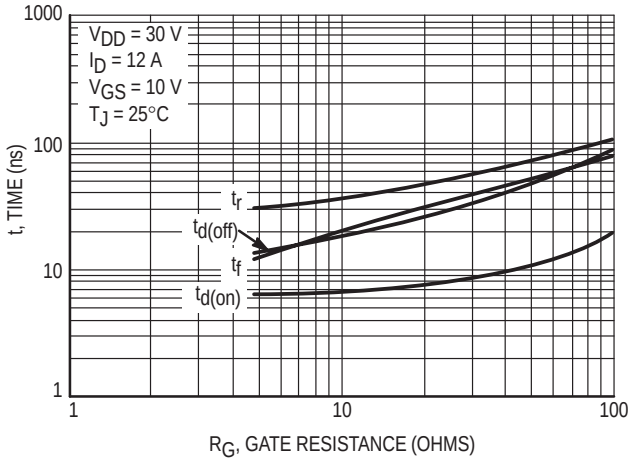


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

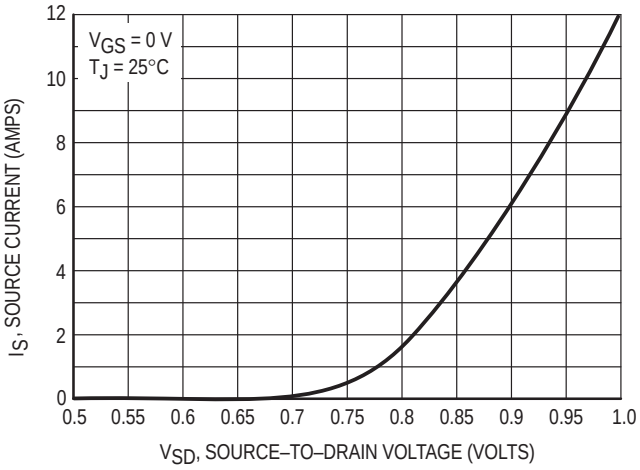


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

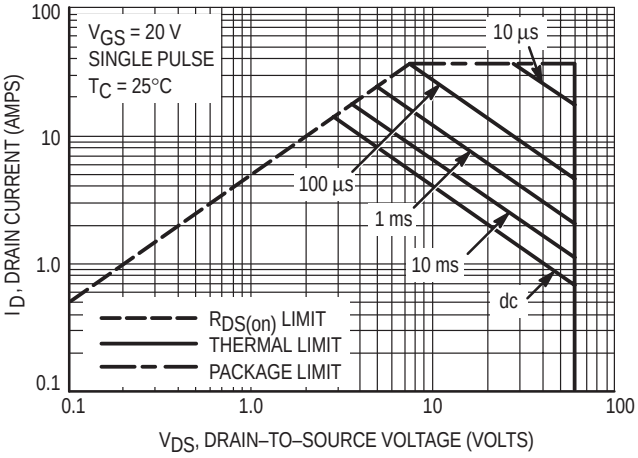


Figure 11. Maximum Rated Forward Biased Safe Operating Area

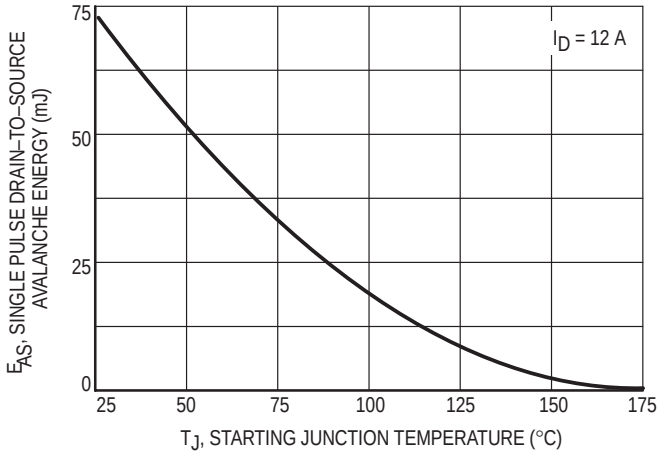


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

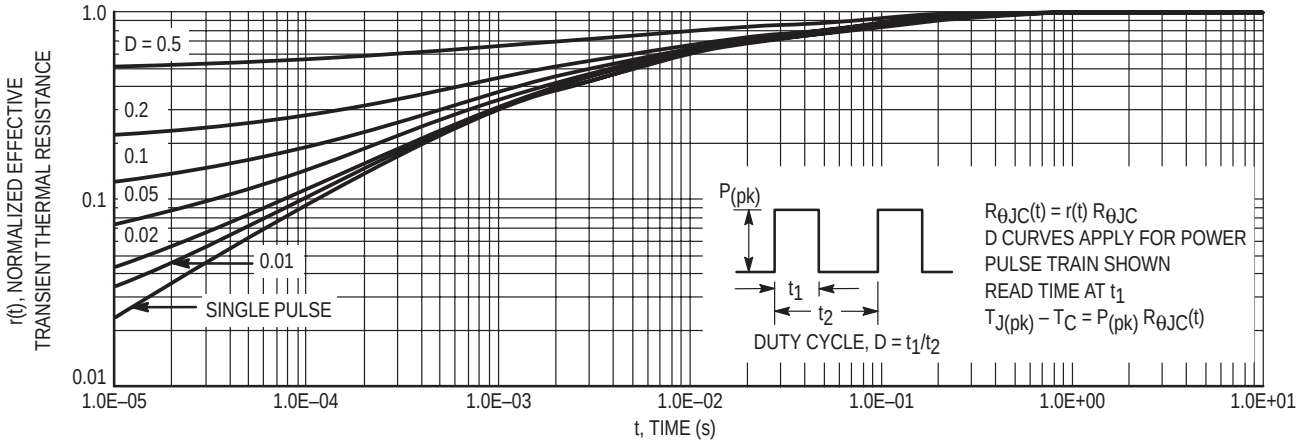


Figure 13. Thermal Response

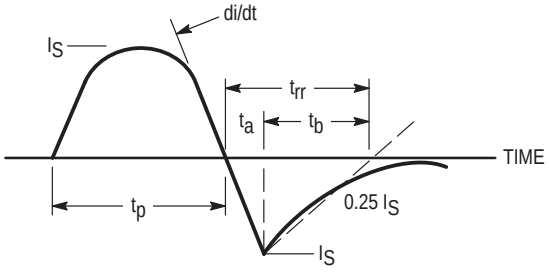


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

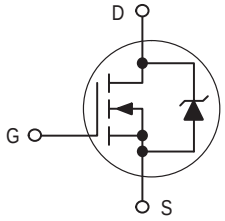
TMOS V
Power Field Effect Transistor
DPAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

MTD3055VL

Motorola Preferred Device

TMOS POWER FET
12 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.18 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.



CASE 369A–13, Style 2
DPAK Surface Mount

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Surface Mount Package Available in 16 mm 13–inch/2500 Unit Tape & Reel, Add T4 Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Single Pulse ($t_p \le 50$ ms)	V_{GS} V_{GSM}	±15 ± 20	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	12 8.0 42	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C, when mounted to minimum recommended pad size	P_D	48 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 12 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	72	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient, when mounted to minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	60 —	— 62	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	1.0 —	1.6 3.0	2.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	—	0.12	0.18	Ohm
Drain–Source On–Voltage (V_{GS} = 5.0 Vdc) (I_D = 12 Adc) (I_D = 6.0 Adc, T_J = 150°C)		$V_{DS(on)}$	— —	1.6 —	2.6 2.5	Vdc
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 6.0 Adc)		g_{FS}	5.0	8.8	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	410	570	pF
Output Capacitance		C_{oss}	—	114	160	
Reverse Transfer Capacitance		C_{rss}	—	21	40	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 12 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	9.0	20	ns
Rise Time		t_r	—	85	190	
Turn–Off Delay Time		$t_{d(off)}$	—	14	30	
Fall Time		t_f	—	43	90	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 12 Adc, V_{GS} = 5 Vdc)	Q_T	—	8.1	10	nC
		Q_1	—	1.8	—	
		Q_2	—	4.2	—	
		Q_3	—	3.8	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 12 Adc, V_{GS} = 0 Vdc) (I_S = 12 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	— —	0.97 0.86	1.3 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 12 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	55.7	—	ns
		t_a	—	37	—	
		t_b	—	18.7	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.116	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	3.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

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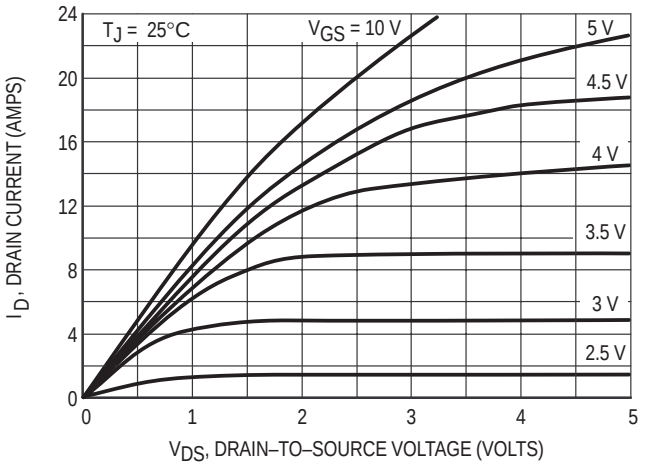

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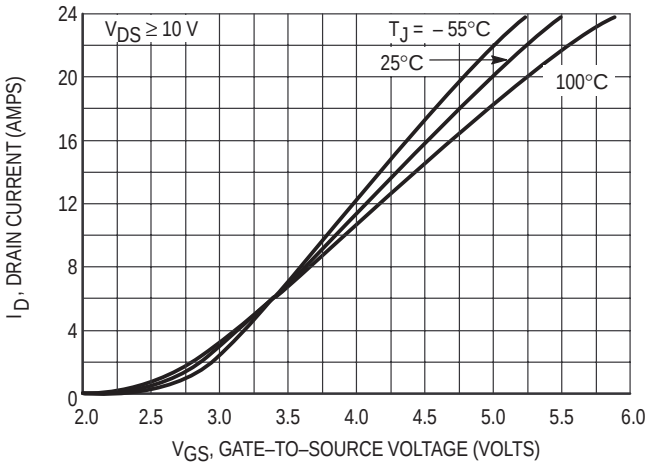

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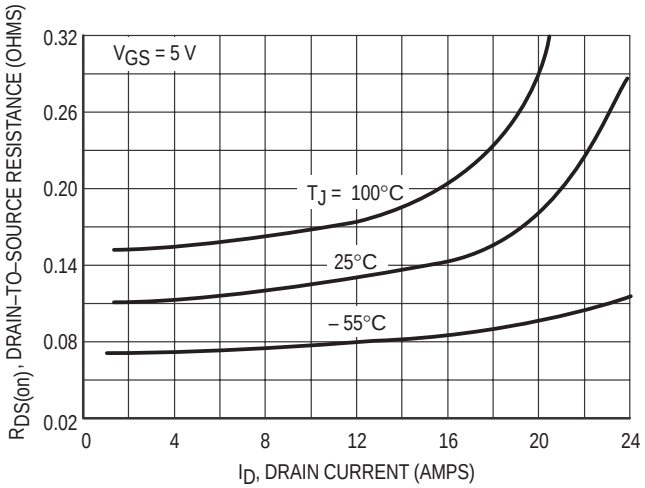

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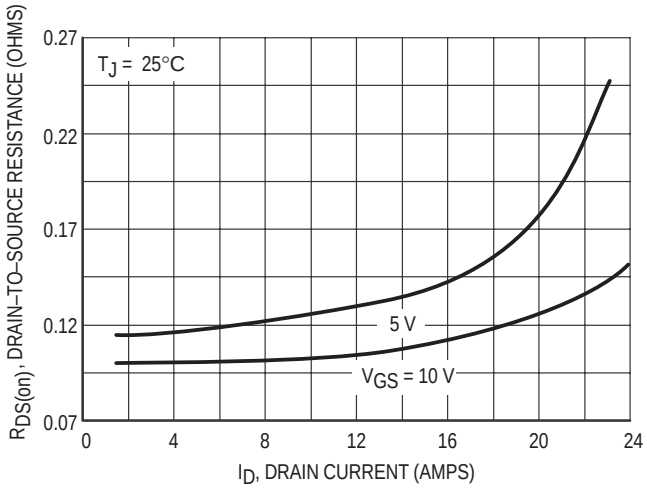

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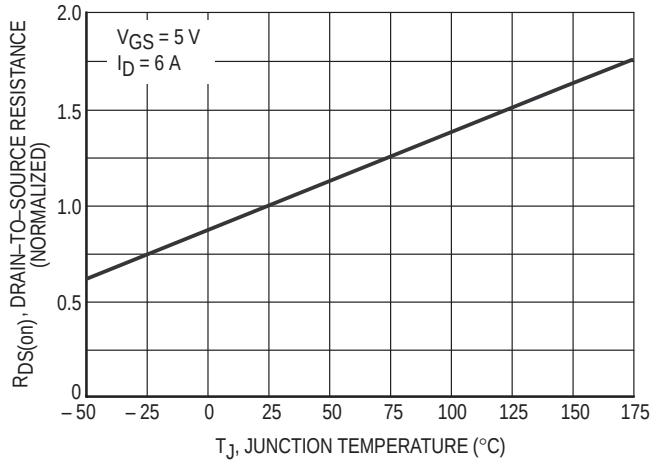

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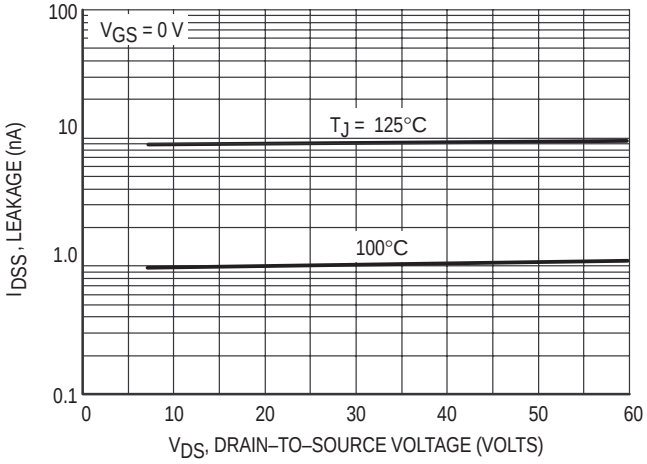

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$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

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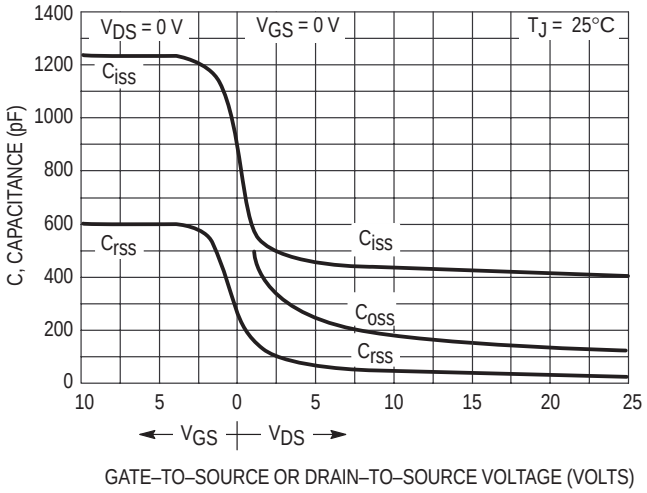


Figure 7. Capacitance Variation

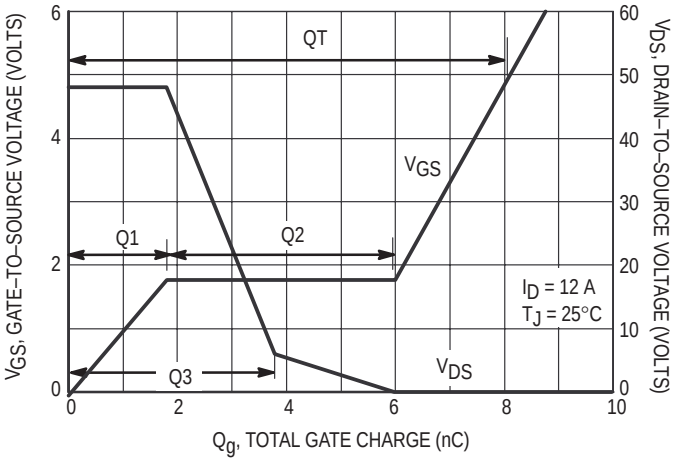


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

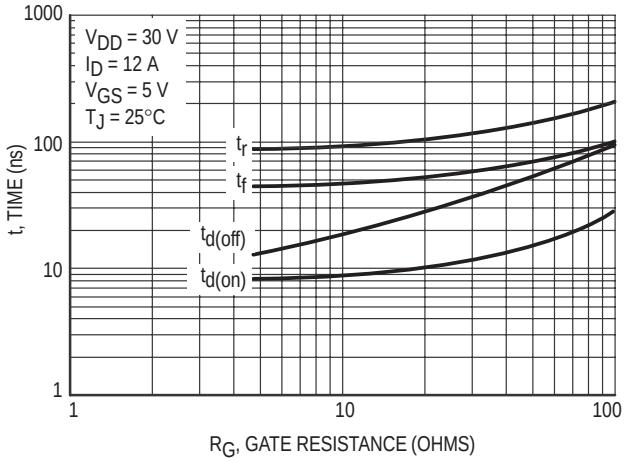


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

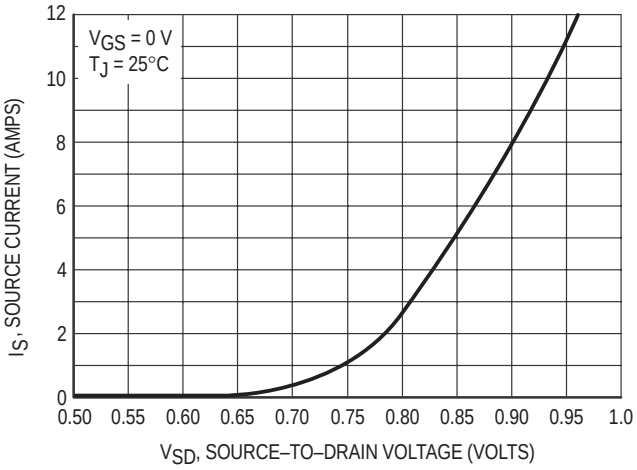


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

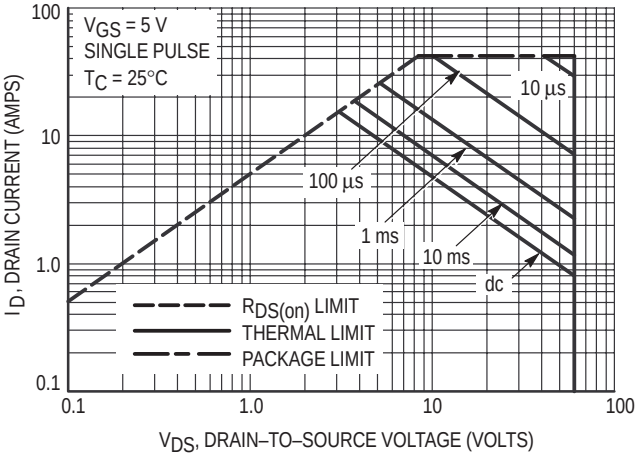


Figure 11. Maximum Rated Forward Biased Safe Operating Area

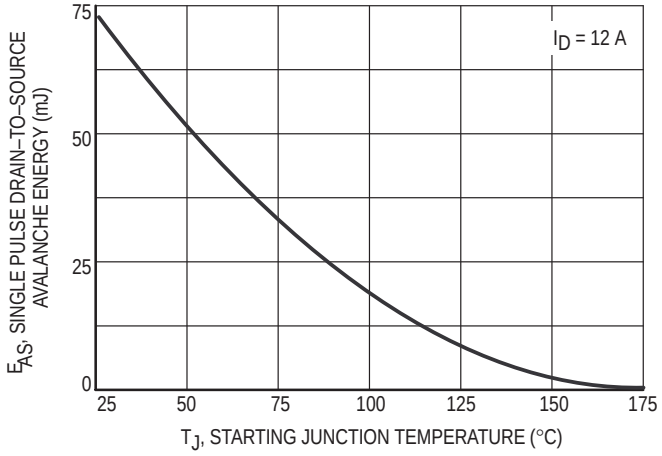


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

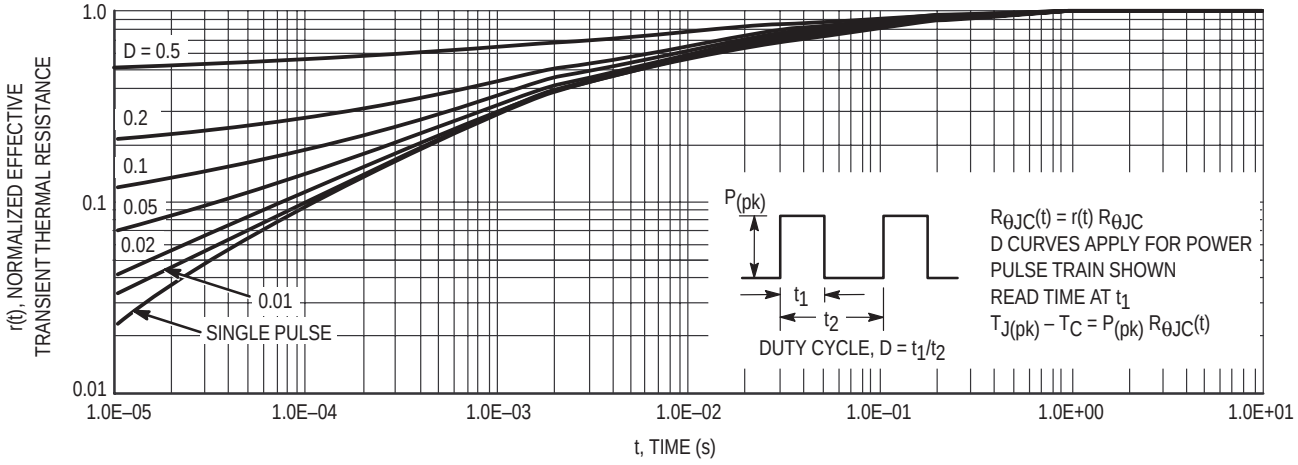


Figure 13. Thermal Response

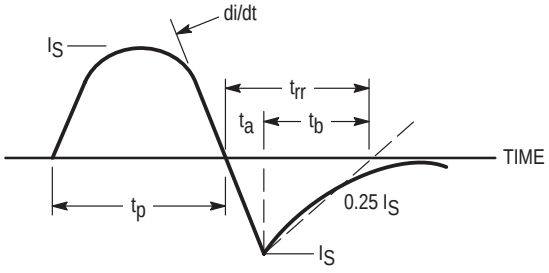


Figure 14. Diode Reverse Recovery Waveform

Advance Information

Medium Power Surface Mount Products

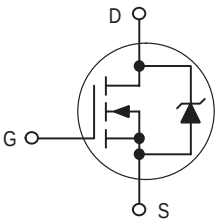
TMOS Dual N-Channel Field Effect Transistor

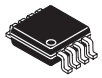
MTDF1N02HD

Motorola Preferred Device

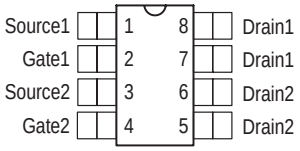
SINGLE TMOS POWER MOSFET 1.7 AMPERES 20 VOLTS $R_{DS(on)}$ = 0.120 OHM

Micro8™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process to achieve lowest possible on–resistance per silicon area. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Micro8™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.





CASE 846A–02, Style 2
Micro8



Top View

- Miniature Micro8 Surface Mount Package — Saves Board Space
- Extremely Low Profile (<1.1mm) for thin applications such as PCMCIA cards
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for Micro8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 8.0	Vdc
Drain Current — Continuous @ T_A = 25°C (1) — Continuous @ T_A = 70°C (1) — Pulsed Drain Current (4)	I_D I_D I_{DM}	1.9 1.7 14	Adc Apk
Total Power Dissipation @ T_A = 25°C (1) Linear Derating Factor (1)	P_D	0.625 5.0	Watts mW/°C
Total Power Dissipation @ T_A = 25°C (3) Linear Derating Factor (3)	P_D	1.25 10	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C

THERMAL RESISTANCE

Rating		Symbol	Typ.	Max.	Unit
Thermal Resistance	— Junction to Ambient, PCB Mount (1)	$R_{\theta JA}$	160	200	°C/W
	— Junction to Ambient, PCB Mount (2)	$R_{\theta JA}$	240	300	
	— Junction to Ambient, PBD Mount (3)	$R_{\theta JA}$	80	100	

(1) When mounted on FR–4/G–10 board using min. recommended footprint, based on PD in 1 die, 1 die operating. (V_{GS} = 4.5 V, @ Steady State)
(2) When mounted on FR–4/G–10 board using min. recommended footprint, based on PD in 1 die, both dies operating. (V_{GS} = 4.5 V, @ Steady State)
(3) When mounted on 1 inch square copper board, for comparison to the other SMD devices. (V_{GS} = 4.5 V, @ Steady State)
(4) Repetitive rating; pulse width limited by maximum junction temperature.

DEVICE MARKING **ORDERING INFORMATION**

	Device	Reel Size	Tape Width	Quantity
BA	MTDF1N02HDR2	13″	12 mm embossed tape	4000 units

This document contains information on a new product. Specifications and information are subject to change without notice.
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (1) (3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 20 —	 — 5.0	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 16 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 1.0 25	μAdc
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 0.7 —	 0.9 2.5	 — —	Vdc mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (3) (V_{GS} = 4.5 Vdc, I_D = 1.7 Adc) (V_{GS} = 2.7 Vdc, I_D = 0.85 Adc)		$R_{DS(on)}$	 — —	 99 133	 120 160	mΩ
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 0.85 Adc)		g_{FS}	2.0	—	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 15 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	145	—	pF
Output Capacitance		C_{oss}	—	90	—	
Transfer Capacitance		C_{rss}	—	38	—	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DS} = 10 Vdc, I_D = 1.7 Adc, V_{GS} = 4.5 Vdc, R_G = 6 Ω) (1)	$t_{d(on)}$	—	8.0	—	ns
Rise Time		t_r	—	27	—	
Turn–Off Delay Time		$t_{d(off)}$	—	23	—	
Fall Time		t_f	—	34	—	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 0.85 Adc, V_{GS} = 2.7 Vdc, R_G = 6 Ω) (1)	$t_{d(on)}$	—	16	—	ns
Rise Time		t_r	—	79	—	
Turn–Off Delay Time		$t_{d(off)}$	—	24	—	
Fall Time		t_f	—	31	—	
Gate Charge	(V_{DS} = 16 Vdc, I_D = 1.7 Adc, V_{GS} = 4.5 Vdc)	Q_T	—	3.9	5.5	nC
		Q_1	—	0.4	—	
		Q_2	—	1.7	—	
		Q_3	—	1.5	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 1.7 Adc, V_{GS} = 0 Vdc) (1) (I_S = 1.7 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 0.84 0.71	 1.0 —	Vdc
Reverse Recovery Time	(I_S = 1.7 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (1)	t_{rr}	—	29	—	ns
		t_a	—	14	—	
		t_b	—	15	—	
Reverse Recovery Storage Charge		Q_{RR}	—	0.018	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

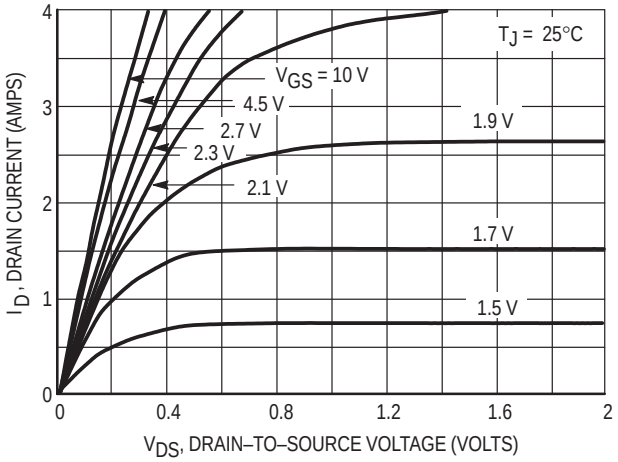


Figure 1. On–Region Characteristics

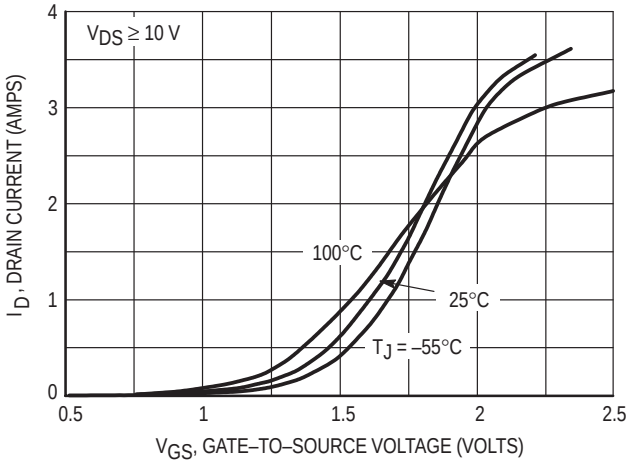


Figure 2. Transfer Characteristics

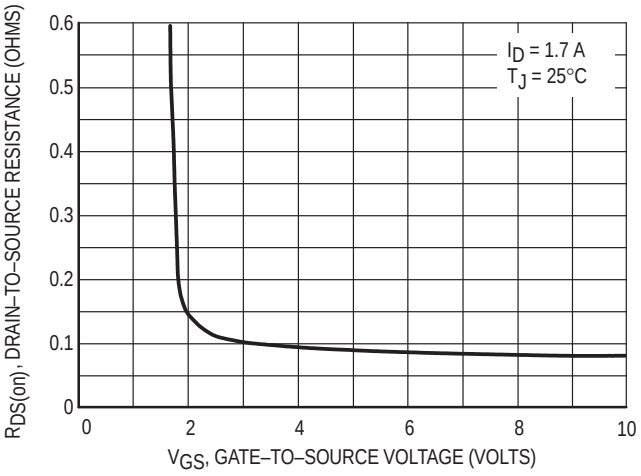


Figure 3. On–Resistance versus Gate–to–Source Voltage

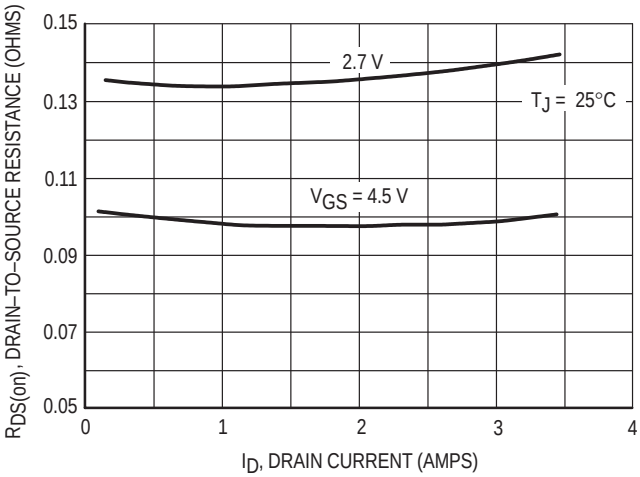


Figure 4. On–Resistance versus Drain Current and Gate Voltage

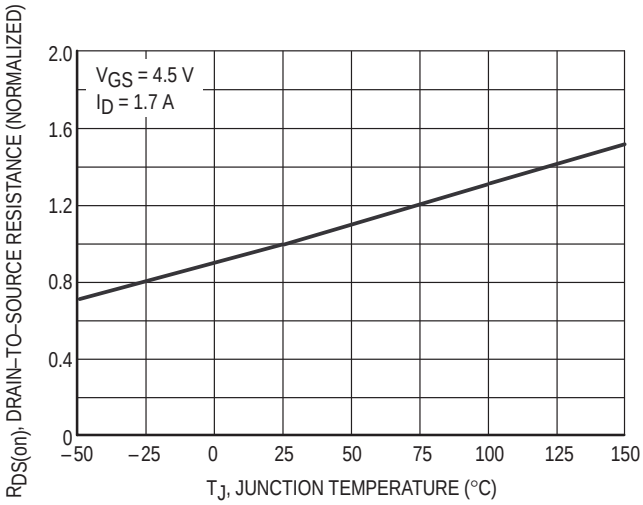


Figure 5. On–Resistance Variation with Temperature

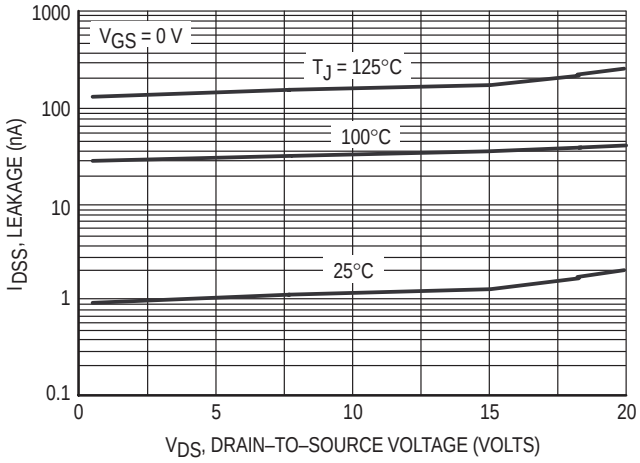


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

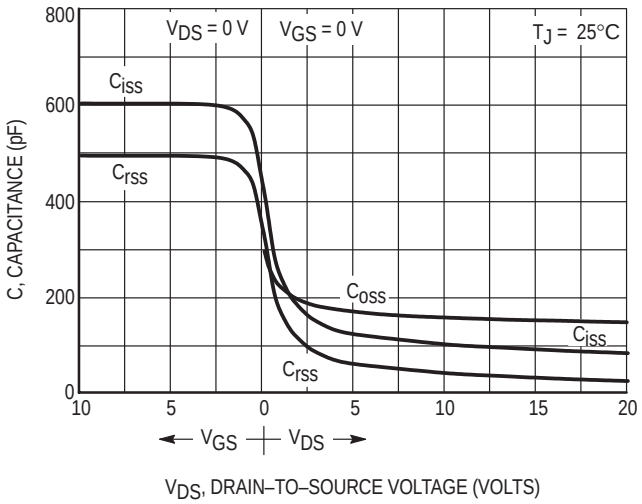


Figure 7. Capacitance Variation

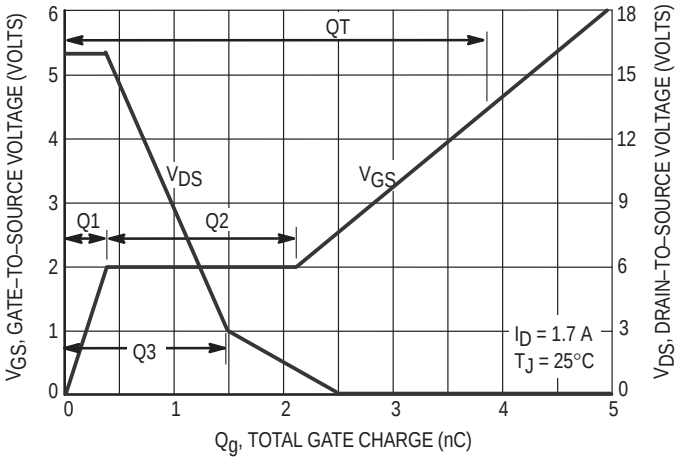


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

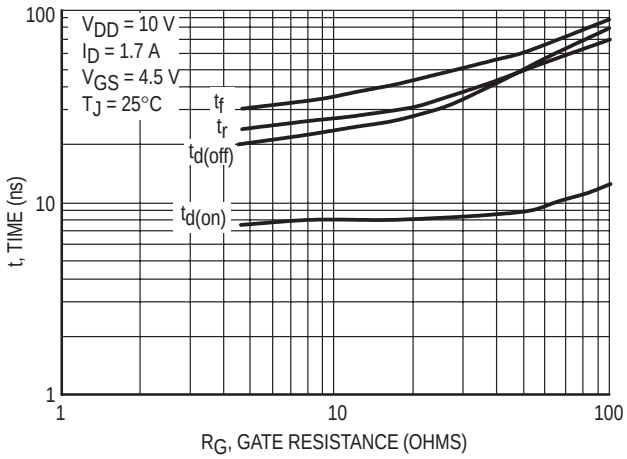


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

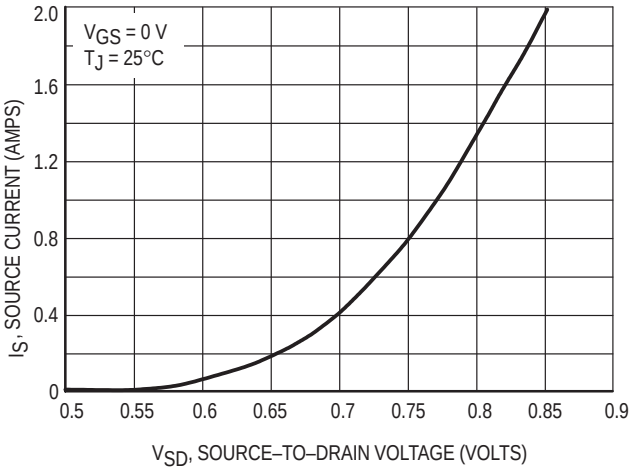


Figure 10. Diode Forward Voltage versus Current

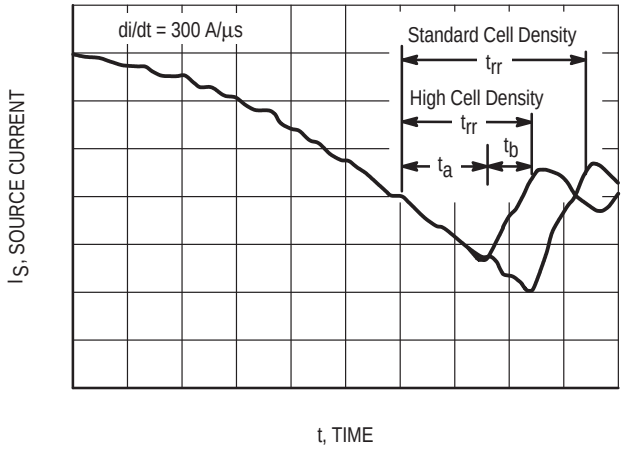


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curve (Figure 12) defines the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

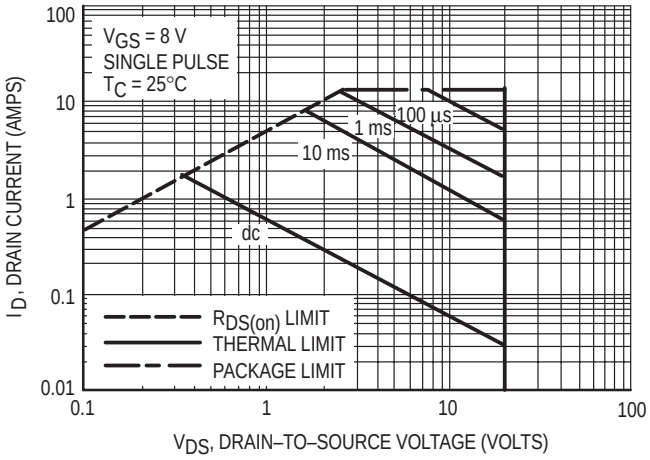


Figure 12. Maximum Rated Forward Biased Safe Operating Area

TYPICAL ELECTRICAL CHARACTERISTICS

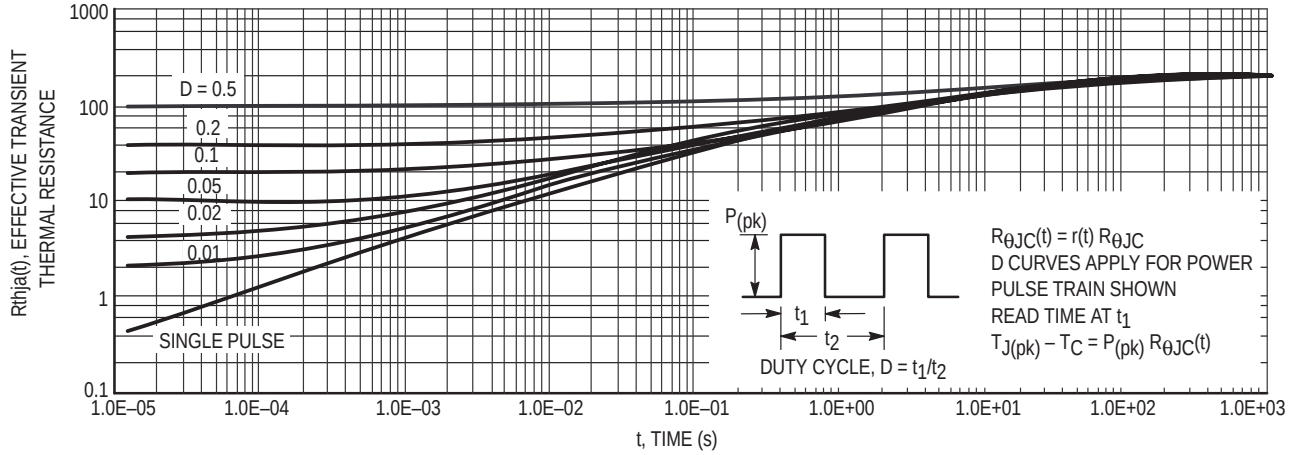


Figure 13. Thermal Response

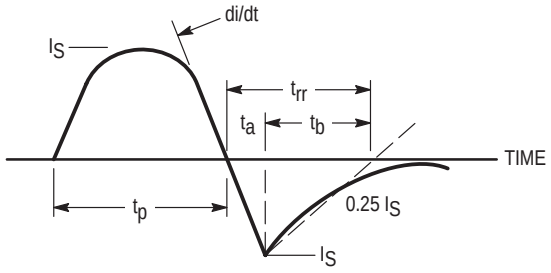
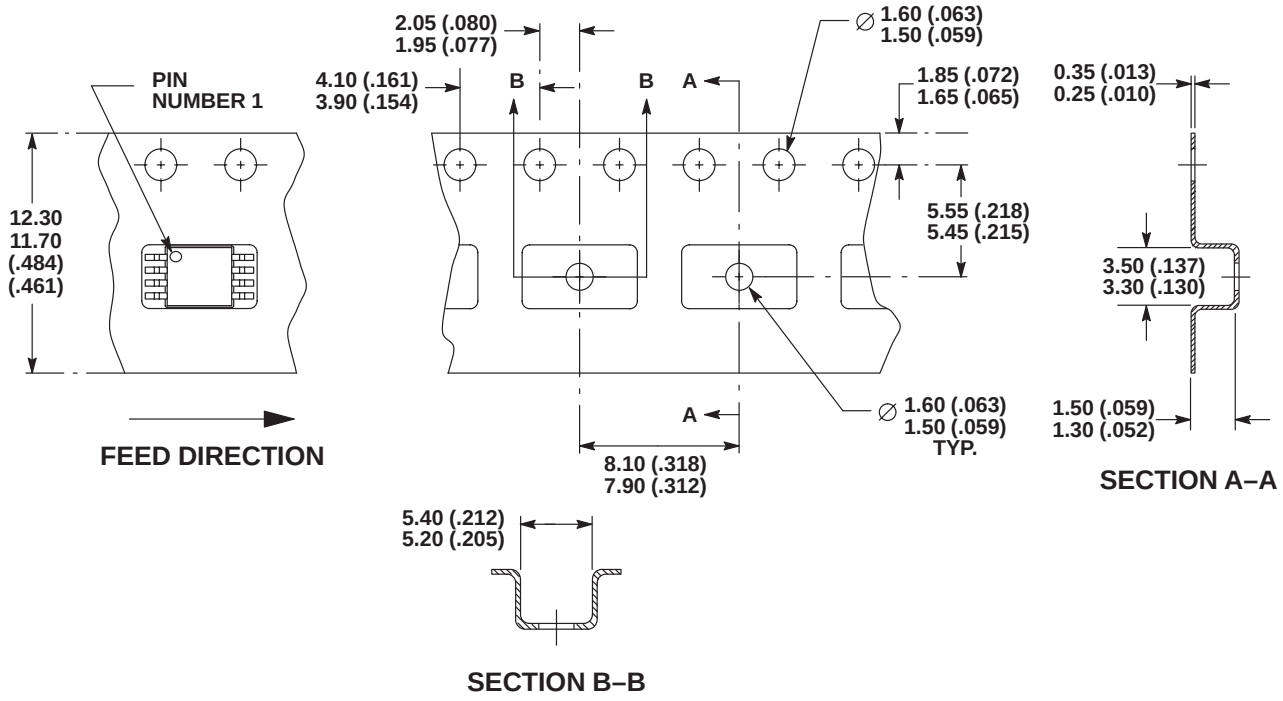


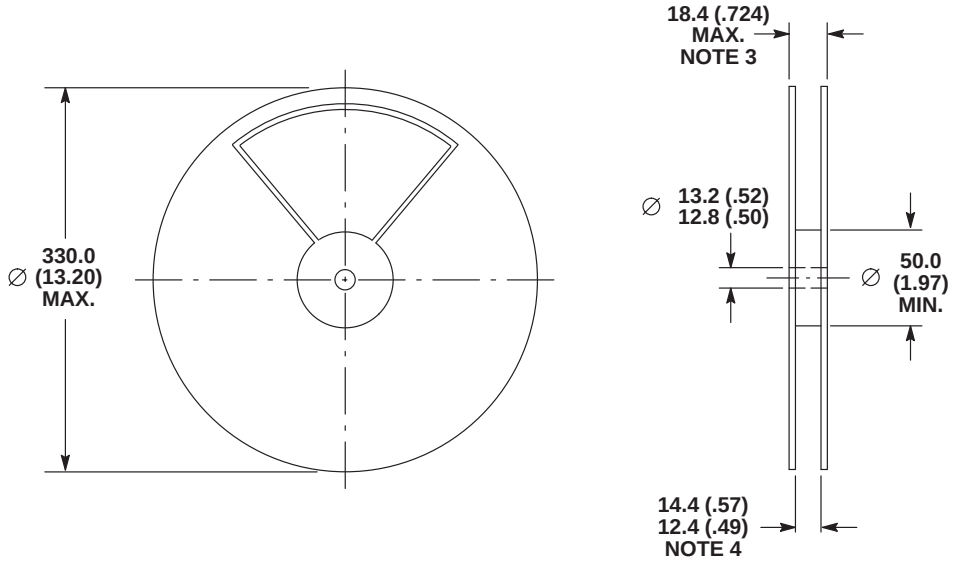
Figure 14. Diode Reverse Recovery Waveform

TAPE & REEL INFORMATION

Micro8
Dimensions are shown in millimeters (inches)



NOTES:
1. **CONFORMS TO EIA–481–1.**
2. **CONTROLLING DIMENSION: MILLIMETER.**



NOTES:
1. **CONFORMS TO EIA–481–1.**
2. **CONTROLLING DIMENSION: MILLIMETER.**
3. **INCLUDES FLANGE DISTORTION AT OUTER EDGE.**
4. **DIMENSION MEASURED AT INNER HUB.**

Advance Information

Medium Power Surface Mount Products

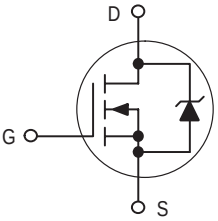
TMOS Dual N-Channel Field Effect Transistor

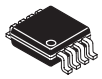
MTDF1N03HD

Motorola Preferred Device

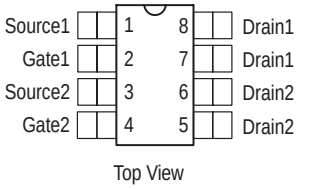
SINGLE TMOS POWER MOSFET 1.7 AMPERES 30 VOLTS $R_{DS(on)}$ = 0.120 OHM

Micro8™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process to achieve lowest possible on–resistance per silicon area. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Micro8™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.





CASE 846A–02, Style 2
Micro8



- Miniature Micro8 Surface Mount Package — Saves Board Space
- Extremely Low Profile (<1.1mm) for thin applications such as PCMCIA cards
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for Micro8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	30	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C (1) — Continuous @ T_A = 70°C (1) — Pulsed Drain Current (4)	I_D I_D I_{DM}	1.9 1.6 14	Adc Apk
Total Power Dissipation @ T_A = 25°C (1) Linear Derating Factor (1)	P_D	0.625 5.0	Watts mW/°C
Total Power Dissipation @ T_A = 25°C (3) Linear Derating Factor (3)	P_D	1.25 10	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C

THERMAL RESISTANCE

Rating		Symbol	Typ.	Max.	Unit
Thermal Resistance	— Junction to Ambient, PCB Mount (1)	$R_{\theta JA}$	160	200	°C/W
	— Junction to Ambient, PCB Mount (2)	$R_{\theta JA}$	240	300	
	— Junction to Ambient, PBD Mount (3)	$R_{\theta JA}$	80	100	

(1) When mounted on FR–4/G–10 board using min. recommended footprint, based on PD in 1 die, 1 die operating. (V_{GS} = 10 V, @ Steady State)
(2) When mounted on FR–4/G–10 board using min. recommended footprint, based on PD in 1 die, both dies operating. (V_{GS} = 10 V, @ Steady State)
(3) When mounted on 1 inch square copper board, for comparison to the other SMD devices. (V_{GS} = 10 V, @ Steady State)
(4) Repetitive rating; pulse width limited by maximum junction temperature.

DEVICE MARKING **ORDERING INFORMATION**

	Device	Reel Size	Tape Width	Quantity
BB	MTDF1N03HDR2	13″	12 mm embossed tape	4000 units

This document contains information on a new product. Specifications and information are subject to change without notice.
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (1) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			30	—	—	
Temperature Coefficient (Positive)			—	29	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc)			—	—	1.0	
(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	25	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			1.0	1.6	—	
Threshold Temperature Coefficient (Negative)			—	3.7	—	mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (3)		$R_{DS(on)}$				mΩ
(V_{GS} = 10 Vdc, I_D = 1.7 Adc)			—	96	120	
(V_{GS} = 4.5 Vdc, I_D = 0.85 Adc)			—	135	160	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 0.85 Adc) (1)		g_{FS}	1.0	2.0	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	140	—	pF
Output Capacitance		C_{oss}	—	70	—	
Transfer Capacitance		C_{rss}	—	30	—	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DS} = 15 Vdc, I_D = 1.7 Adc, V_{GS} = 10 Vdc, R_G = 6 Ω) (1)	$t_{d(on)}$	—	7.5	—	ns
Rise Time		t_r	—	10	—	
Turn–Off Delay Time		$t_{d(off)}$	—	22	—	
Fall Time		t_f	—	18	—	
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 0.85 Adc, V_{GS} = 4.5 Vdc, R_G = 6 Ω) (1)	$t_{d(on)}$	—	7.0	—	ns
Rise Time		t_r	—	8.2	—	
Turn–Off Delay Time		$t_{d(off)}$	—	22	—	
Fall Time		t_f	—	14.5	—	
Gate Charge	(V_{DS} = 24 Vdc, I_D = 1.7 Adc, V_{GS} = 10 Vdc)	Q_T	—	5.0	7.0	nC
		Q_1	—	0.5	—	
		Q_2	—	1.65	—	
		Q_3	—	1.3	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 1.7 Adc, V_{GS} = 0 Vdc) (1)	V_{SD}				Vdc
	(I_S = 1.7 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.84	1.0	
			—	0.7	—	
Reverse Recovery Time	(I_S = 1.7 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (1)	t_{rr}	—	20	—	ns
		t_a	—	12	—	
		t_b	—	8.0	—	
Reverse Recovery Storage Charge		Q_{RR}	—	0.012	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

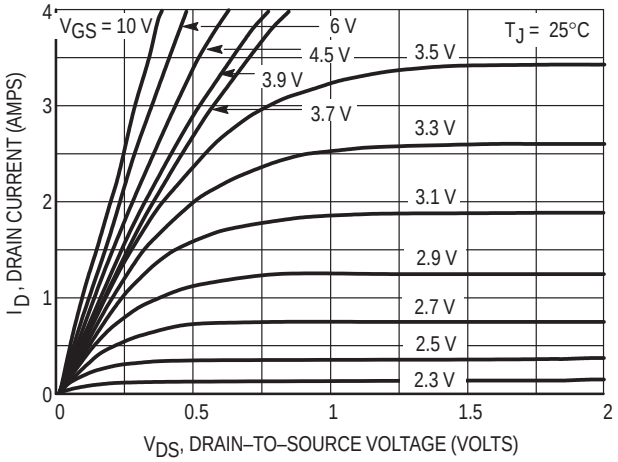


Figure 1. On–Region Characteristics

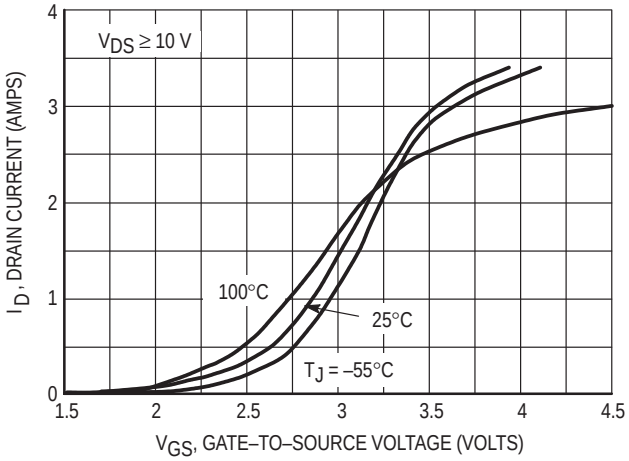


Figure 2. Transfer Characteristics

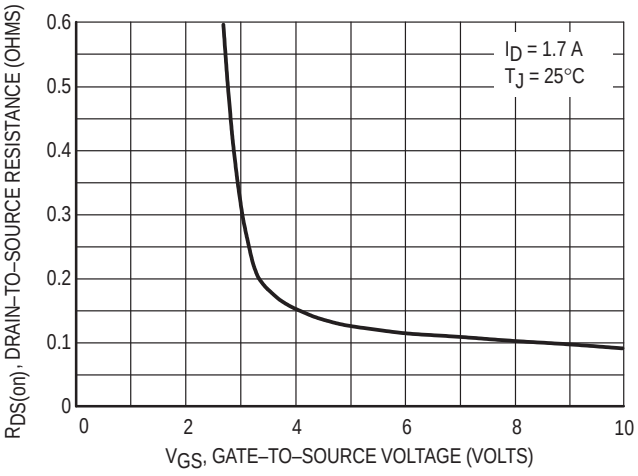


Figure 3. On–Resistance versus Gate–to–Source Voltage

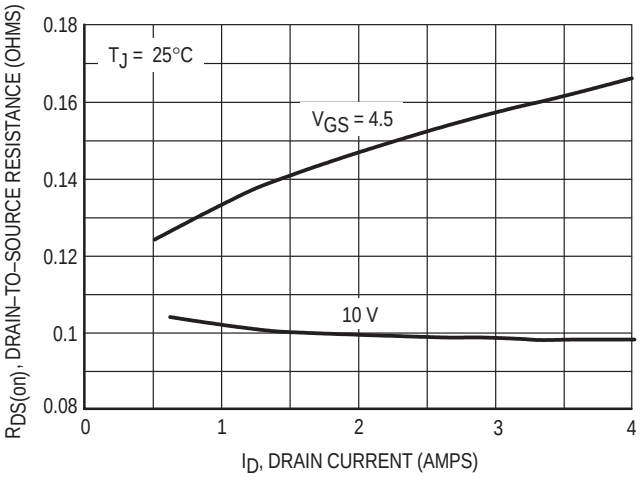


Figure 4. On–Resistance versus Drain Current and Gate Voltage

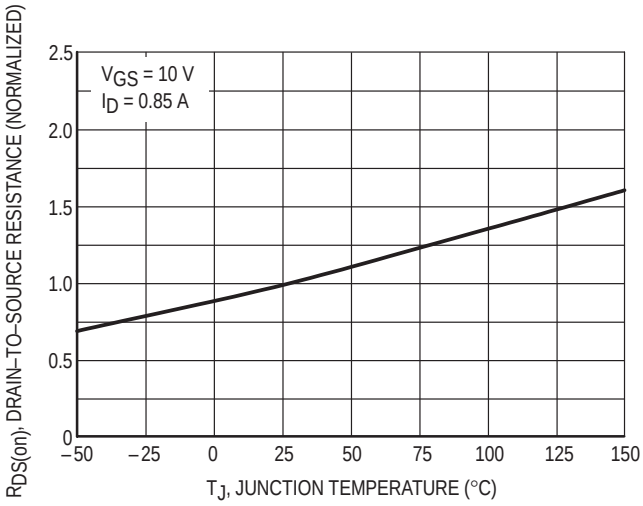


Figure 5. On–Resistance Variation with Temperature

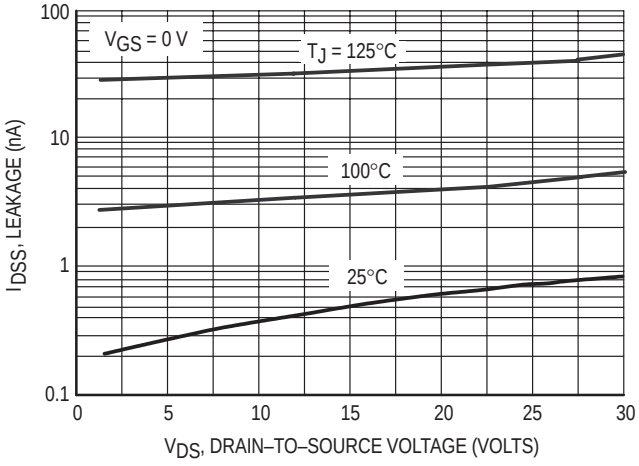


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

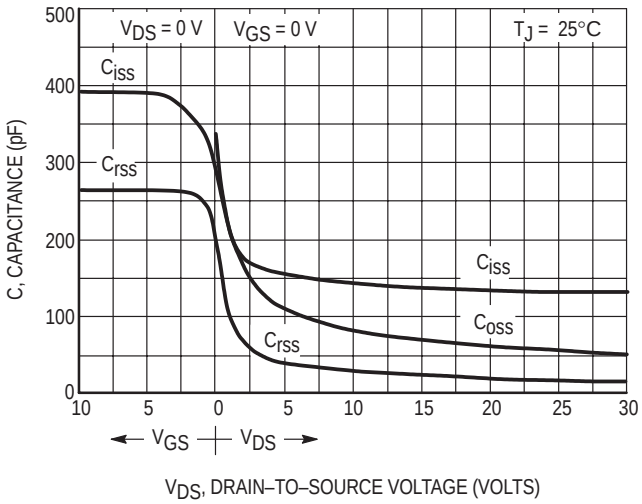


Figure 7. Capacitance Variation

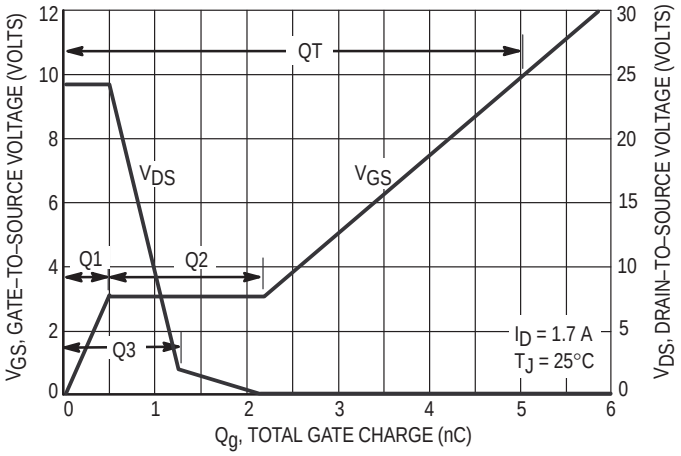


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

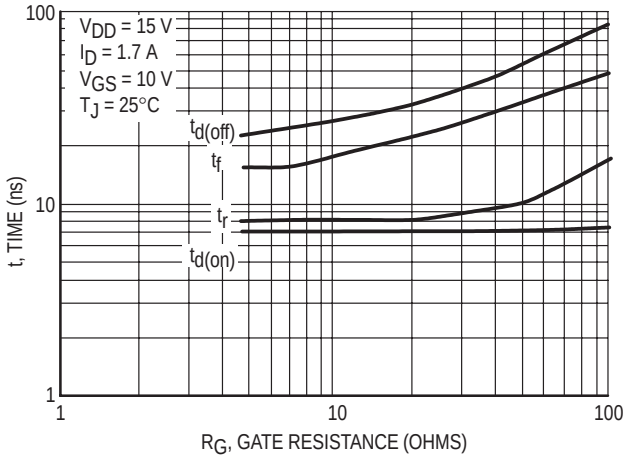


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

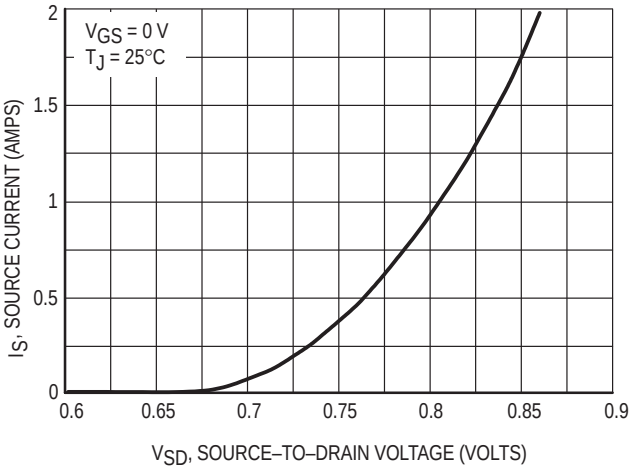


Figure 10. Diode Forward Voltage versus Current

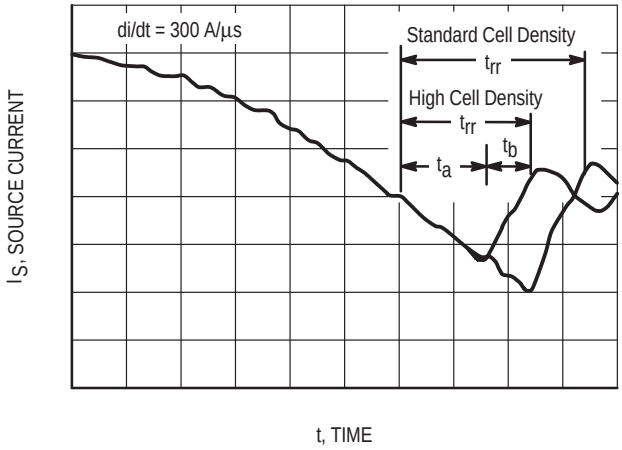


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curve (Figure 12) defines the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

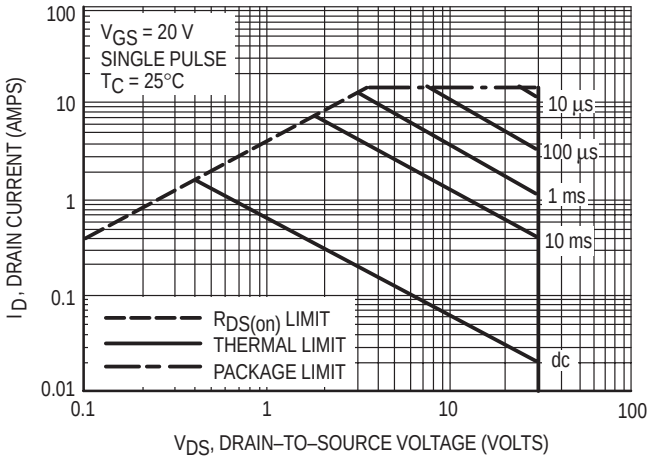


Figure 12. Maximum Rated Forward Biased Safe Operating Area

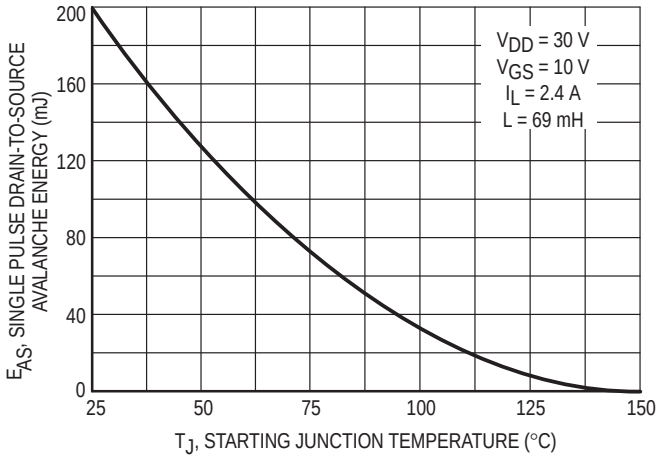


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

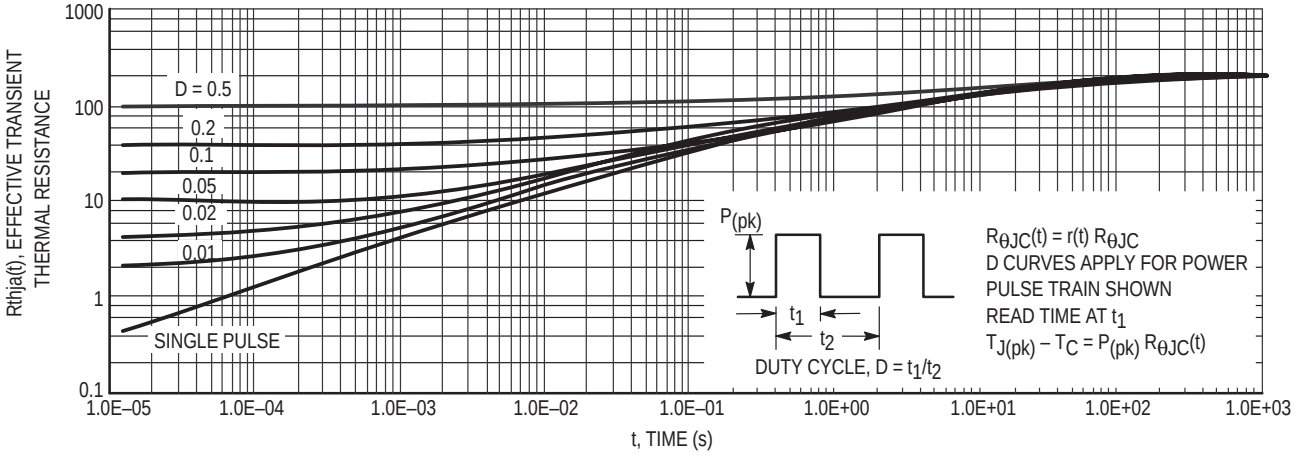


Figure 14. Thermal Response

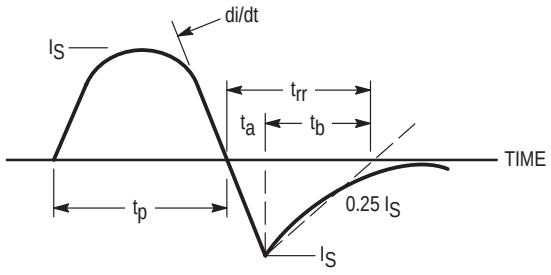
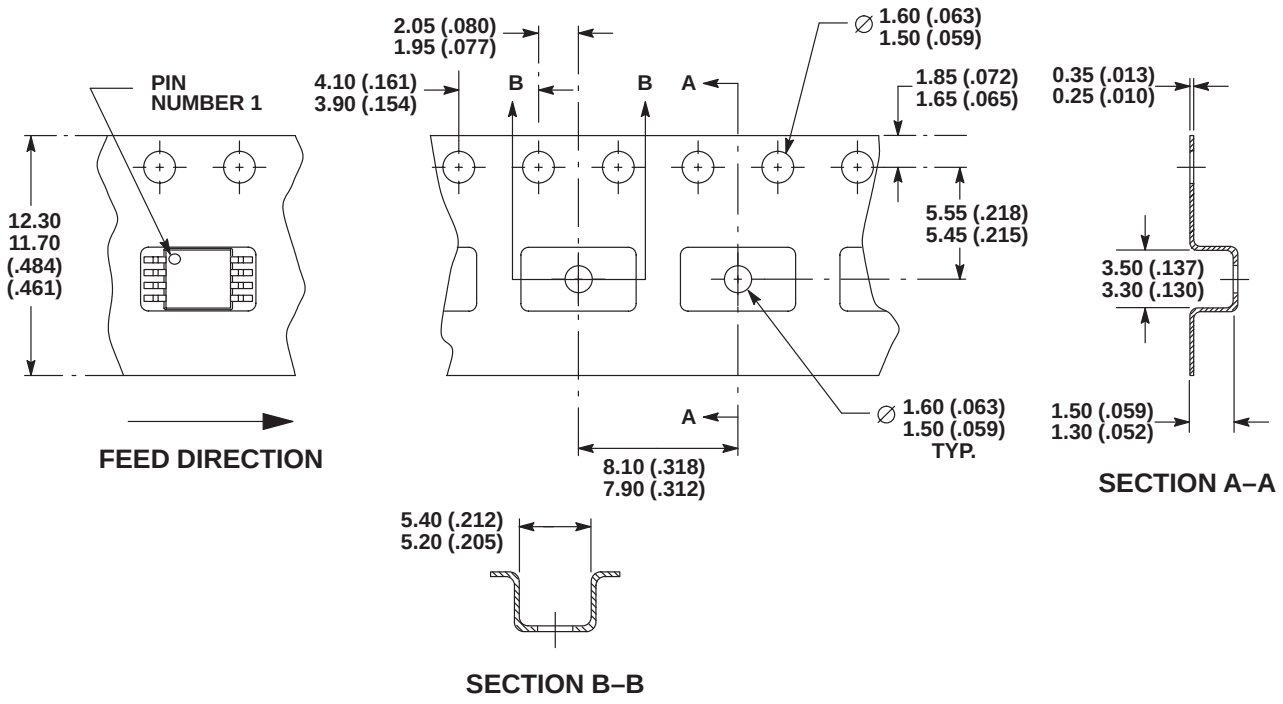


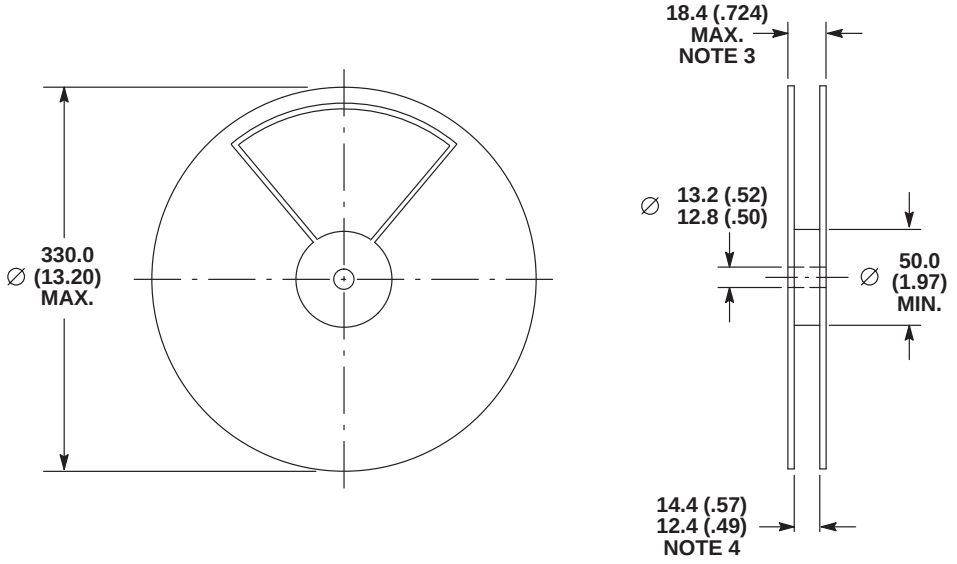
Figure 15. Diode Reverse Recovery Waveform

TAPE & REEL INFORMATION

Micro8
Dimensions are shown in millimeters (inches)



NOTES:
1. **CONFORMS TO EIA–481–1.**
2. **CONTROLLING DIMENSION: MILLIMETER.**



NOTES:
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2. **CONTROLLING DIMENSION: MILLIMETER.**
3. **INCLUDES FLANGE DISTORTION AT OUTER EDGE.**
4. **DIMENSION MEASURED AT INNER HUB.**

Advance Information

ISOTOP™ TMOS E-FET ™ Power Field Effect Transistor

N–Channel Enhancement–Mode Silicon Gate

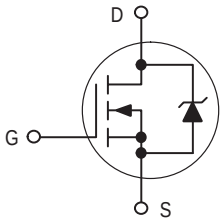
MTE30N50E

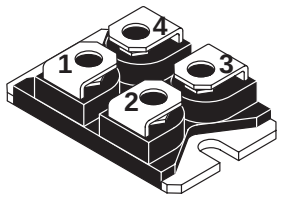
Motorola Preferred Device

TMOS POWER FET
30 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.150 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new energy design also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, PWM motor controls, and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- 2500 V RMS Isolated ISOTOP Package
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- Very Low Internal Parasitic Inductance
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- U.L. Recognized, File #E69369





SOT–227B

1. Source
2. Gate
3. Drain
4. Source 2

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	500	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	30 12 80	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C	P_D	250 2.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 30 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	3000	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	500	560	—	Vdc
Temperature Coefficient (Positive)			—	566	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	200	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.2	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)		$R_{DS(on)}$	—	0.13	0.15	Ohms
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 30 Adc)		$V_{DS(on)}$	—	4.1	5.0	Vdc
(V_{GS} = 10 Vdc, I_D = 15 Adc)			—	—	7.0	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 15 Adc)		g_{FS}	17	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	7200	10080	pF
Output Capacitance		C_{oss}	—	775	1200	
Transfer Capacitance		C_{rss}	—	120	250	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 30 Adc, V_{GS} = 10 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	32	60	ns
Rise Time		t_r	—	105	175	
Turn–Off Delay Time		$t_{d(off)}$	—	160	275	
Fall Time		t_f	—	115	200	
Gate Charge (see figure 8)	(V_{DS} = 400 Vdc, I_D = 30 Adc, V_{GS} = 10 Vdc)	Q_T	—	235	350	nC
		Q_1	—	35	—	
		Q_2	—	110	—	
		Q_3	—	65	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 30 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.95	1.2	Vdc
	(I_S = 30 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.88	—	
Reverse Recovery Time	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	485	—	ns
		t_a	—	312	—	
		t_b	—	173	—	
Reverse Recovery Stored Charge		Q_{RR}	—	8.2	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D	—	5.0	—	nH
Internal Source Inductance		L_S	—	5.0	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

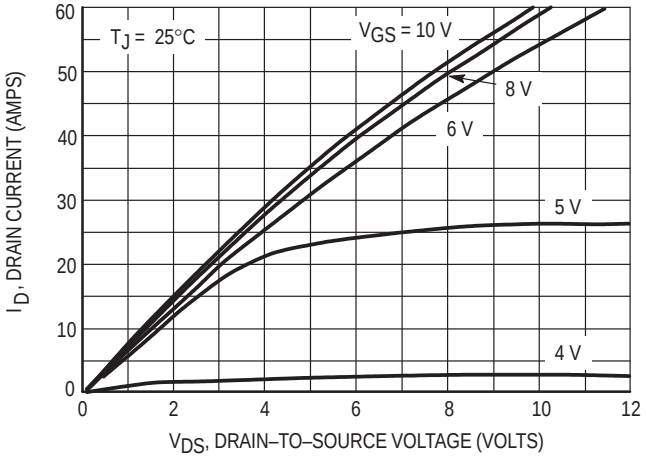


Figure 1. On–Region Characteristics

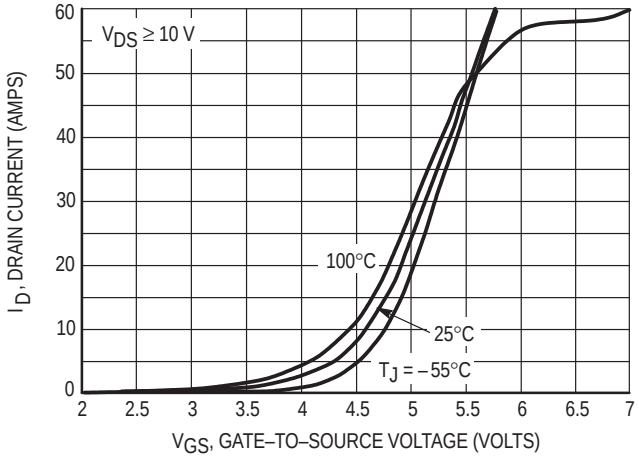


Figure 2. Transfer Characteristics

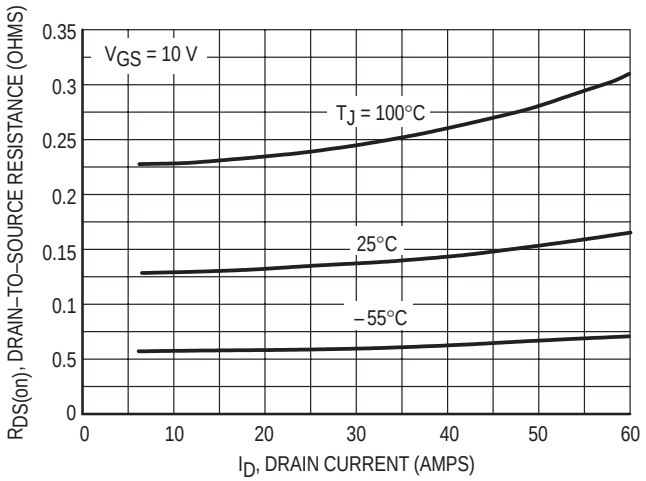


Figure 3. On–Resistance versus Drain Current and Temperature

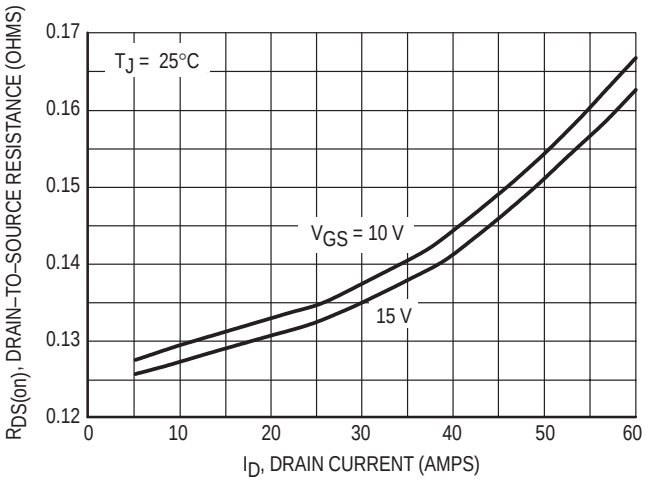


Figure 4. On–Resistance versus Drain Current and Gate Voltage

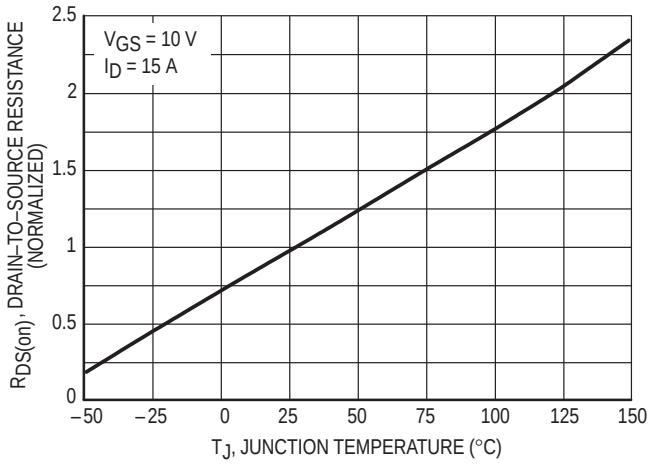


Figure 5. On–Resistance Variation with Temperature

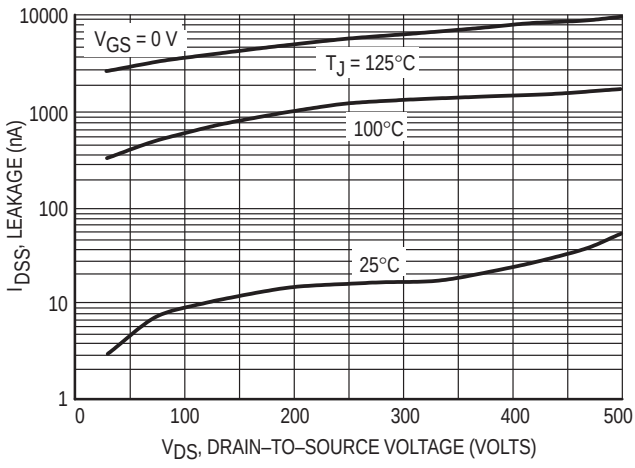


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

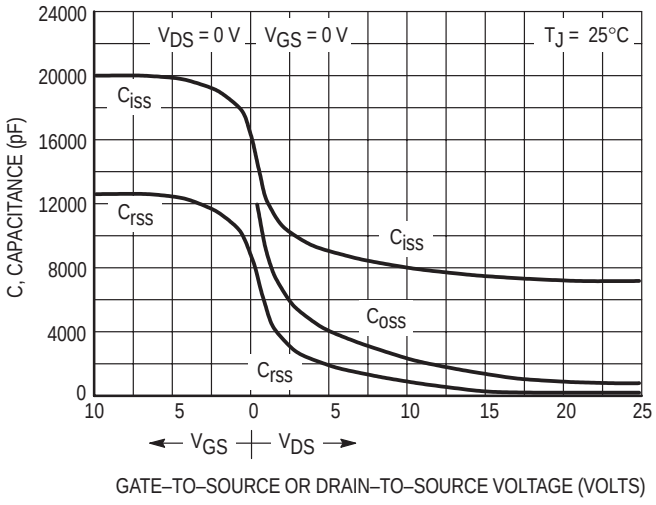


Figure 7. Capacitance Variation

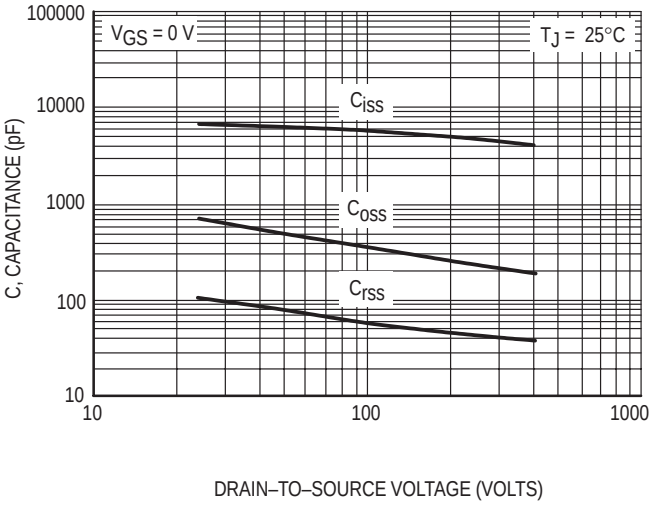


Figure 7b. High Voltage Capacitance Variation

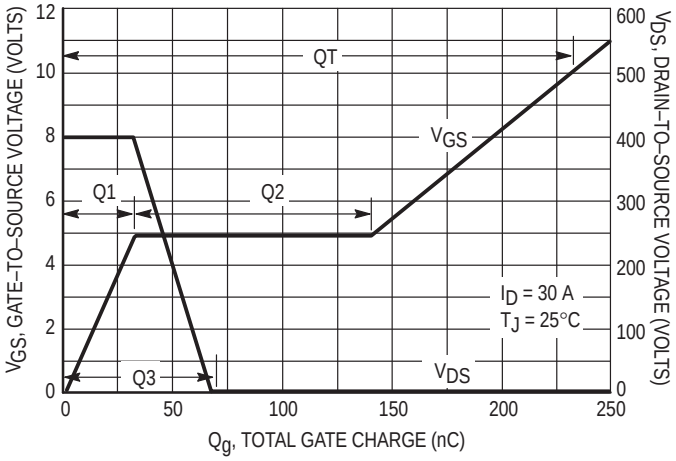


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

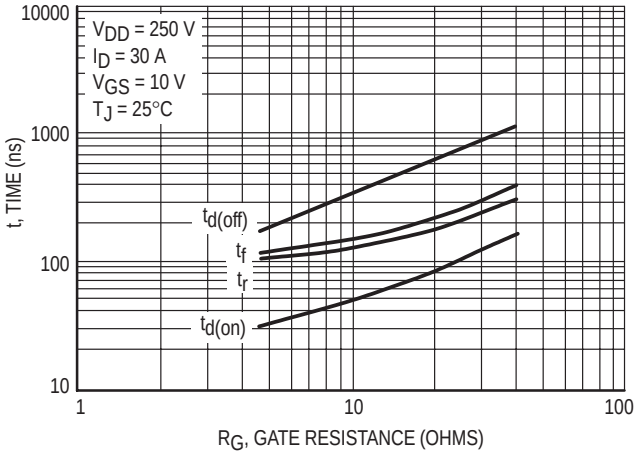


Figure 9. Resistive Switching Time Variation versus Gate Resistance

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

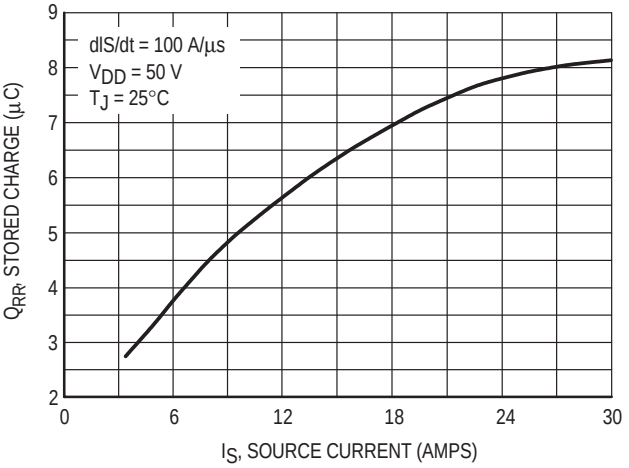


Figure 10. Stored Charge

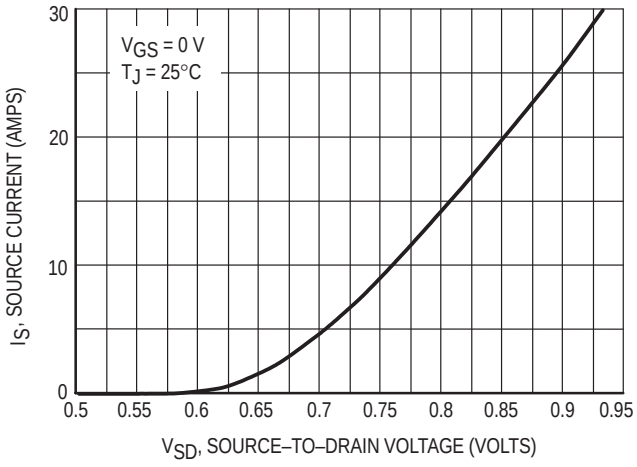


Figure 11. Diode Forward Voltage versus Current

SAFE OPERATING AREA

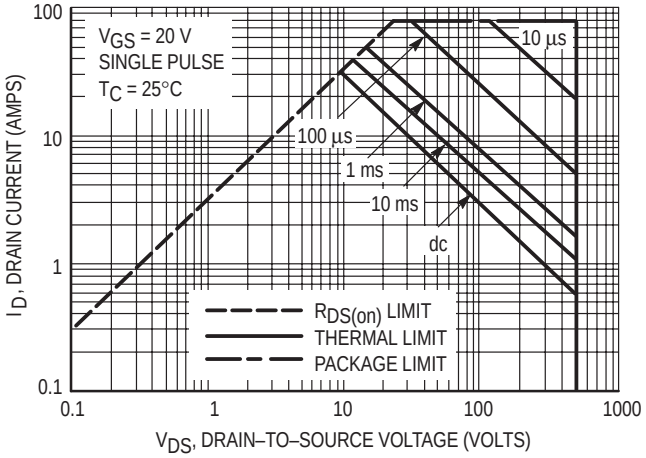


Figure 12. Maximum Rated Forward Biased Safe Operating Area

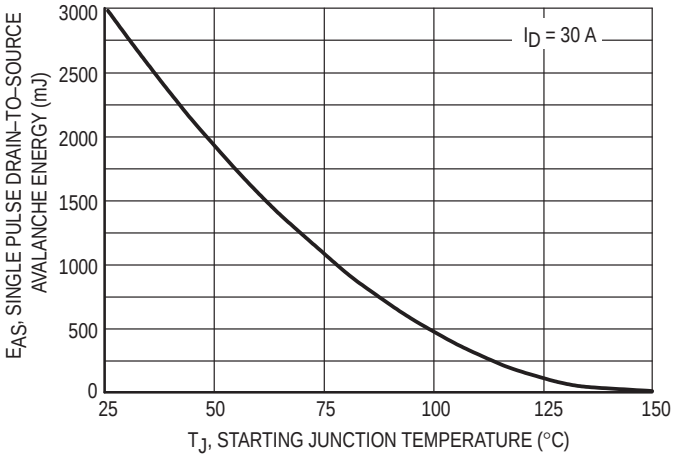


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

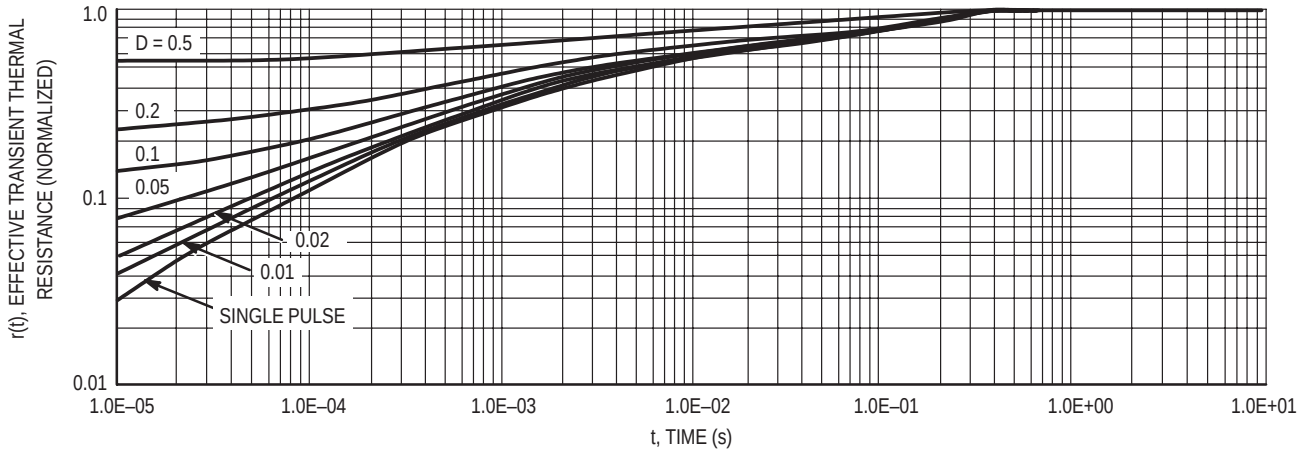


Figure 14. Thermal Response

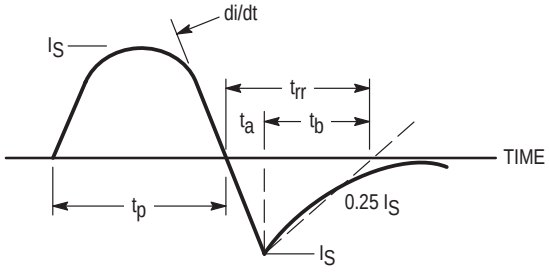


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

ISOTOP™ TMOS E-FET ™ Power Field Effect Transistor

N–Channel Enhancement–Mode Silicon Gate

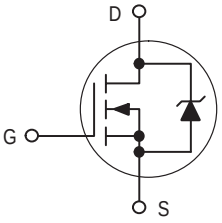
MTE53N50E

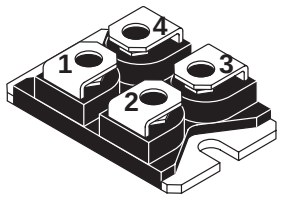
Motorola Preferred Device

TMOS POWER FET
53 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.080 OHM

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- 2500 V RMS Isolated Isotop Package
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- Very Low Internal Parasitic Inductance
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- U. L. Recognized, File #E69369





SOT–227B

1. Source
2. Gate
3. Drain
4. Source 2

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	53 33 210	Adc
Total Power Dissipation Derate above 25°C	P_D	460 3.70	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–40 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 53 Apk, L = 0.29 mH, R_G = 25Ω)	E_{AS}	400	mJ
RMS Isolation Voltage	V_{ISO}	2500	Vac
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.28 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)	$V_{(BR)DSS}$	500	560	—	Vdc
Temperature Coefficient (Positive)		—	550	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	200	nAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)	$V_{GS(th)}$	2.0	3.2	4.0	Vdc
Threshold Temperature Coefficient (Negative)		—	—	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 26.5 Adc)	$R_{DS(on)}$	—	63	80	mOhm
Drain–Source On–Voltage (V_{GS} = Vdc) (I_D = 53 Adc)	$V_{DS(on)}$	—	—	4.8	Vdc
(I_D = 26.5 Adc, T_J = 125°C)		—	—	4.3	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 26.5 Adc)	g_{FS}	25	45	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	14400	—	pF
Output Capacitance	C_{oss}	—	1560	—	
Reverse Transfer Capacitance	C_{rss}	—	240	—	
SWITCHING CHARACTERISTICS (2)					
Turn–On Delay Time (V_{DD} = 250 Vdc, I_D = 53 Adc, V_{GS} = 10 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	67	—	ns
Rise Time	t_r	—	322	—	
Turn–Off Delay Time	$t_{d(off)}$	—	362	—	
Fall Time	t_f	—	310	—	
Gate Charge (V_{DS} = 400 Vdc, I_D = 53 Adc, V_{GS} = 10 Vdc)	Q_T	—	474	—	nC
	Q_1	—	86	—	
	Q_2	—	206	—	
	Q_3	—	148	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (1) (I_S = 53 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.95	1.3	Vdc
(I_S = 53 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.90	—	
Reverse Recovery Time (I_S = 53 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	720	—	ns
	t_a	—	460	—	
	t_b	—	260	—	
Reverse Recovery Stored Charge	Q_{RR}	—	15	—	μC
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from contact screw on tab to center of die)	L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)		—	5.0	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to center of die)	L_S	—	5.0	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

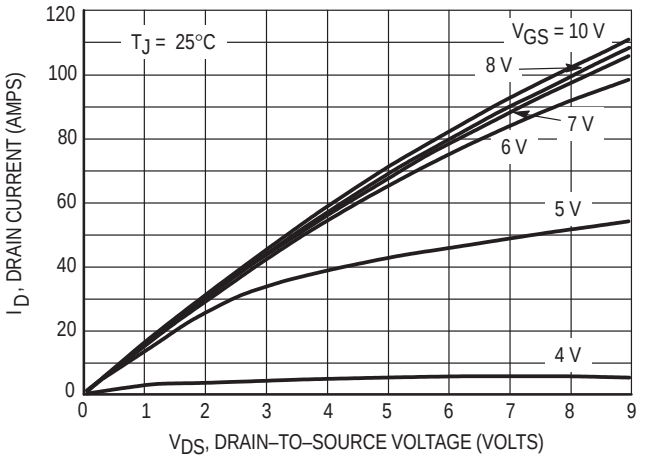


Figure 1. On–Region Characteristics

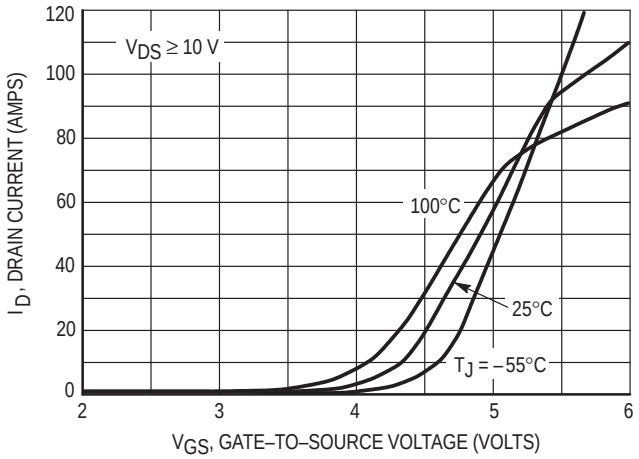


Figure 2. Transfer Characteristics

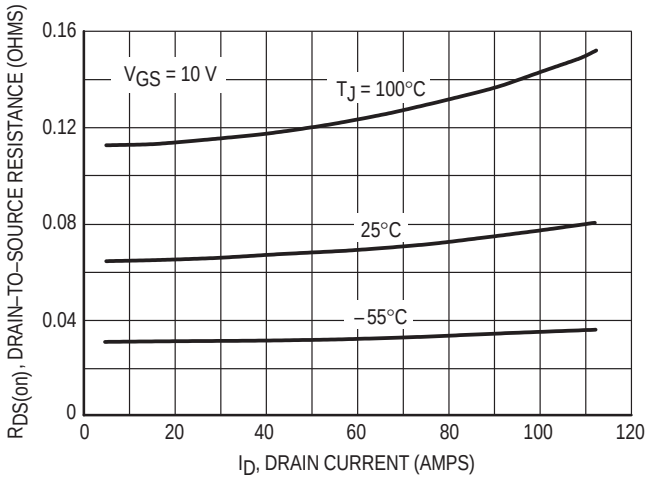


Figure 3. On–Resistance versus Drain Current and Temperature

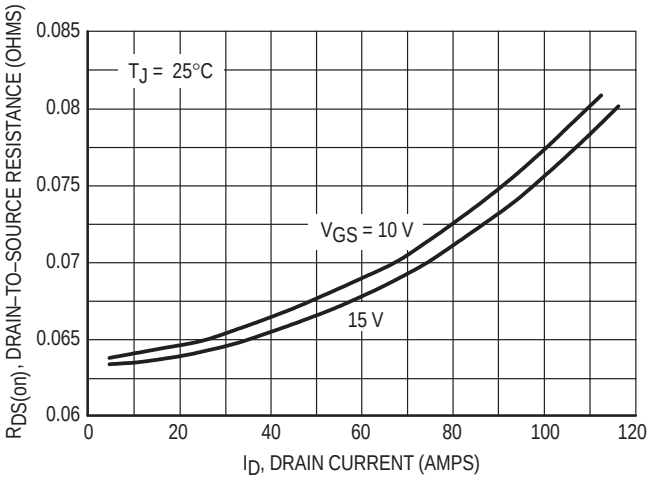


Figure 4. On–Resistance versus Drain Current and Gate Voltage

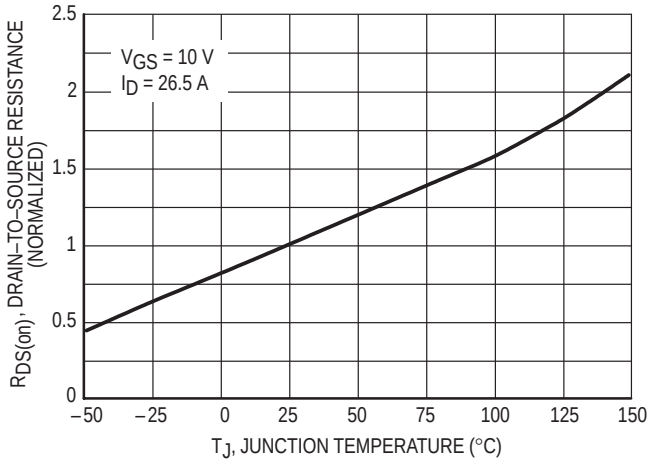


Figure 5. On–Resistance Variation with Temperature

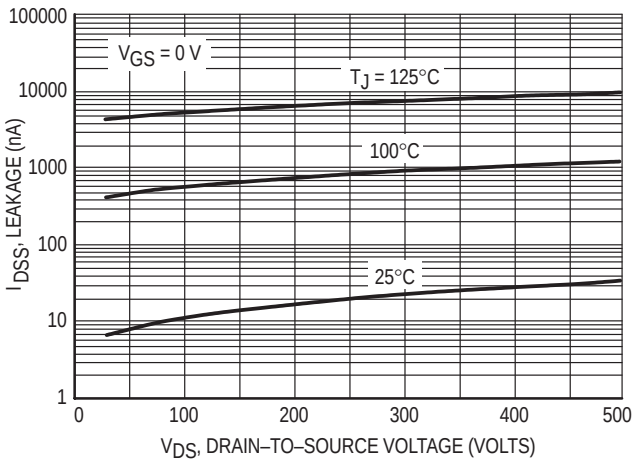


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

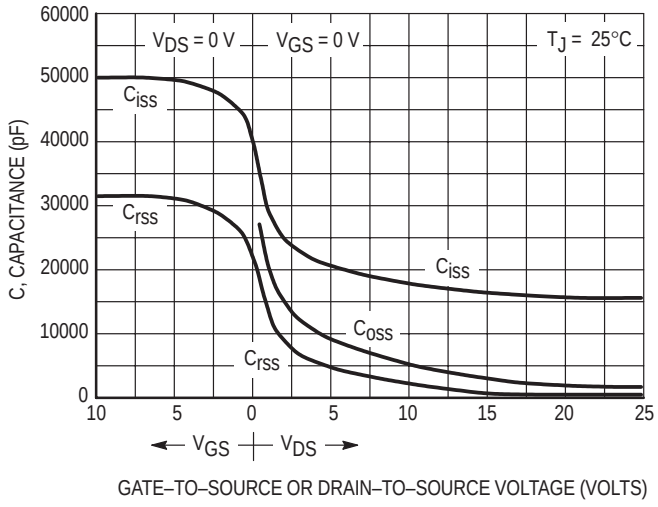


Figure 7. Capacitance Variation

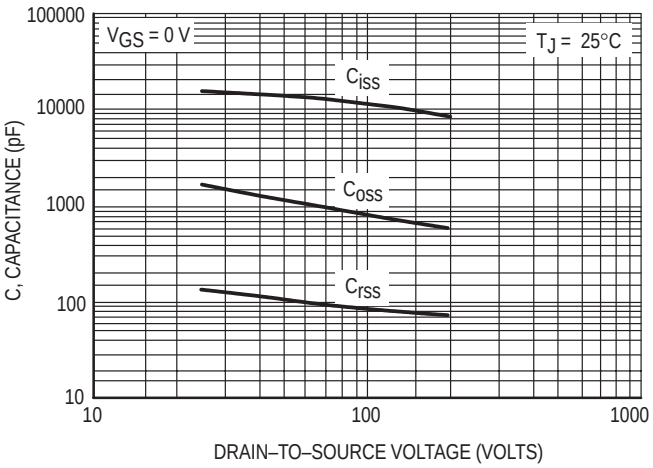


Figure 7b. High Voltage Capacitance Variation

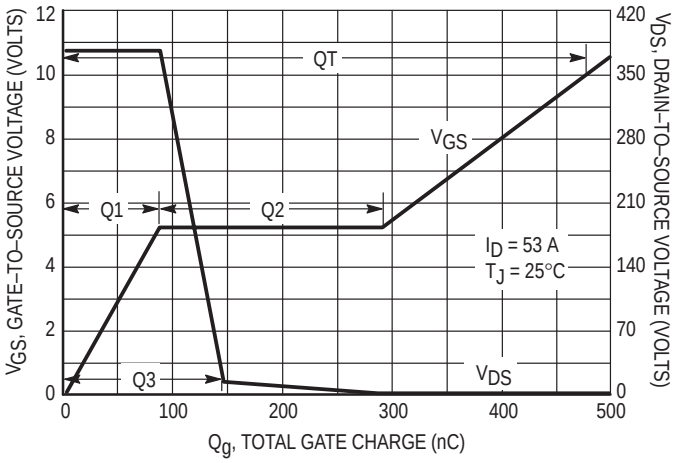


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

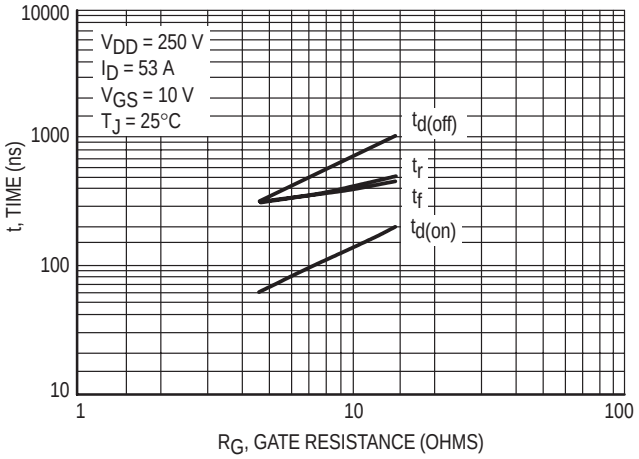


Figure 9. Resistive Switching Time Variation versus Gate Resistance

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

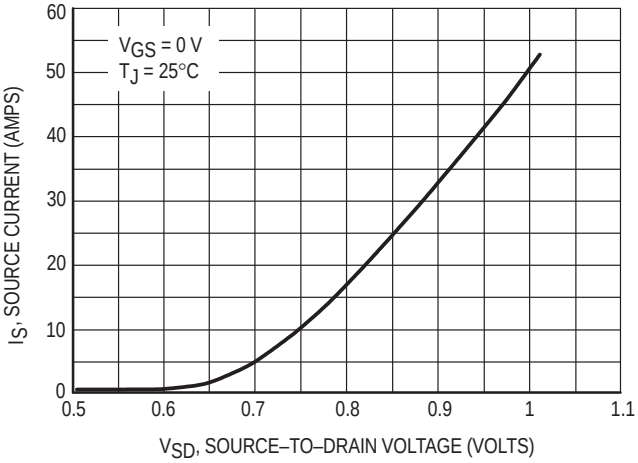


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

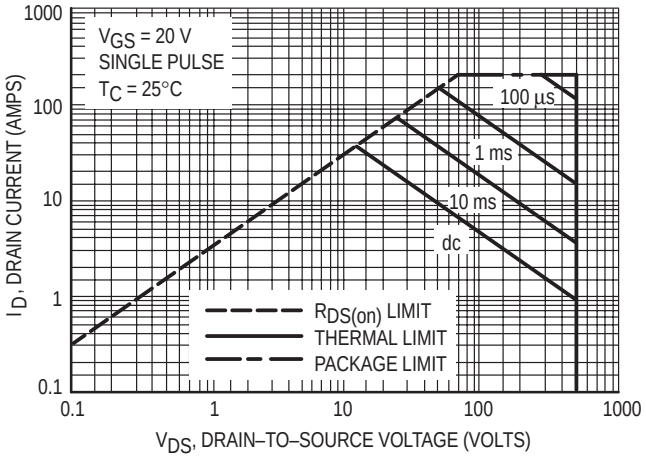


Figure 11. Maximum Rated Forward Biased Safe Operating Area

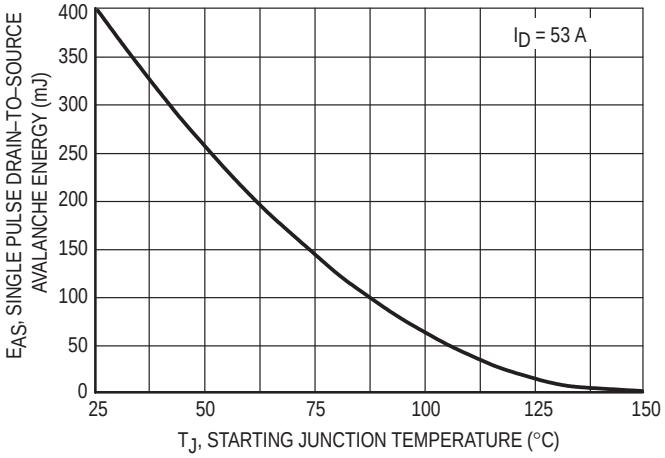


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

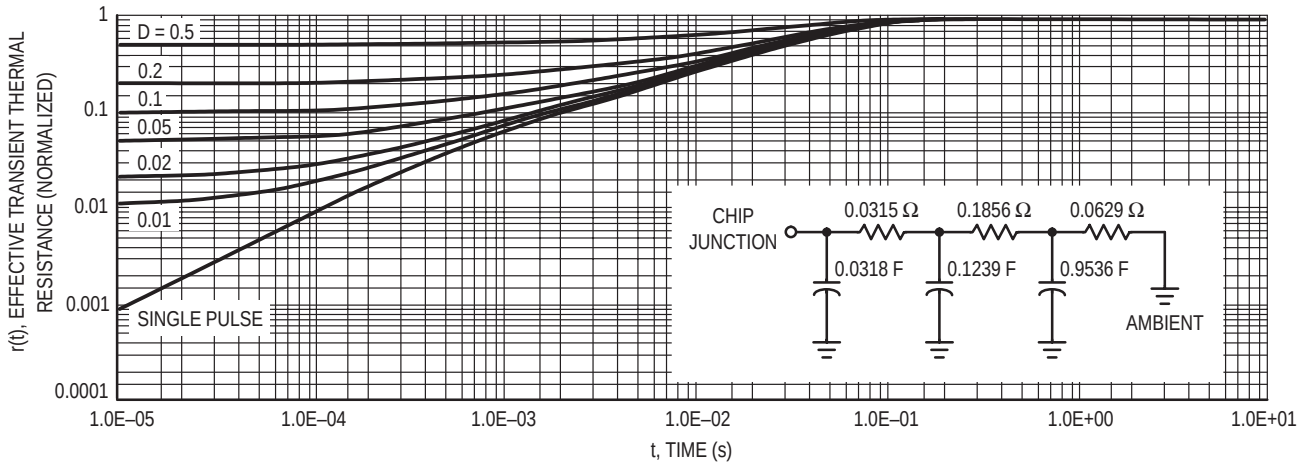


Figure 13. Thermal Response

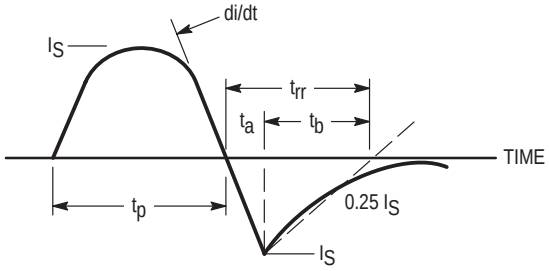


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

ISOTOP™ TMOS E-FET ™ Power Field Effect Transistor

N–Channel Enhancement–Mode Silicon Gate

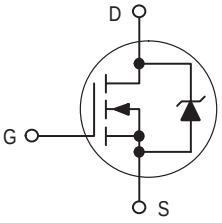
MTE125N20E

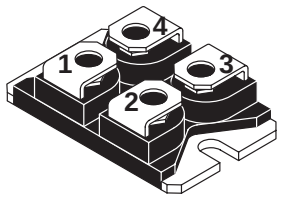
Motorola Preferred Device

TMOS POWER FET
125 AMPERES
200 VOLTS
$R_{DS(on)}$ = 0.015 OHM

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- 2500 V RMS Isolated Isotop Package
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- Very Low Internal Parasitic Inductance
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- U.L. Recognized, File #E69369





SOT–227B

1. Source
2. Gate
3. Drain
4. Source 2

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	200	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	Vdc
Gate–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	125 79 500	Adc
Total Power Dissipation Derate above 25°C	P_D	460 3.70	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–40 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, I_L = 125 Apk, L = 0.05mH, R_G = 25 Ω)	E_{AS}	400	mJ
RMS Isolation Voltage	V_{ISO}	2500	Vac
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.28 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	200	215	—	Vdc
Temperature Coefficient (Positive)			—	250	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	200	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	—	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 62.5 Adc)		$R_{DS(on)}$	—	12	15	mOhm
Drain–Source On–Voltage (V_{GS} = Vdc)		$V_{DS(on)}$				Vdc
(I_D = 125 Adc)			—	—	2.1	
(I_D = 62.5 Adc, T_J = 125°C)			—	—	1.9	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 62.5 Adc)		g_{FS}	50	80	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	14400	—	pF
Output Capacitance		C_{oss}	—	3600	—	
Reverse Transfer Capacitance		C_{rss}	—	920	—	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 125 Adc, V_{GS} = 10 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	72	—	ns
Rise Time		t_r	—	574	—	
Turn–Off Delay Time		$t_{d(off)}$	—	327	—	
Fall Time		t_f	—	376	—	
Gate Charge	(V_{DS} = 160 Vdc, I_D = 125 Adc, V_{GS} =10 Vdc)	Q_T	—	510	—	nC
		Q_1	—	100	—	
		Q_2	—	245	—	
		Q_3	—	158	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 125 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.00	1.5	Vdc
	(I_S = 125 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.00	—	
Reverse Recovery Time	(I_S = 125 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	310	—	ns
		t_a	—	220	—	
		t_b	—	90	—	
Reverse Recovery Stored Charge		Q_{RR}	—	9.2	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)			—	5.0	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	5.0	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
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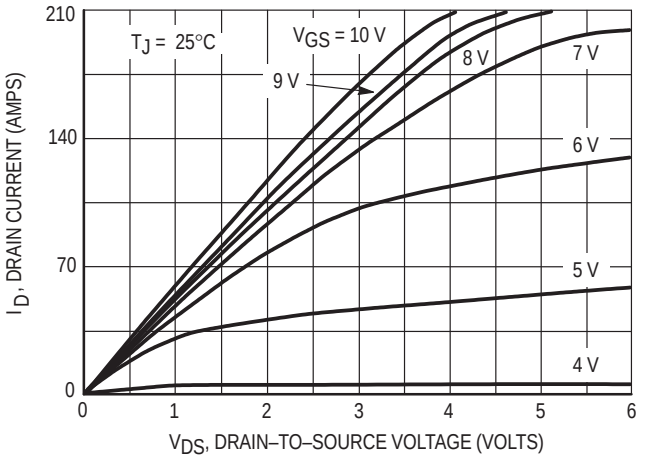
TYPICAL ELECTRICAL CHARACTERISTICS



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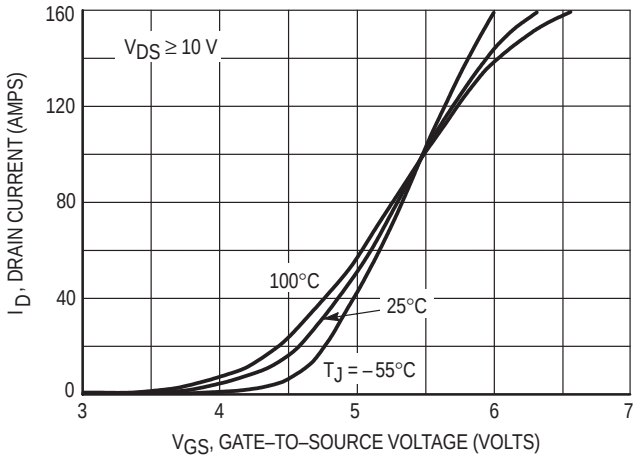

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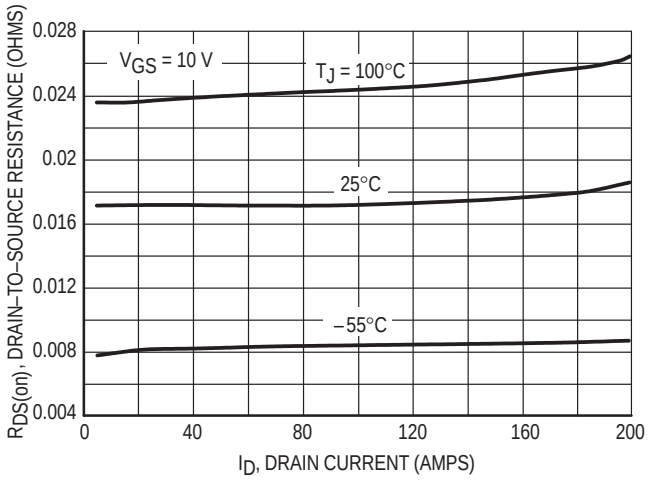

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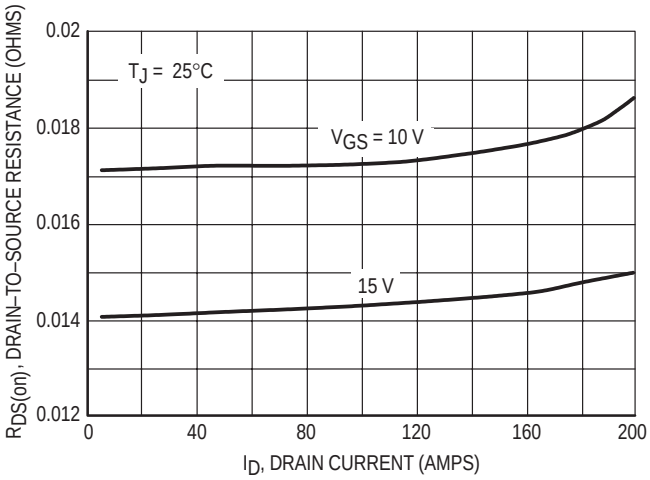

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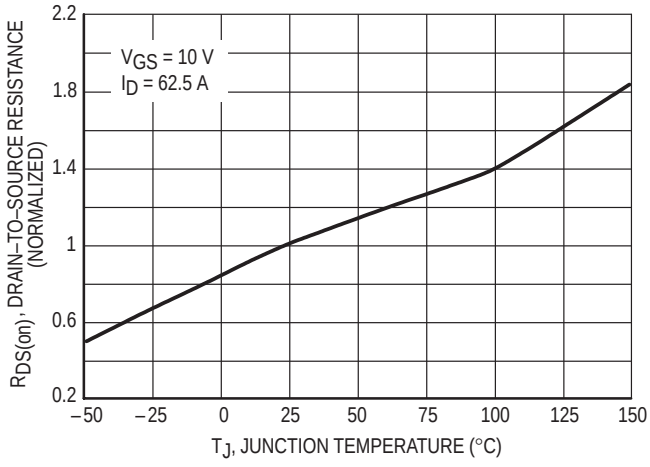

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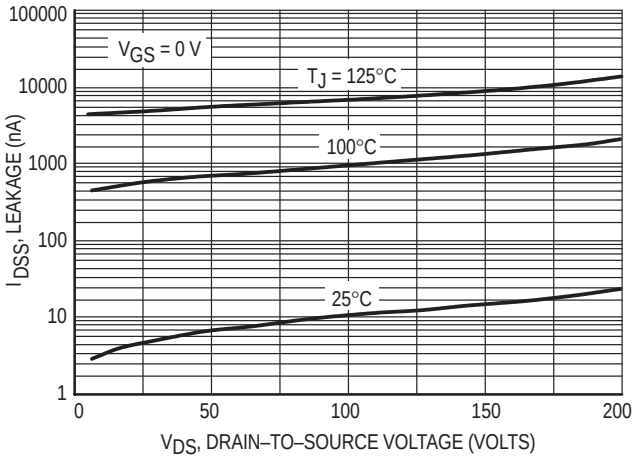

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where

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R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

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$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

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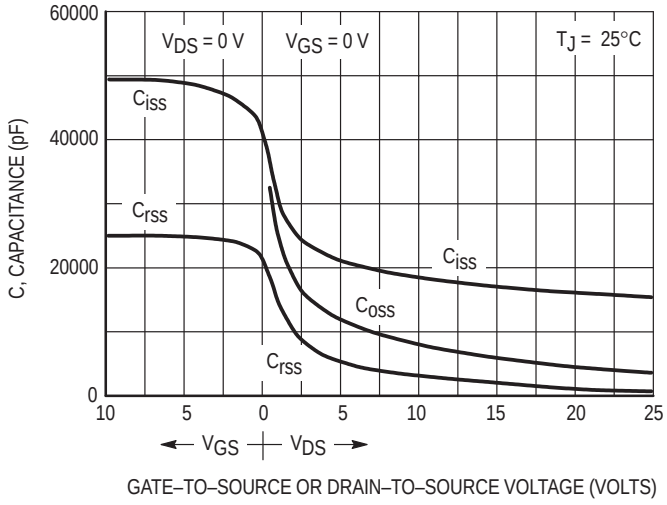


Figure 7. Capacitance Variation

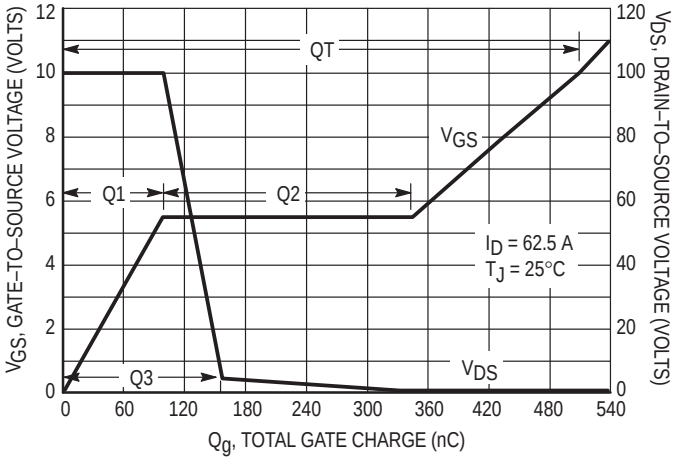


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

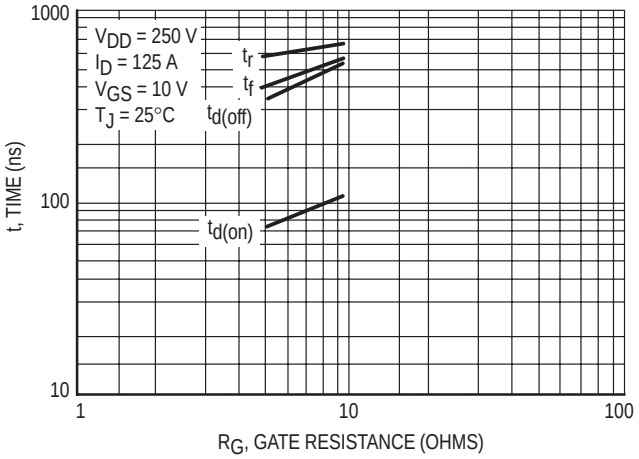


Figure 9. Resistive Switching Time Variation versus Gate Resistance

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

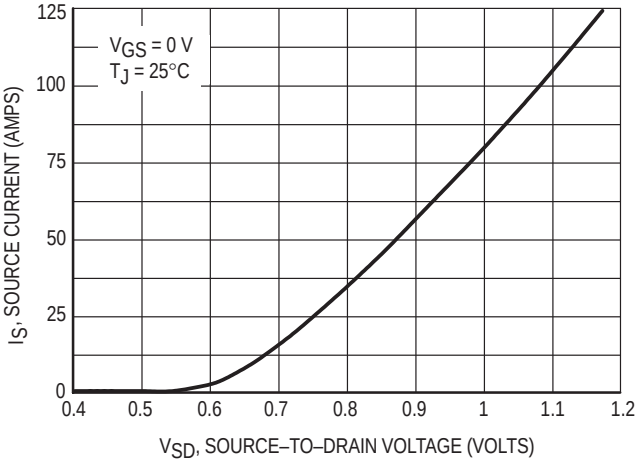


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

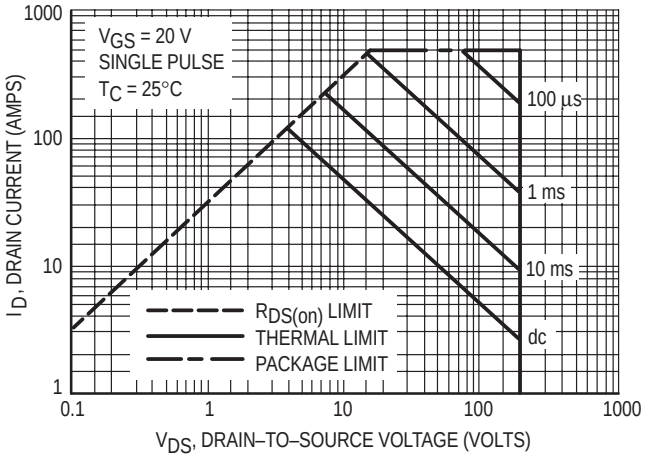


Figure 11. Maximum Rated Forward Biased Safe Operating Area

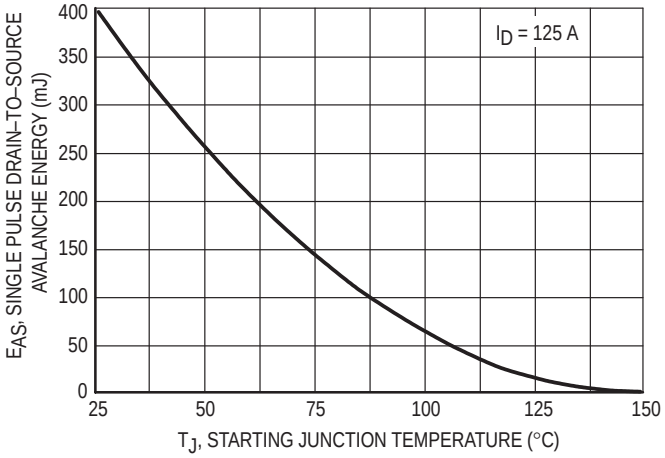


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

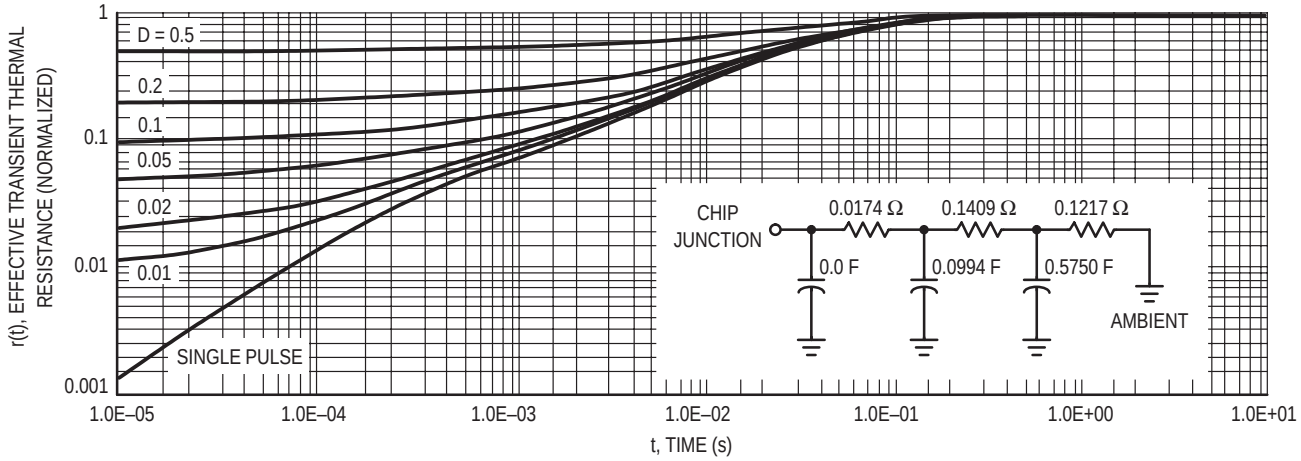


Figure 13. Thermal Response

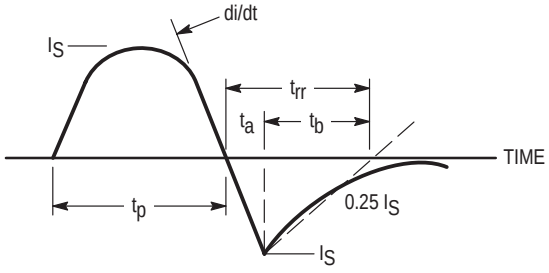


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

ISOTOP™ TMOS E-FET ™ Power Field Effect Transistor

N–Channel Enhancement–Mode Silicon Gate

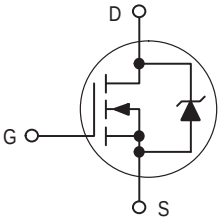
MTE215N10E

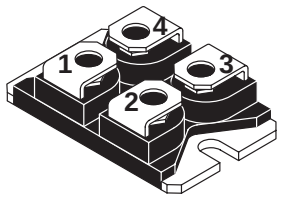
Motorola Preferred Device

TMOS POWER FET
215 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.0055 OHM

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- 2500 V RMS Isolated Isotop Package
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- Very Low Internal Parasitic Inductance
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- U. L. Recognized, File #E69369





SOT–227B

1. Source
2. Gate
3. Drain
4. Source 2

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	100	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	215 136 860	Adc
Total Power Dissipation Derate above 25°C	P_D	460 3.70	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–40 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 215 Apk, L = 0.017 mH, R_G = 25 Ω,)	E_{AS}	400	mJ
RMS Isolation Voltage	V_{ISO}	2500	Vac
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.28 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	100	110	—	Vdc
Temperature Coefficient (Positive)			—	120	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	200	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	—	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 107.5 Adc)		$R_{DS(on)}$	—	4.6	5.5	mOhm
Drain–Source On–Voltage (V_{GS} = Vdc)		$V_{DS(on)}$				Vdc
(I_D = 215 Adc)			—	—	1.5	
(I_D = 107.5 Adc, T_J = 125°C)			—	—	1.2	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 107.5 Adc)		g_{FS}	100	140	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	15200	—	pF
Output Capacitance		C_{oss}	—	6600	—	
Reverse Transfer Capacitance		C_{rss}	—	2400	—	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 50 Vdc, I_D = 215 Adc, V_{GS} = 10 Vdc, R_G = 5.0 Ω)	$t_{d(on)}$	—	48	—	ns
Rise Time		t_r	—	490	—	
Turn–Off Delay Time		$t_{d(off)}$	—	186	—	
Fall Time		t_f	—	384	—	
Gate Charge	(V_{DS} = 80 Vdc, I_D = 215 Adc, V_{GS} =10 Vdc)	Q_T	—	540	—	nC
		Q_1	—	104	—	
		Q_2	—	300	—	
		Q_3	—	440	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 215 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.5	Vdc
	(I_S = 215 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.2	—	
Reverse Recovery Time	(I_S = 215 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	145	—	ns
		t_a	—	90	—	
		t_b	—	55	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4.6	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)			—	5.0	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source pad)		L_S	—	5.0	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

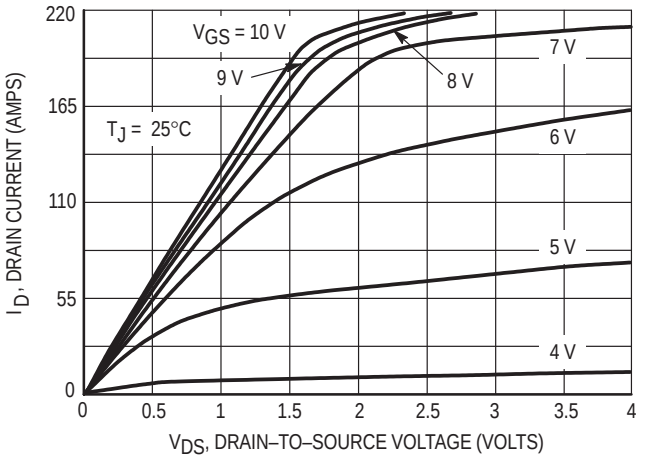


Figure 1. On–Region Characteristics

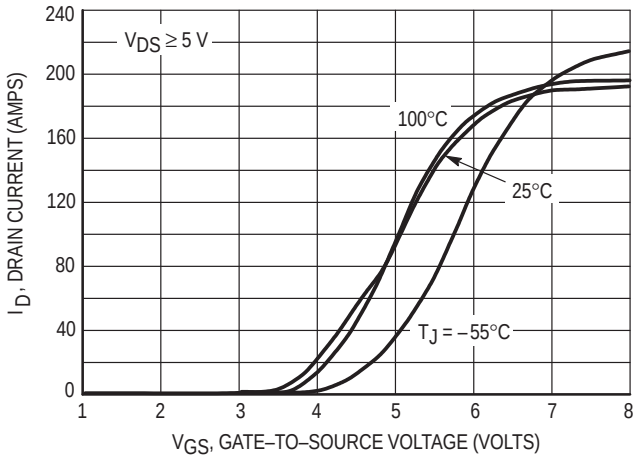


Figure 2. Transfer Characteristics

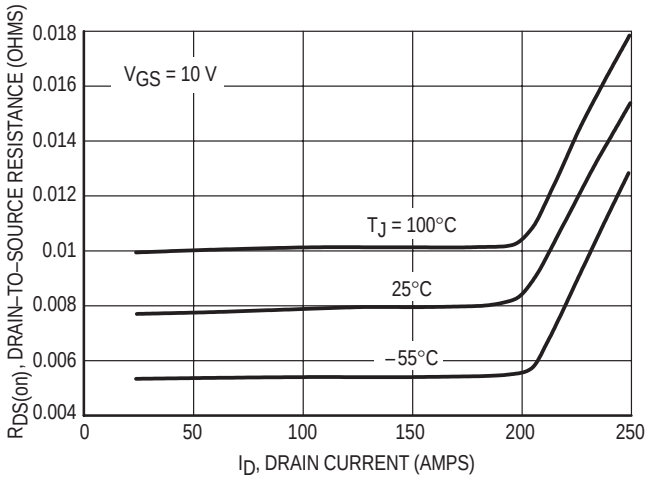


Figure 3. On–Resistance versus Drain Current and Temperature

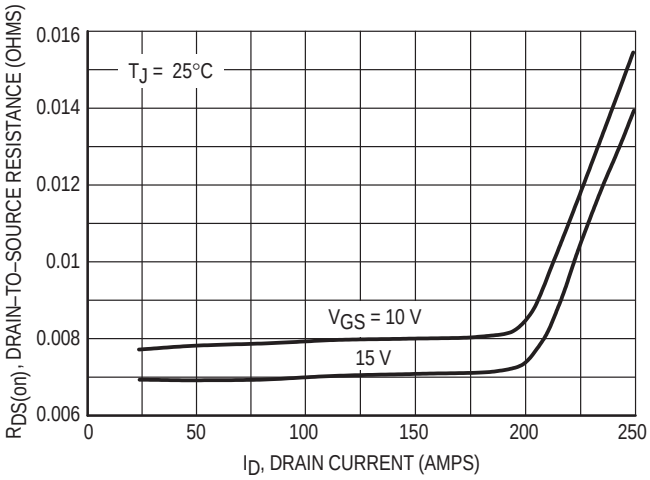


Figure 4. On–Resistance versus Drain Current and Gate Voltage

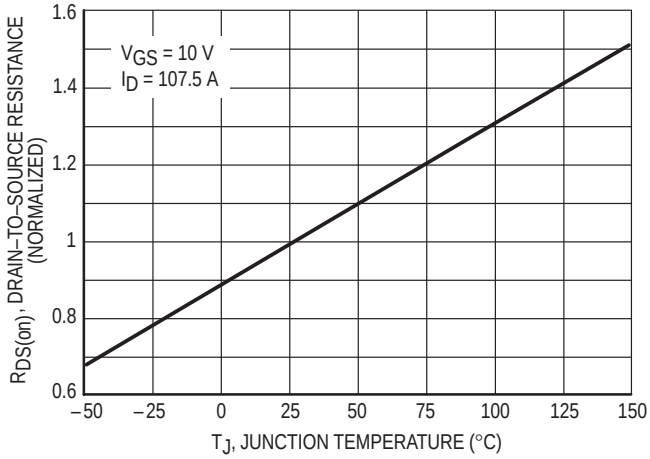


Figure 5. On–Resistance Variation with Temperature

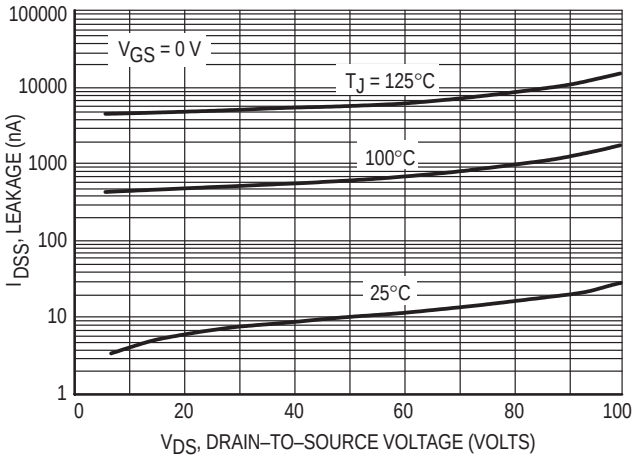


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

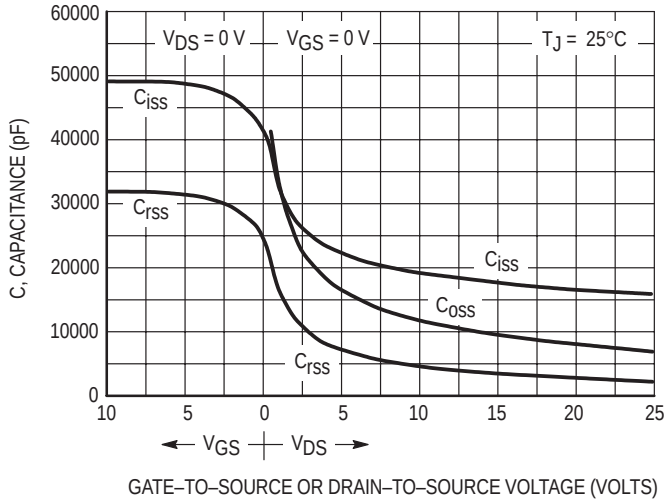


Figure 7. Capacitance Variation

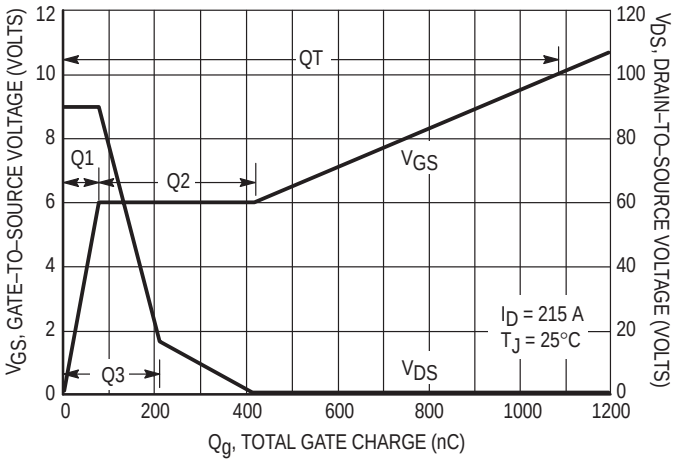


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

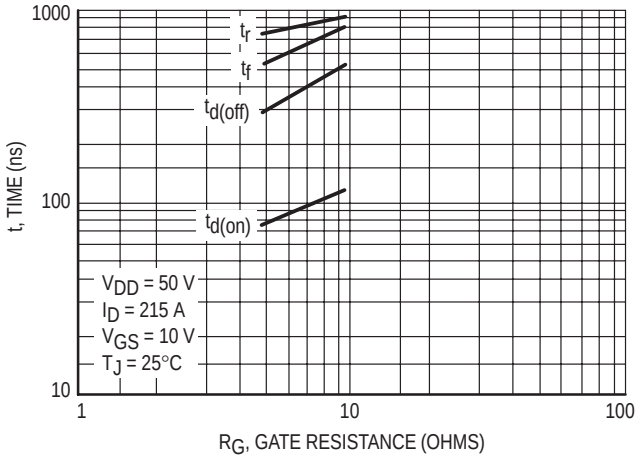


Figure 9. Resistive Switching Time Variation versus Gate Resistance

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

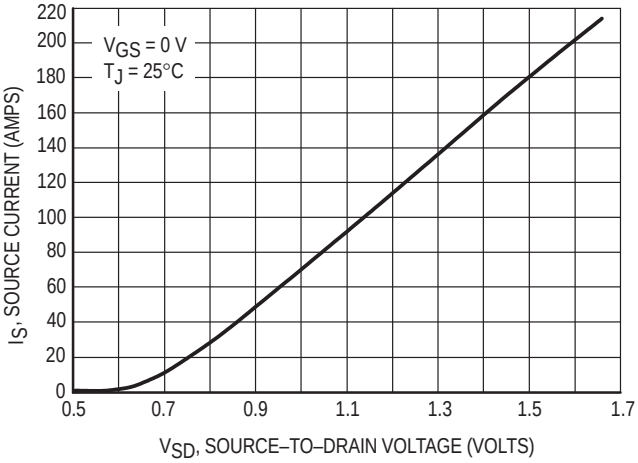


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

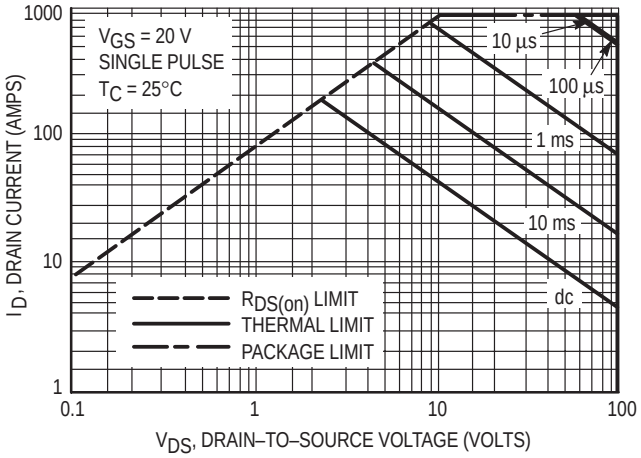


Figure 11. Maximum Rated Forward Biased Safe Operating Area

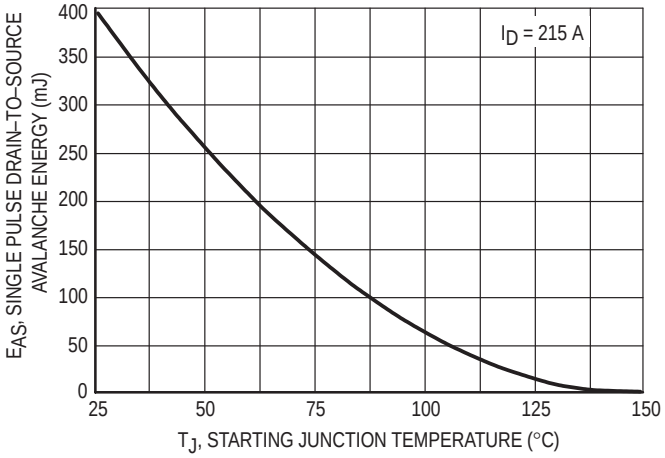


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

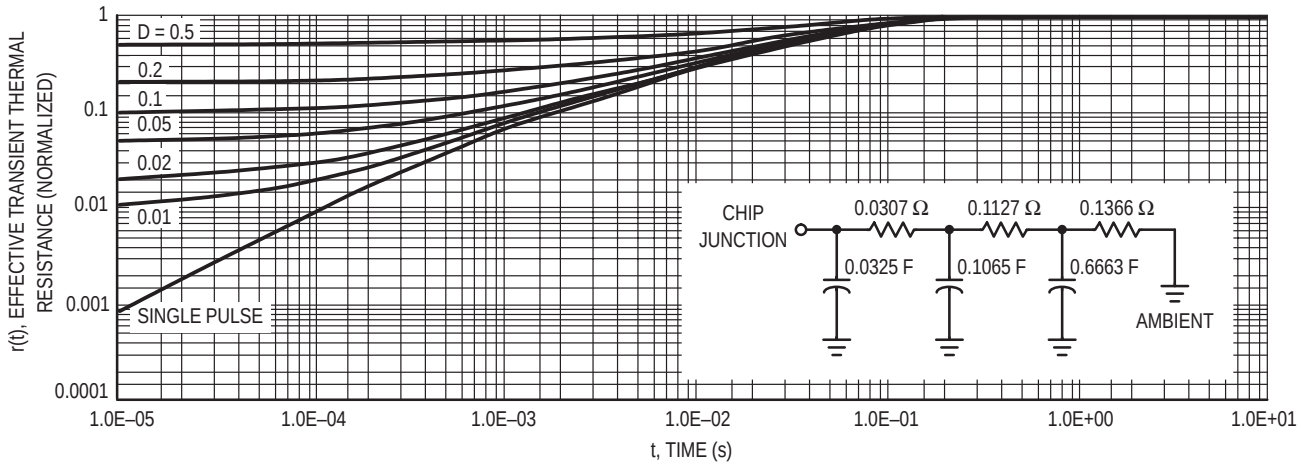


Figure 13. Thermal Response

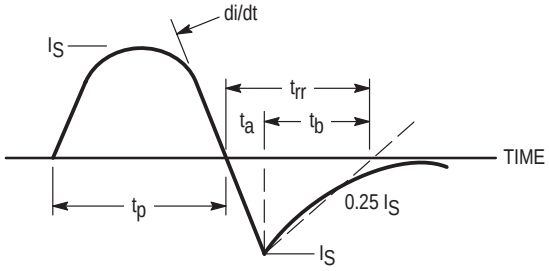


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

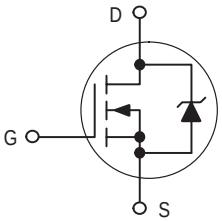
MTP1N50E

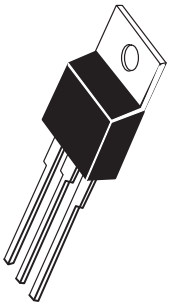
Motorola Preferred Device

TMOS POWER FET
1.0 AMPERES
500 VOLTS
$R_{DS(on)}$ = 5.0 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	1.0 0.8 3.0	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} =10 Vdc, I_L = 3.0 Apk, L =10 mH, R_G = 25 Ω)	E_{AS}	45	mJ
Thermal Resistance — Junction to Case — Junction to Ambient, when surface mounted using minimum recommended pad size	 $R_{\theta JC}$ $R_{\theta JA}$	 3.13 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	500 —	— 480	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125 °C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.2 6.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$R_{DS(on)}$	—	4.3	5.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 1 .0 Adc) (I_D = 0.5 Adc, T_J = 125 °C)		$V_{DS(on)}$	— —	4.5 —	6.0 5.30	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 0.5 Adc)		g_{FS}	0.5	0.9	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	215	315	pF
Output Capacitance		C_{oss}	—	30.2	42	
Reverse Transfer Capacitance		C_{rss}	—	6.7	12	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.0	20	ns
Rise Time		t_r	—	9.0	10	
Turn–Off Delay Time		$t_{d(off)}$	—	14	30	
Fall Time		t_f	—	17	30	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	7.4	9.0	nC
		Q_1	—	1.6	—	
		Q_2	—	3.8	—	
		Q_3	—	5	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc) (I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 125 °C)	V_{SD}	— —	0.81 0.68	1.2 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	145	—	ns
		t_a	—	85	—	
		t_b	—	60	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.702	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

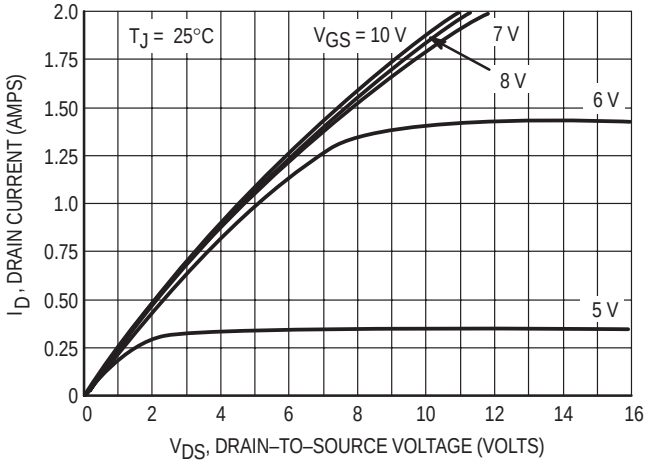


Figure 1. On–Region Characteristics

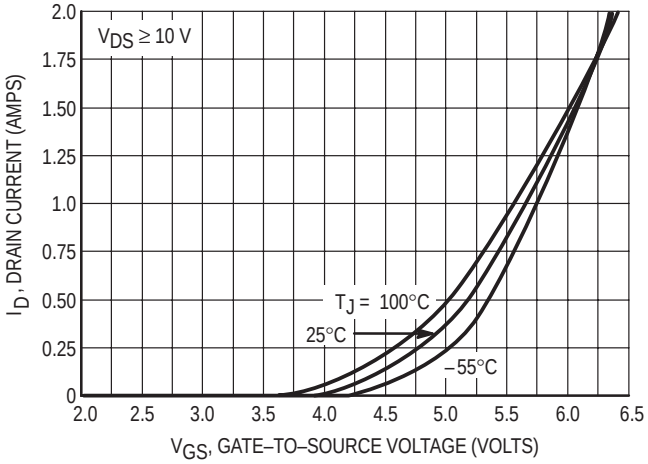


Figure 2. Transfer Characteristics

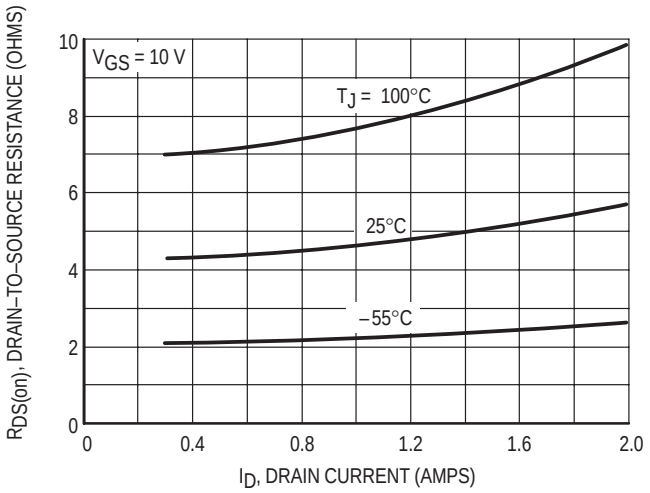


Figure 3. On–Resistance versus Drain Current and Temperature

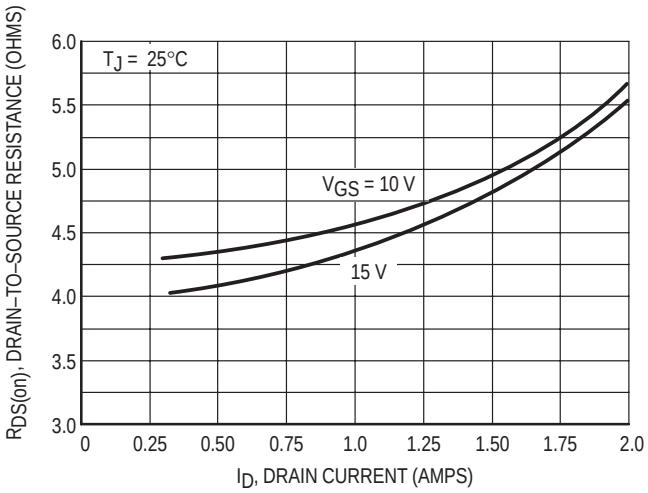


Figure 4. On–Resistance versus Drain Current and Gate Voltage

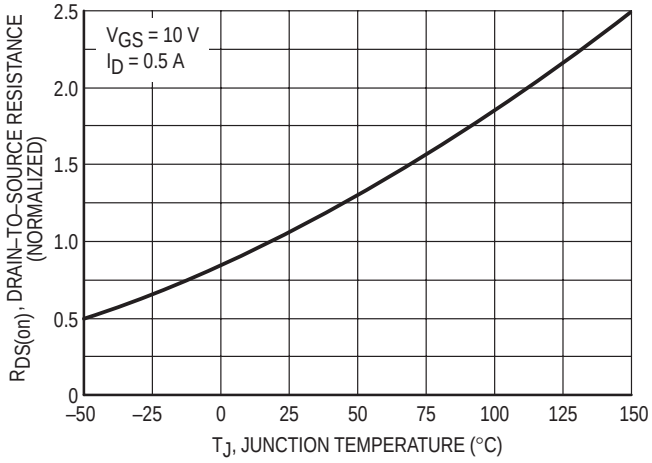


Figure 5. On–Resistance Variation with Temperature

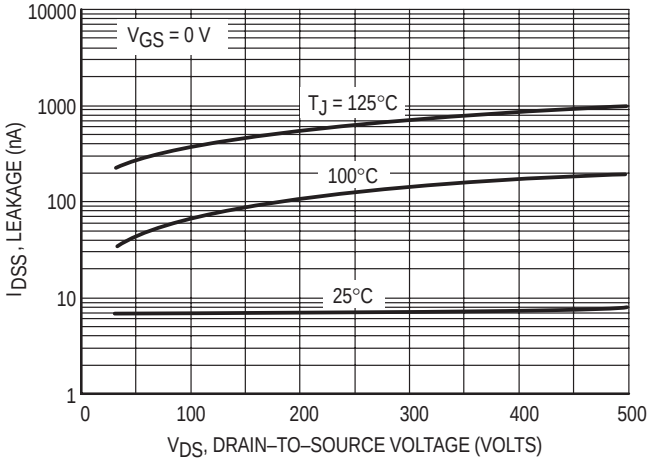


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

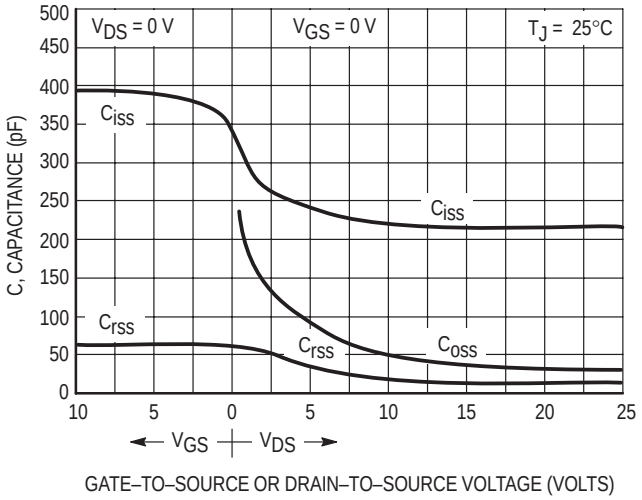


Figure 7a. Capacitance Variation

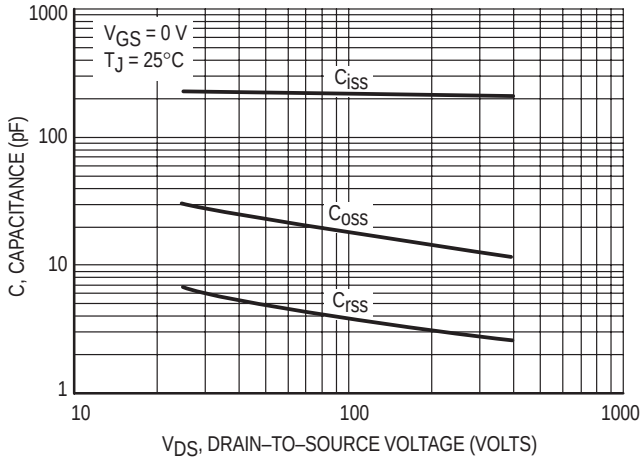


Figure 7b. High Voltage Capacitance Variation

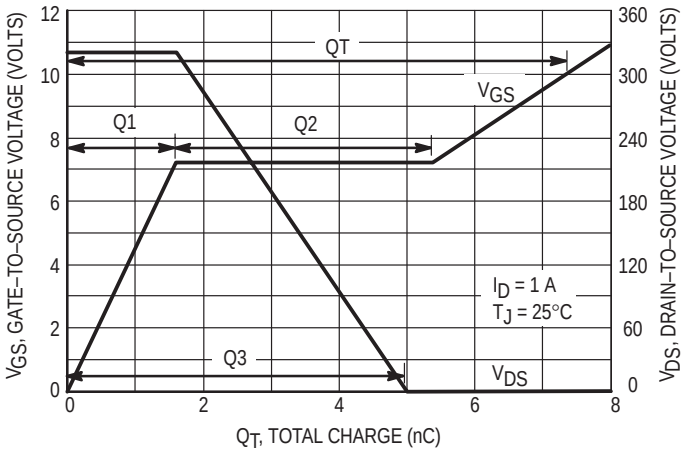


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

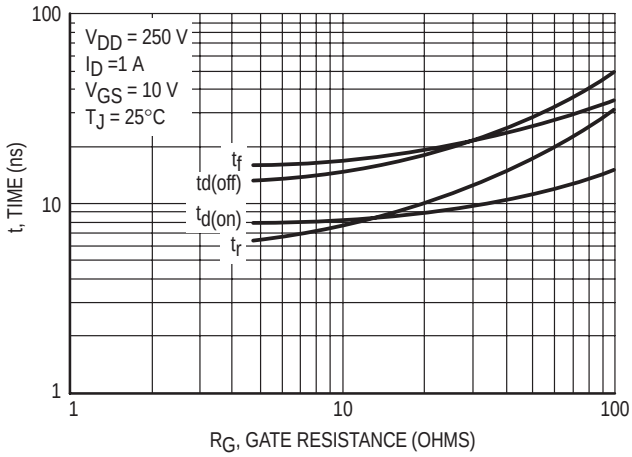


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

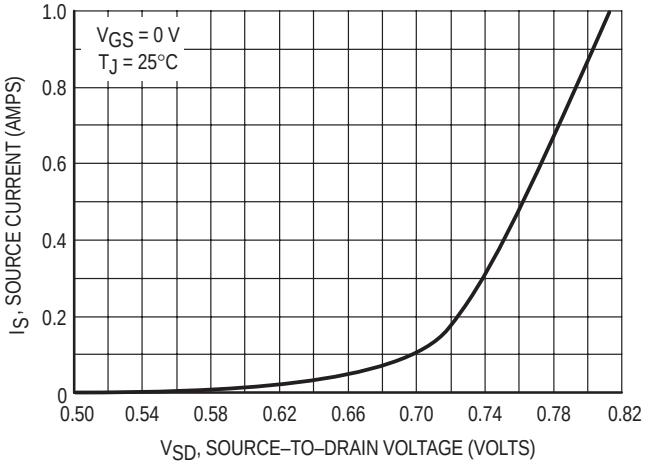


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

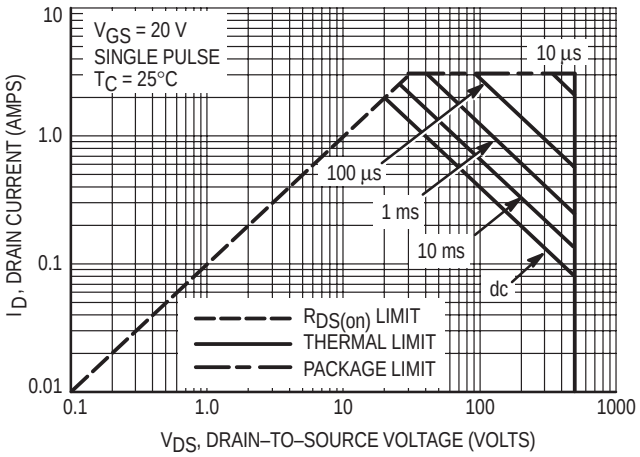


Figure 11. Maximum Rated Forward Biased Safe Operating Area

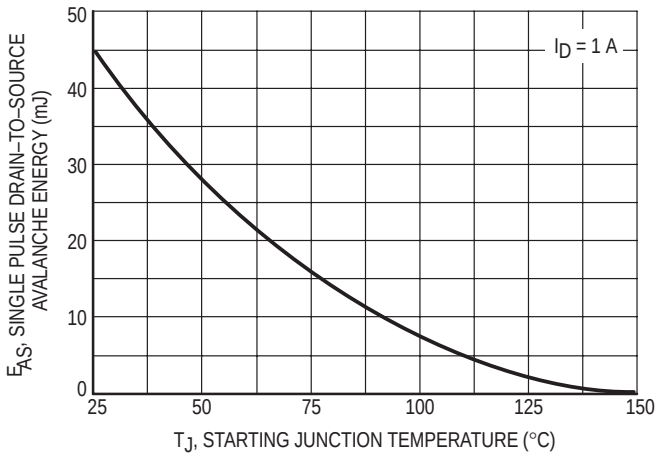


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

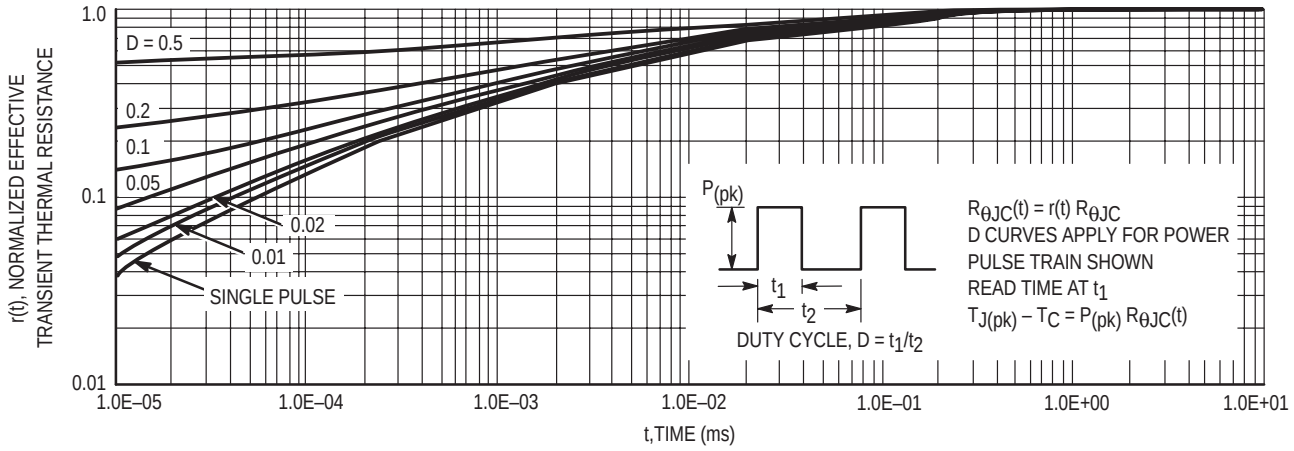


Figure 13. Thermal Response

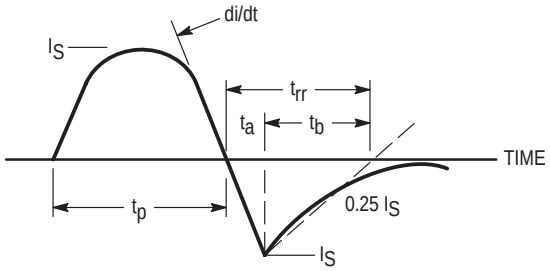


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

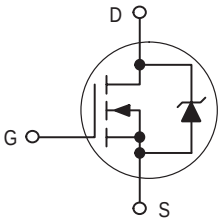
MTP1N60E

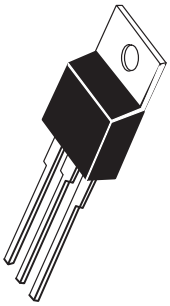
Motorola Preferred Device

TMOS POWER FET
1.0 AMPERES
600 VOLTS
$R_{DS(on)}$ = 8.0 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	600	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	1.0 0.8 3.0	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.50 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	689	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 600 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	7.1	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$R_{DS(on)}$	—	5.9	8.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 1.0 Adc)		$V_{DS(on)}$	—	6.4	9.6	Vdc
(I_D = 0.5 Adc, T_J = 125°C)			—	—	8.4	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 0.5 Adc)		g_{FS}	0.5	0.8	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	224	310	pF
Output Capacitance		C_{oss}	—	27	40	
Reverse Transfer Capacitance		C_{rss}	—	6.0	10	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 300 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.8	17.6	ns
Rise Time		t_r	—	6.8	13.6	
Turn–Off Delay Time		$t_{d(off)}$	—	15	30	
Fall Time		t_f	—	20	40	
Gate Charge (See Figure 8)	(V_{DS} = 300 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	7.1	10	nC
		Q_1	—	1.7	—	
		Q_2	—	3.2	—	
		Q_3	—	3.9	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.82	1.4	Vdc
	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.7	—	
Reverse Recovery Time (See Figure 14)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	464	—	ns
		t_a	—	36	—	
		t_b	—	428	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.629	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

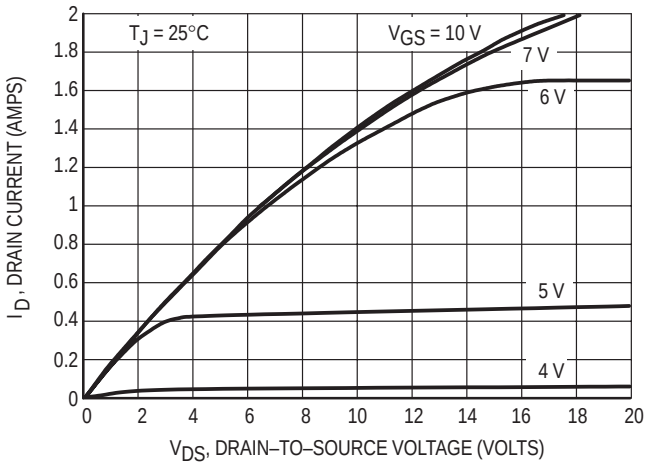


Figure 1. On–Region Characteristics

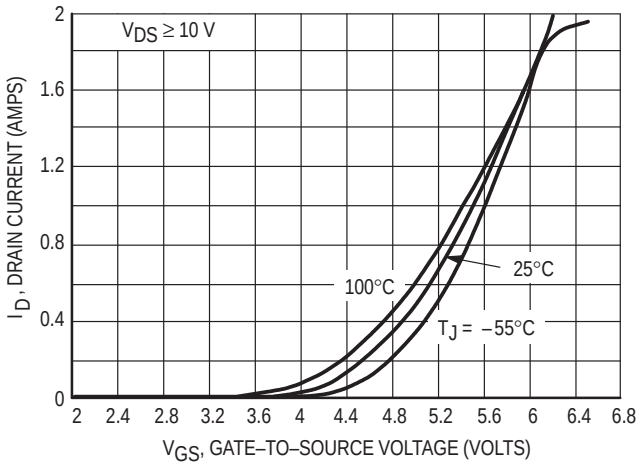


Figure 2. Transfer Characteristics

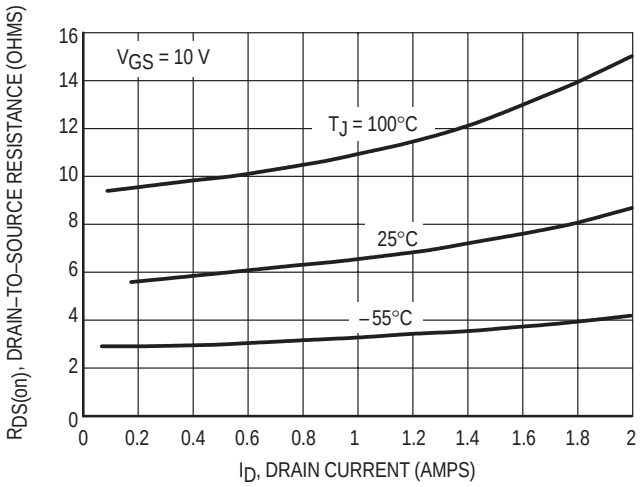


Figure 3. On–Resistance versus Drain Current and Temperature

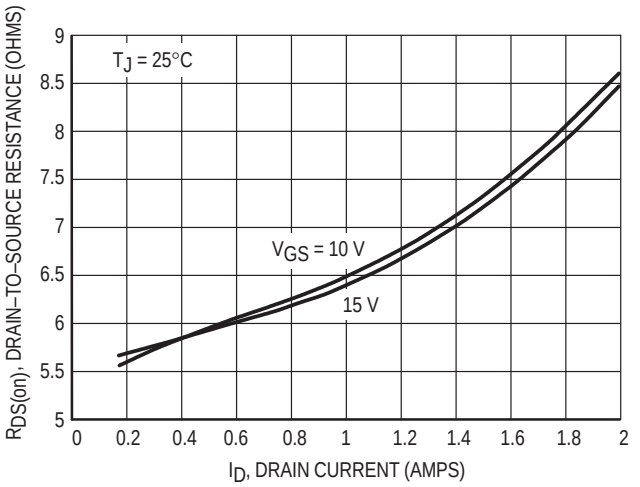


Figure 4. On–Resistance versus Drain Current and Gate Voltage

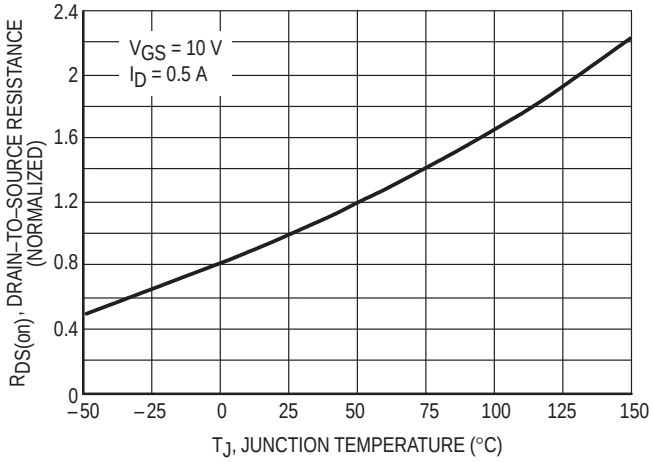


Figure 5. On–Resistance Variation with Temperature

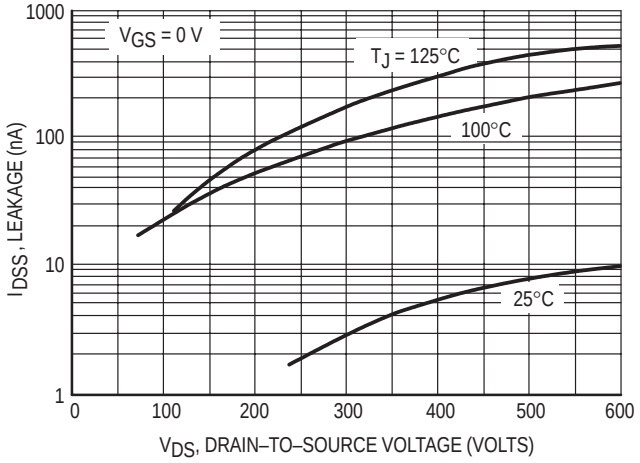


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

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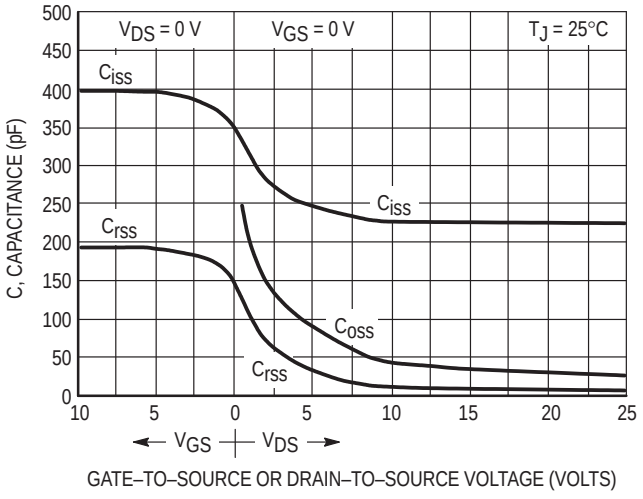


Figure 7a. Capacitance Variation

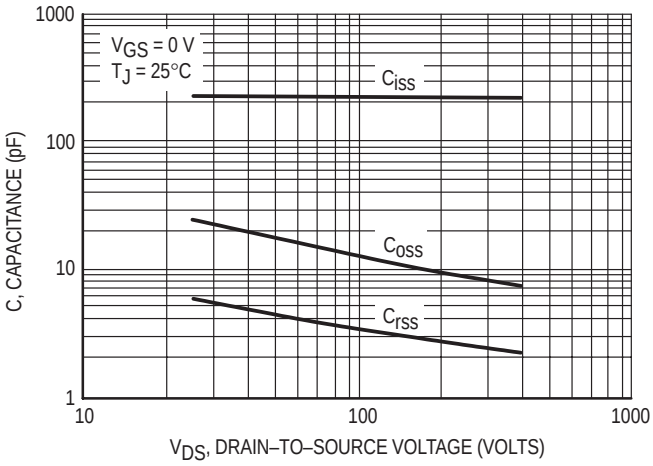


Figure 7b. High Voltage Capacitance Variation

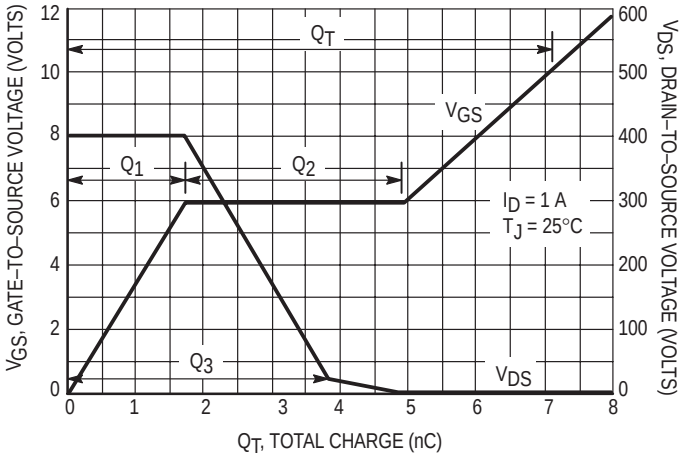


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

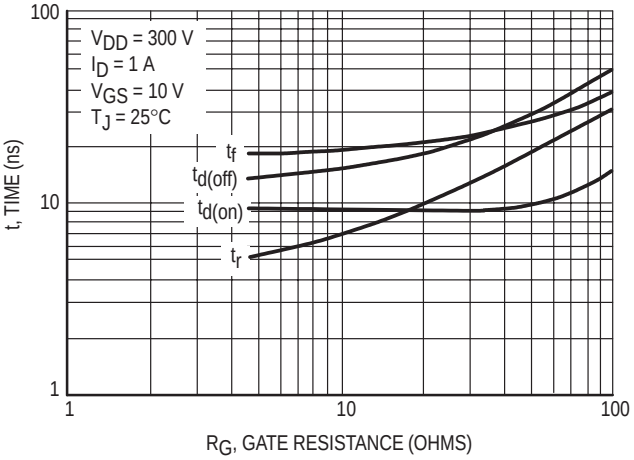


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

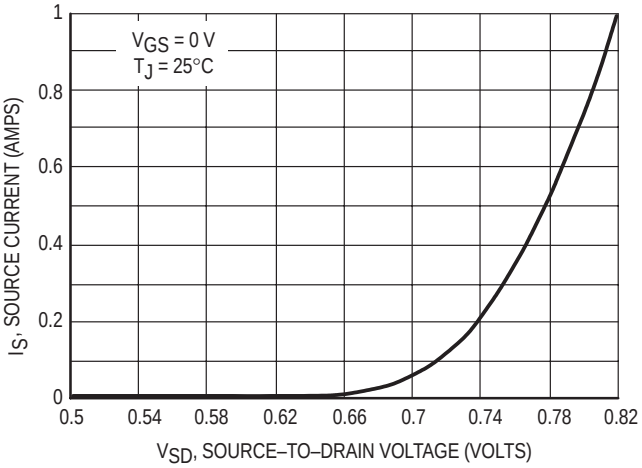


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

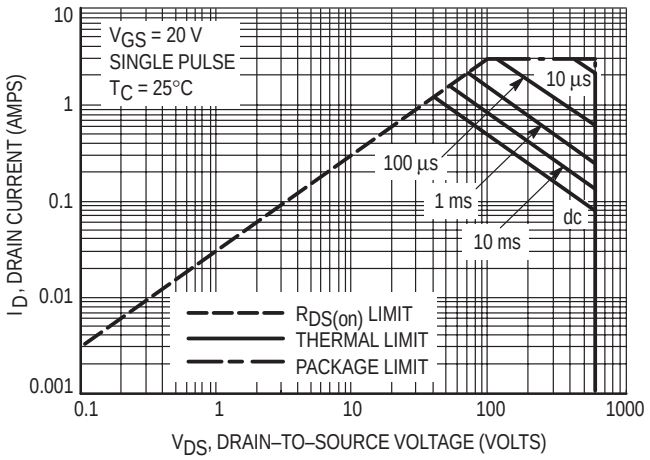


Figure 11. Maximum Rated Forward Biased Safe Operating Area

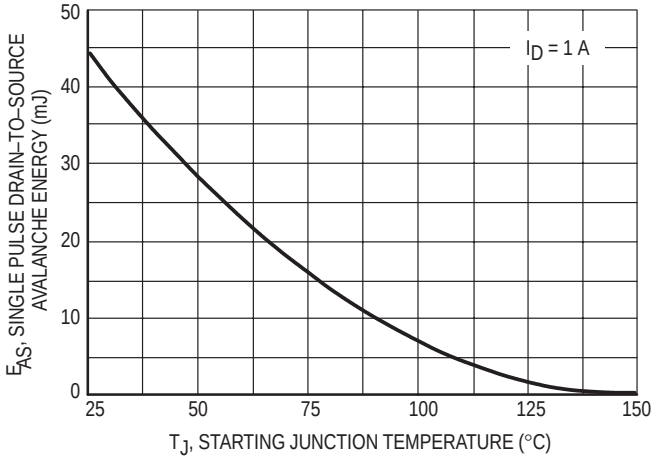


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

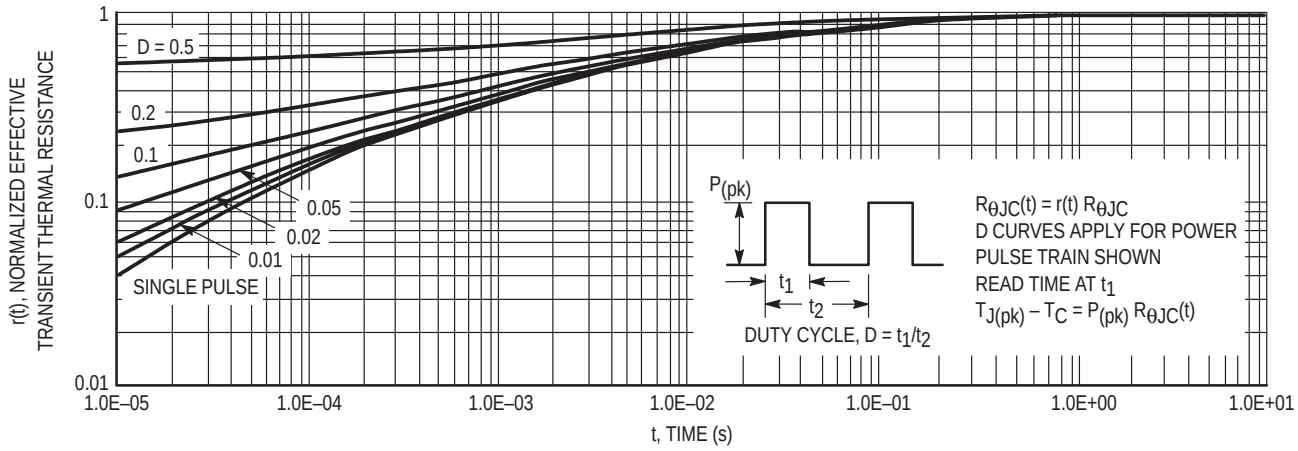


Figure 13. Thermal Response

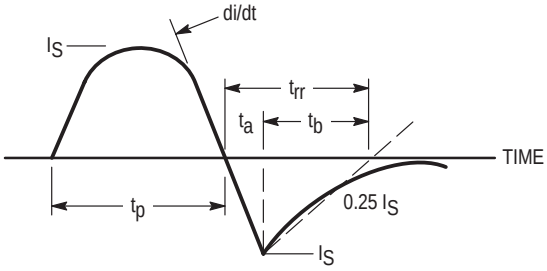


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet
TMOS E-FET ™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

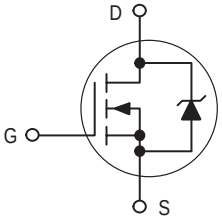
MTP1N80E

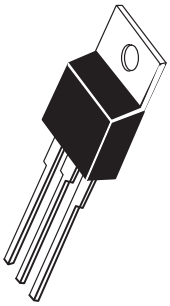
Motorola Preferred Device

TMOS POWER FET
1.0 AMPERES
800 VOLTS
$R_{DS(on)}$ = 12 OHMS

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	800	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	800	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	1.0 0.8 4.0	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	48 0.38	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 2.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	20	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.63 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	800	—	—	Vdc
Temperature Coefficient (Positive)			—	0.981	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 800 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 800 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.3	4.0	Vdc
Temperature Coefficient (Negative)			—	6.3	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$R_{DS(on)}$	—	10.3	12	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$V_{DS(on)}$	—	11	14.4	Vdc
(V_{GS} = 10 Vdc, I_D = 0.5 Adc, T_J = 125°C)			—	—	12.6	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 0.5 Adc)		g_{FS}	0.4	1.4	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	297	420	pF
Output Capacitance		C_{oss}	—	29	40	
Reverse Transfer Capacitance		C_{rss}	—	6.0	10	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	9.0	20	ns
Rise Time		t_r	—	10	20	
Turn–Off Delay Time		$t_{d(off)}$	—	20	40	
Fall Time		t_f	—	27	50	
Gate Charge	(V_{DS} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	9.6	14	nC
		Q_1	—	2.1	—	
		Q_2	—	4.2	—	
		Q_3	—	4.7	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.82	1.2	Vdc
	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.7	—	
Reverse Recovery Time	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	317	—	ns
		t_a	—	56	—	
		t_b	—	261	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.98	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

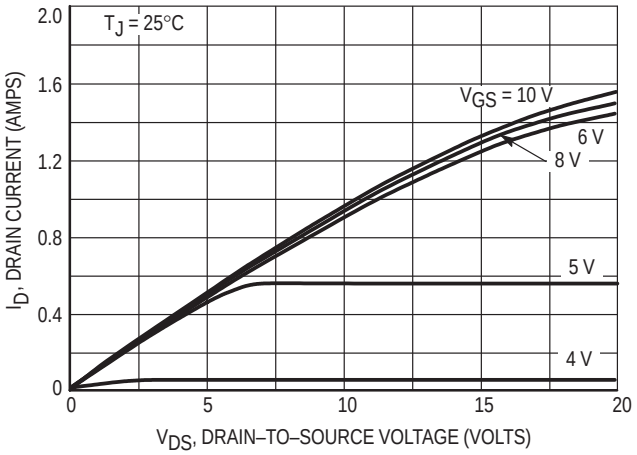


Figure 1. On–Region Characteristics

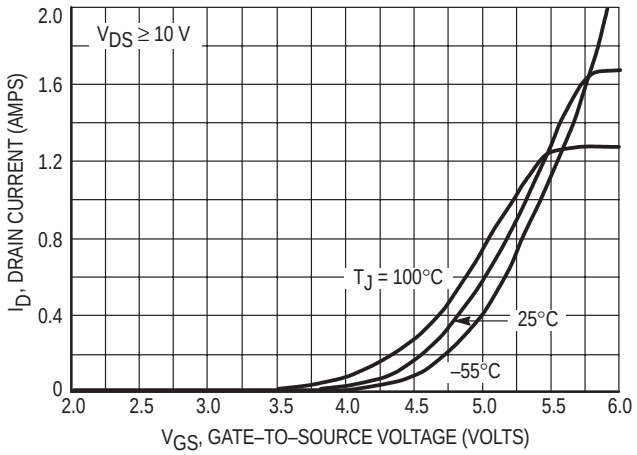
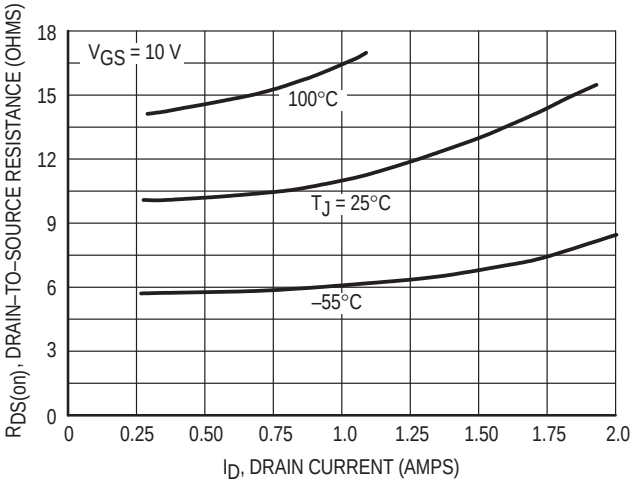


Figure 2. Transfer Characteristics



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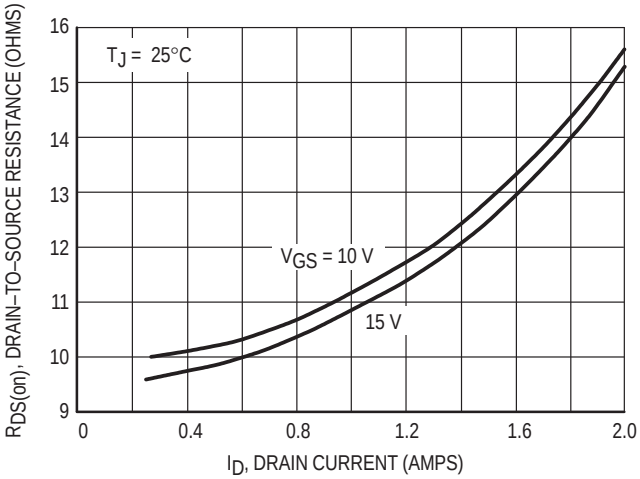

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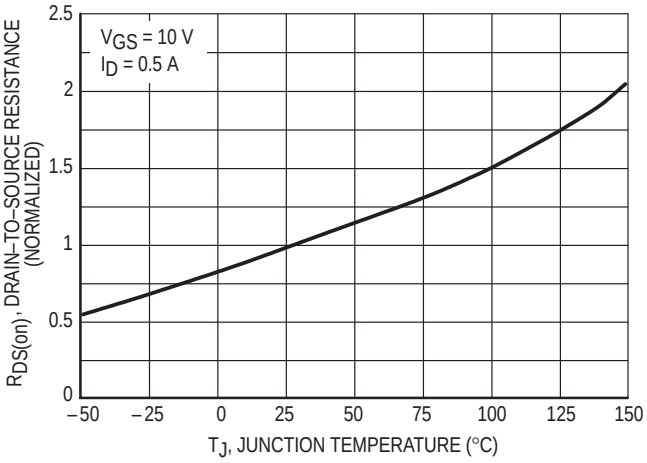

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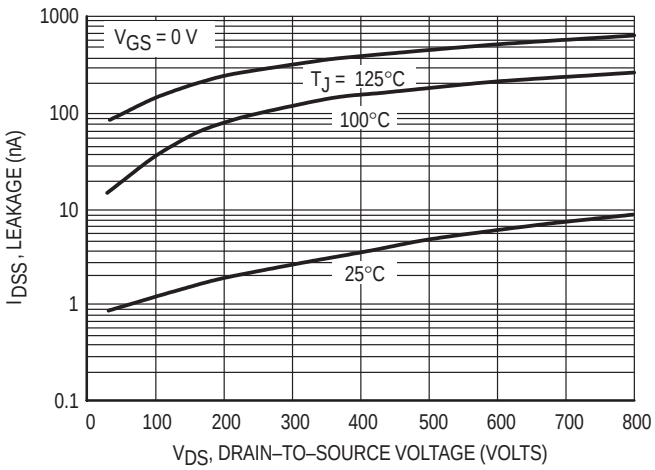

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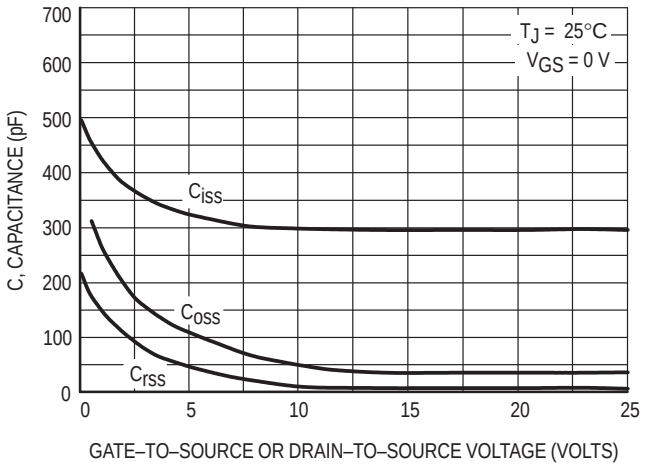

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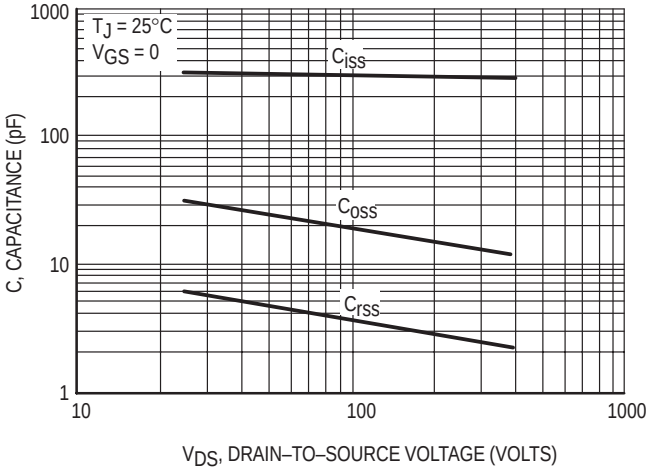
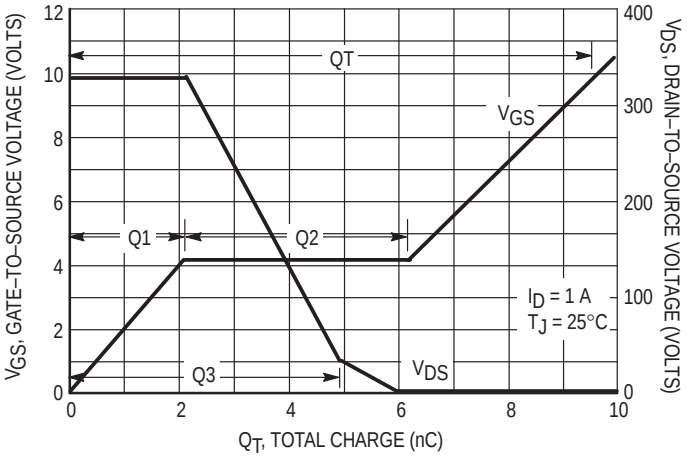


Figure 7b. High Voltage Capacitance Variation



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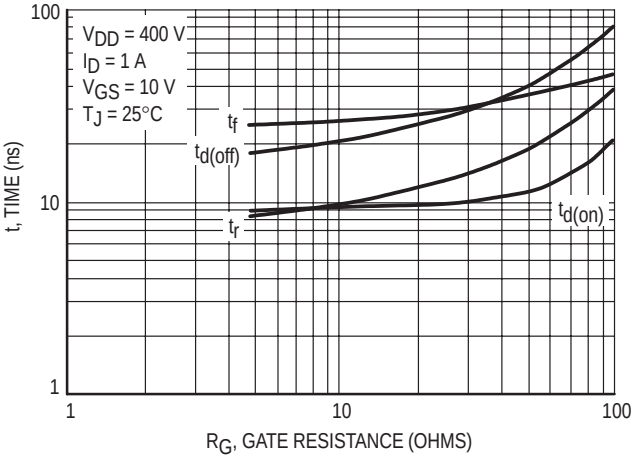

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DRAIN–TO–SOURCE DIODE CHARACTERISTICS

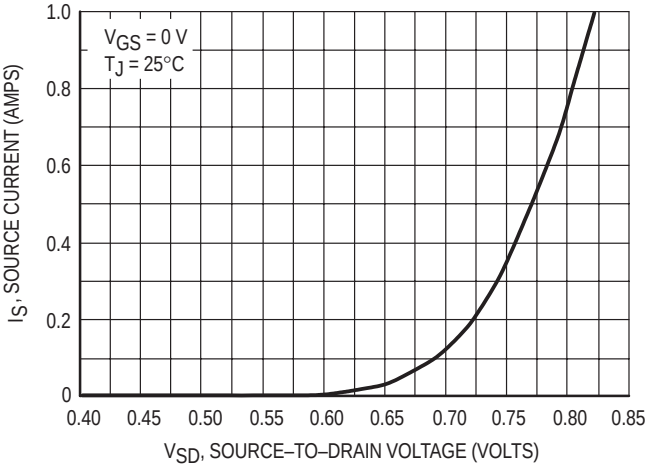


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

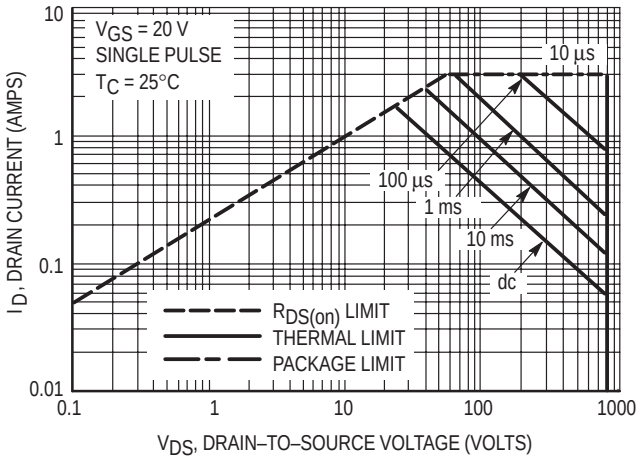


Figure 11. Maximum Rated Forward Biased Safe Operating Area

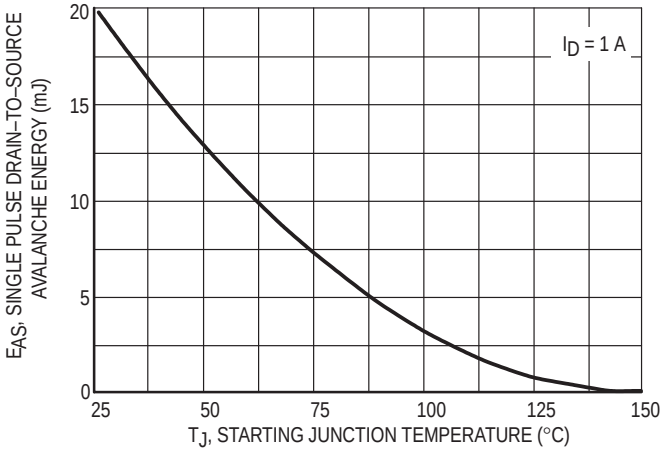


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

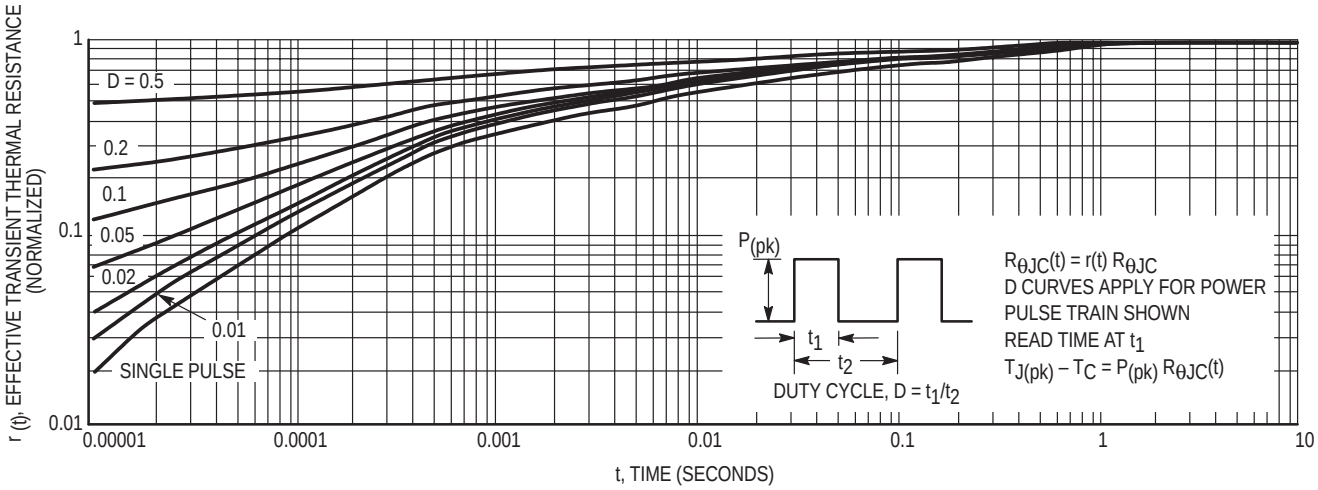


Figure 13. Thermal Response

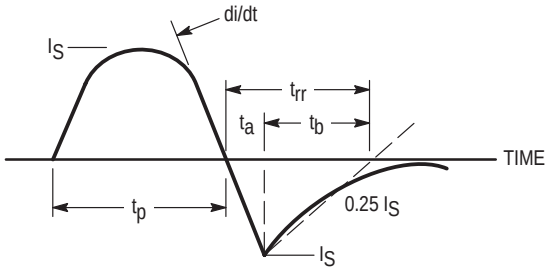


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

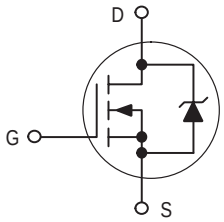
MTP1N100E

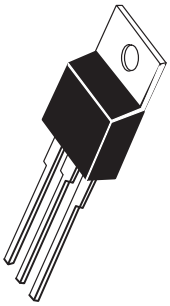
Motorola Preferred Device

TMOS POWER FET
1.0 AMPERES
1000 VOLTS
$R_{DS(on)}$ = 9.0 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	1000	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	1000	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	1.0 0.8 3.0	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	1000 —	— 1.251	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 6.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 0.5 Adc)		$R_{DS(on)}$	—	6.7	9.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 1.0 Adc) (I_D = 0.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	4.86 —	9.0 9.9	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 0.5 Adc)		g_{FS}	0.9	1.32	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	587	810	pF
Output Capacitance		C_{oss}	—	59.6	120	
Reverse Transfer Capacitance		C_{rss}	—	12.2	25	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 500 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	9.0	20	ns
Rise Time		t_r	—	12	25	
Turn–Off Delay Time		$t_{d(off)}$	—	28	55	
Fall Time		t_f	—	34	70	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 1.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	14.6	21	nC
		Q_1	—	2.8	—	
		Q_2	—	6.8	—	
		Q_3	—	5.2	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc) (I_S = 1.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.764 0.62	1.0 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 1.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	655	—	ns
		t_a	—	42	—	
		t_b	—	613	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.957	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

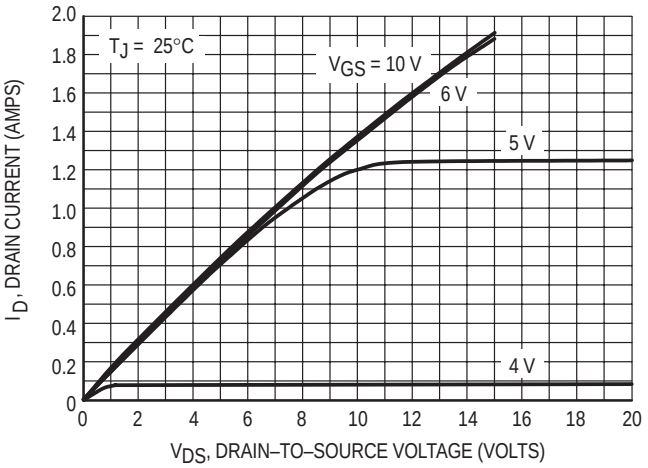


Figure 1. On–Region Characteristics

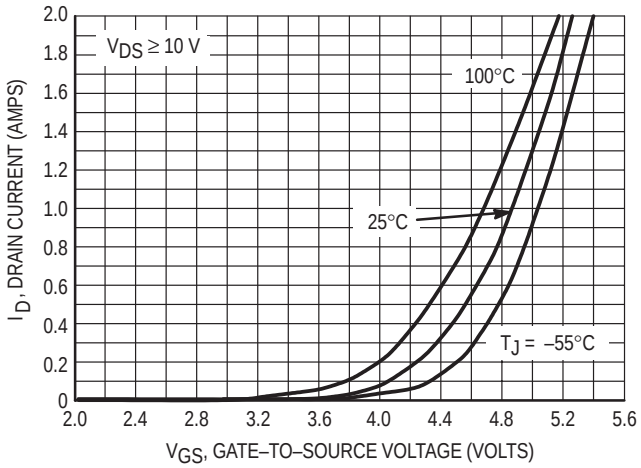


Figure 2. Transfer Characteristics

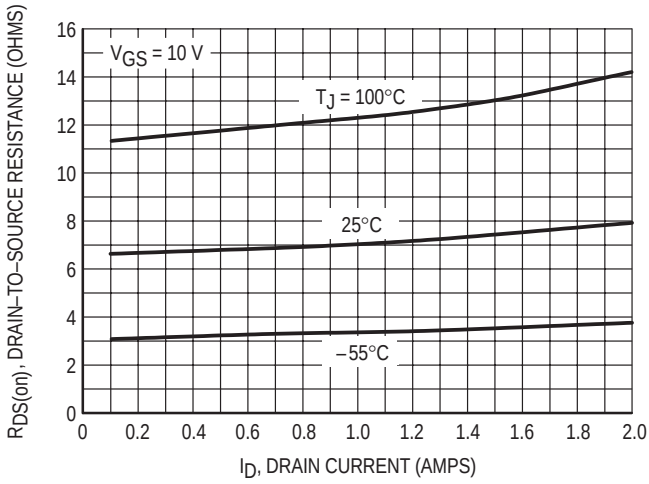


Figure 3. On–Resistance versus Drain Current and Temperature

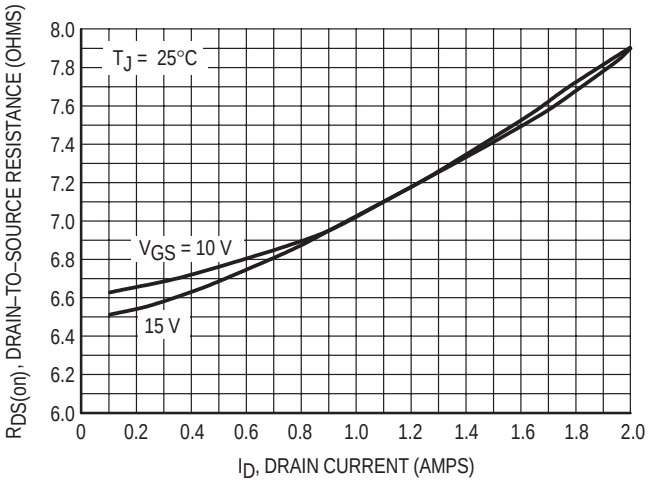


Figure 4. On–Resistance versus Drain Current and Gate Voltage

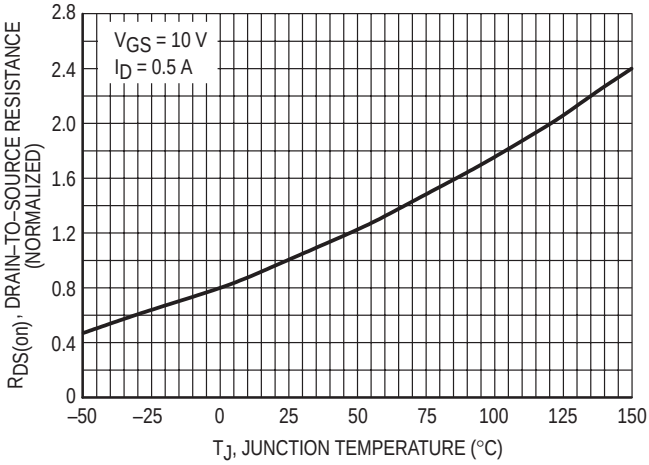


Figure 5. On–Resistance Variation with Temperature

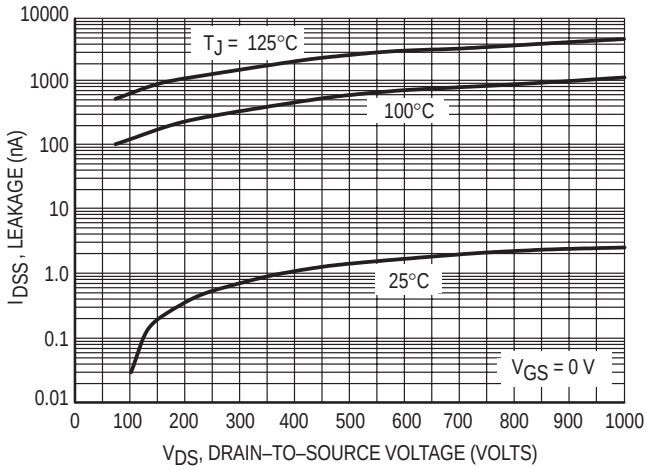


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

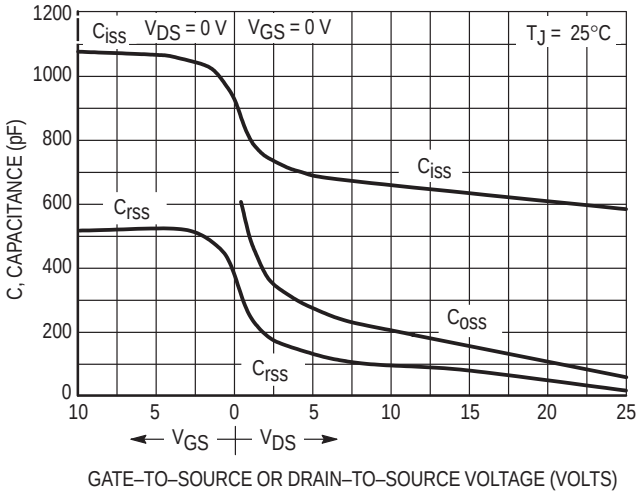


Figure 7a. Capacitance Variation

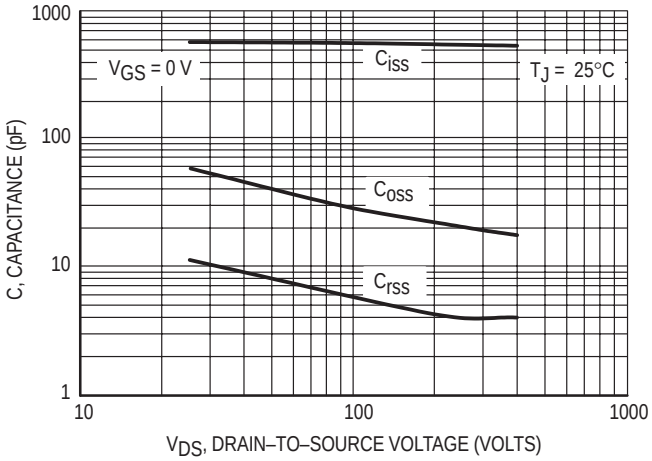


Figure 7b. High Voltage Capacitance Variation

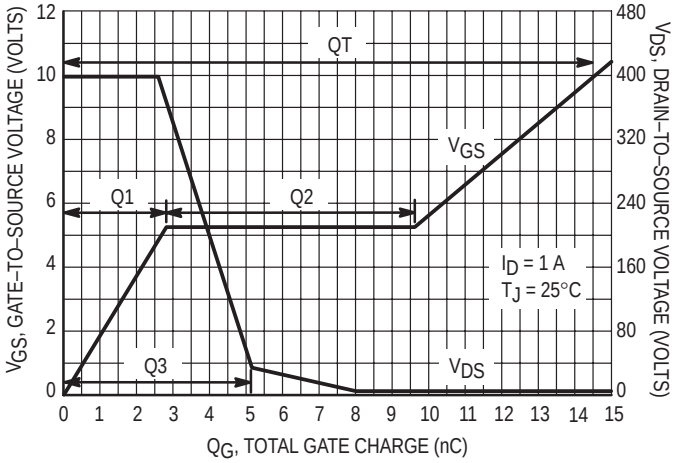


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

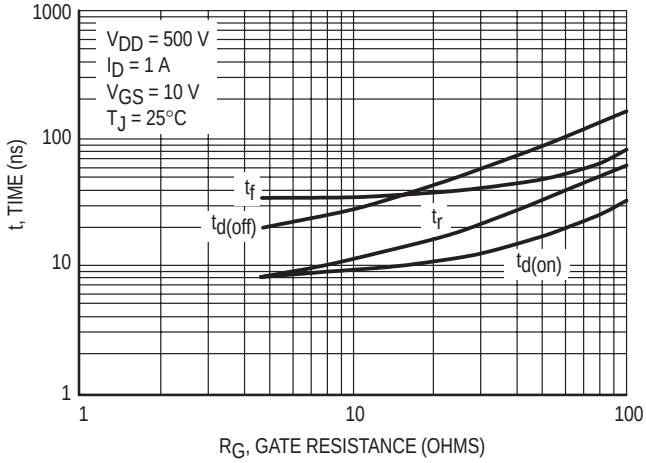
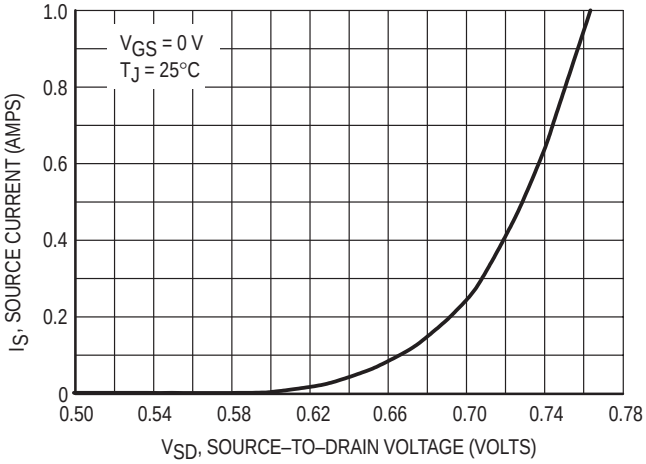


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS



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SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

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SAFE OPERATING AREA

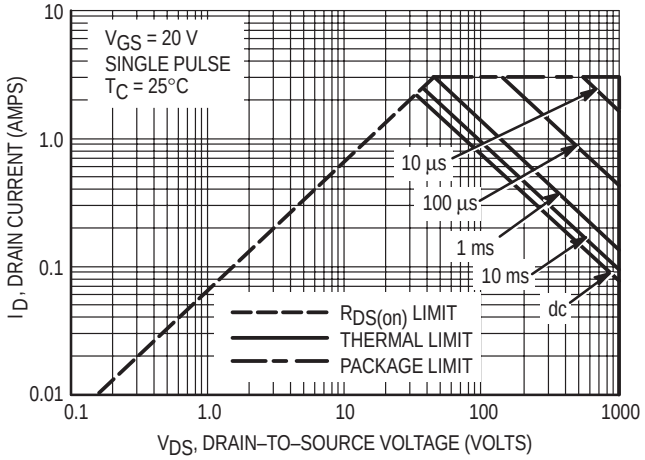
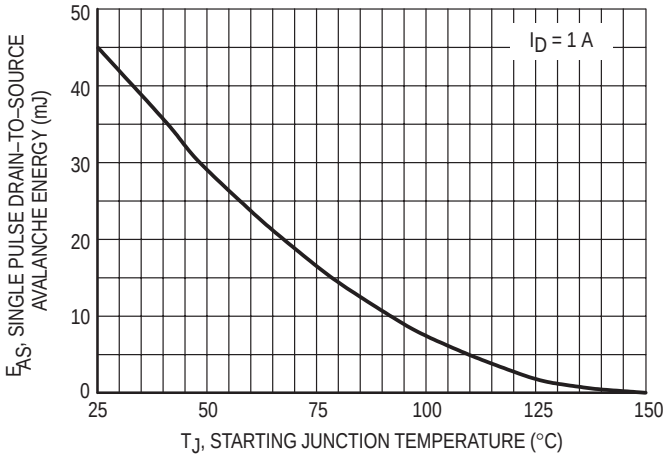


Figure 11. Maximum Rated Forward Biased Safe Operating Area



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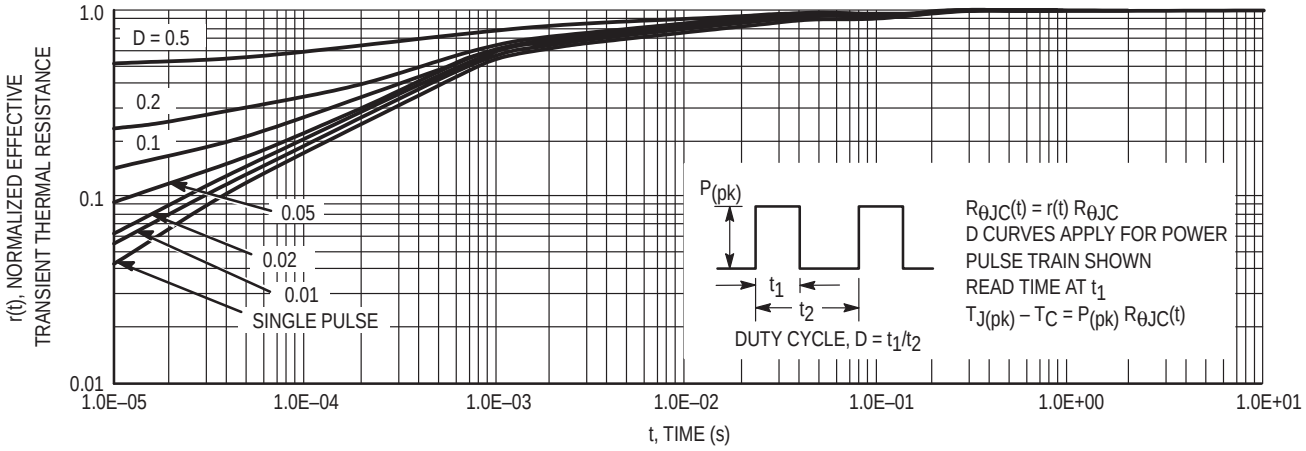

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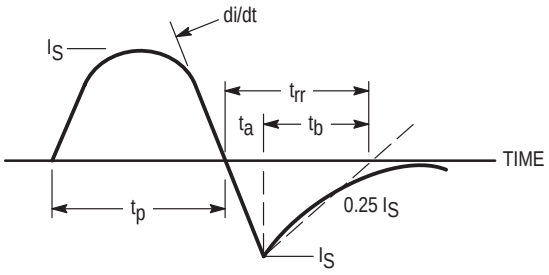

Figure 14. Diode Reverse Recovery Waveform

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N–Channel Enhancement–Mode Silicon Gate

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Motorola Preferred Device

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$R_{DS(on)}$ = 3.5 OHM

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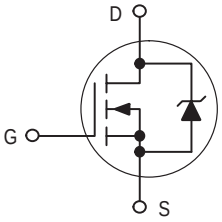
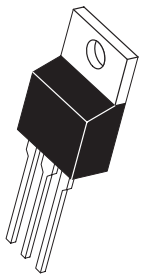
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	400	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	2.0 1.5 6.0	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	40 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 3.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	45	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.13 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

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Preferred devices are Motorola recommended choices for future use and best overall value.

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Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	400	—	—	Vdc
Temperature Coefficient (Positive)			—	451	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 400 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 400 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.2	4.0	Vdc
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	—	3.1	3.5	Ohms
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 2.0 Adc)		$V_{DS(on)}$	—	7.3	8.4	Vdc
(I_D = 1.0 Adc, T_J = 125°C)			—	—	7.4	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.0 Adc)		g_{FS}	0.5	1.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	229	320	pF
Output Capacitance		C_{oss}	—	34	40	
Reverse Transfer Capacitance		C_{rss}	—	7.3	10	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 200 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.0	16	ns
Rise Time		t_r	—	8.4	14	
Turn–Off Delay Time		$t_{d(off)}$	—	12	26	
Fall Time		t_f	—	11	20	
Gate Charge	(V_{DS} = 320 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	8.6	12	nC
		Q_1	—	2.6	—	
		Q_2	—	3.2	—	
		Q_3	—	5.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.88	1.2	Vdc
	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.76	—	
Reverse Recovery Time	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	156	—	ns
		t_a	—	99	—	
		t_b	—	57	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.89	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

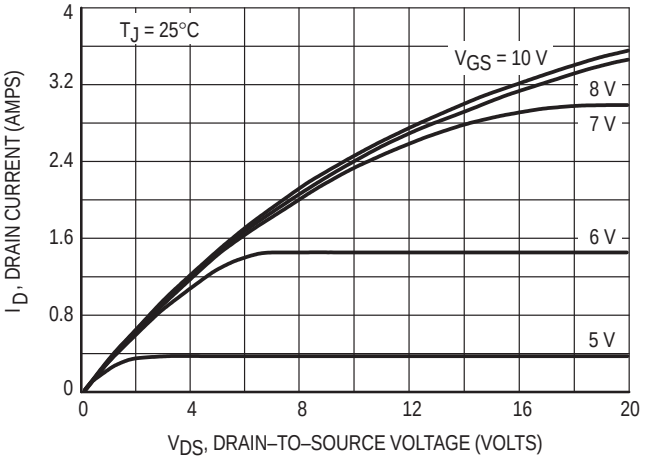


Figure 1. On–Region Characteristics

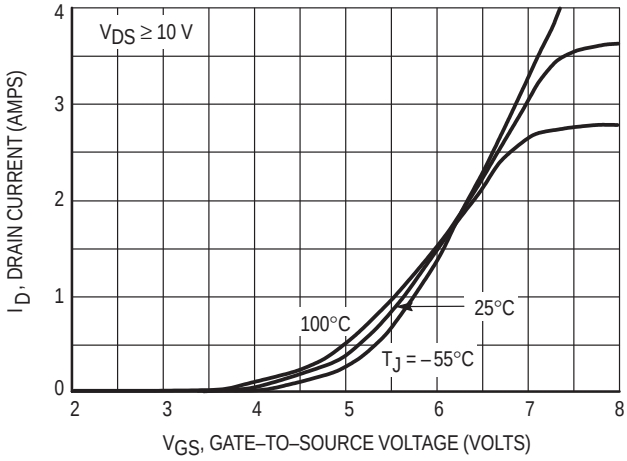


Figure 2. Transfer Characteristics

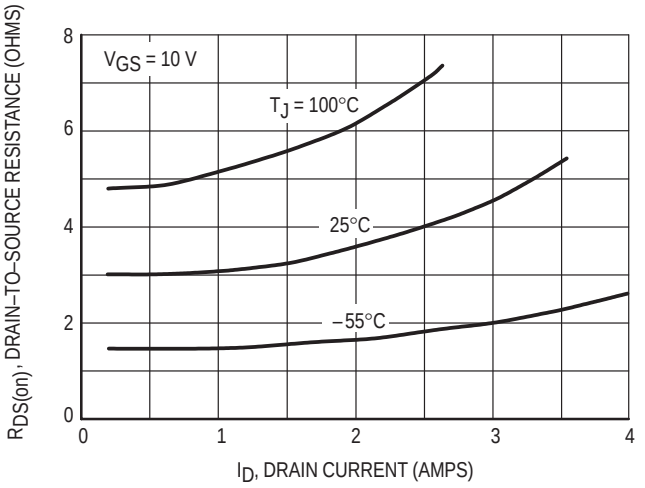


Figure 3. On–Resistance versus Drain Current and Temperature

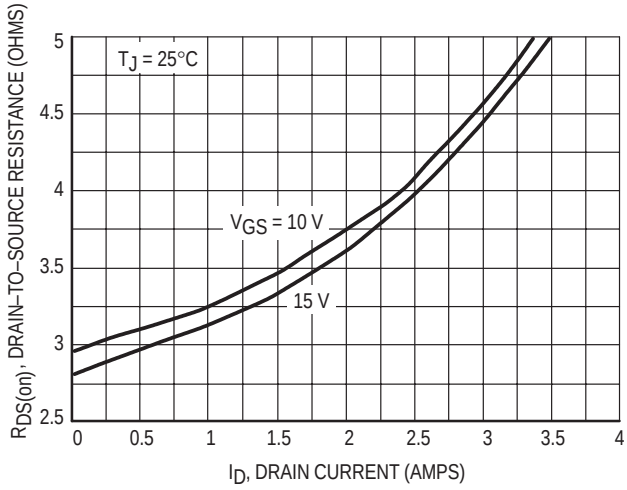


Figure 4. On–Resistance versus Drain Current and Gate Voltage

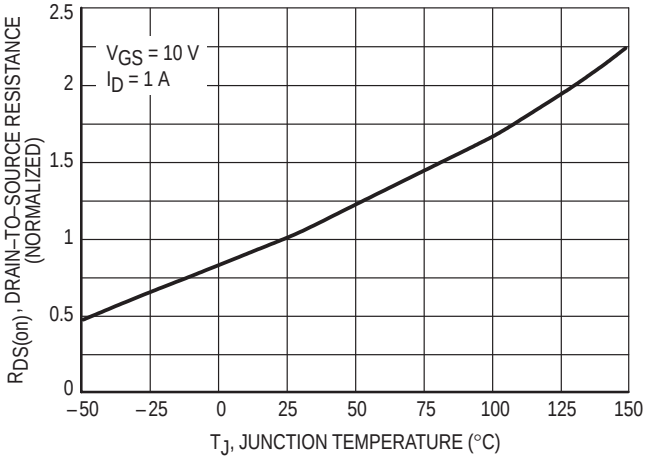


Figure 5. On–Resistance Variation with Temperature

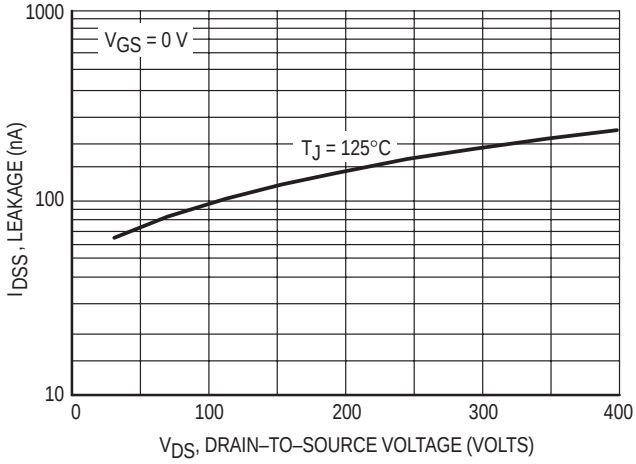


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9.) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

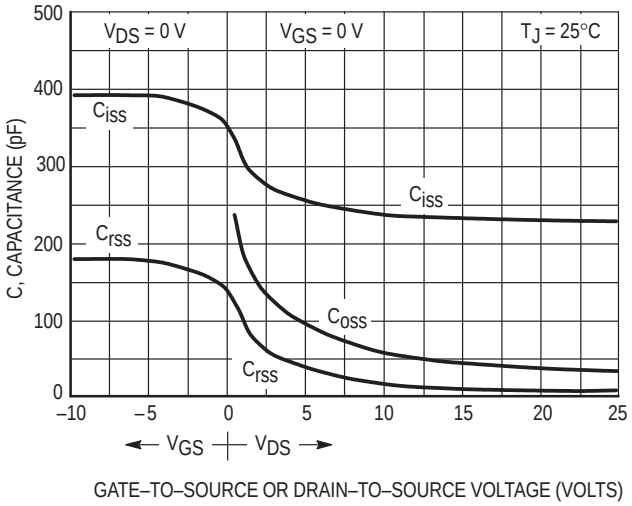


Figure 7. a. Capacitance Variation

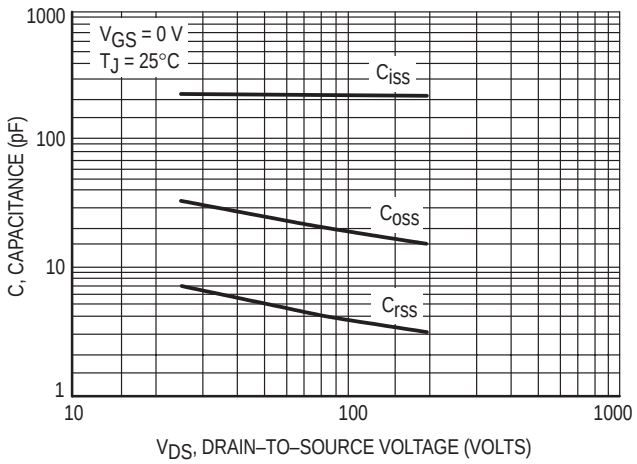


Figure 7. b. High Voltage Capacitance Variation

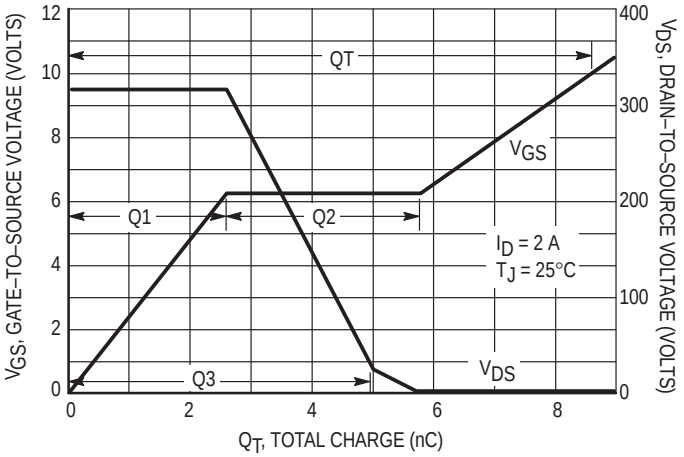


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

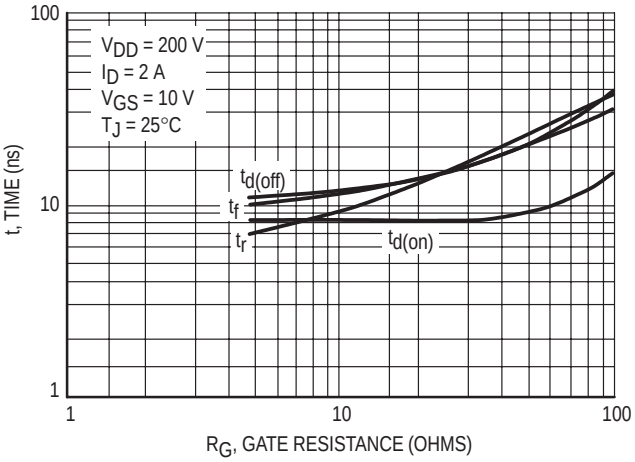


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

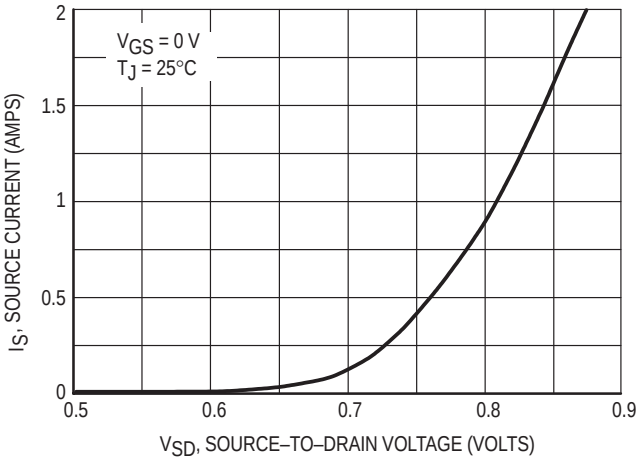


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12.). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

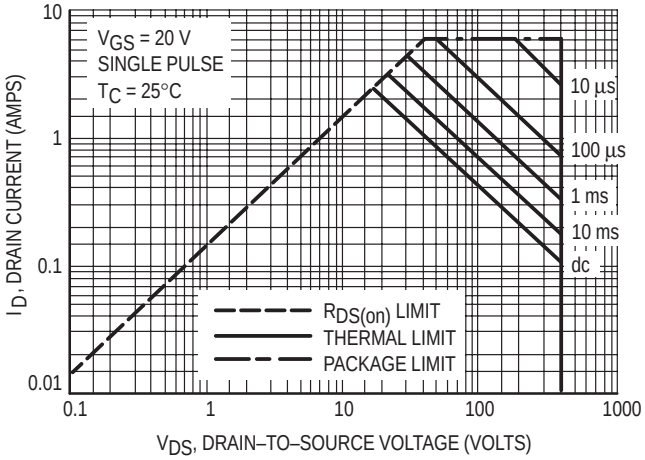


Figure 11. Maximum Rated Forward Biased Safe Operating Area

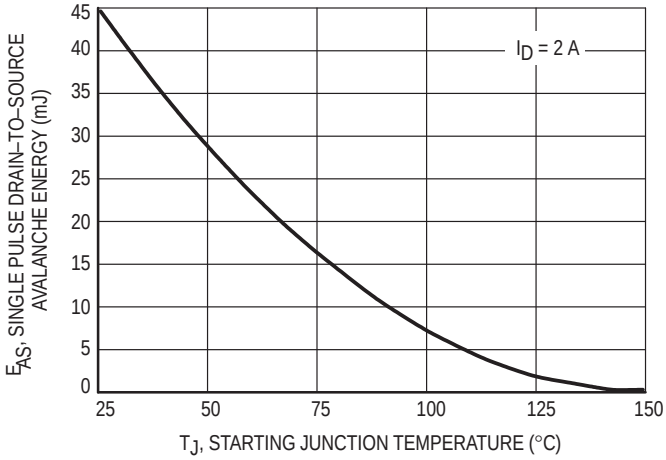


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

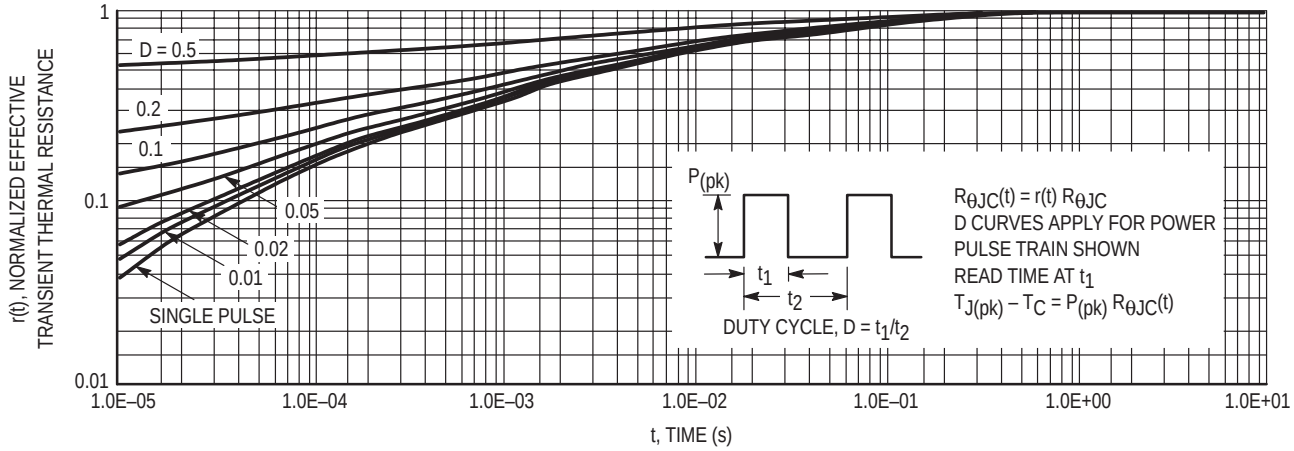


Figure 13. Thermal Response

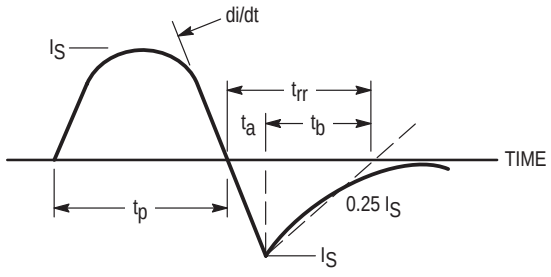


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

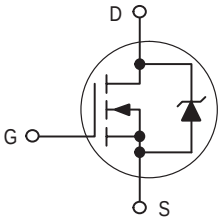
MTP2N50E

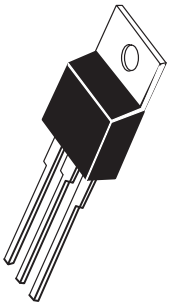
Motorola Preferred Device

TMOS POWER FET
2.0 AMPERES
500 VOLTS
$R_{DS(on)}$ = 3.6 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	2.0 1.6 6.0	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 3.5 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	61	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	500 —	— 689	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 7.1	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	—	2.7	4.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 2.0 Adc) (I_D = 1.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	5.9 —	9.6 8.4	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.0 Adc)		g_{FS}	1.0	1.6	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	323	450	pF
Output Capacitance		C_{oss}	—	45	60	
Reverse Transfer Capacitance		C_{rss}	—	9.0	20	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.0	16	ns
Rise Time		t_r	—	6.0	12	
Turn–Off Delay Time		$t_{d(off)}$	—	16	32	
Fall Time		t_f	—	10	20	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	11	15	nC
		Q_1	—	2.0	—	
		Q_2	—	5.4	—	
		Q_3	—	5.1	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc) (I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.82 0.69	1.6 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	334	—	ns
		t_a	—	62	—	
		t_b	—	272	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.985	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

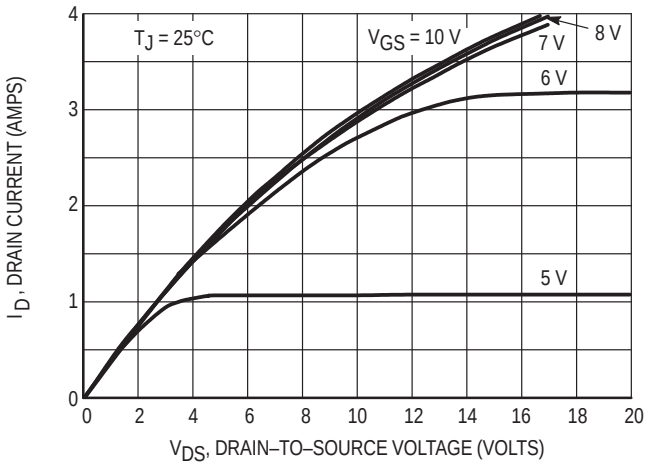


Figure 1. On–Region Characteristics

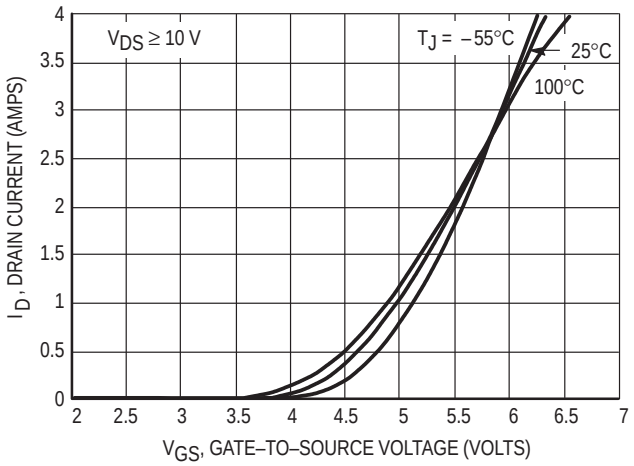


Figure 2. Transfer Characteristics

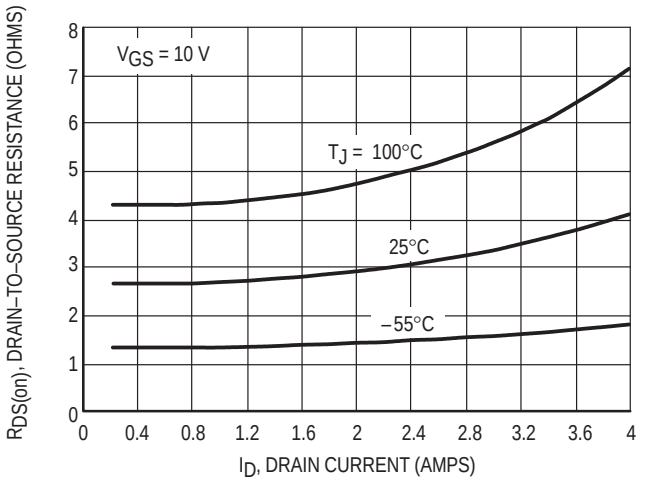


Figure 3. On–Resistance versus Drain Current and Temperature

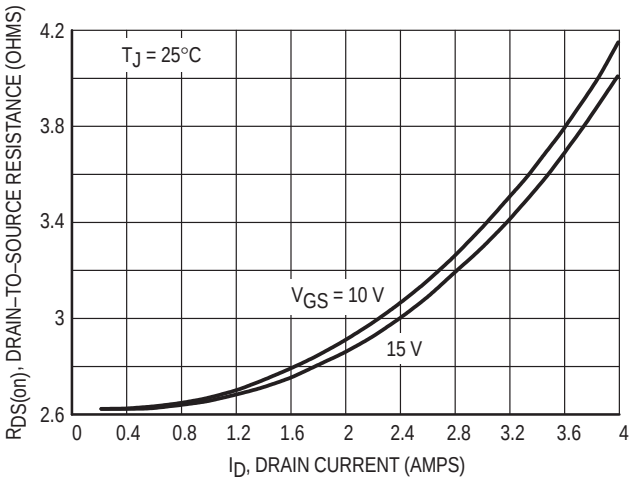


Figure 4. On–Resistance versus Drain Current and Gate Voltage

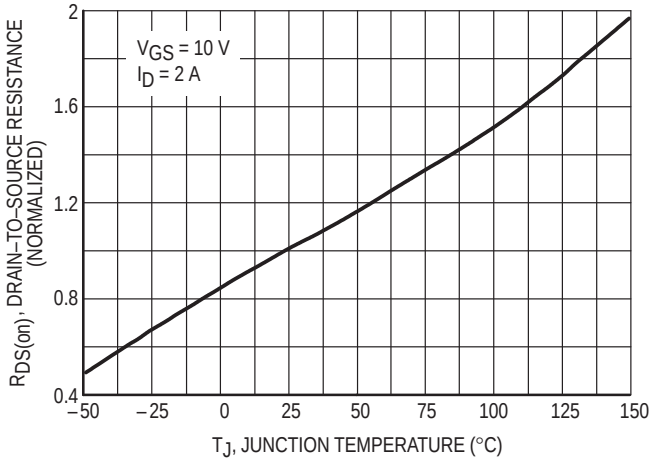


Figure 5. On–Resistance Variation with Temperature

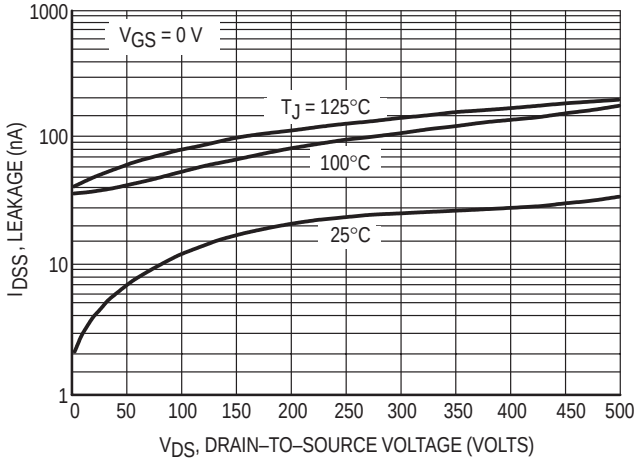


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

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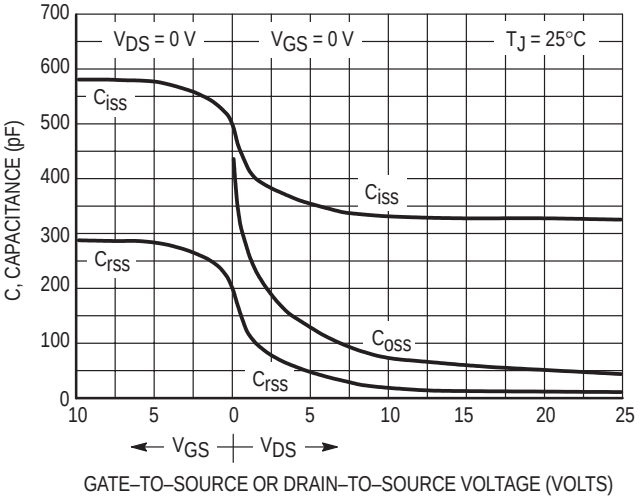

Figure 7a. Capacitance Variation

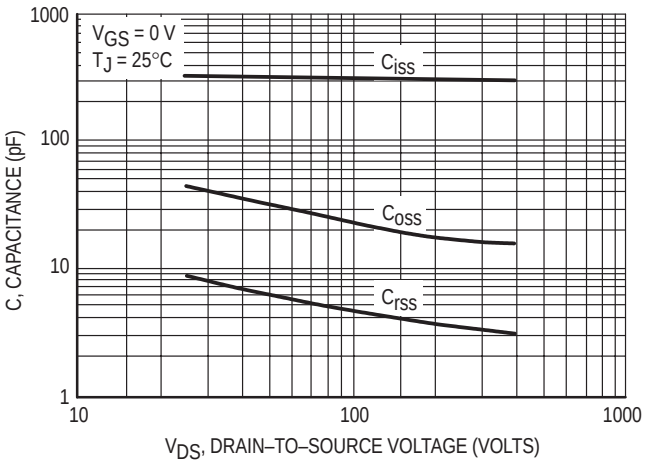

Figure 7b. High Voltage Capacitance Variation

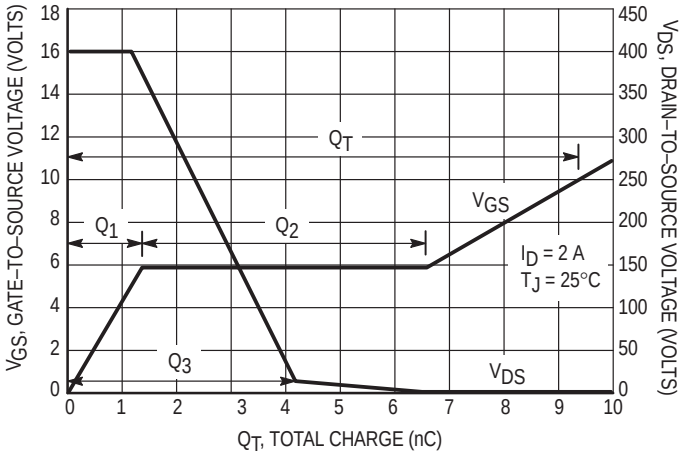

Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

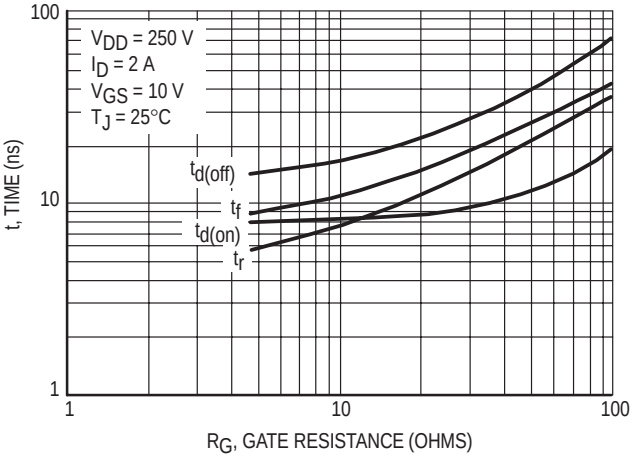

Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

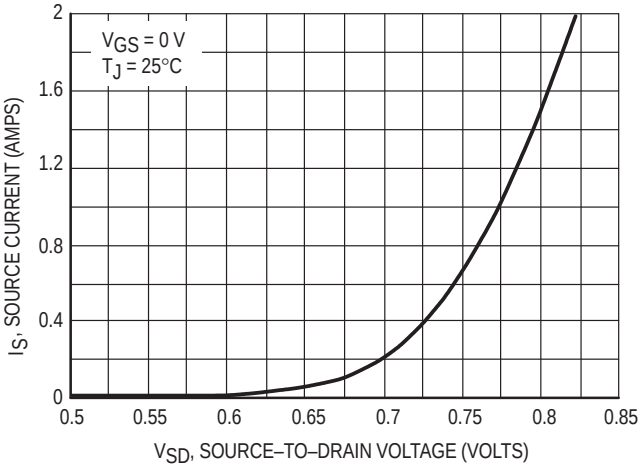

Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

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A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

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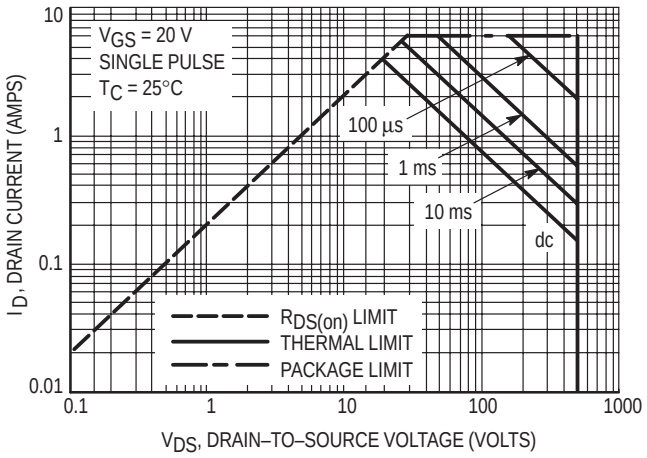


Figure 11. Maximum Rated Forward Biased Safe Operating Area

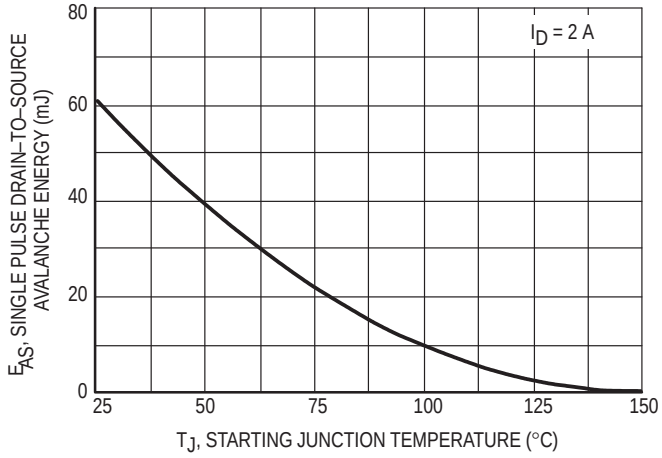


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

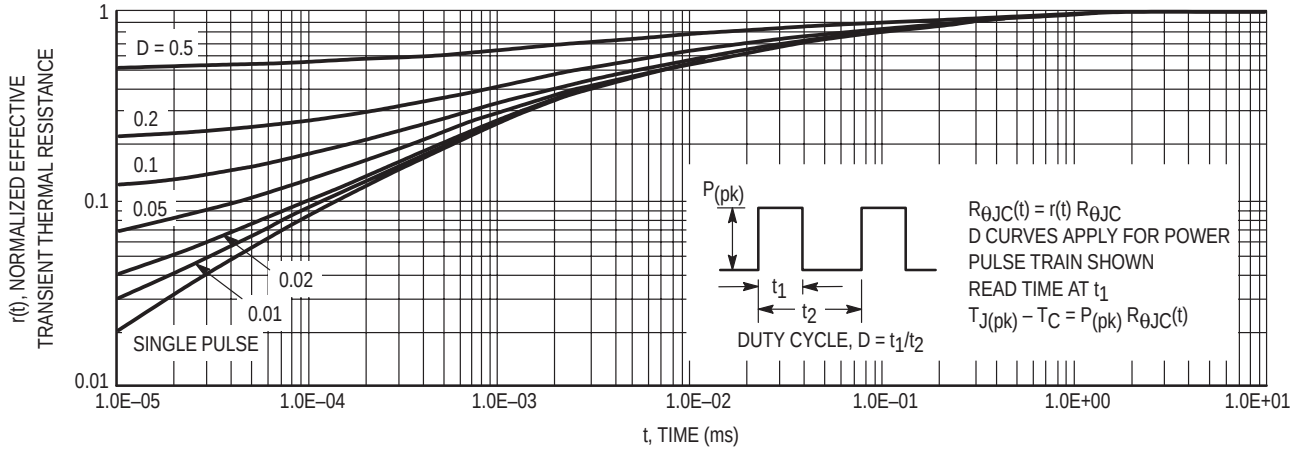
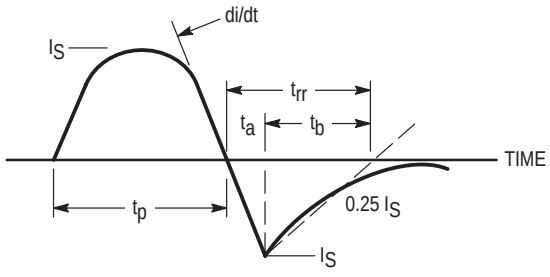


Figure 13. Thermal Response



Fifgure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

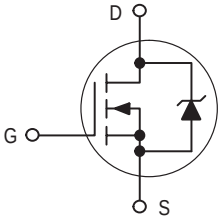
MTP2N60E

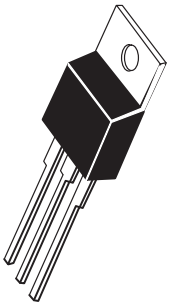
Motorola Preferred Device

TMOS POWER FET
2.0 AMPERES
600 VOLTS
$R_{DS(on)}$ = 3.8 OHMS

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	600	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–to–Source Voltage — Continuous — Single Pulse ($t_p \le 50$ μs)	V_{GS}	±20 ±40	Vdc
Drain Current — Continuous — Single Pulse ($t_p \le 10$ μs)	I_D I_{DM}	2.0 9.0	Adc
Total Power Dissipation Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, L = 95 mH, R_G = 25 Ω, Peak I_L = 2.0 Adc)	E_{AS}	190	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	600	—	—	Vdc
Temperature Coefficient (positive)			—	480	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				mA
(V_{DS} = 600 Vdc, V_{GS} = 0 Vdc)			—	—	0.25	
(V_{DS} = 480 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	1.0	
Gate–Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0 Vdc)		I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0 Vdc)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage		$V_{GS(th)}$				
(V_{DS} = V_{GS}, I_D = 250 μAdc)			2.0	3.1	4.0	Vdc
Temperature Coefficient (negative)			—	8.5	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	—	3.3	3.8	Ohm
Drain–to–Source On–Voltage		$V_{DS(on)}$				Vdc
(V_{GS} = 10 Vdc, I_D = 2.0 Adc)			—	—	8.2	
(V_{GS} = 10 Vdc, I_D = 1.0 Adc, T_J = 125°C)			—	—	8.4	
Forward Transconductance (V_{DS} ≥ 50 Vdc, I_D = 1.0 Adc)		g_{FS}	1.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	435	—	pF
Reverse Transfer Capacitance		C_{rss}	—	56	—	
Output Capacitance		C_{oss}	—	9.2	—	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 300 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_g = 18 Ω)	$t_{d(on)}$	—	12	—	ns
Rise Time		t_r	—	21	—	
Turn–Off Delay Time		$t_{d(off)}$	—	30	—	
Fall Time		t_f	—	24	—	
Gate Charge	(V_{DS} = 400 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	13	22	nC
		Q_1	—	2.0		
		Q_2	—	6.0	—	
		Q_3	—	5.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.6	Vdc
	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.9	—	
Reverse Recovery Time	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	340	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_d				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from the drain 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance		L_s	—	7.5	—	
(Measured from the source pin 0.25″ from package to source bond pad.)						

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

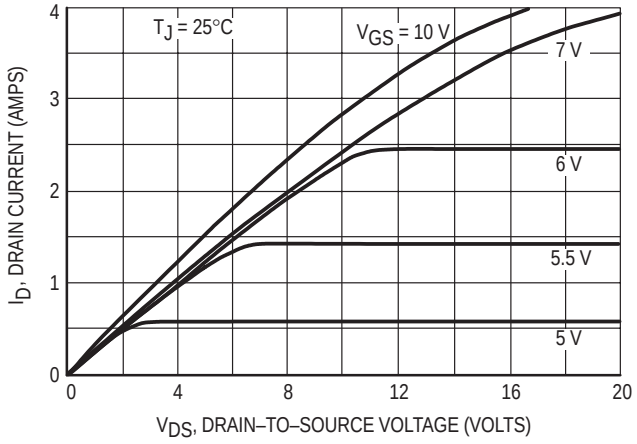


Figure 1. On–Region Characteristics

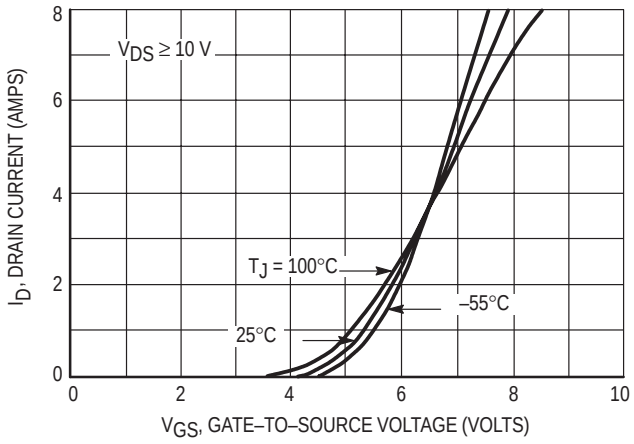


Figure 2. Transfer Characteristics

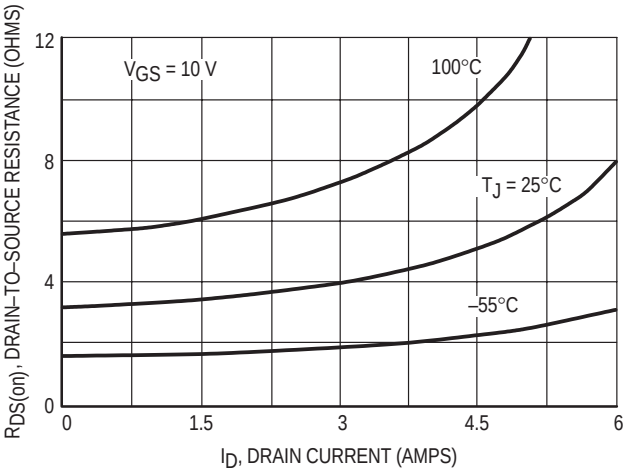


Figure 3. On–Resistance versus Drain Current and Temperature

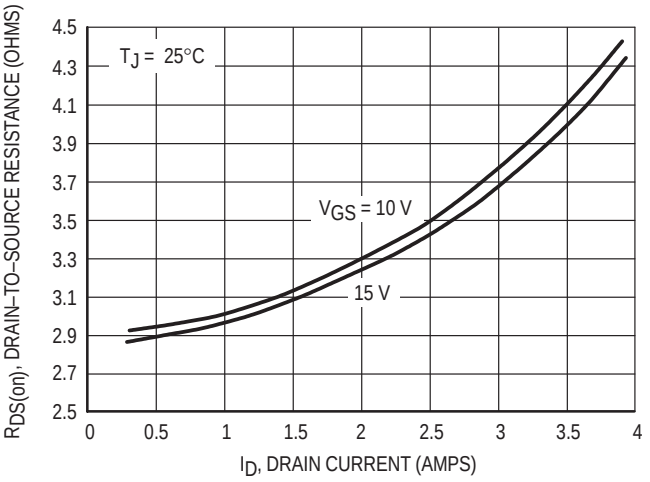


Figure 4. On–Resistance versus Drain Current and Gate Voltage

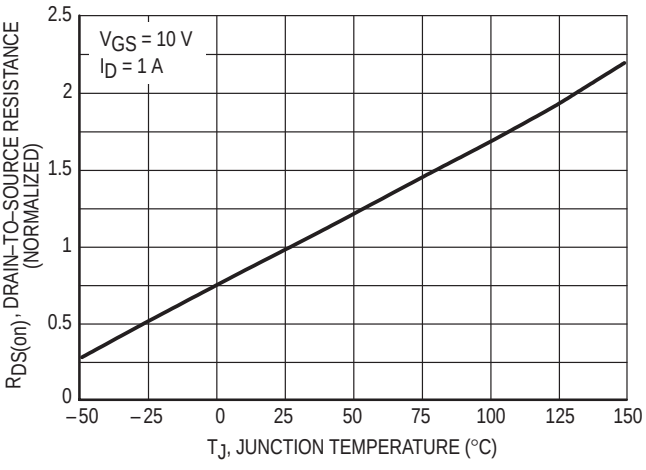
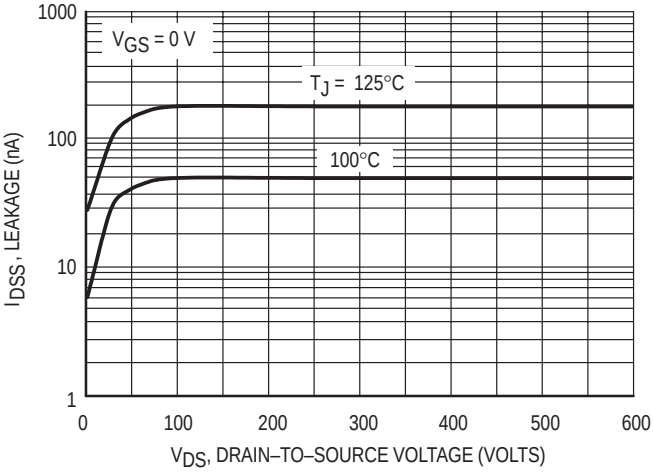


Figure 5. On–Resistance Variation with Temperature



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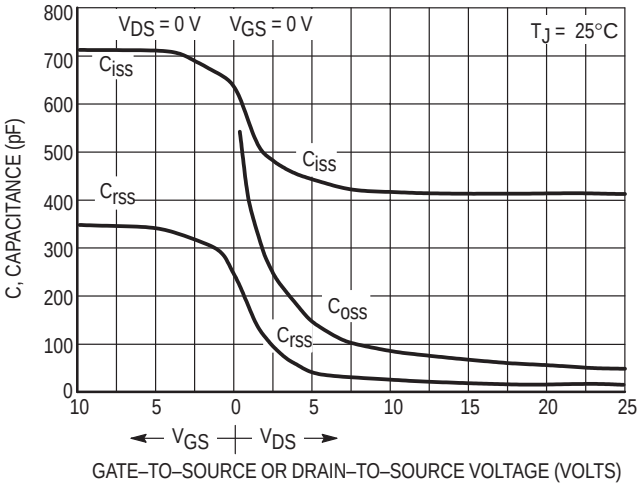

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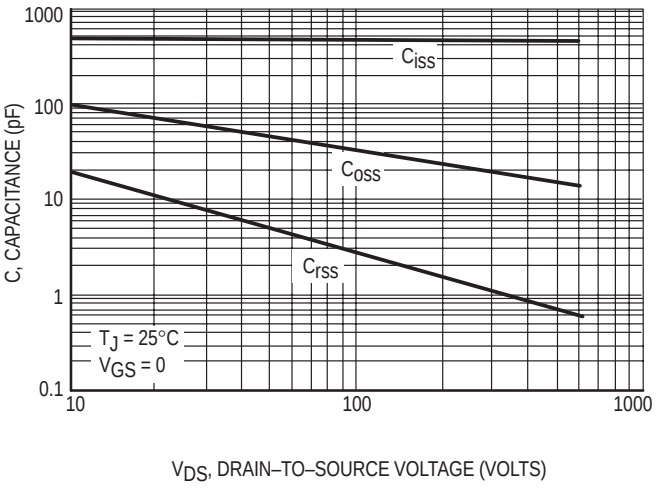

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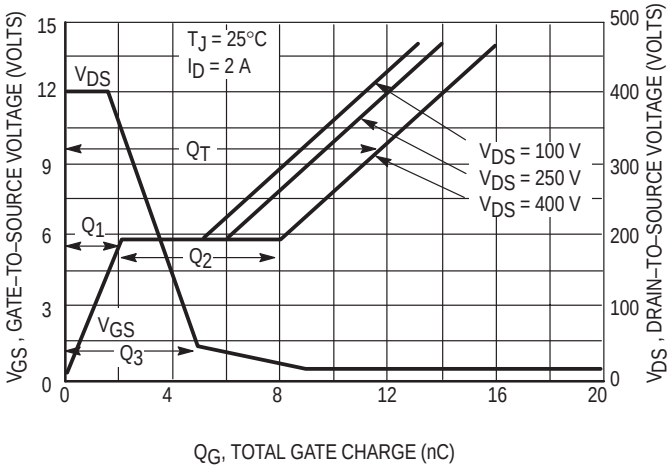

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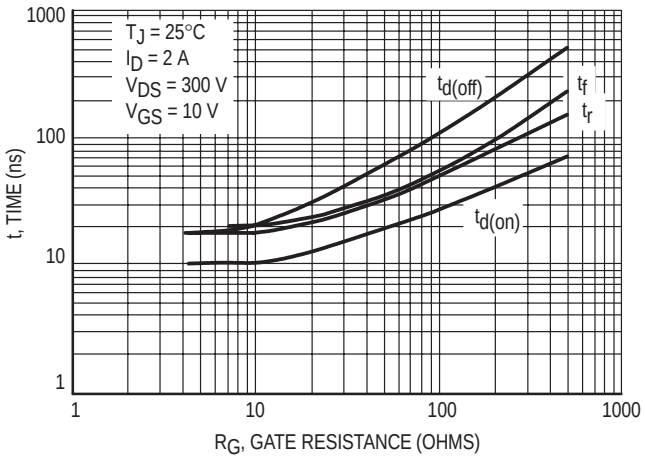

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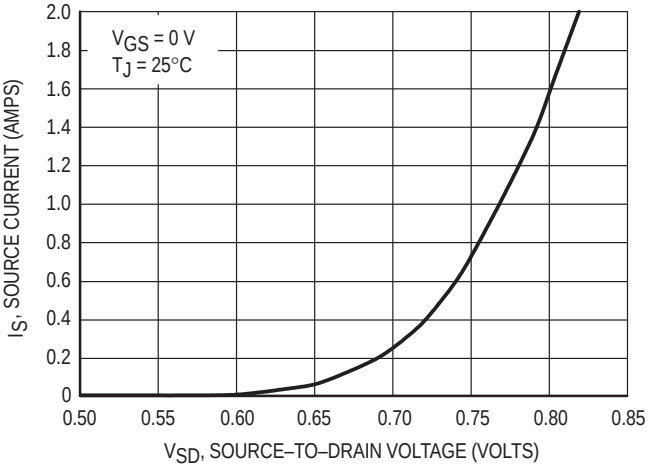
DRAIN–TO–SOURCE DIODE CHARACTERISTICS



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SAFE OPERATING AREA

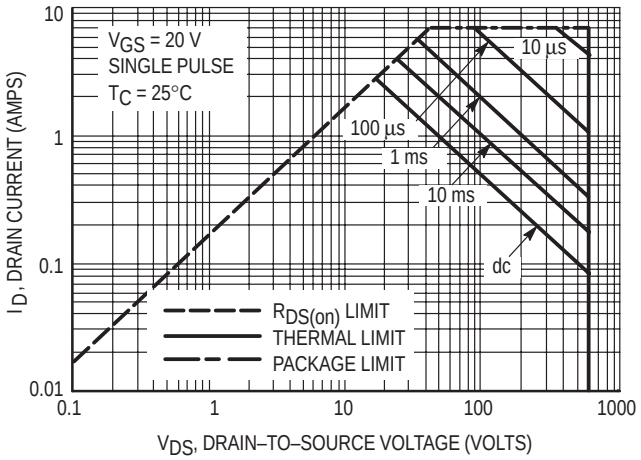


Figure 11. Maximum Rated Forward Biased Safe Operating Area

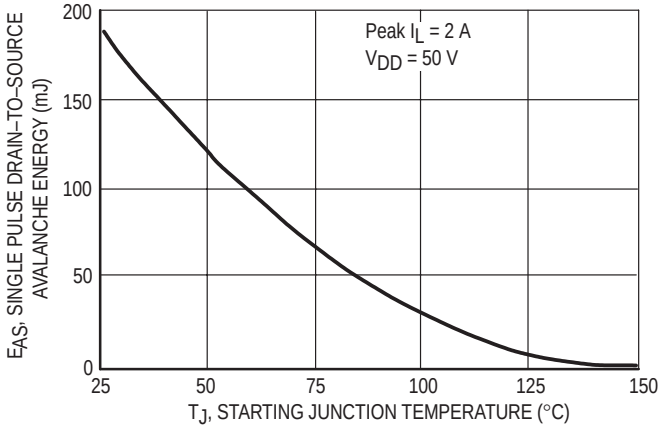


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

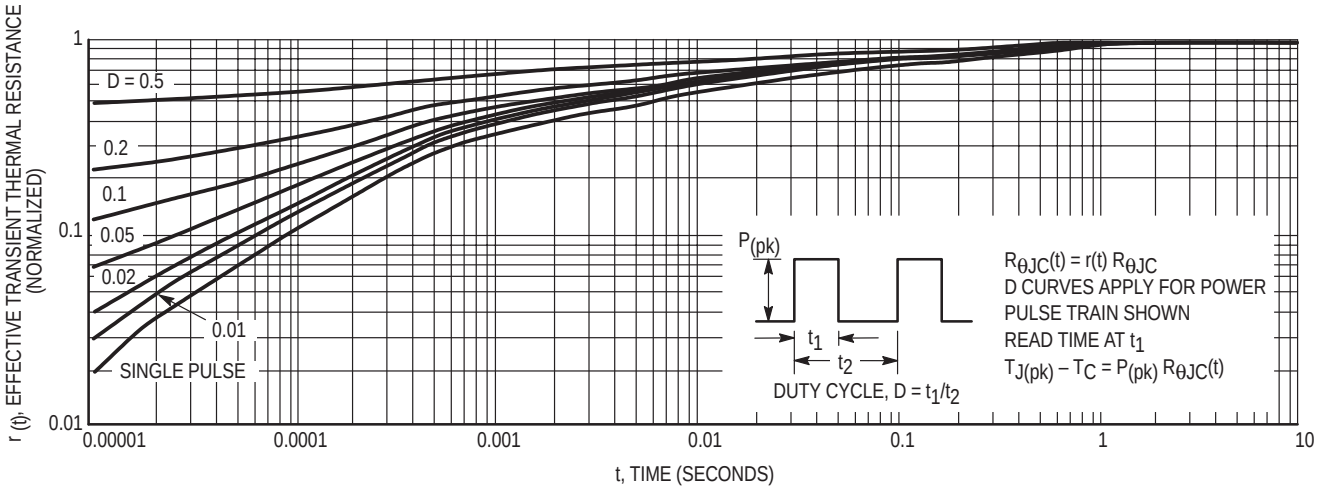


Figure 13. Thermal Response

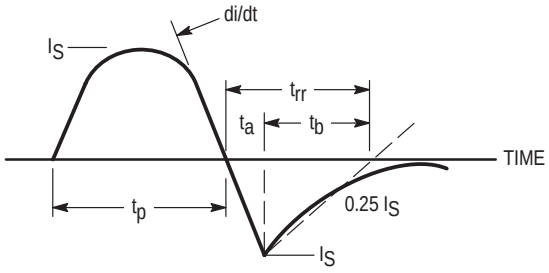


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
P–Channel Enhancement–Mode Silicon Gate

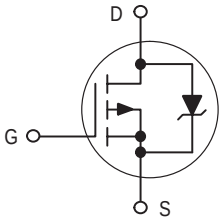
MTP2P50E

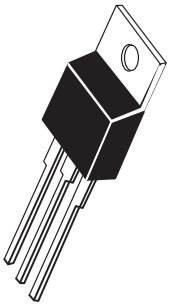
Motorola Preferred Device

TMOS POWER FET
2.0 AMPERES
500 VOLTS
$R_{DS(on)}$ = 6.0 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	2.0 1.6 6.0	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 4.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	80	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	500	—	—	Vdc
Temperature Coefficient (Positive)			—	564	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	4.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.0 Adc)		$R_{DS(on)}$	—	4.5	6.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 2.0 Adc)		$V_{DS(on)}$	—	9.5	14.4	Vdc
(I_D = 1.0 Adc, T_J = 125°C)			—	—	12.6	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.0 Adc)		g_{FS}	1.5	2.9	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	845	1183	pF
Output Capacitance		C_{oss}	—	100	140	
Reverse Transfer Capacitance		C_{rss}	—	26	52	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	12	24	ns
Rise Time		t_r	—	14	28	
Turn–Off Delay Time		$t_{d(off)}$	—	21	42	
Fall Time		t_f	—	19	38	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 2.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	19	27	nC
		Q_1	—	3.7	—	
		Q_2	—	7.9	—	
		Q_3	—	9.9	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	2.3	3.5	Vdc
	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.85	—	
Reverse Recovery Time (See Figure 14)	(I_S = 2.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	223	—	ns
		t_a	—	161	—	
		t_b	—	62	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.92	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

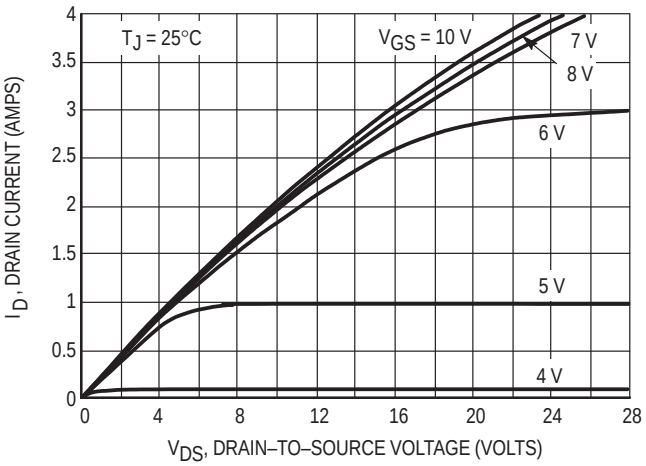


Figure 1. On–Region Characteristics

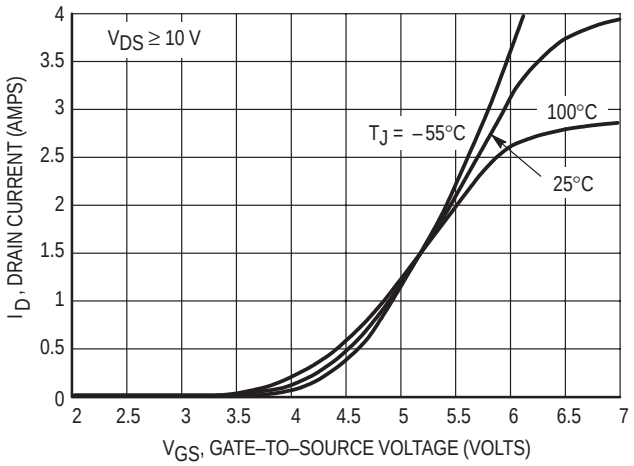


Figure 2. Transfer Characteristics

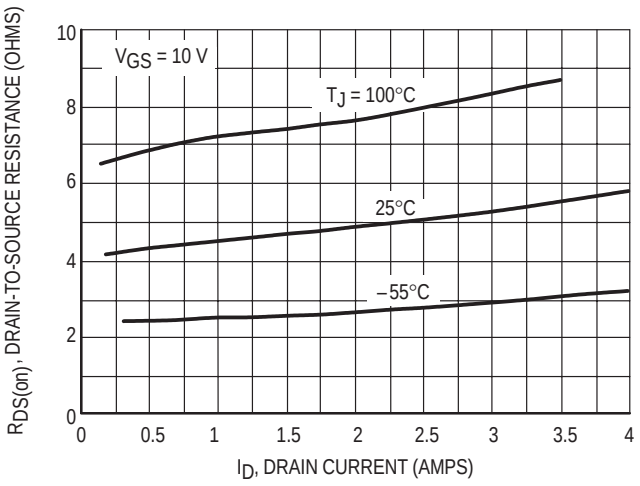


Figure 3. On–Resistance versus Drain Current and Temperature

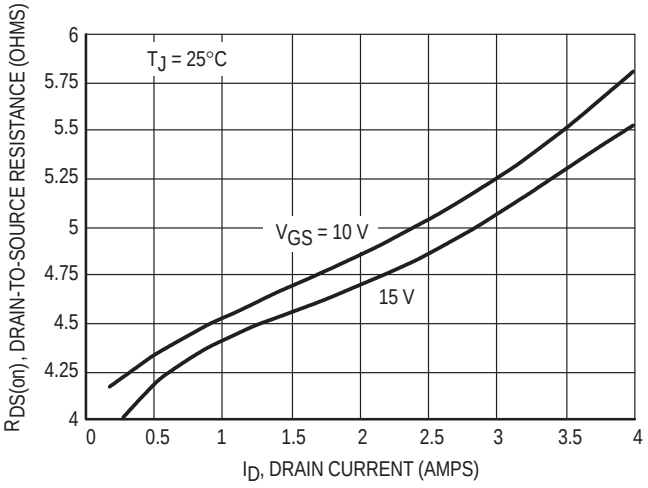


Figure 4. On–Resistance versus Drain Current and Gate Voltage

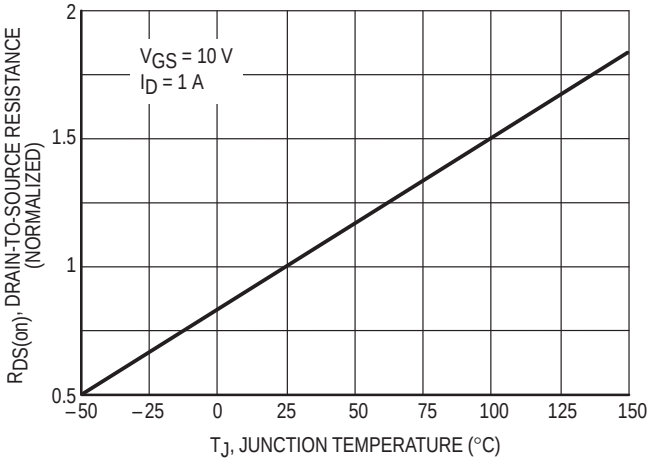


Figure 5. On–Resistance Variation with Temperature

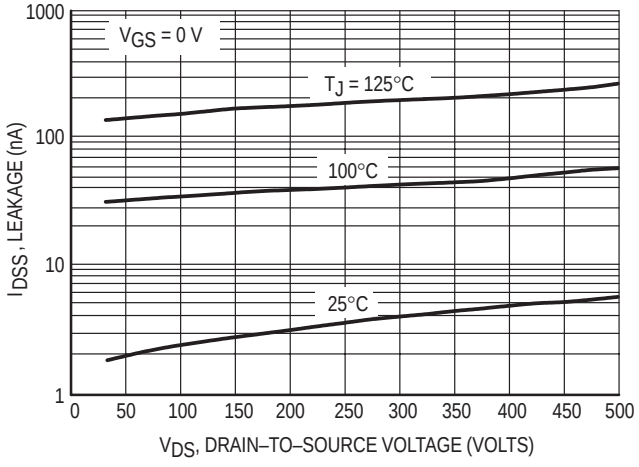


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

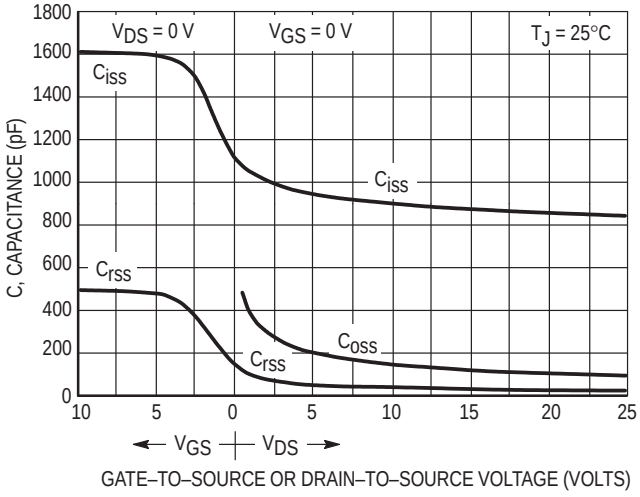


Figure 7a. Capacitance Variation

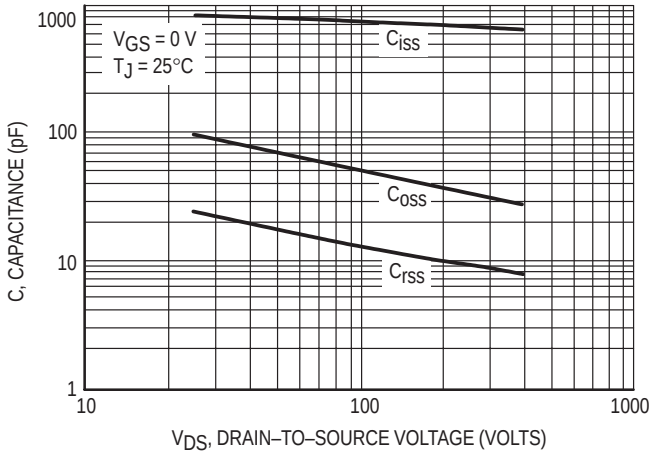


Figure 7b. High Voltage Capacitance Variation

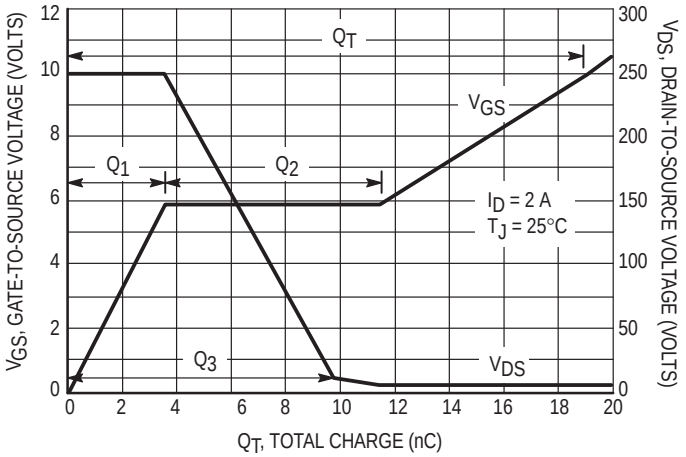


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

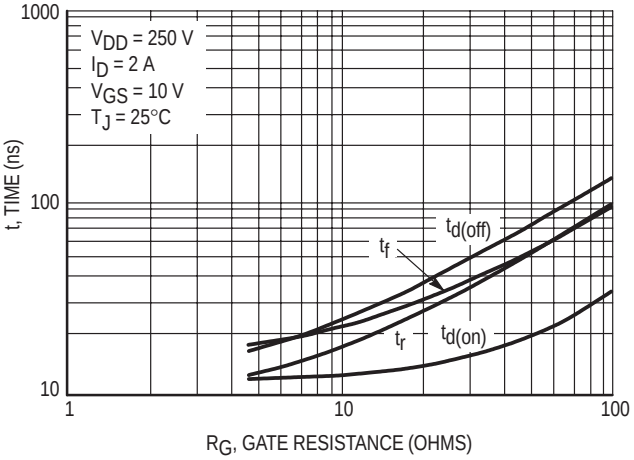


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

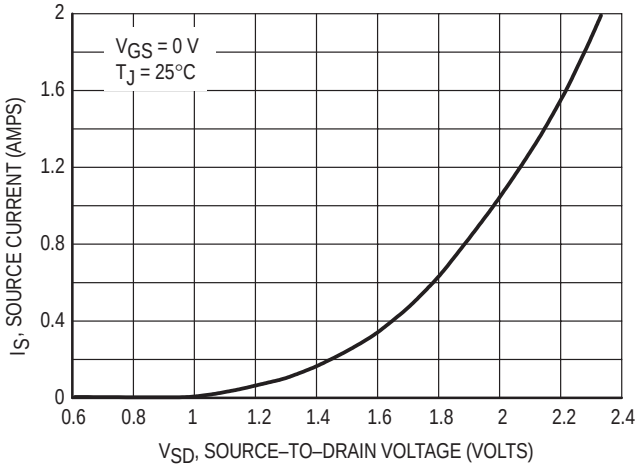


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

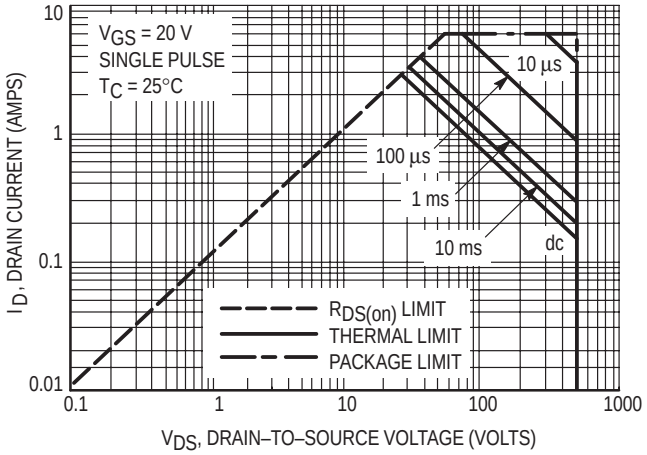


Figure 11. Maximum Rated Forward Biased Safe Operating Area

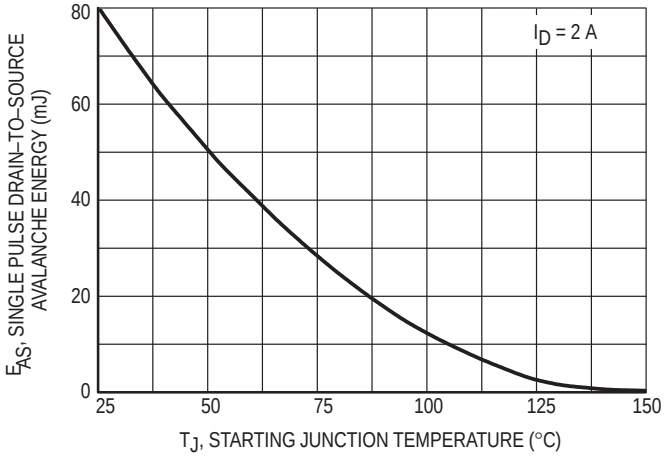


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

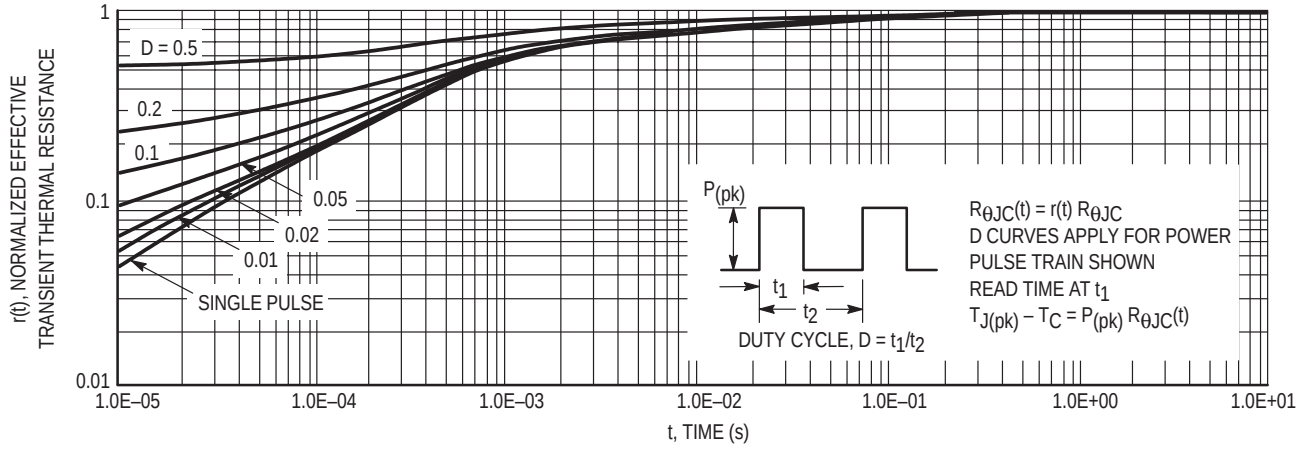


Figure 13. Thermal Response

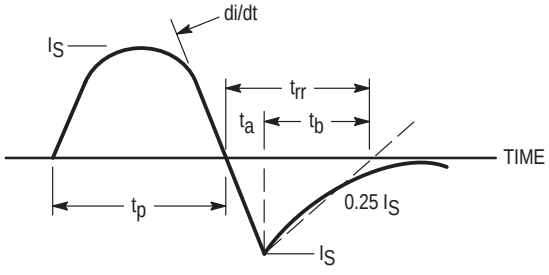


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet
TMOS E-FET™
High Energy Power FET
N–Channel Enhancement–Mode Silicon Gate

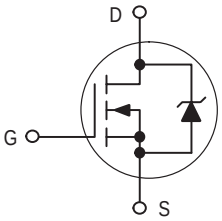
MTP3N50E

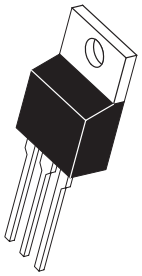
Motorola Preferred Device

TMOS POWER FET
3.0 AMPERES
500 VOLTS
$R_{DS(on)}$ = 3.0 OHMS

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–repetitive ($t_p \leq 50$ μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	3.0 10	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain–to–Source Avalanche Energy — T_J = 25°C — T_J = 100°C Repetitive Pulse Drain–to–Source Avalanche Energy	W_{DSR} (1) W_{DSR} (2)	210 33 5.0	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) V_{DD} = 50 V, I_D = 3.0 A
(2) Pulse Width and frequency is limited by T_J(max) and thermal response

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	500	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 500 V, V_{GS} = 0) (V_{DS} = 400 V, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	— —	0.25 1.0	mAdc
Gate–Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mAdc) (T_J = 125°C)		$V_{GS(th)}$	2.0 1.5	— —	4.0 3.5	Vdc
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$R_{DS(on)}$	—	2.4	3.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 3.0 A) (I_D = 1.5 A, T_J = 100°C)		$V_{DS(on)}$	— —	— —	10 8.0	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.5 Adc)		g_{FS}	1.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	435	—	pF
Output Capacitance		C_{oss}	—	56	—	
Transfer Capacitance		C_{rss}	—	9.2	—	
SWITCHING CHARACTERISTICS*						
Turn–On Delay Time	(V_{DD} = 250 V, $I_D \approx$ 3.0 A, R_G = 18 Ω, R_L = 83 Ω, $V_{GS(on)}$ = 10 V)	$t_{d(on)}$	—	14	—	ns
Rise Time		t_r	—	14	—	
Turn–Off Delay Time		$t_{d(off)}$	—	30	—	
Fall Time		t_f	—	20	—	
Total Gate Charge	(V_{DS} = 400 V, I_D = 3.0 A, V_{GS} = 10 V)	Q_g	—	15	21	nC
Gate–Source Charge		Q_{gs}	—	2.5	—	
Gate–Drain Charge		Q_{gd}	—	10	—	
SOURCE–DRAIN DIODE CHARACTERISTICS*						
Forward On–Voltage	(I_S = 3.0 A)	V_{SD}	—	—	1.5	Vdc
Forward Turn–On Time	(I_S = 3.0 A, di/dt = 100 A/μs)	t_{on}	—	**	—	ns
Reverse Recovery Time		t_{rr}	—	200	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	—	7.5	—	

* Indicates Pulse Test: Pulse Width = 300 μs Max, Duty Cycle ≤ 2.0%.

** Limited by circuit inductance.

TYPICAL ELECTRICAL CHARACTERISTICS

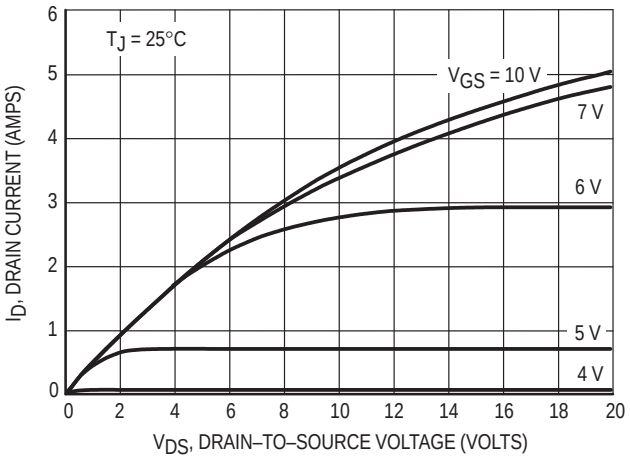


Figure 1. On–Region Characteristics

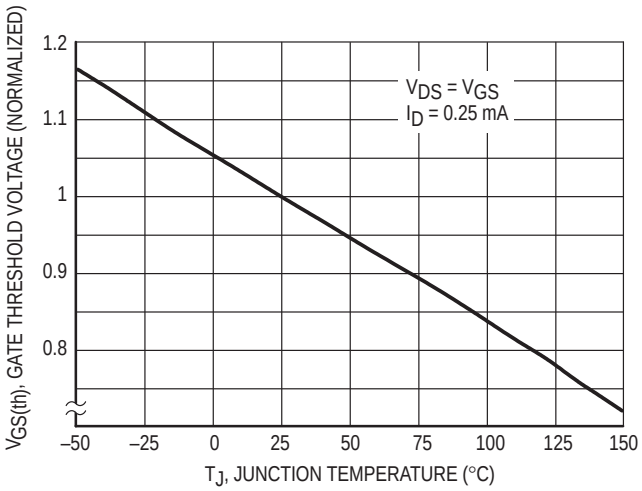


Figure 2. Gate–Threshold Voltage Variation With Temperature

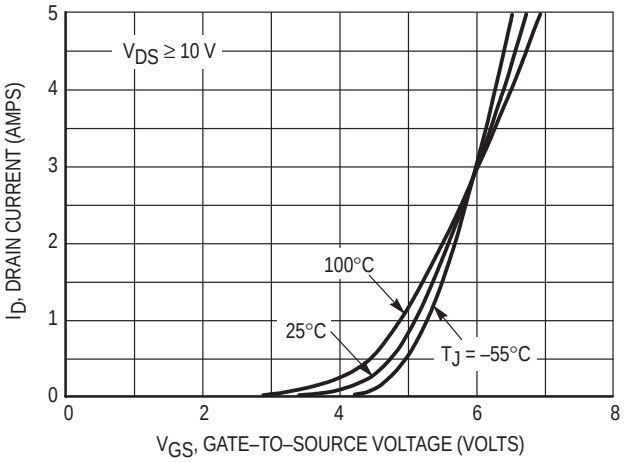


Figure 3. Transfer Characteristics

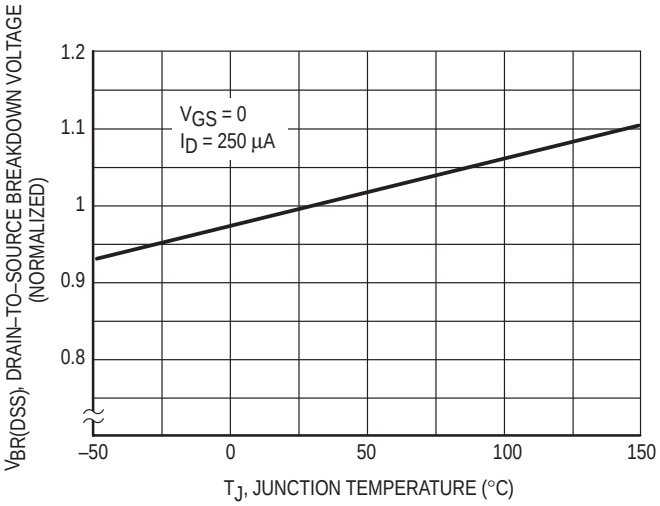


Figure 4. Breakdown Voltage Variation With Temperature

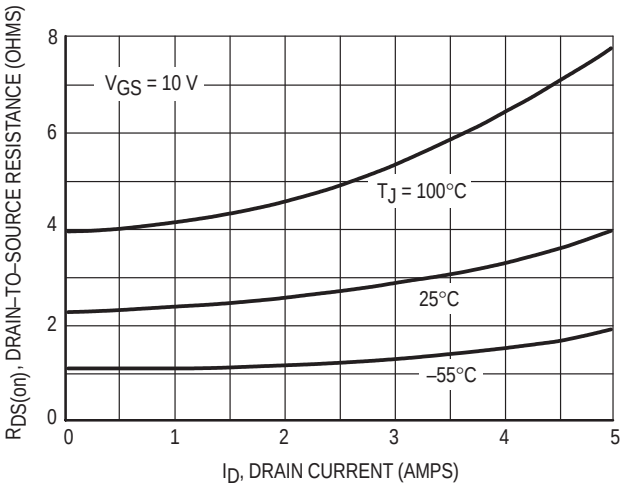


Figure 5. On–Resistance versus Drain Current

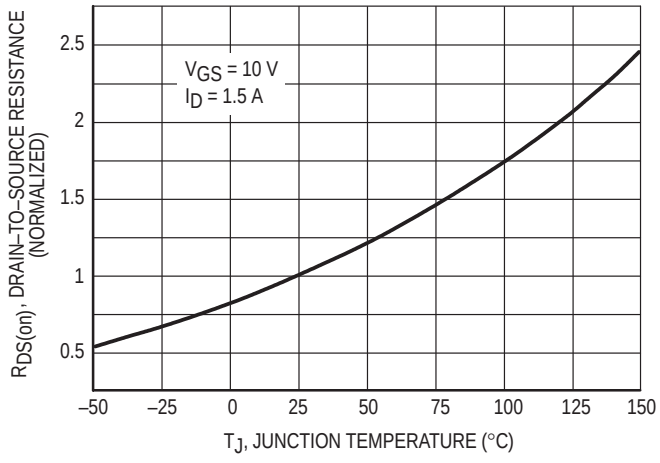


Figure 6. On–Resistance versus Temperature

SAFE OPERATING AREA INFORMATION

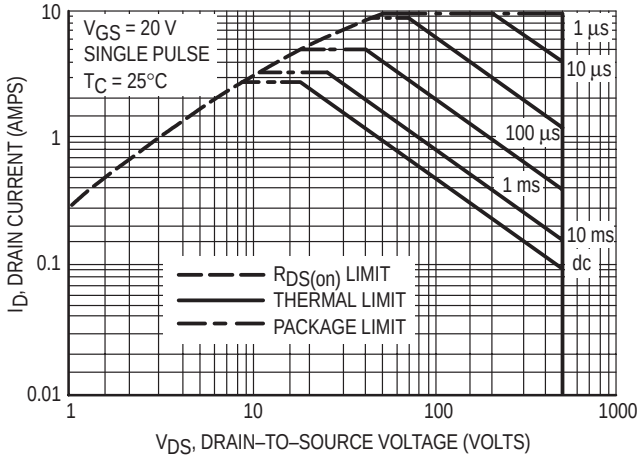


Figure 7. Maximum Rated Forward Biased Safe Operating Area

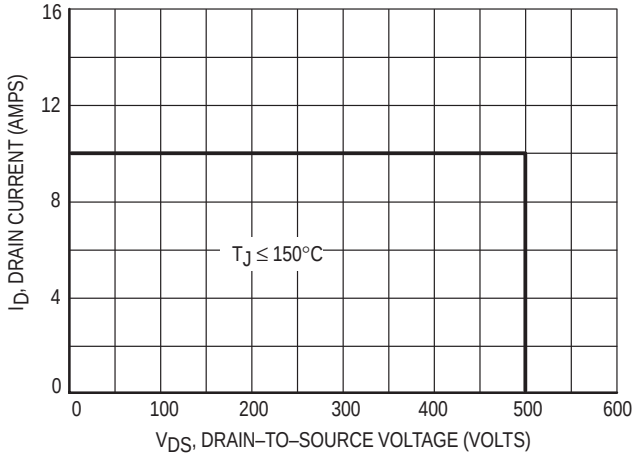


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

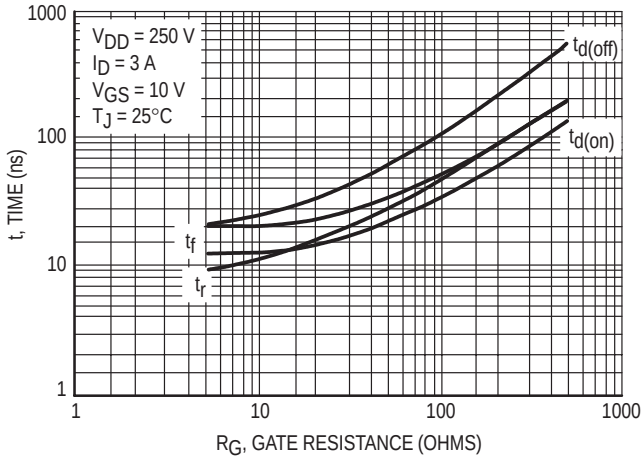


Figure 9. Resistive Switching Time Variation versus Gate Resistance

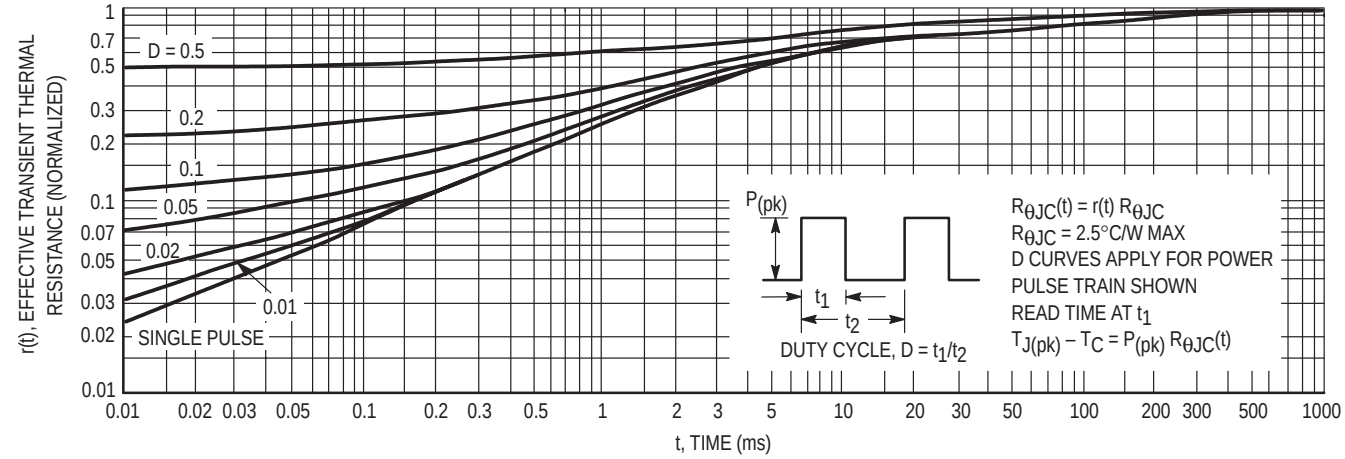


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

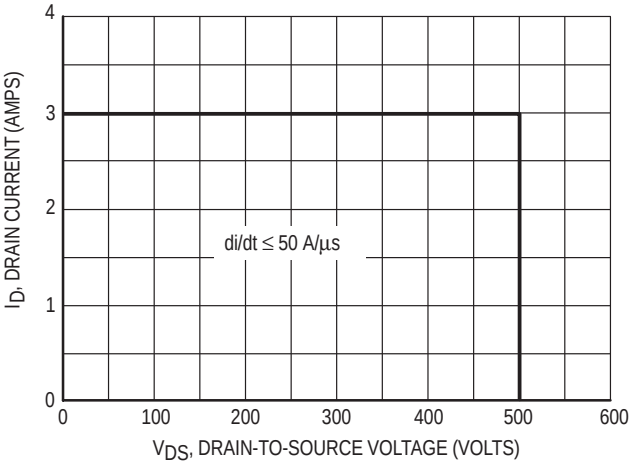


Figure 12. Commutating Safe Operating Area (CSOA)

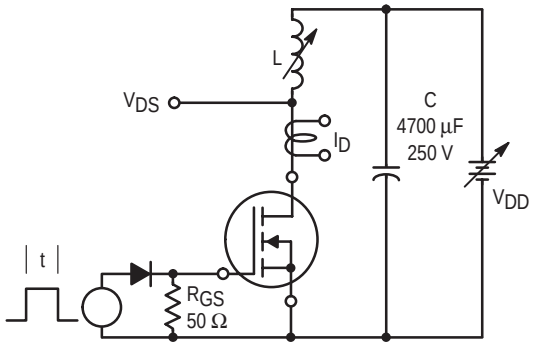


Figure 14. Unclamped Inductive Switching Test Circuit

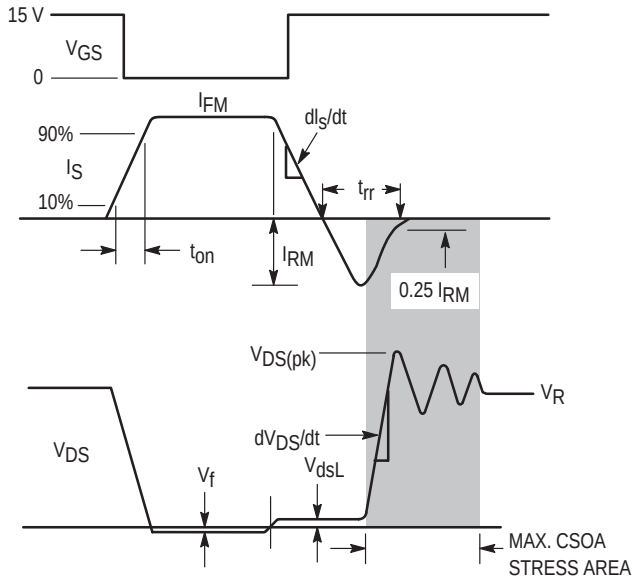


Figure 11. Commutating Waveforms

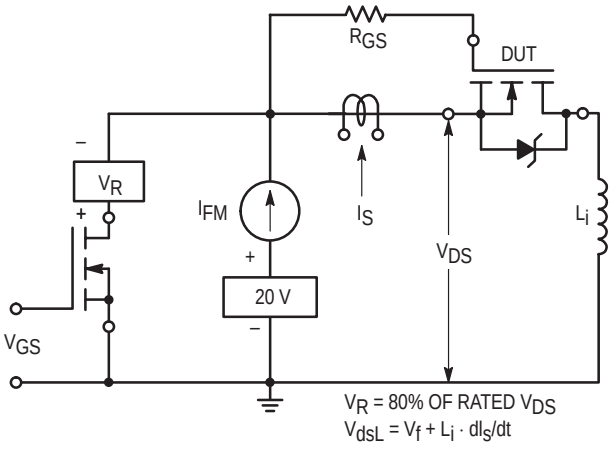


Figure 13. Commutating Safe Operating Area Test Circuit

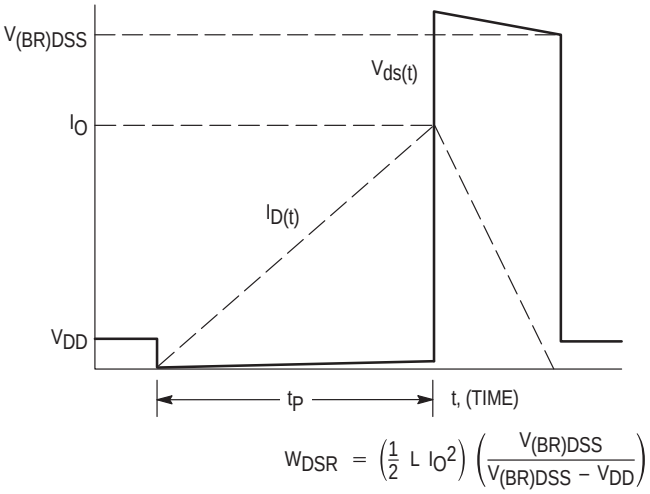


Figure 15. Unclamped Inductive Switching Waveforms

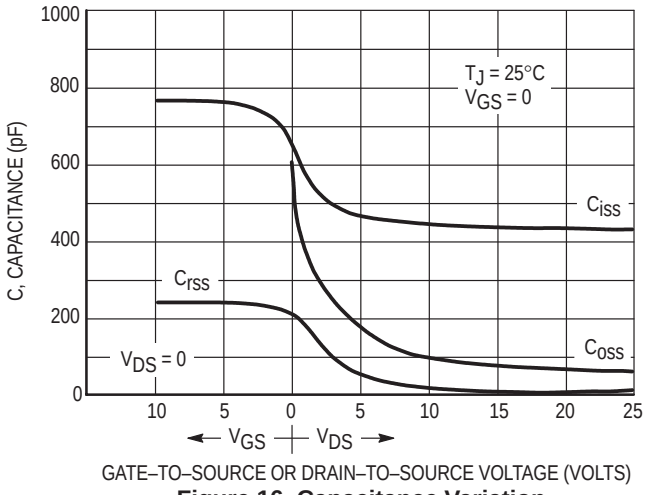


Figure 16. Capacitance Variation

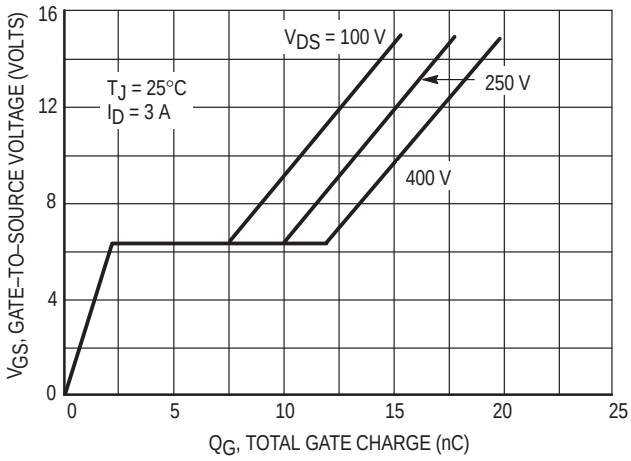
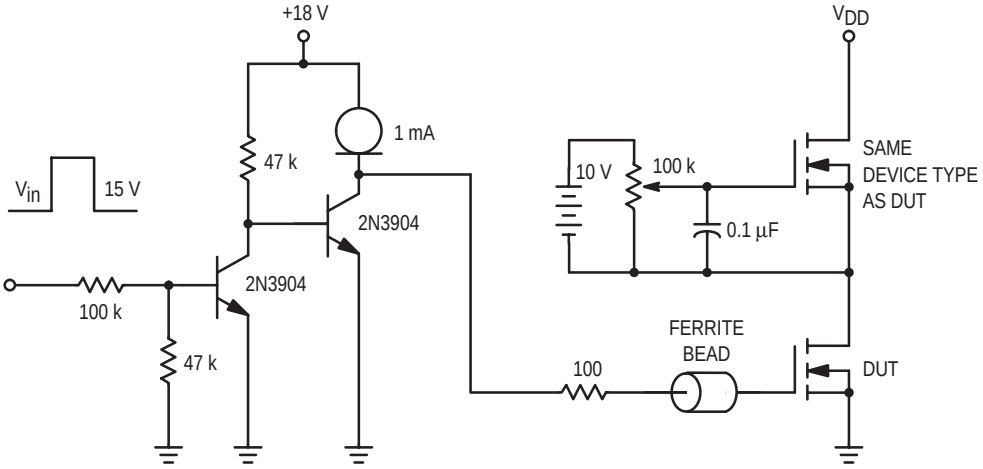


Figure 17. Gate Charge versus Gate–To–Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

Designer's™ Data Sheet
TMOS E-FET ™
High Energy Power FET
N–Channel Enhancement–Mode Silicon Gate

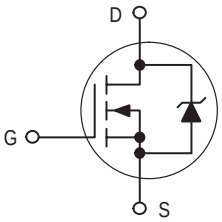
MTP3N60E

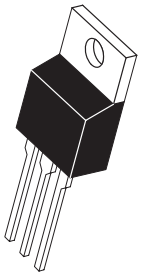
Motorola Preferred Device

TMOS POWER FET
3.0 AMPERES
600 VOLTS
$R_{DS(on)}$ = 2.2 OHMS

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode





CASE 221A–06, Style 5
TO-220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	600	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–repetitive	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	3.0 14	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain–to–Source Avalanche Energy — T_J = 25°C — T_J = 100°C	$W_{DSR(1)}$	290 46	mJ
Repetitive Pulse Drain–to–Source Avalanche Energy	$W_{DSR(2)}$	7.5	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) V_{DD} = 50 V, I_D = 3.0 A
(2) Pulse Width and frequency is limited by T_J(max) and thermal response

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μAdc)	$V_{(BR)DSS}$	600	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 600 V, V_{GS} = 0) (V_{DS} = 480 V, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— —	— —	0.25 1.0	mAdc
Gate–Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) (T_J = 125°C)	$V_{GS(th)}$	2.0 1.5	— —	4.0 3.5	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.5 A)	$R_{DS(on)}$	—	2.1	2.2	Ohms
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 3.0 A) (I_D = 1.5 A, T_J = 100°C)	$V_{DS(on)}$	— —	— —	9.0 7.5	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.5 A)	g_{FS}	1.5	—	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	770	—	pF
Output Capacitance		C_{oss}	—	105	—	
Transfer Capacitance		C_{rss}	—	19	—	
SWITCHING CHARACTERISTICS*					
Turn–On Delay Time	(V_{DD} = 300 V, I_D ≈ 3.0 A, R_L = 100 Ω, R_G = 12 Ω, $V_{GS(on)}$ = 10 V)	$t_{d(on)}$	—	23	—	ns
Rise Time		t_r	—	34	—	
Turn–Off Delay Time		$t_{d(off)}$	—	58	—	
Fall Time		t_f	—	35	—	
Total Gate Charge	(V_{DS} = 420 V, I_D = 3.0 A, V_{GS} = 10 V)	Q_g	—	28	31	nC
Gate–Source Charge		Q_{gs}	—	5.0	—	
Gate–Drain Charge		Q_{gd}	—	17	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage	(I_S = 3.0 A, di/dt = 100 A/μs)	V_{SD}	—	—	1.4	Vdc
Forward Turn–On Time		t_{on}	—	**	—	ns
Reverse Recovery Time		t_{rr}	—	400	—	
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)	L_d	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_s	—	7.5	—	

* Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

** Limited by circuit inductance.

TYPICAL ELECTRICAL CHARACTERISTICS

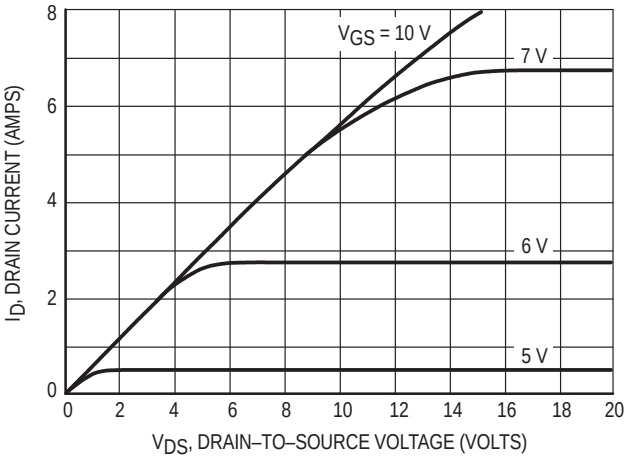


Figure 1. On–Region Characteristics

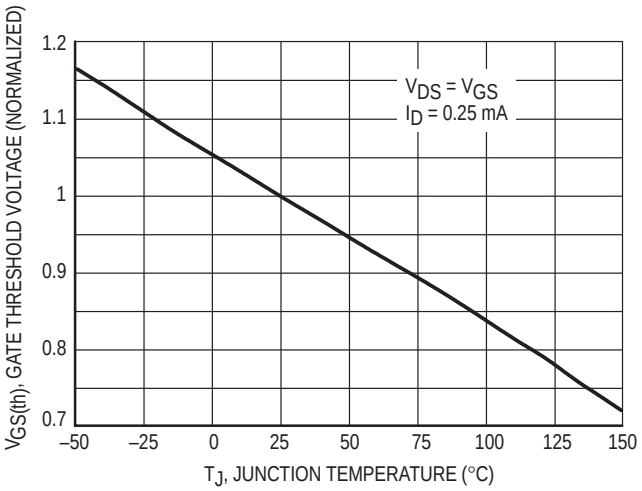


Figure 2. Gate–Threshold Voltage Variation With Temperature

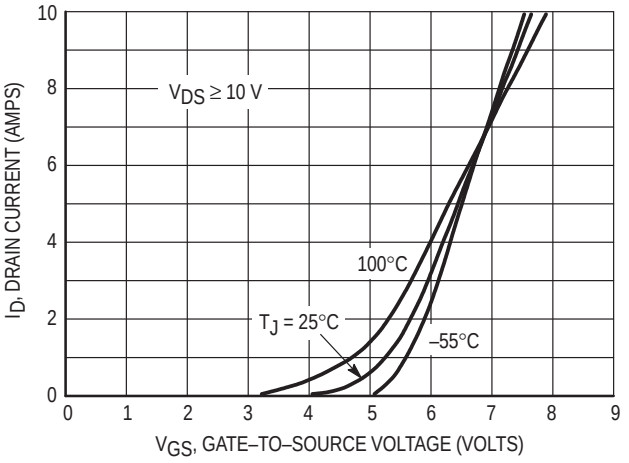


Figure 3. Transfer Characteristics

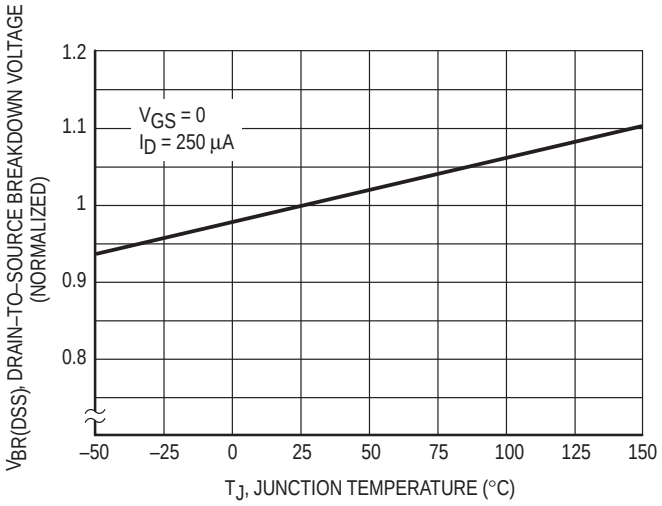


Figure 4. Breakdown Voltage Variation With Temperature

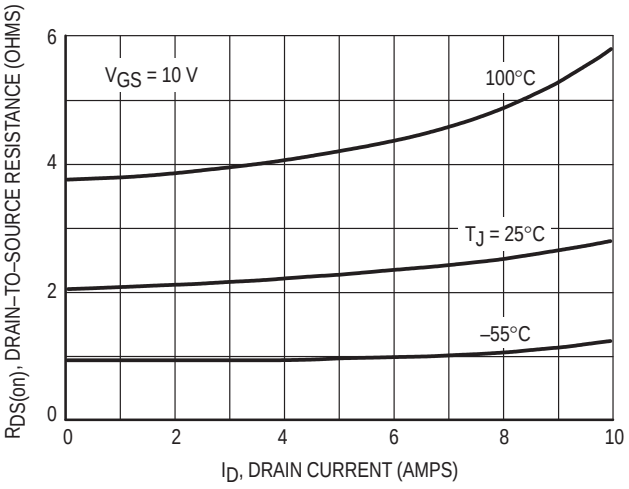


Figure 5. On–Resistance versus Drain Current

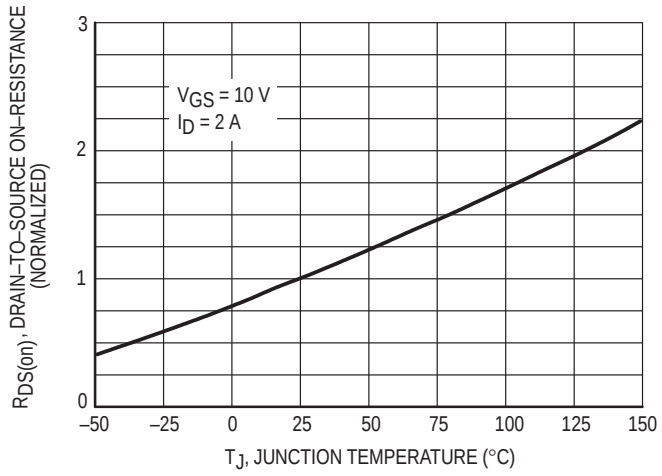


Figure 6. On–Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

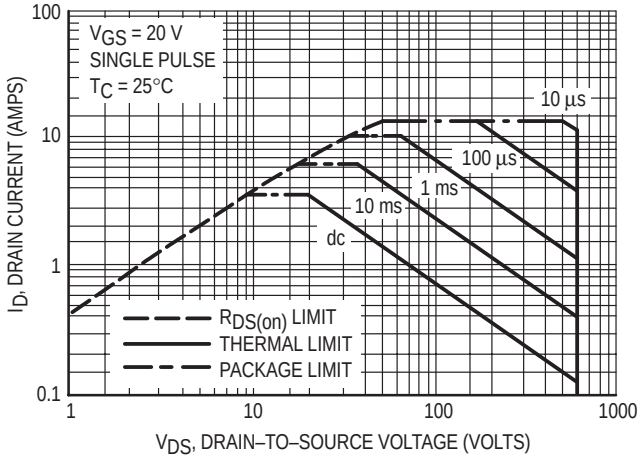


Figure 7. Maximum Rated Forward Biased Safe Operating Area

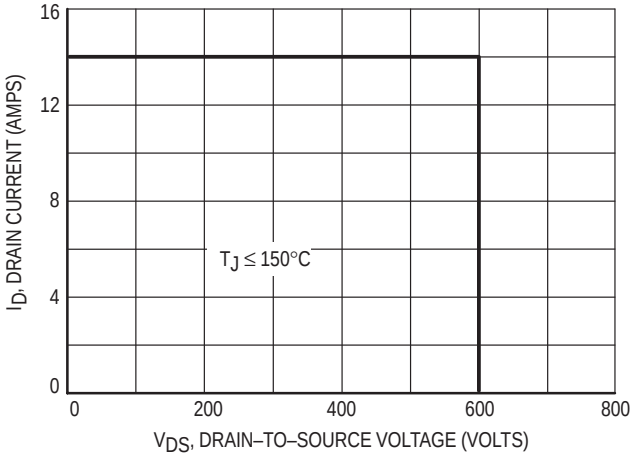


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

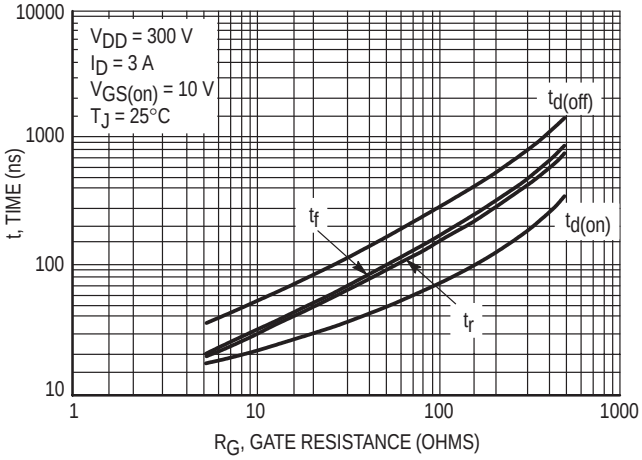


Figure 9. Resistive Switching Time Variation versus Gate Resistance

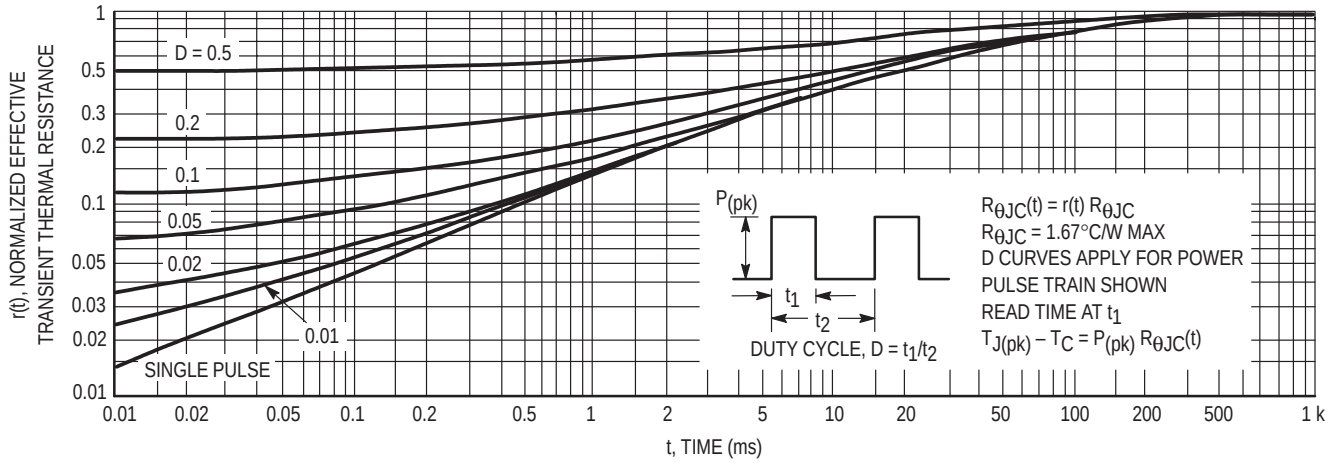


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

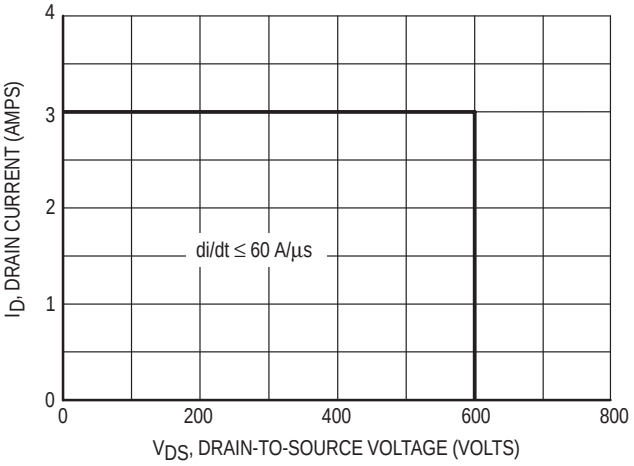


Figure 12. Commutating Safe Operating Area (CSOA)

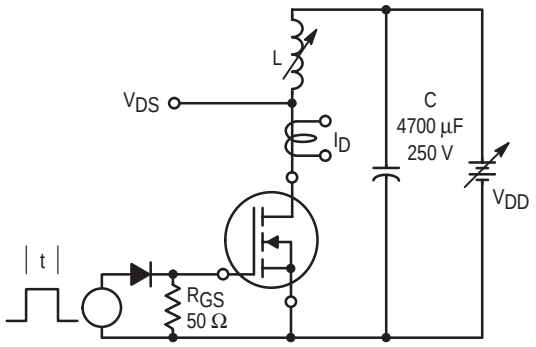


Figure 14. Unclamped Inductive Switching Test Circuit

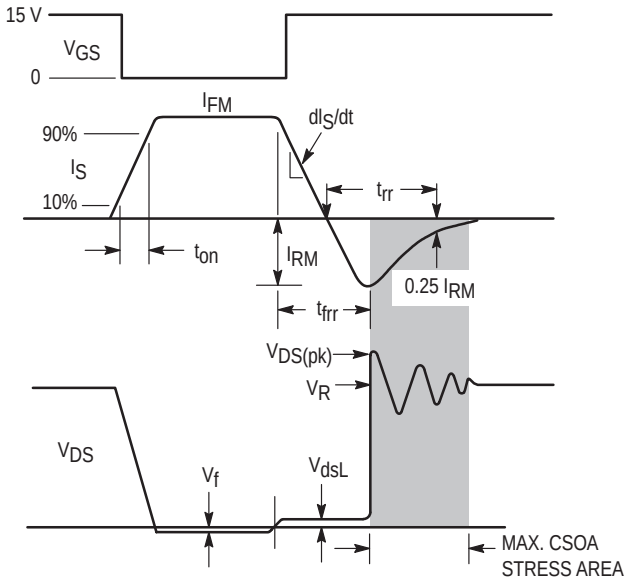


Figure 11. Commutating Waveforms

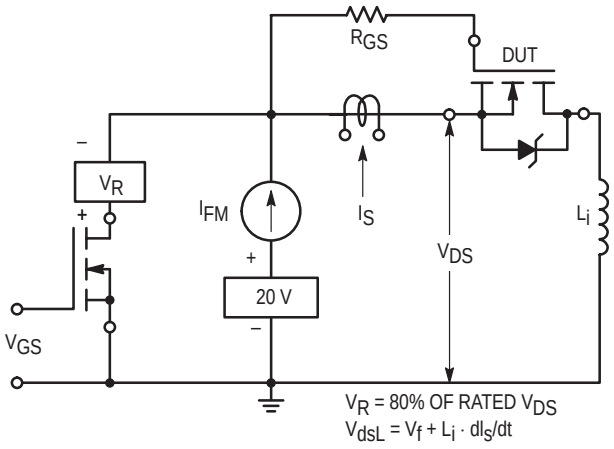


Figure 13. Commutating Safe Operating Area Test Circuit

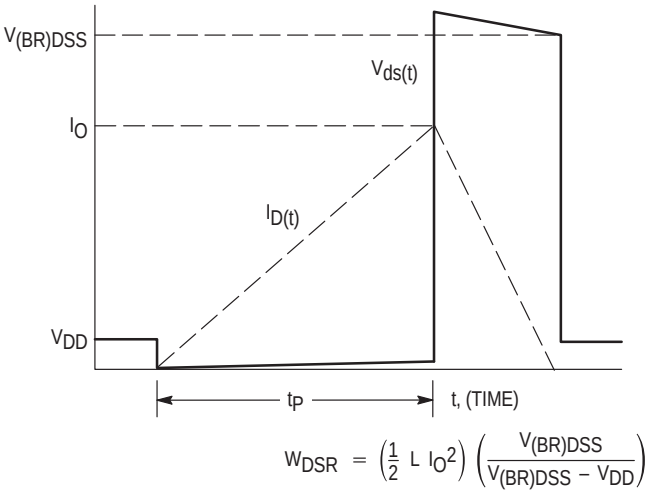


Figure 15. Unclamped Inductive Switching Waveforms

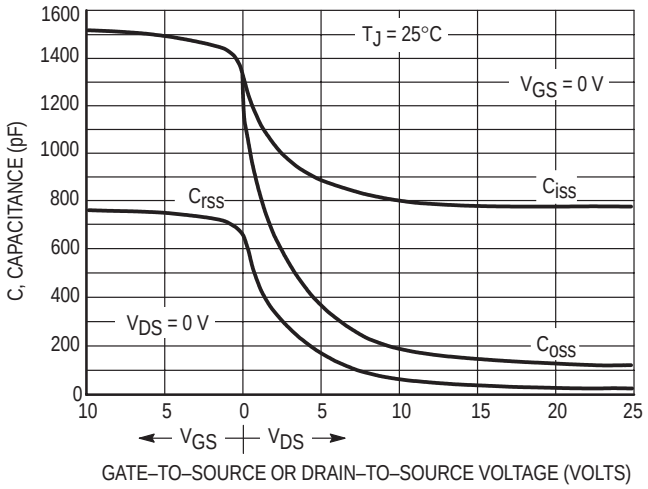


Figure 16. Capacitance Variation

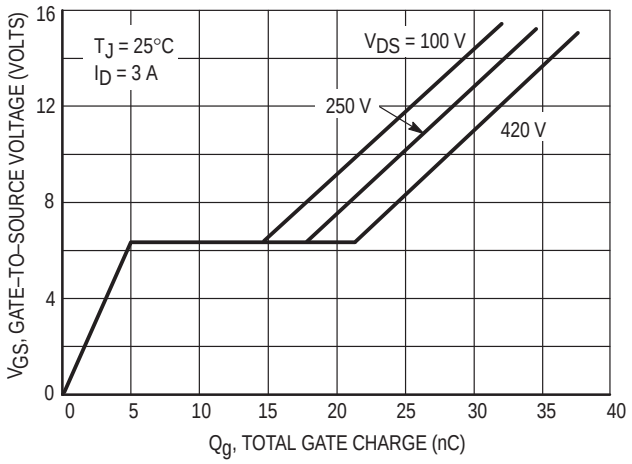
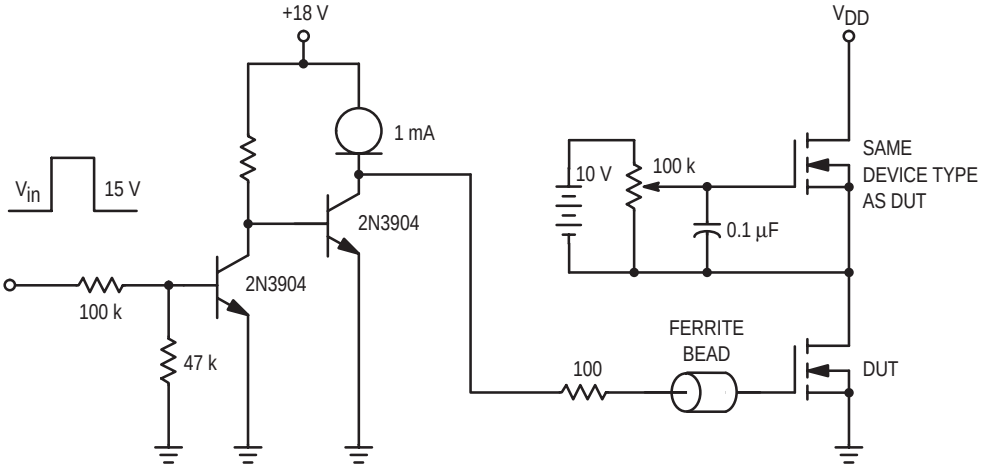


Figure 17. Gate Charge versus Gate–To–Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

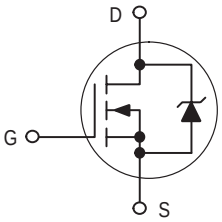
MTP3N100E

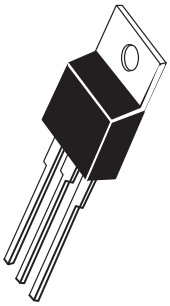
Motorola Preferred Device

TMOS POWER FET
3.0 AMPERES
1000 VOLTS
$R_{DS(on)}$ = 4.0 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	1000	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	1000	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	3.0 2.4 9.0	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 150 Vdc, V_{GS} = 10 Vdc, I_L = 7.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	245	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.00 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	1000 —	— 1.23	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 6.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$R_{DS(on)}$	—	2.96	4.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 3.0 Adc) (I_D = 1.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	4.97 —	12 10	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.5 Adc)		g_{FS}	2.0	3.56	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1316	1800	pF
Output Capacitance		C_{oss}	—	117	260	
Reverse Transfer Capacitance		C_{rss}	—	26	75	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 400 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	13	25	ns
Rise Time		t_r	—	19	40	
Turn–Off Delay Time		$t_{d(off)}$	—	42	90	
Fall Time		t_f	—	33	55	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	32.5	45	nC
		Q_1	—	6.0	—	
		Q_2	—	14.6	—	
		Q_3	—	13.5	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.794 0.63	1.1 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	615	—	ns
		t_a	—	104	—	
		t_b	—	511	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.92	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

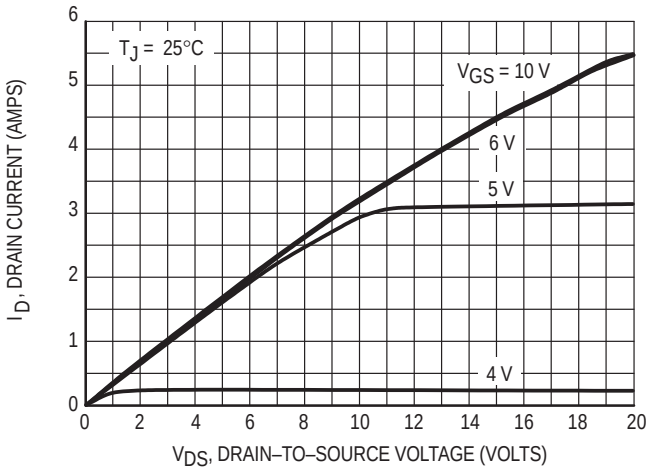


Figure 1. On–Region Characteristics

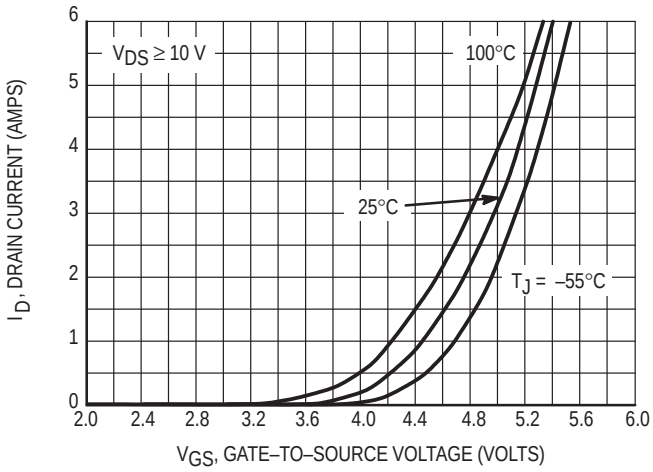


Figure 2. Transfer Characteristics

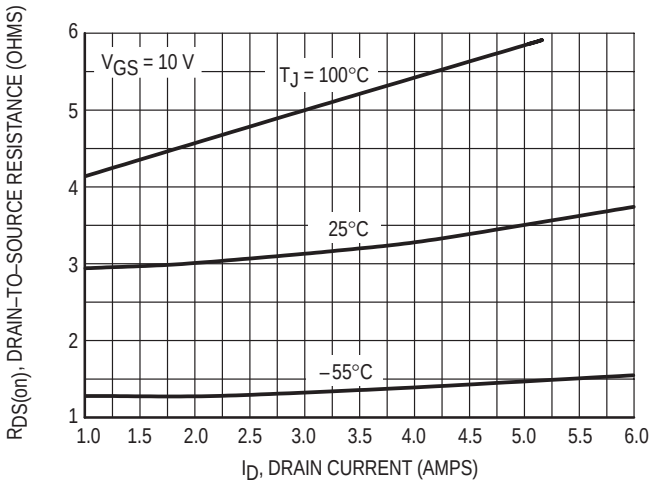


Figure 3. On–Resistance versus Drain Current and Temperature

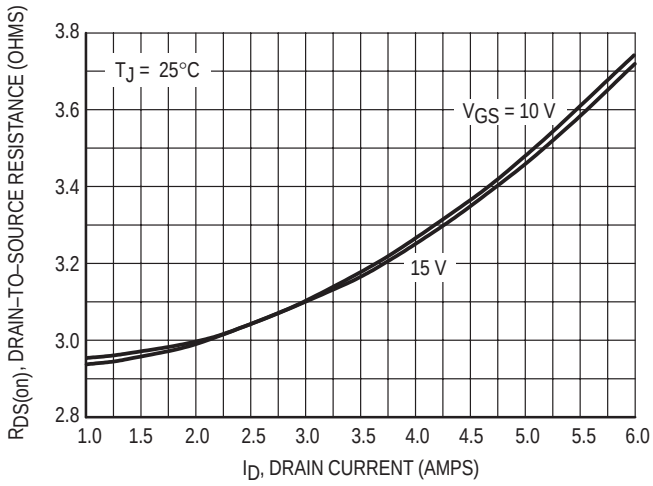


Figure 4. On–Resistance versus Drain Current and Gate Voltage

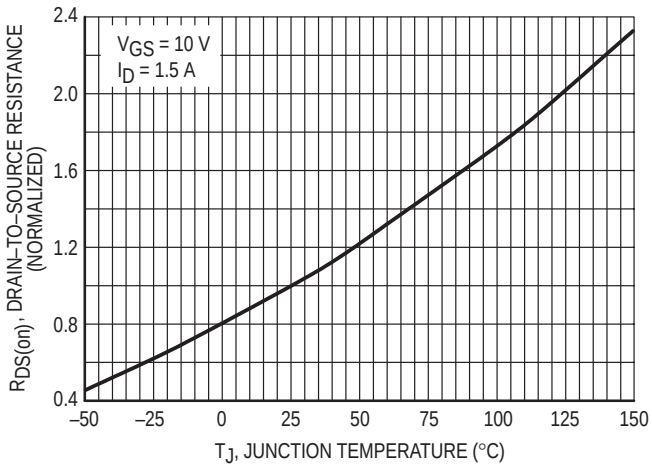


Figure 5. On–Resistance Variation with Temperature

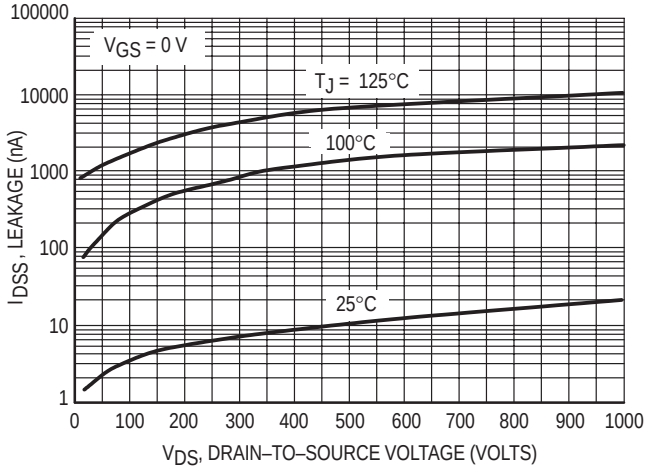


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

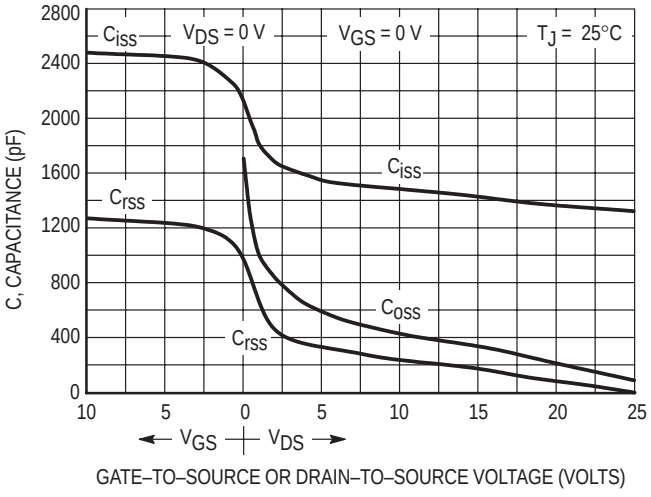


Figure 7a. Capacitance Variation

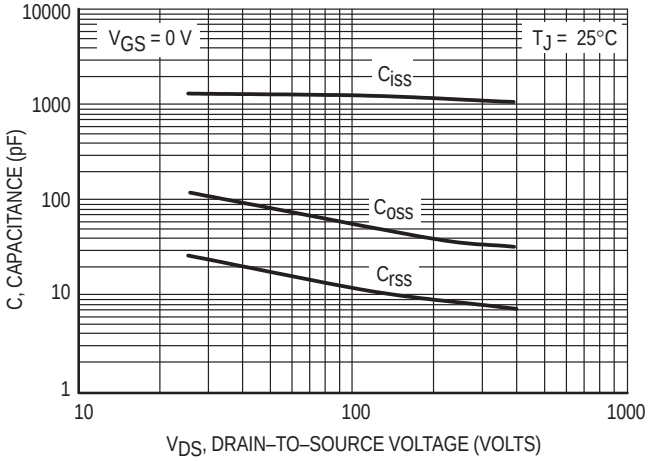


Figure 7b. High Voltage Capacitance Variation

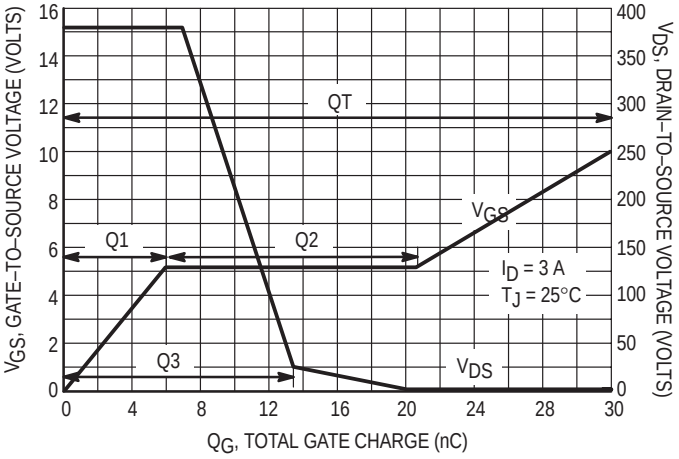


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

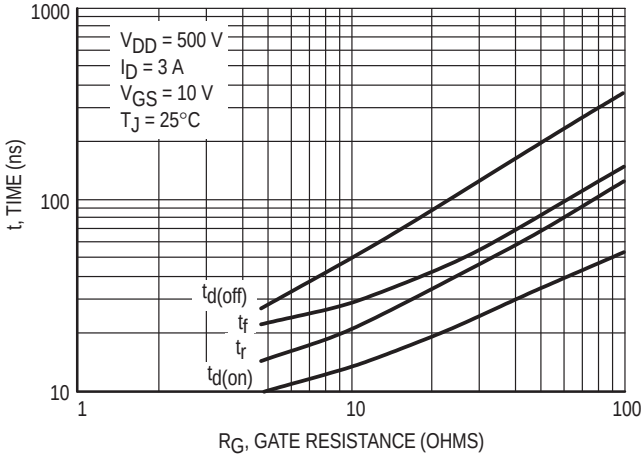


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

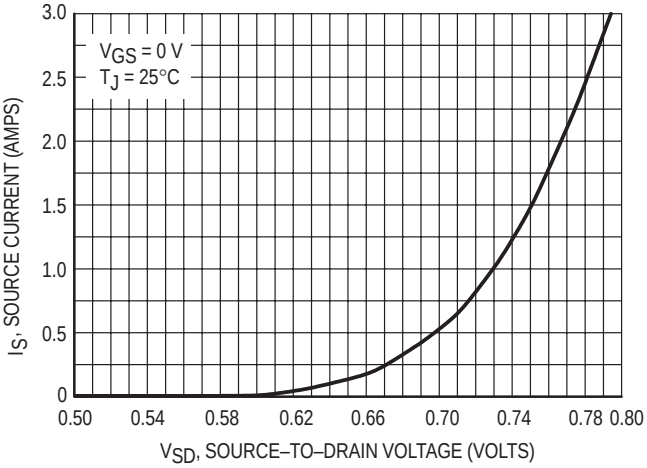


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

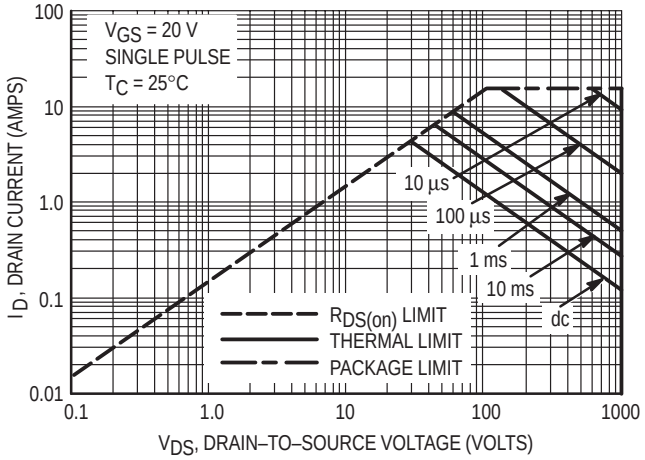


Figure 11. Maximum Rated Forward Biased Safe Operating Area

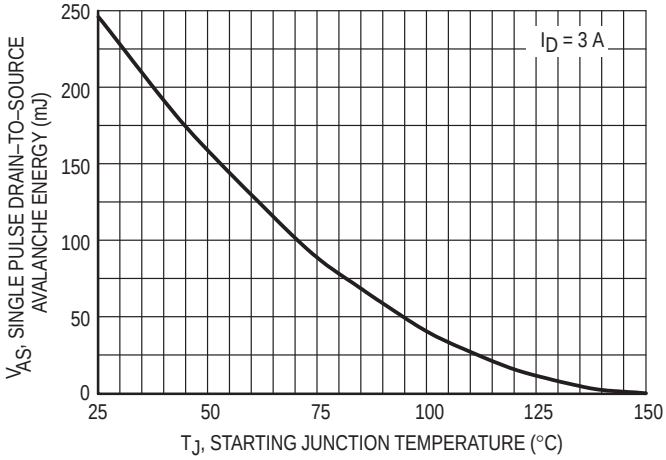


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

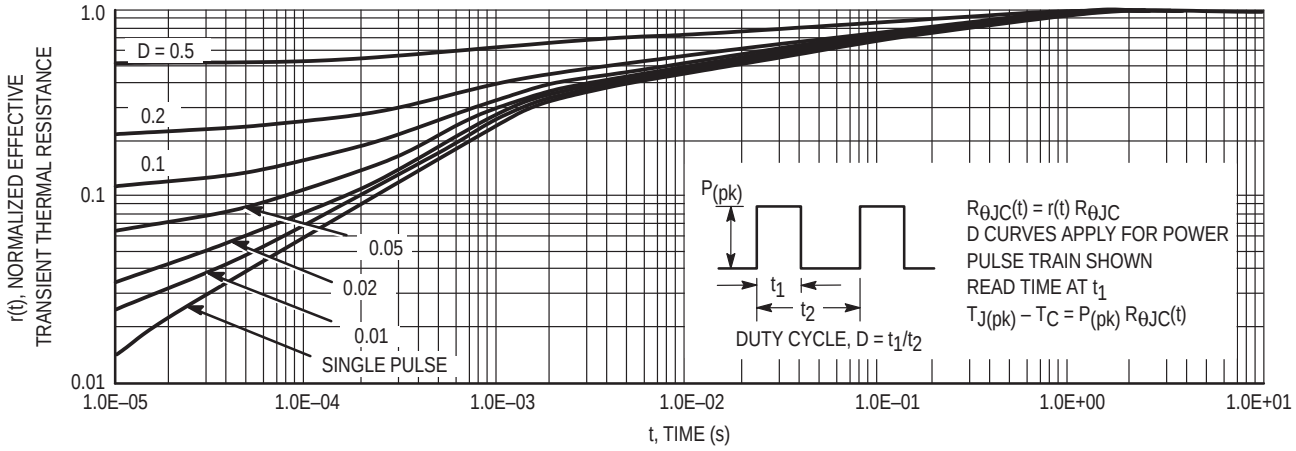


Figure 13. Thermal Response

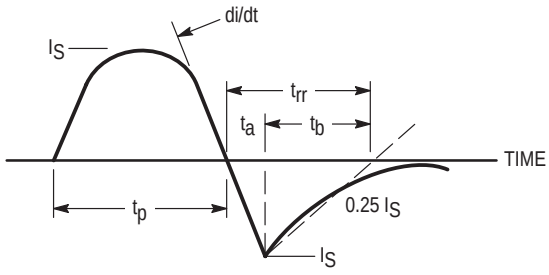


Figure 14. Diode Reverse Recovery Waveform

Designer's Data Sheet

TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

MTP3N120E

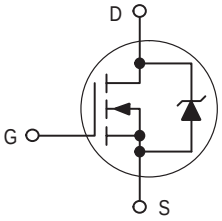
Motorola Preferred Device

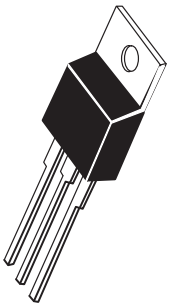
TMOS POWER FET
3.0 AMPERES
1200 VOLTS
$R_{DS(on)}$ = 5.0 OHM

This advanced high–voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls, and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode

* See App. Note AN1327 — Very Wide Input Voltage Range; Off–line Flyback Switching Power Supply





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	1200	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	1200	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 50$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	3.0 2.2 11	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, PEAK I_L = 4.5 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	101	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	1200	—	—	Vdc
Temperature Coefficient (Positive)			—	1.28	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 1200 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 1200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	7.1	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 1.5 Adc)		$R_{DS(on)}$	—	4.0	5.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 3.0 Adc)		$V_{DS(on)}$	—	—	18.0	Vdc
(I_D = 1.5 Adc, T_J = 125°C)			—	—	15.8	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 1.5 Adc)		g_{FS}	2.5	3.1	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	2130	2980	pF
Output Capacitance		C_{oss}	—	1710	2390	
Reverse Transfer Capacitance		C_{rss}	—	932	1860	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 600 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	13.6	30	ns
Rise Time		t_r	—	12.6	30	
Turn–Off Delay Time		$t_{d(off)}$	—	35.8	70	
Fall Time		t_f	—	20.7	40	
Gate Charge	(V_{DS} = 600 Vdc, I_D = 3.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	31	40	nC
		Q_1	—	8.0	—	
		Q_2	—	11	—	
		Q_3	—	14	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 3.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.80	1.0	Vdc
	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.65	—	
Reverse Recovery Time	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	394	—	ns
		t_a	—	118	—	
		t_b	—	276	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.11	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

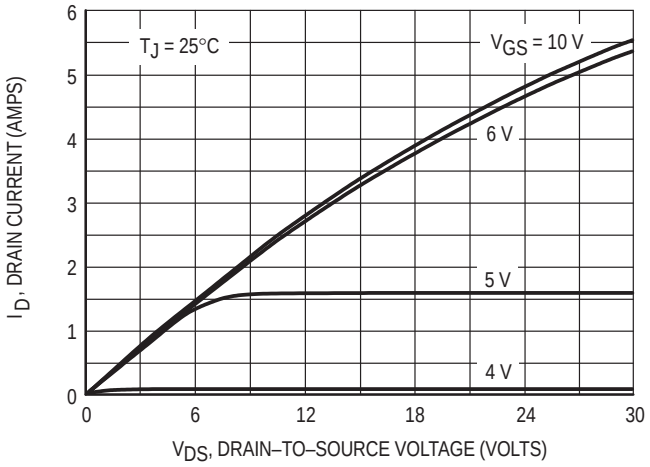


Figure 1. On–Region Characteristics

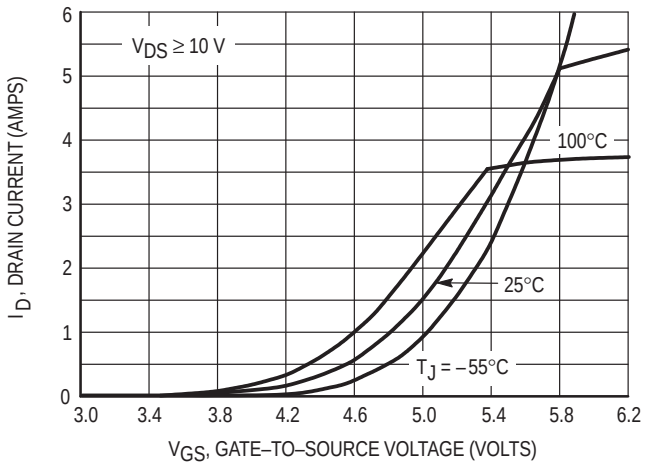


Figure 2. Transfer Characteristics

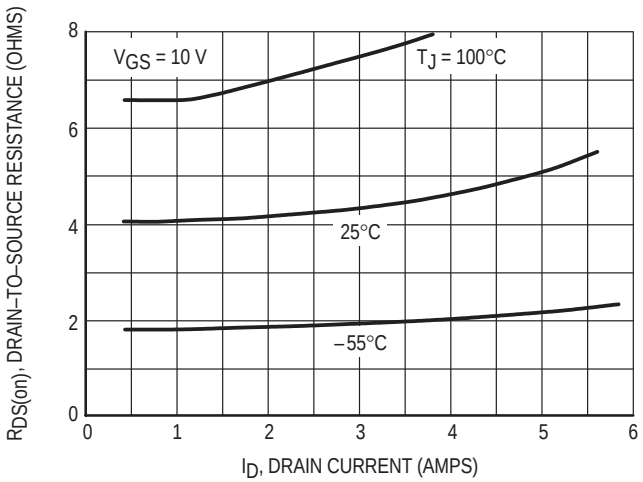


Figure 3. On–Resistance versus Drain Current and Temperature

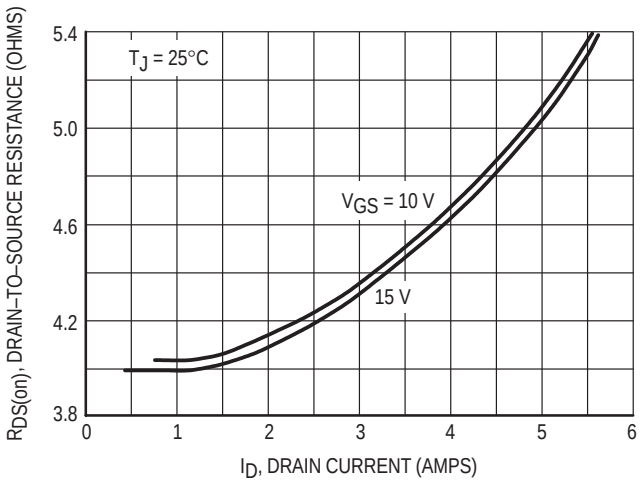


Figure 4. On–Resistance versus Drain Current and Gate Voltage

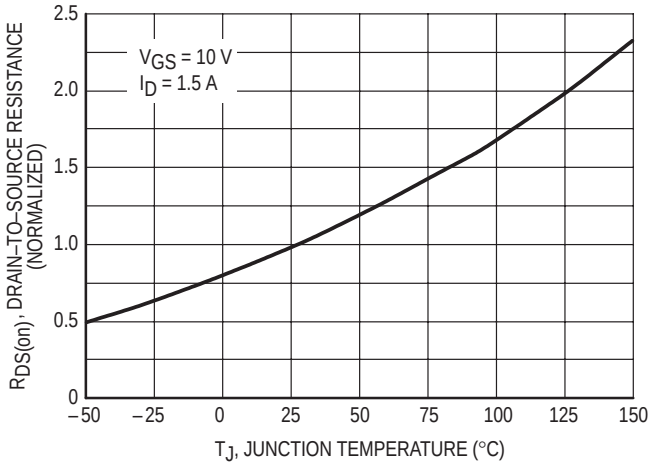


Figure 5. On–Resistance Variation with Temperature

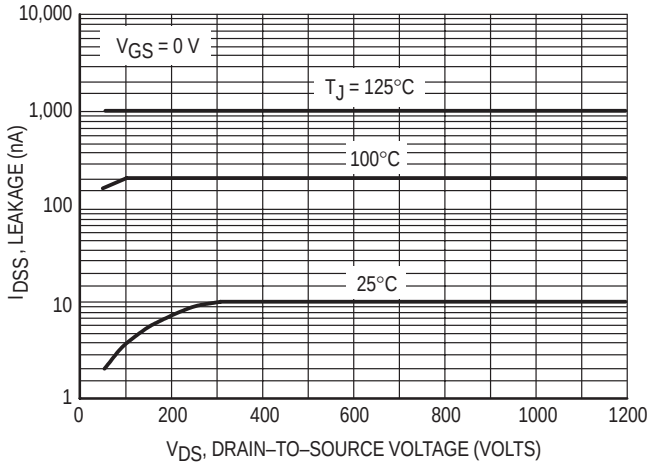


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

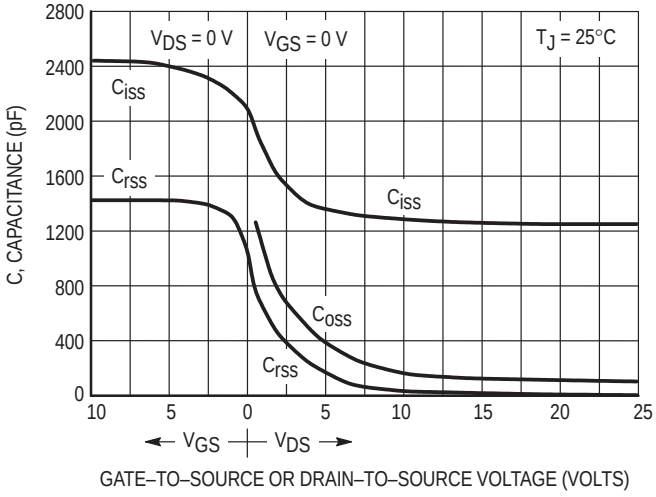


Figure 7a. Capacitance Variation

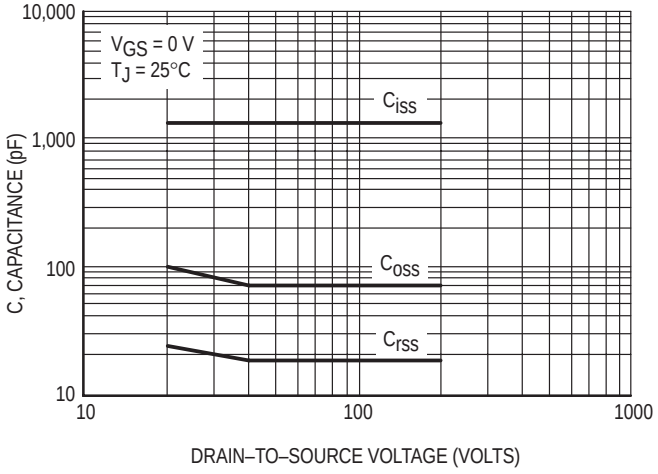


Figure 7b. High Voltage Capacitance Variation

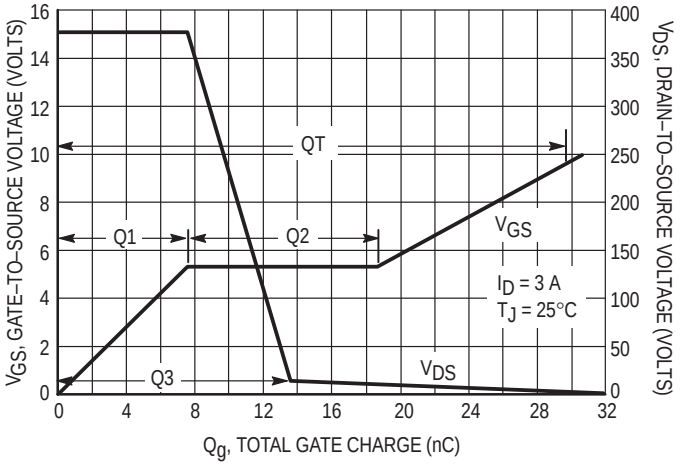


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

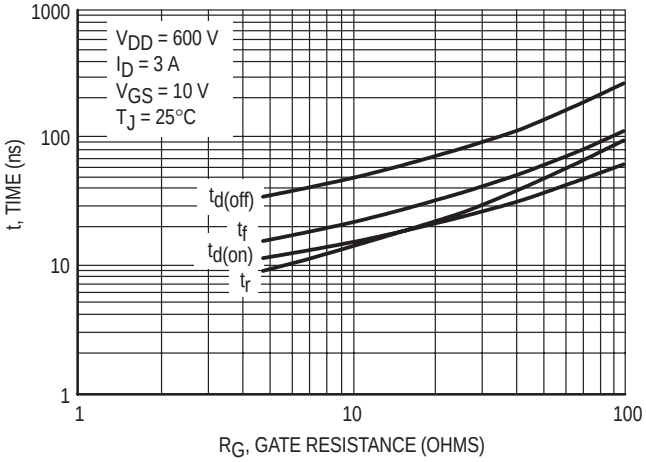


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

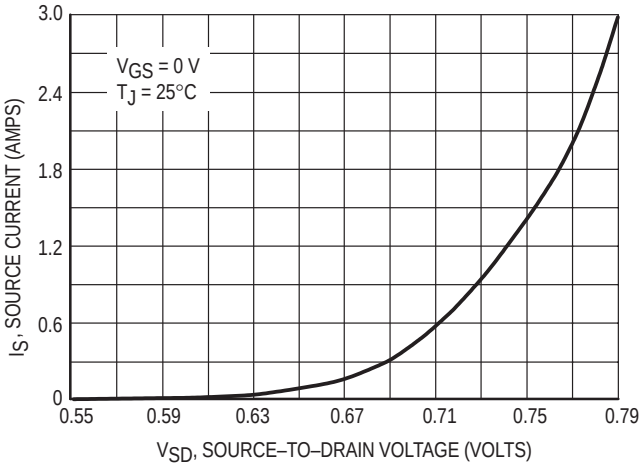


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

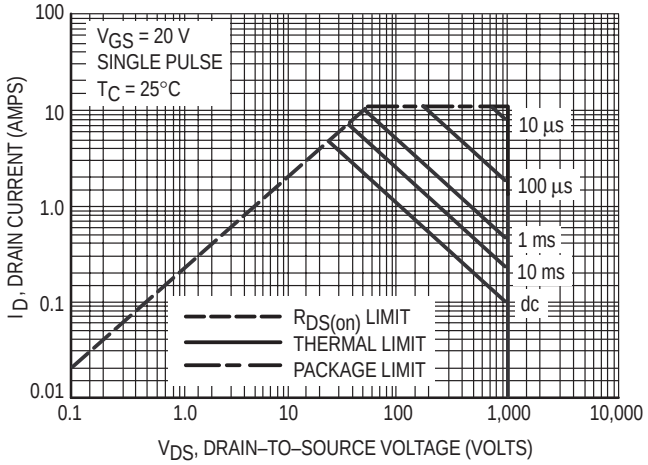


Figure 11. Maximum Rated Forward Biased Safe Operating Area

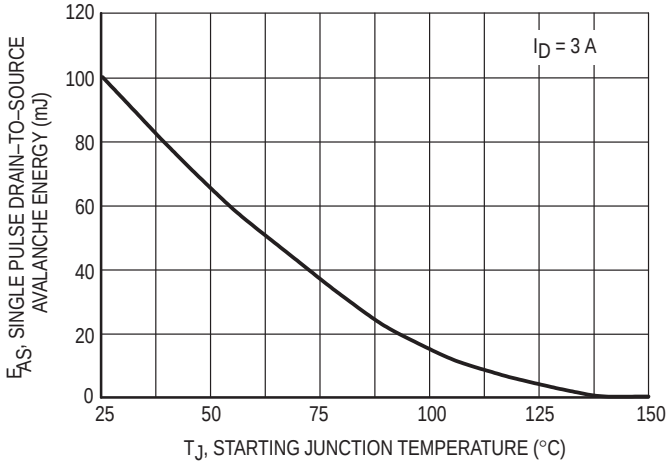


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

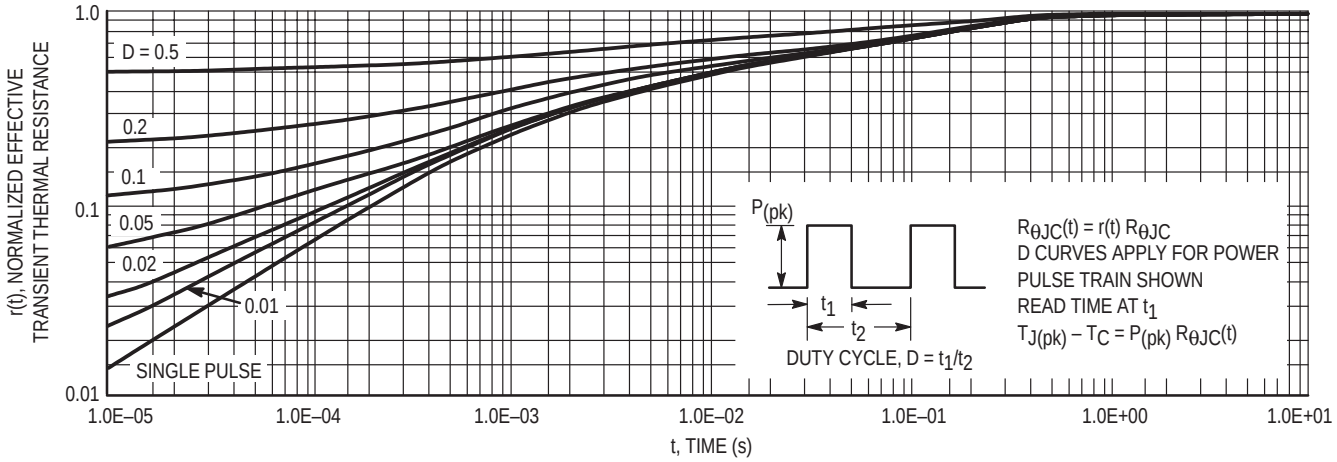


Figure 13. Thermal Response

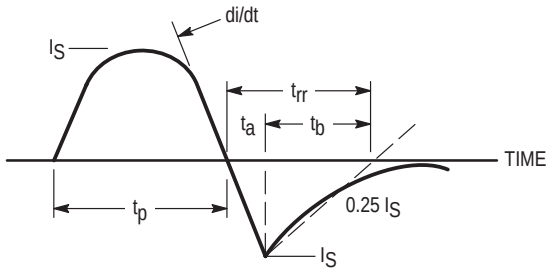


Figure 14. Diode Reverse Recovery Waveform

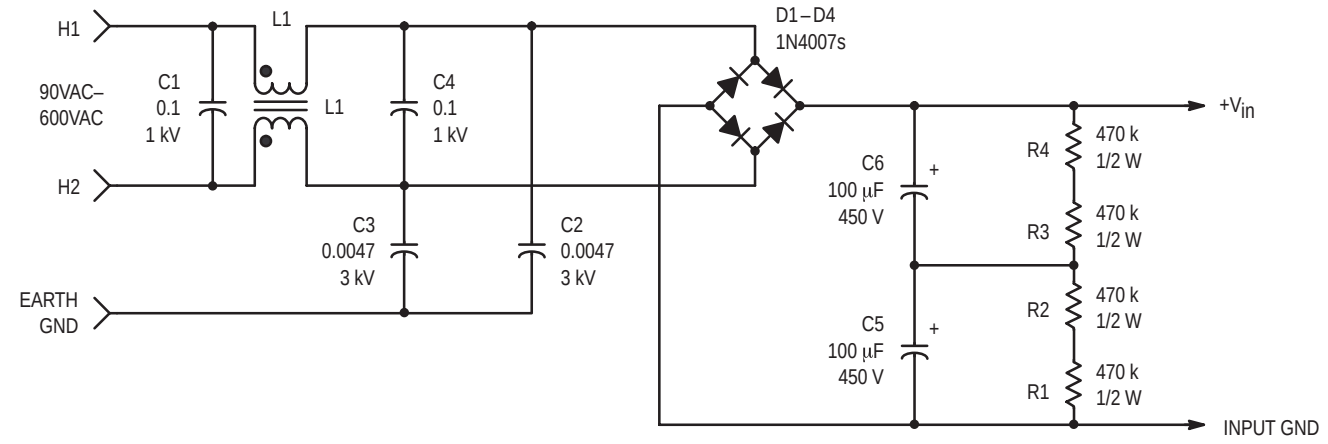


Figure 15. The AC Input/Filter Circuit Section

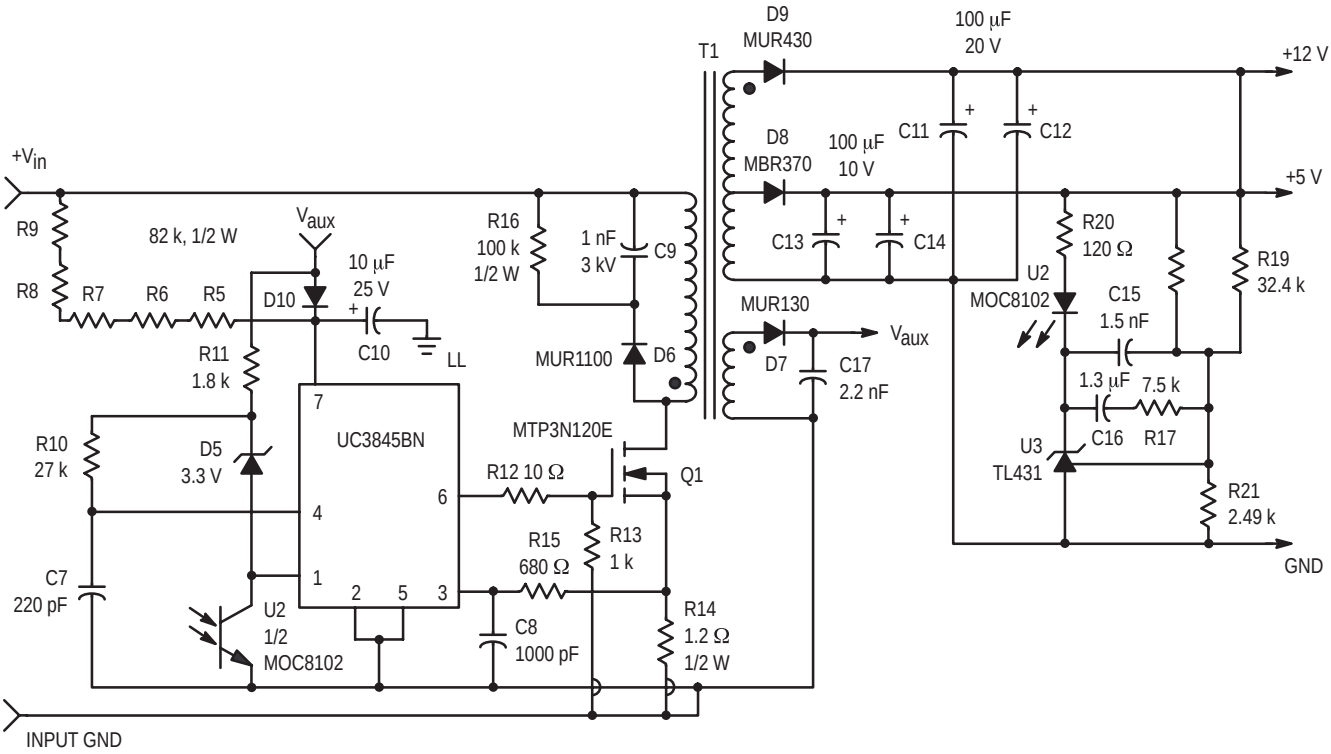


Figure 16. The DC/DC Converter Circuit Section

Product Preview

TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

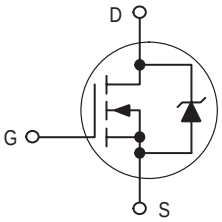
MTP4N40E

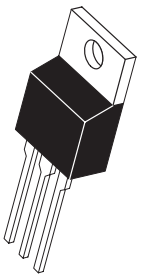
Motorola Preferred Device

TMOS POWER FET
4.0 AMPERES
400 VOLTS
$R_{DS(on)}$ = 1.8 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	400	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \leq$ 10 ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \leq$ 10 μs)	I_D I_D I_{DM}	4.0 2.9 12	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	74 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 8.0 Apk, L = TBD mH, R_G = 25 Ω)	E_{AS}	TBD	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	400 —	— —	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 400 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 400 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 —	4.0 —	Vdc mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc)		$R_{DS(on)}$	—	—	1.8	Ohms
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 4.0 Adc) (I_D = 2.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	12 10	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.0 Adc)		g_{FS}	TBD	TBD	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	TBD	TBD	pF
Output Capacitance		C_{oss}	—	TBD	TBD	
Reverse Transfer Capacitance		C_{rss}	—	TBD	TBD	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 200 Vdc, I_D = 4.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	TBD	TBD	ns
Rise Time		t_r	—	TBD	TBD	
Turn–Off Delay Time		$t_{d(off)}$	—	TBD	TBD	
Fall Time		t_f	—	TBD	TBD	
Gate Charge	(V_{DS} = 320 Vdc, I_D = 4.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	TBD	80	nC
		Q_1	—	TBD	—	
		Q_2	—	TBD	—	
		Q_3	—	TBD	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 4.0 Adc, V_{GS} = 0 Vdc) (I_S = 4.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	TBD TBD	TBD —	Vdc
Reverse Recovery Time	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	TBD	—	ns
		t_a	—	TBD	—	
		t_b	—	TBD	—	
Reverse Recovery Stored Charge		Q_{RR}	—	TBD	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	— —	TBD TBD	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	TBD	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

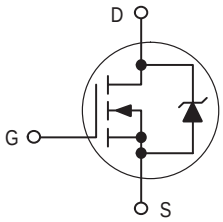
Designer's™ Data Sheet
TMOS E-FET ™
High Energy Power FET
N–Channel Enhancement–Mode Silicon Gate

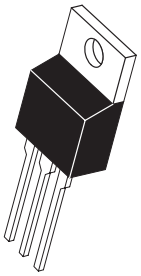
MTP4N50E
Motorola Preferred Device

TMOS POWER FET
4.0 AMPERES
500 VOLTS
$R_{DS(on)}$ = 1.5 OHMS

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–repetitive	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	4.0 10	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain–to–Source Avalanche Energy — T_J = 25°C — T_J = 100°C Repetitive Pulse Drain–to–Source Avalanche Energy	W_{DSR} (1) W_{DSR} (2)	280 44 7.4	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) V_{DD} = 50 V, I_D = 4.0 A
(2) Pulse Width and frequency is limited by T_J(max) and thermal response

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μAdc)		$V_{(BR)DSS}$	500	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 500 V, V_{GS} = 0) (V_{DS} = 400 V, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	— —	0.25 1.0	mAdc
Gate–Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) (T_J = 125°C)		$V_{GS(th)}$	2.0 1.5	— —	4.0 3.5	Vdc
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.0 A)		$R_{DS(on)}$	—	1.3	1.5	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 4.0 Adc) (I_D = 2.0 A, T_J = 100°C)		$V_{DS(on)}$	— —	— —	7.5 6.0	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.0 A)		g_{FS}	1.5	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	775	—	pF
Output Capacitance		C_{oss}	—	84	—	
Transfer Capacitance		C_{rss}	—	19	—	
SWITCHING CHARACTERISTICS*						
Turn–On Delay Time	(V_{DD} = 250 V, I_D ≈ 4.0 A, R_G = 12 Ω, R_L = 62 Ω, $V_{GS(on)}$ = 10 V)	$t_{d(on)}$	—	24	—	ns
Rise Time		t_r	—	34	—	
Turn–Off Delay Time		$t_{d(off)}$	—	60	—	
Fall Time		t_f	—	36	—	
Total Gate Charge	(V_{DS} = 400 V, I_D = 4.0 A, V_{GS} = 10 V)	Q_g	—	27	32	nC
Gate–Source Charge		Q_{gs}	—	3.5	—	
Gate–Drain Charge		Q_{gd}	—	14	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 4.0 A, di/dt = 100 A/μs)	V_{SD}	—	—	1.4	Vdc
Forward Turn–On Time		t_{on}	—	**	—	ns
Reverse Recovery Time		t_{rr}	—	—	760	
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	—	7.5	—	

* Indicates Pulse Test: Pulse Width = 300 μs Max, Duty Cycle ≤ 2.0%.

** Limited by circuit inductance.

TYPICAL ELECTRICAL CHARACTERISTICS

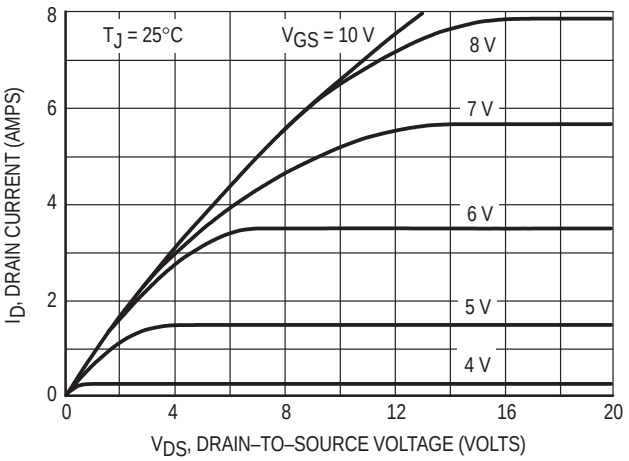


Figure 1. On–Region Characteristics

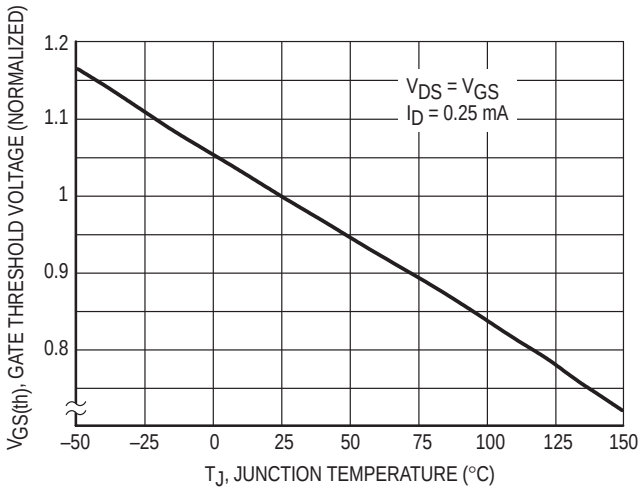


Figure 2. Gate–To–Source Threshold Voltage Variation With Temperature

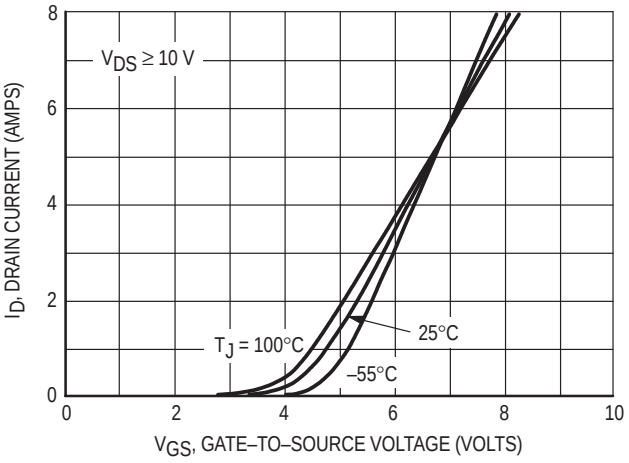


Figure 3. Transfer Characteristics

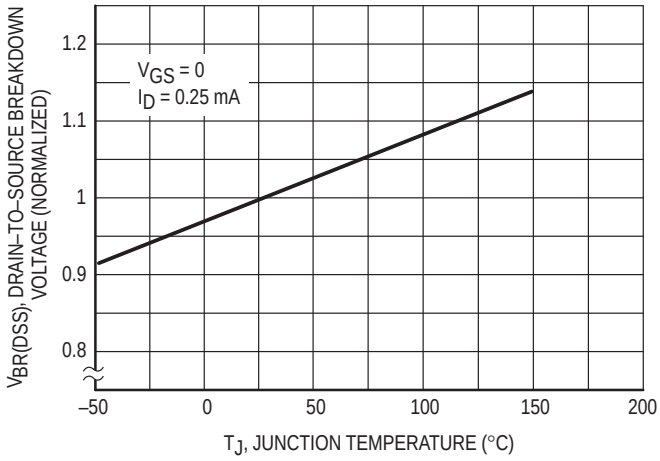


Figure 4. Breakdown Voltage Variation With Temperature

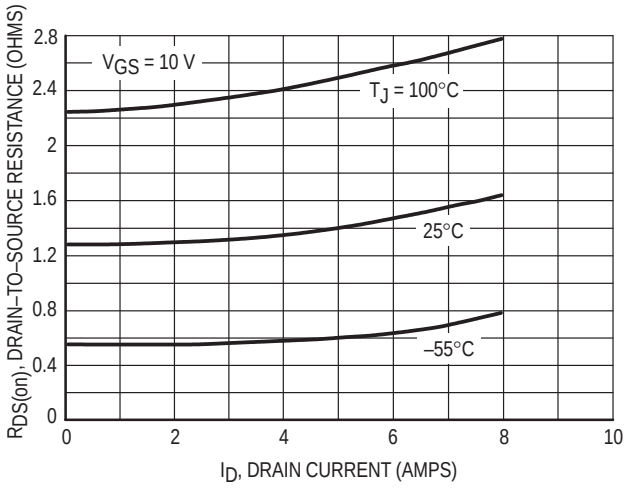


Figure 5. On–Resistance versus Drain Current

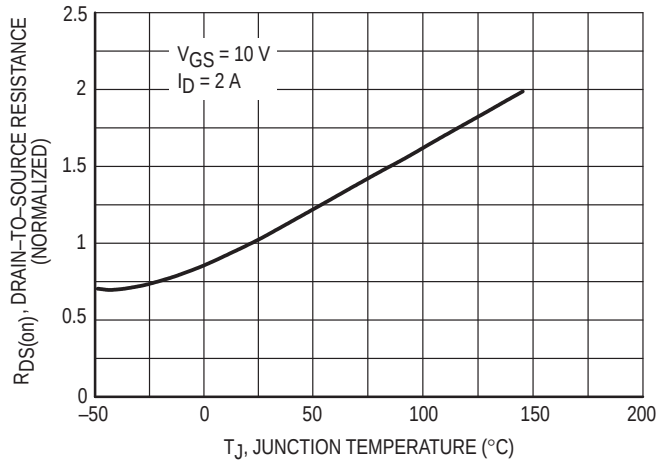


Figure 6. On–Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

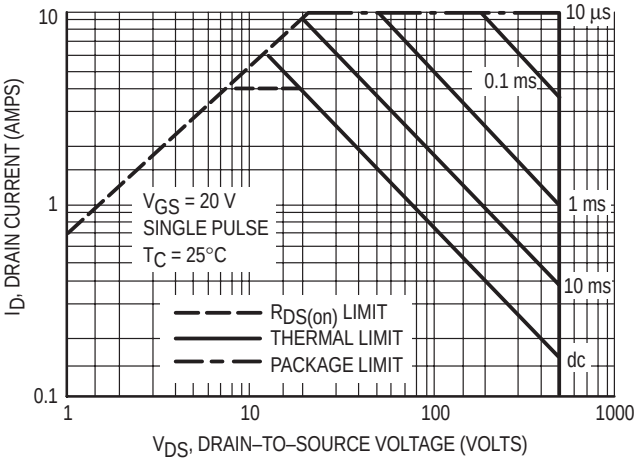


Figure 7. Maximum Rated Forward Biased Safe Operating Area

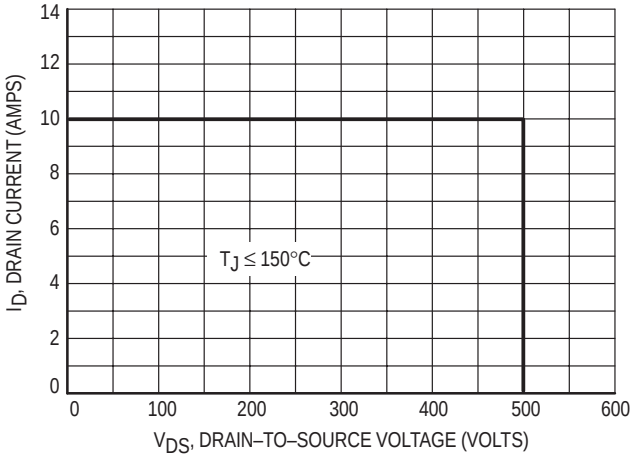


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

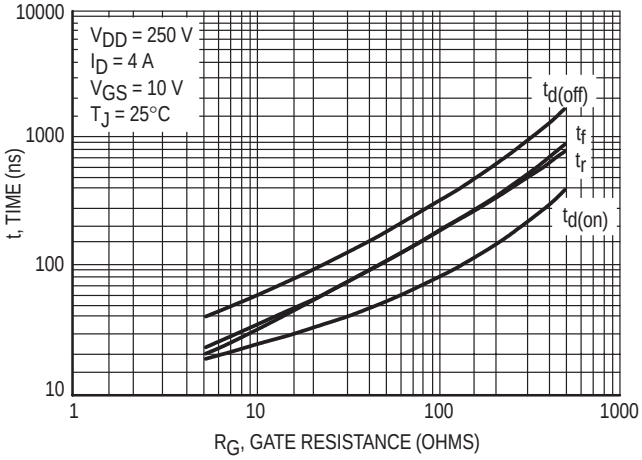


Figure 9. Resistive Switching Time Variation versus Gate Resistance

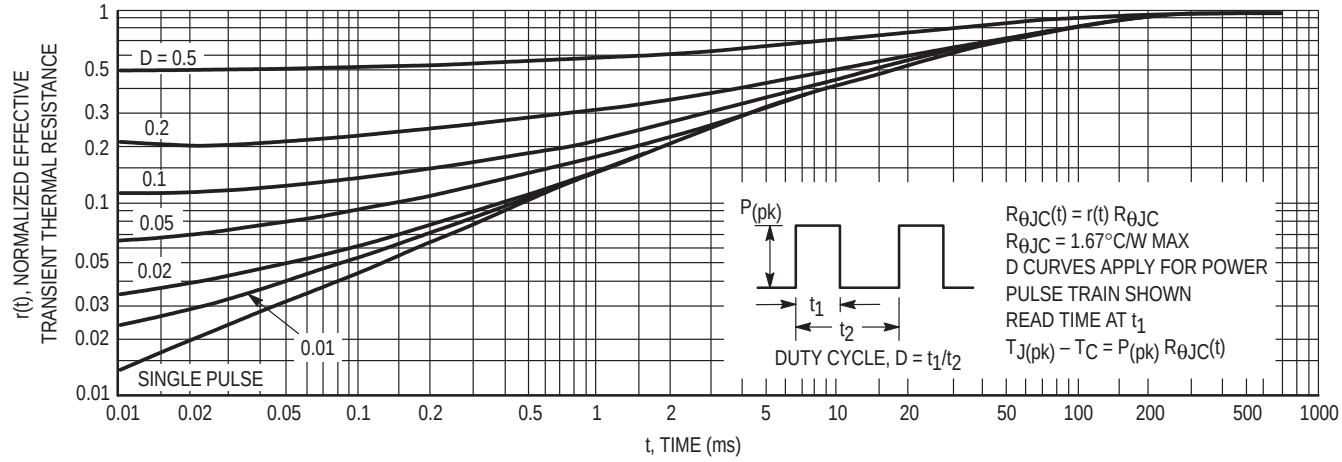


Figure 10. Thermal Response

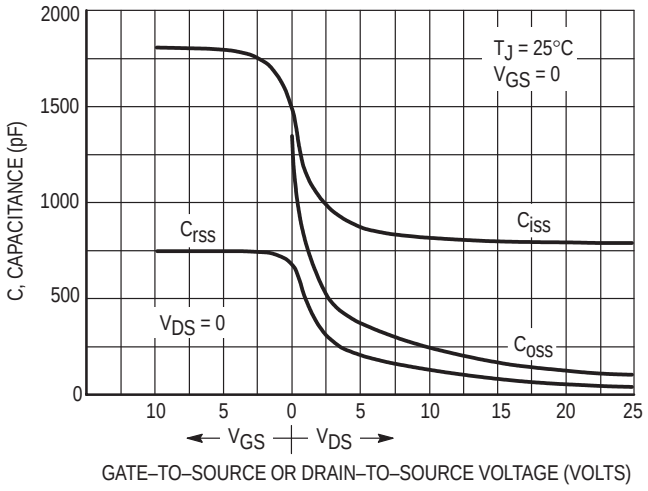


Figure 11. Capacitance Variation

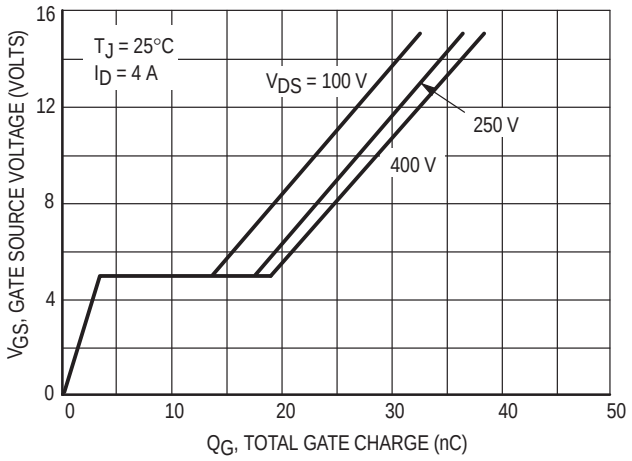


Figure 12. Gate Charge versus Gate–To–Source Voltage

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 14 defines the limits of safe operation for commutated source–drain current versus re–applied drain voltage when the source–drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 13 are present. Full or half–bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source–drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

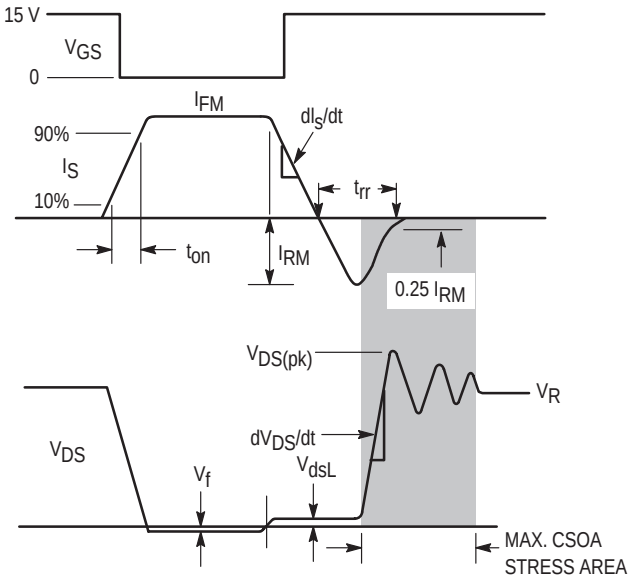


Figure 15. Commutating Waveforms

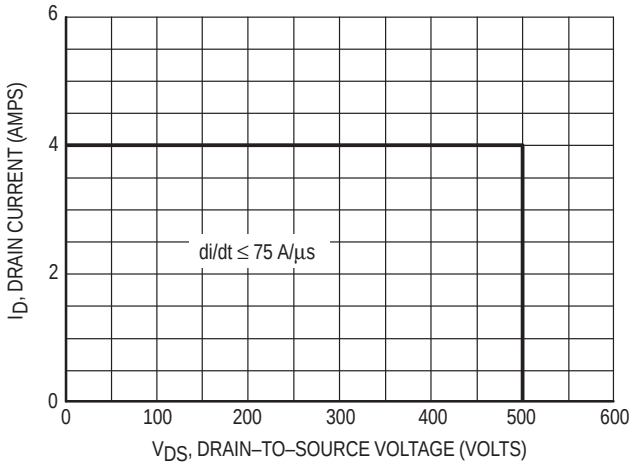


Figure 13. Commutating Safe Operating Area (CSOA)

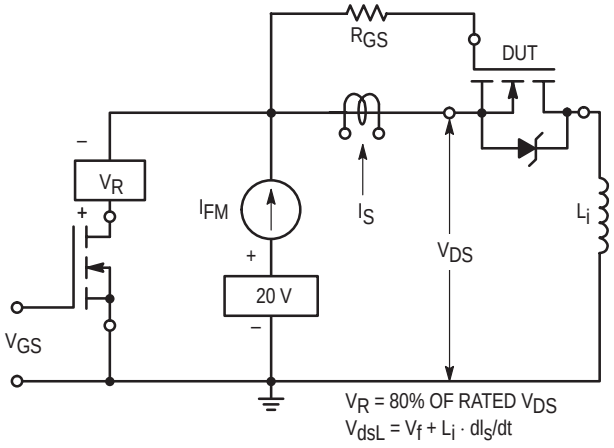


Figure 14. Commutating Safe Operating Area Test Circuit

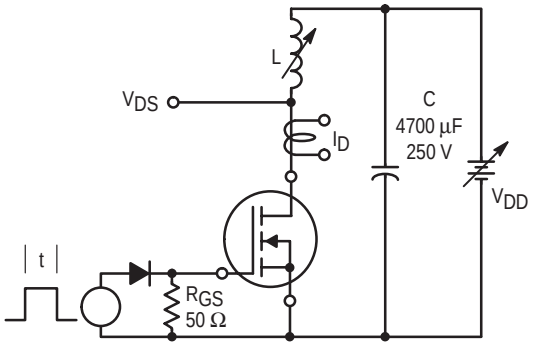


Figure 16. Unclamped Inductive Switching Test Circuit

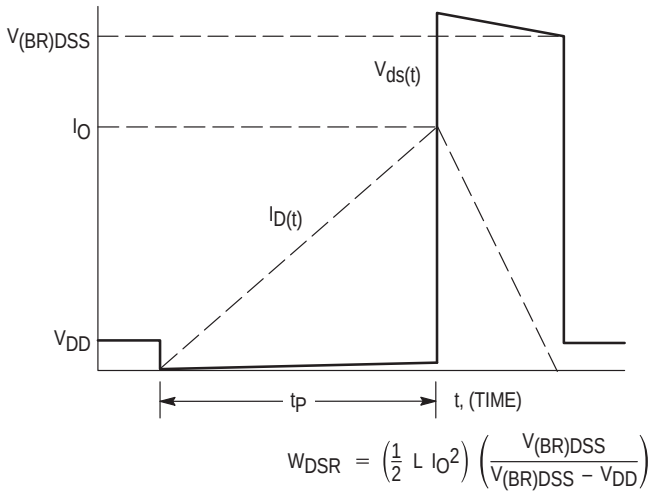
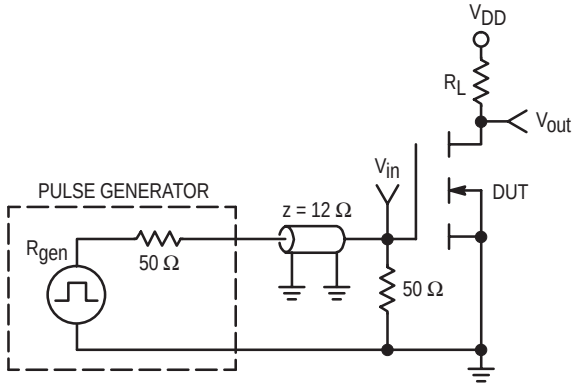


Figure 17. Unclamped Inductive Switching Waveforms

RESISTIVE SWITCHING



* Note: The Mirror is shorted to the Kelvin terminal for this test.

Figure 18. Switching Test Circuit

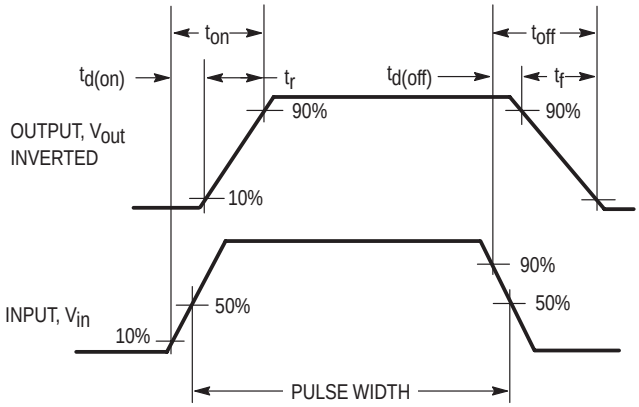
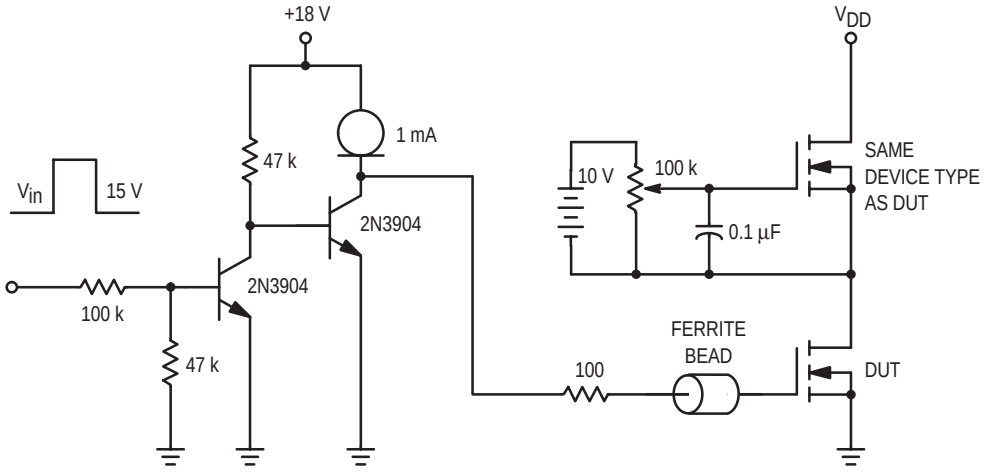


Figure 19. Switching Waveforms



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

Figure 20. Gate Charge Test Circuit

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

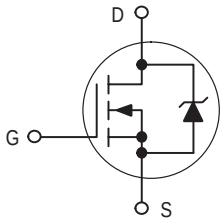
MTP4N80E

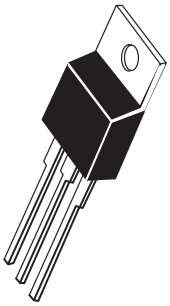
Motorola Preferred Device

TMOS POWER FET
4.0 AMPERES
800 VOLTS
$R_{DS(on)}$ = 3.0 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	800	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	800	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	4.0 2.9 12	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 8.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	320	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 63	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	800 —	— 1.02	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 800 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 800 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 7.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.0 Adc)		$R_{DS(on)}$	—	1.95	3.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 4.0 Adc) (I_D = 2.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	8.24 —	12 10	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.0 Adc)		g_{FS}	2.0	4.3	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1320	2030	pF
Output Capacitance		C_{oss}	—	187	400	
Reverse Transfer Capacitance		C_{rss}	—	72	160	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 400 Vdc, I_D = 4.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	13	30	ns
Rise Time		t_r	—	36	90	
Turn–Off Delay Time		$t_{d(off)}$	—	40	80	
Fall Time		t_f	—	30	75	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 4.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	36	80	nC
		Q_1	—	7.0	—	
		Q_2	—	16.5	—	
		Q_3	—	12	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc) (I_S = 4.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.812 0.7	1.5 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 4.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	557	—	ns
		t_a	—	100	—	
		t_b	—	457	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.33	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

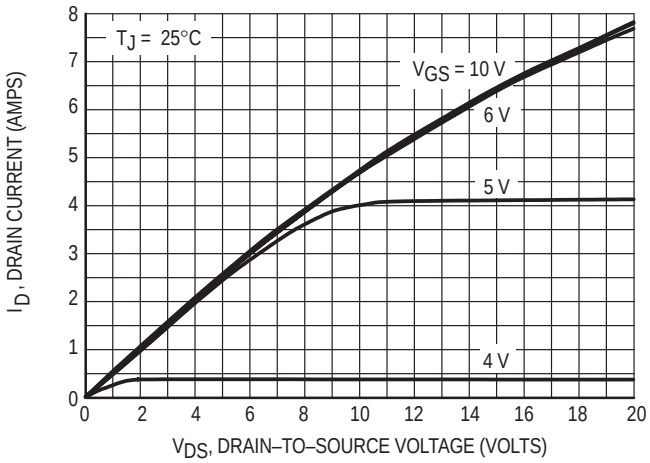


Figure 1. On–Region Characteristics

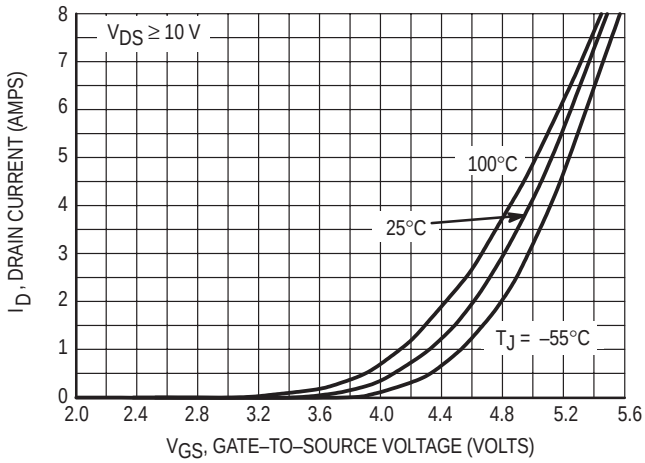


Figure 2. Transfer Characteristics

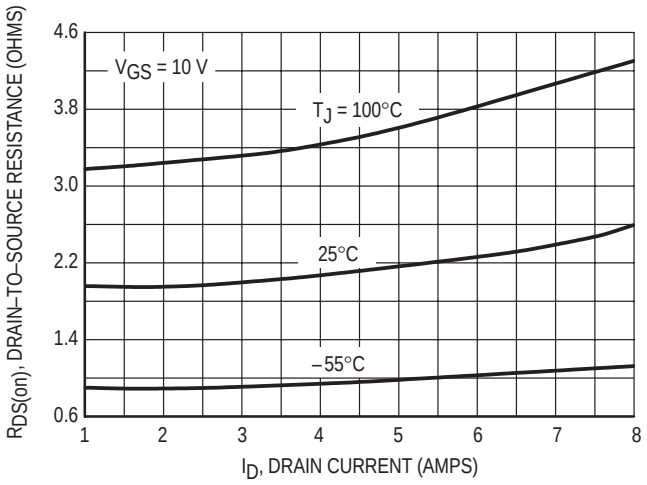


Figure 3. On–Resistance versus Drain Current and Temperature

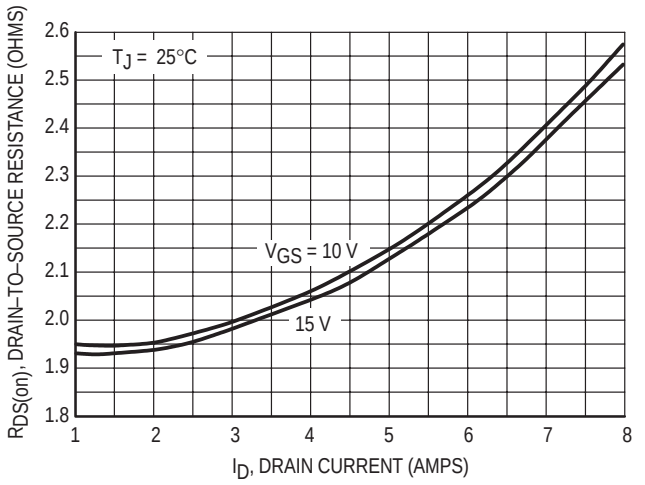


Figure 4. On–Resistance versus Drain Current and Gate Voltage

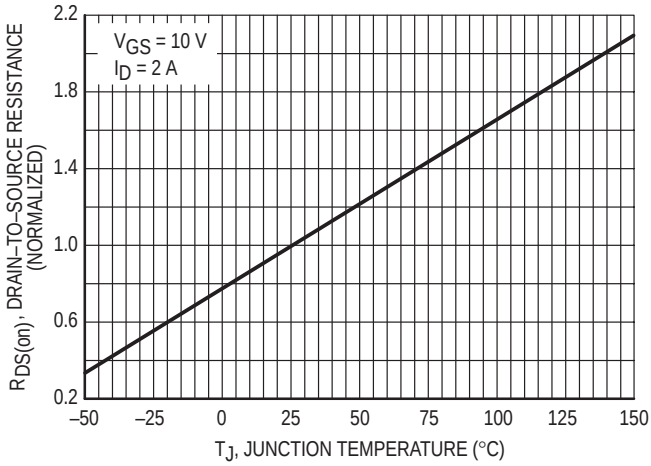


Figure 5. On–Resistance Variation with Temperature

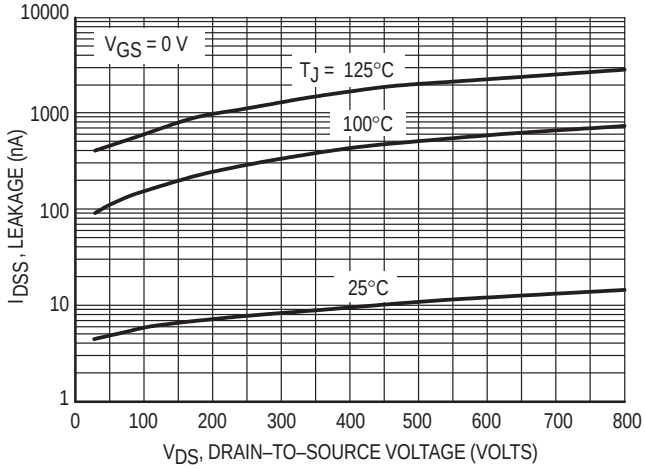


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

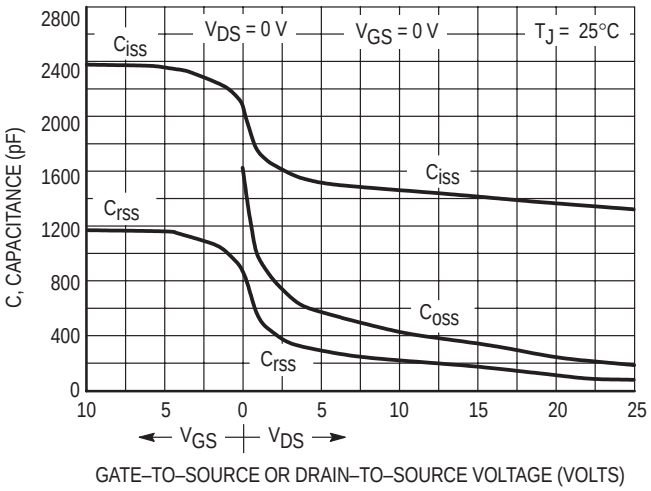


Figure 7a. Capacitance Variation

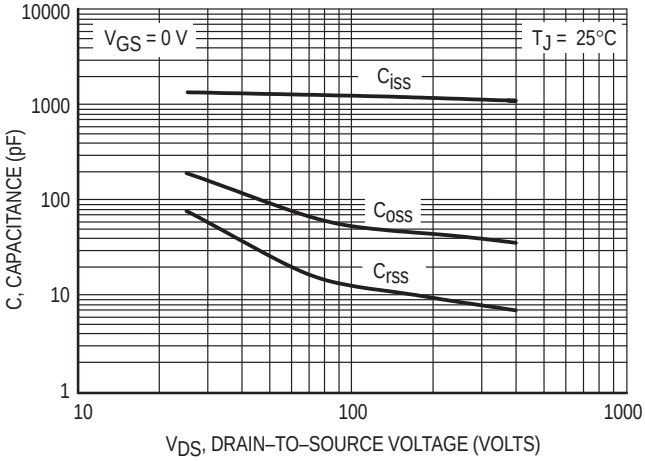


Figure 7b. High Voltage Capacitance Variation

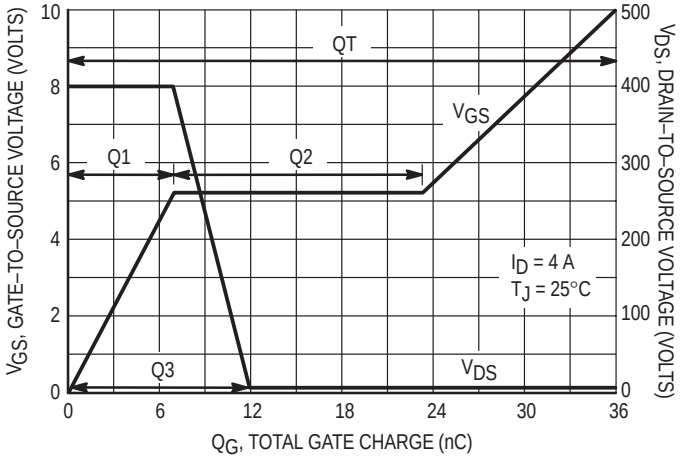


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

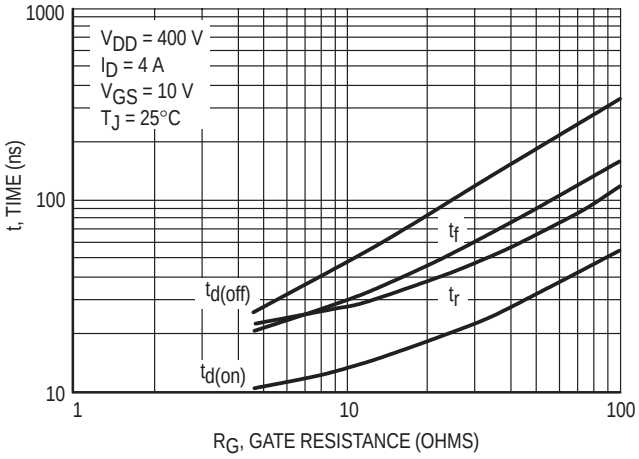


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

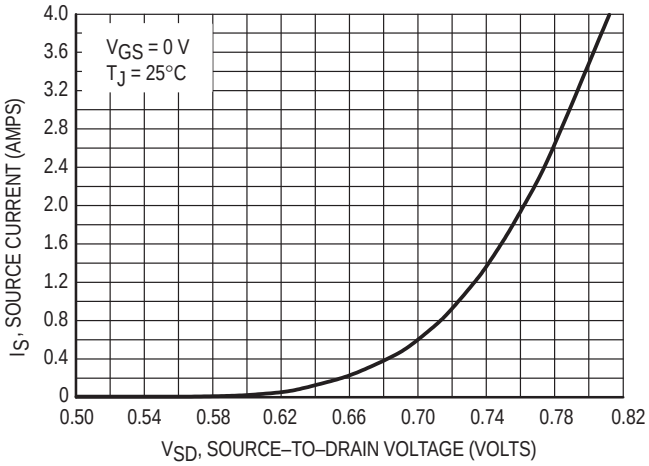


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

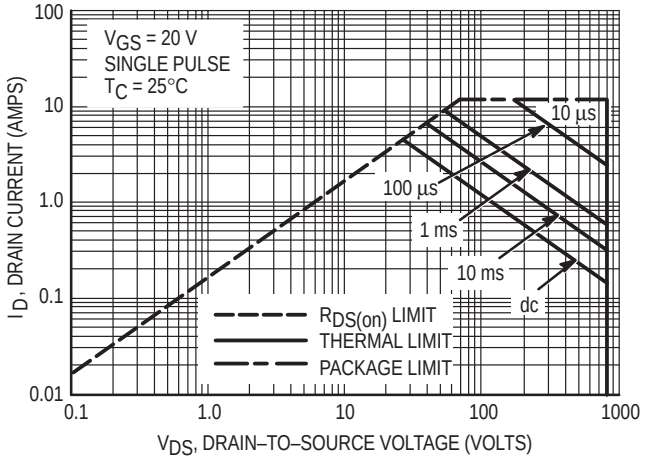


Figure 11. Maximum Rated Forward Biased Safe Operating Area

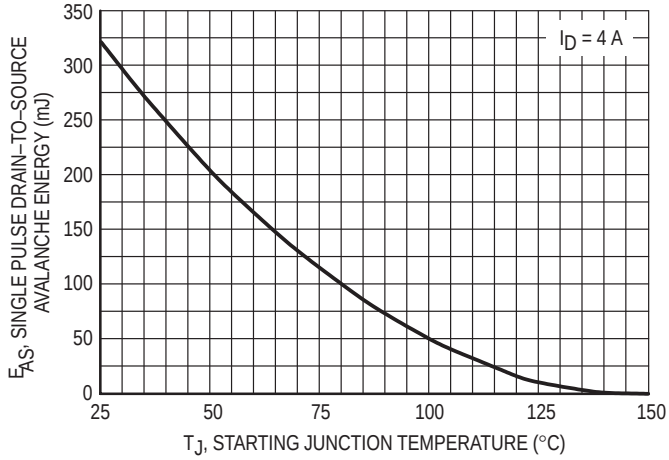


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

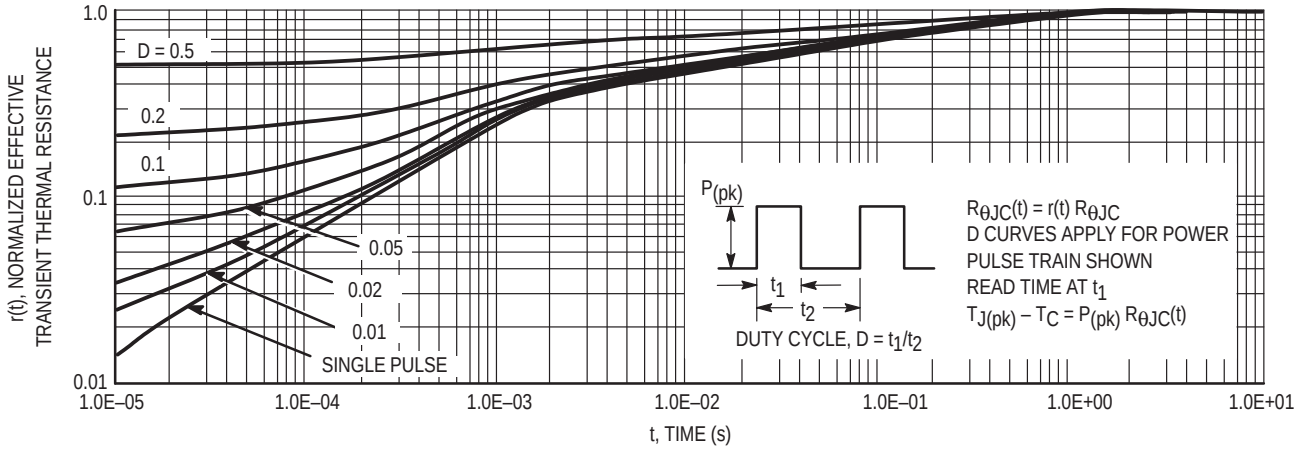


Figure 13. Thermal Response

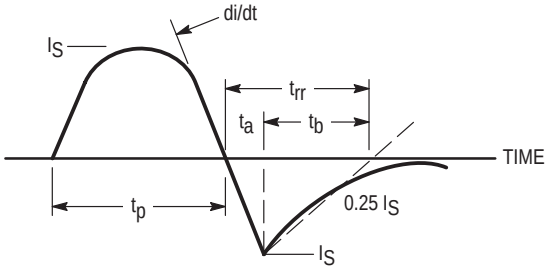


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
High Energy Power FET
N–Channel Enhancement–Mode Silicon Gate

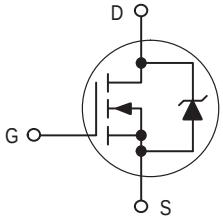
MTP5N40E

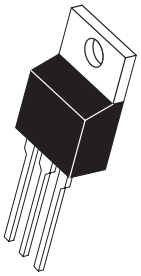
Motorola Preferred Device

TMOS POWER FET
5.0 AMPERES
400 VOLTS
$R_{DS(on)}$ = 1.0 OHM

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	400	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate–Source Voltage — Continuous — Non–repetitive	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	5.0 12	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain–to–Source Avalanche Energy — T_J = 25°C — T_J = 100°C	W_{DSR} (1)	290 46	mJ
Repetitive Pulse Drain–to–Source Avalanche Energy	W_{DSR} (2)	7.4	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) V_{DD} = 50 V, I_D = 5.0 A
(2) Pulse Width and frequency is limited by T_J(max) and thermal response

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μAdc)	$V_{(BR)DSS}$	400	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 400 V, V_{GS} = 0) (V_{DS} = 320 V, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 — —	 0.25 1.0	mAdc
Gate–Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) (T_J = 125°C)	$V_{GS(th)}$	 2.0 1.5	 — —	 4.0 3.5	Vdc
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)	$R_{DS(on)}$	—	0.8	1.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 5.0 A) (I_D = 2.5 A, T_J = 100°C)	$V_{DS(on)}$	 — —	 — —	 6.2 5.0	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.5 Adc)	g_{FS}	2.0	—	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	—	775	—	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	96	—	
Transfer Capacitance	C_{rss}	—	22	—	
SWITCHING CHARACTERISTICS*					
Turn–On Delay Time	$t_{d(on)}$	—	24	—	ns
Rise Time (V_{DD} = 250 V, I_D ≈ 5.0 A, R_G = 12 Ω, R_L = 50 Ω, $V_{GS(on)}$ = 10 V)	t_r	—	34	—	
Turn–Off Delay Time	$t_{d(off)}$	—	60	—	
Fall Time	t_f	—	36	—	
Total Gate Charge	Q_g	—	27	32	nC
Gate–Source Charge (V_{DS} = 320 V, I_D = 5.0 A, V_{GS} = 10 V)	Q_{gs}	—	3.5	—	
Gate–Drain Charge	Q_{gd}	—	14	—	
SOURCE–DRAIN DIODE CHARACTERISTICS*					
Forward On–Voltage	V_{SD}	—	—	1.4	Vdc
Forward Turn–On Time (I_S = 5.0 A, di/dt = 100 A/μs)	t_{on}		**		ns
Reverse Recovery Time	t_{rr}	—	—	660	
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)	L_d	 — —	 3.5 4.5	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_s	—	7.5	—	

* Indicates Pulse Test: Pulse Width = 300 μs Max, Duty Cycle ≤ 2.0%.

** Limited by circuit inductance.

TYPICAL ELECTRICAL CHARACTERISTICS

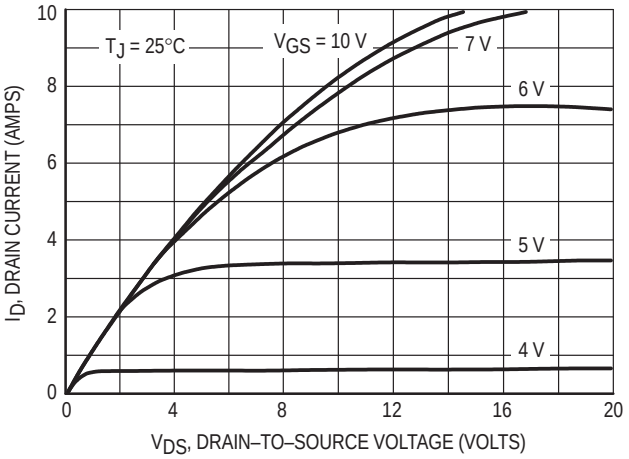


Figure 1. On–Region Characteristics

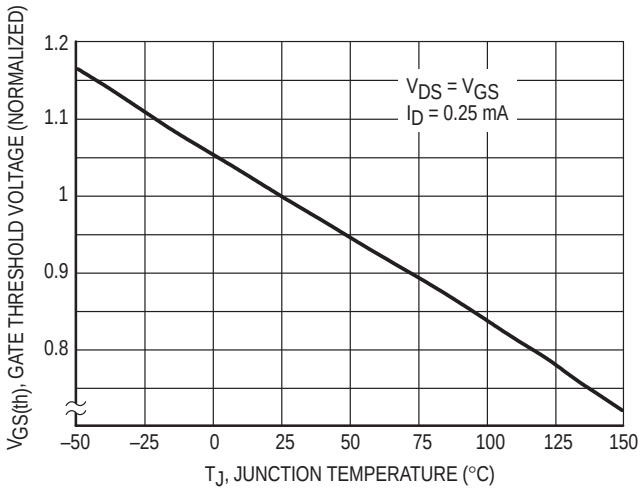


Figure 2. Gate–Threshold Voltage Variation With Temperature

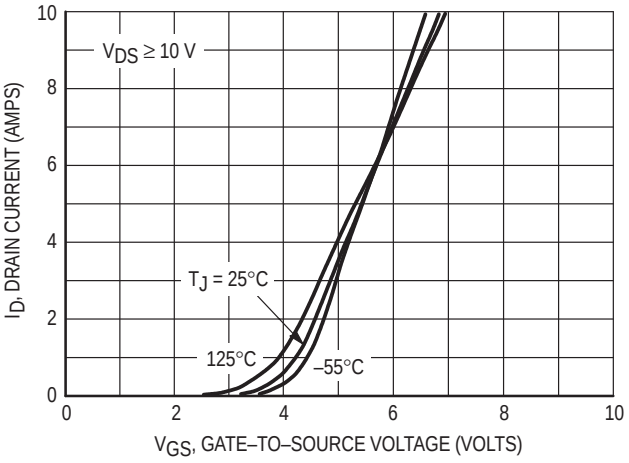


Figure 3. Transfer Characteristics

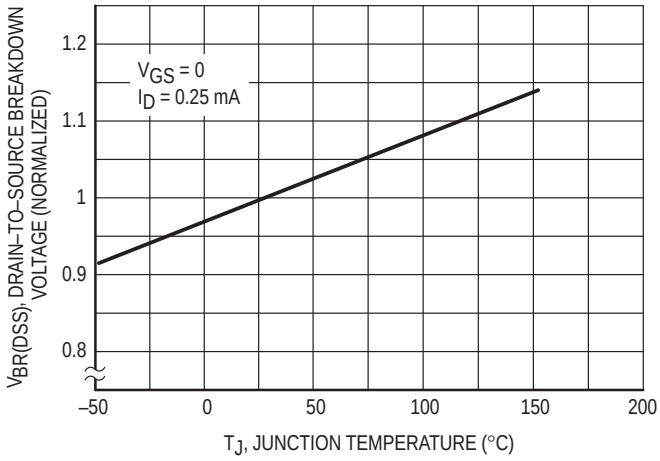


Figure 4. Breakdown Voltage Variation With Temperature

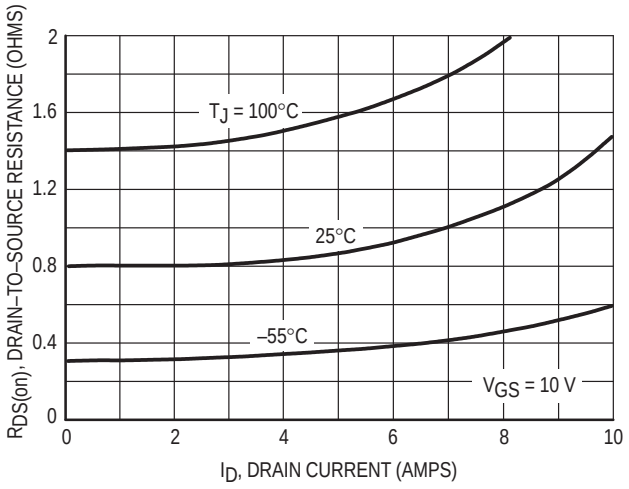


Figure 5. On–Resistance versus Drain Current

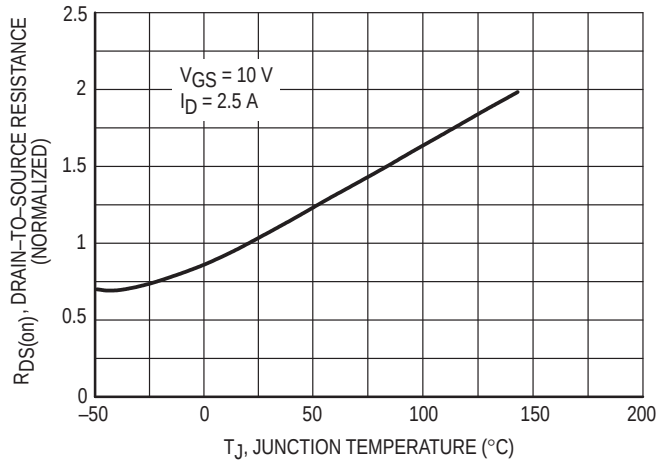


Figure 6. On–Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

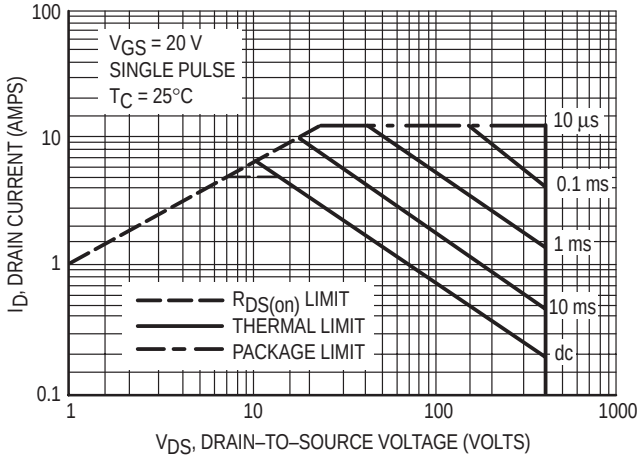


Figure 7. Maximum Rated Forward Biased Safe Operating Area

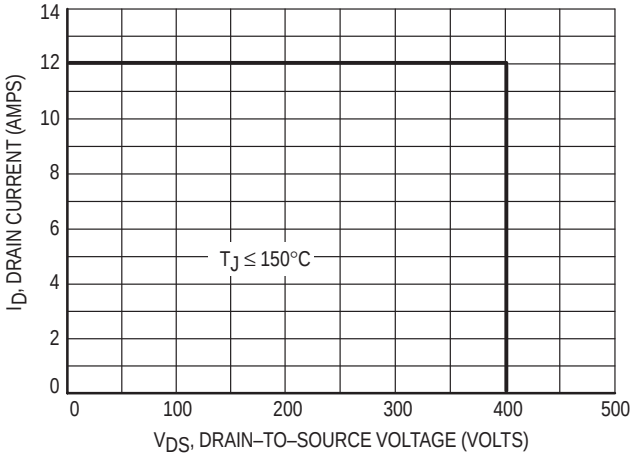


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

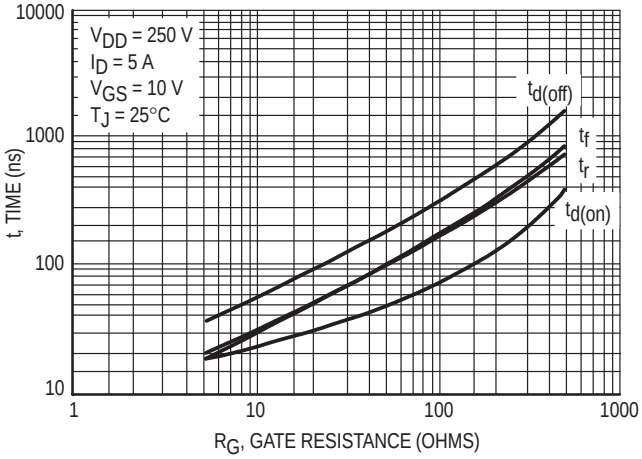


Figure 9. Resistive Switching Time Variation versus Gate Resistance

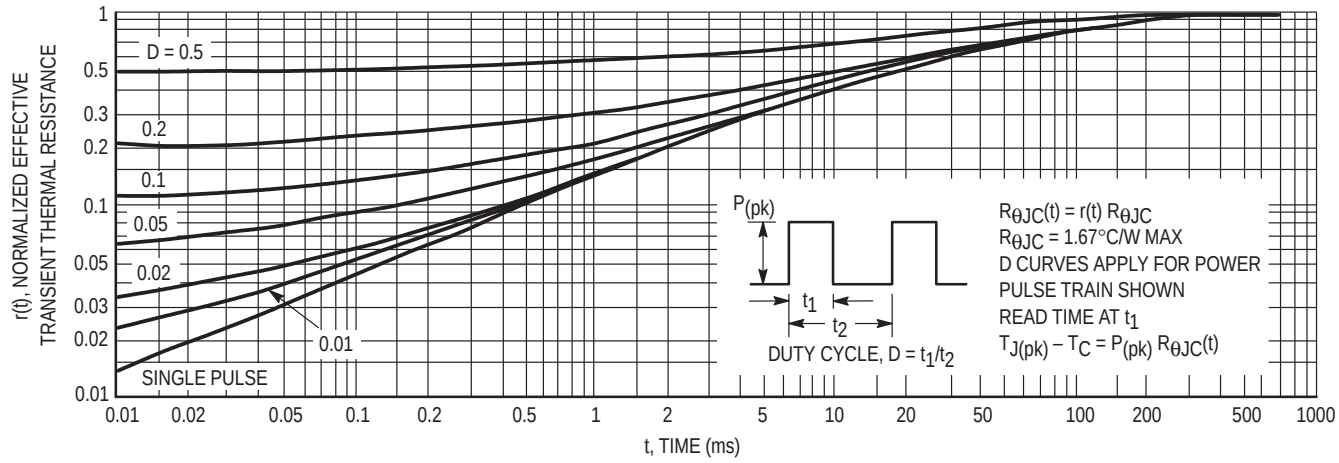


Figure 10. Thermal Response

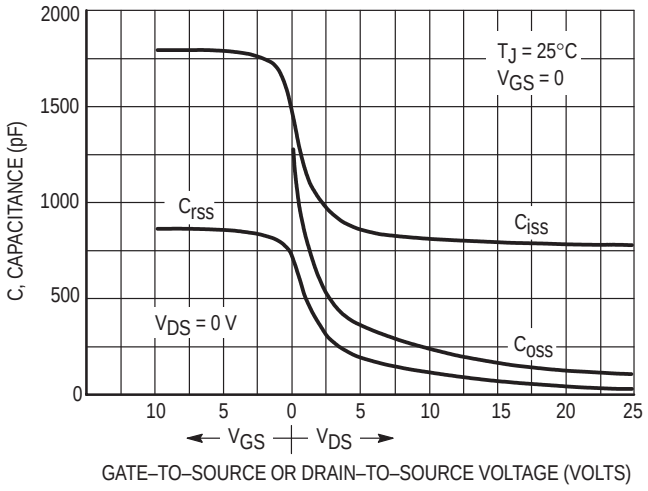


Figure 11. Capacitance Variation

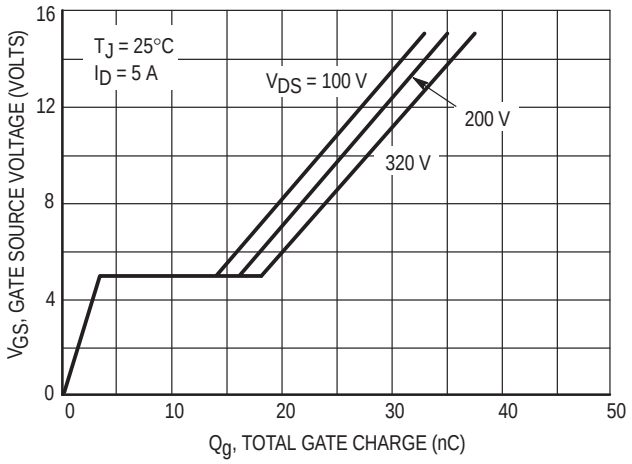


Figure 12. Gate Charge versus Gate–To–Source Voltage

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 14 defines the limits of safe operation for commutated source–drain current versus re–applied drain voltage when the source–drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half–bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source–drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/µs.

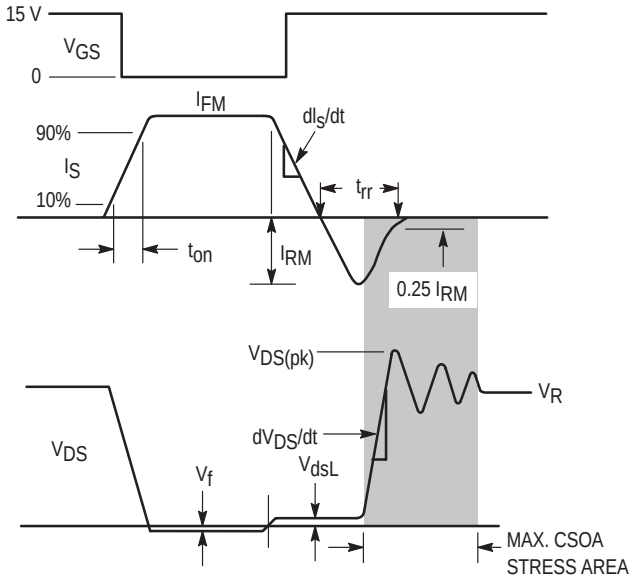


Figure 15. Commutating Waveforms

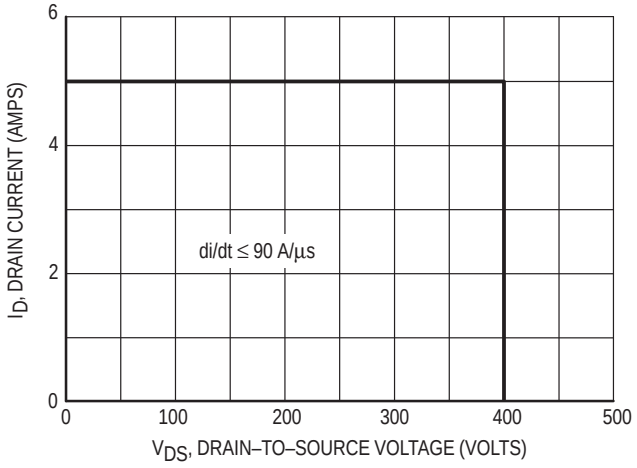


Figure 13. Commutating Safe Operating Area (CSOA)

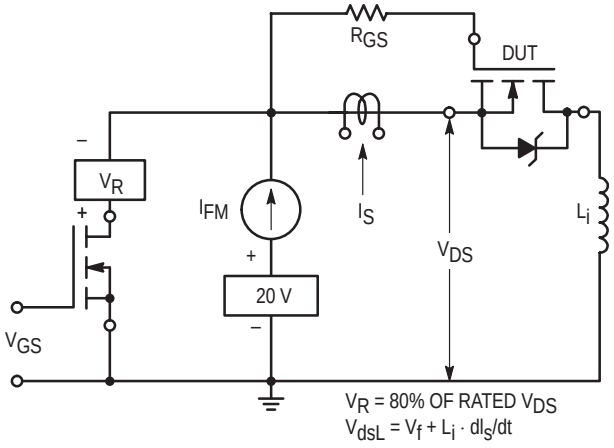


Figure 14. Commutating Safe Operating Area Test Circuit

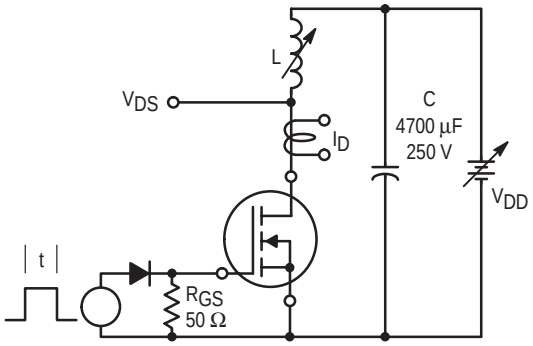


Figure 16. Unclamped Inductive Switching Test Circuit

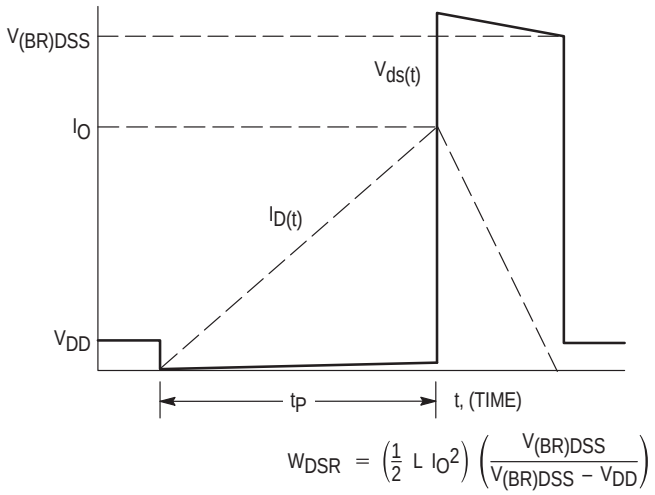
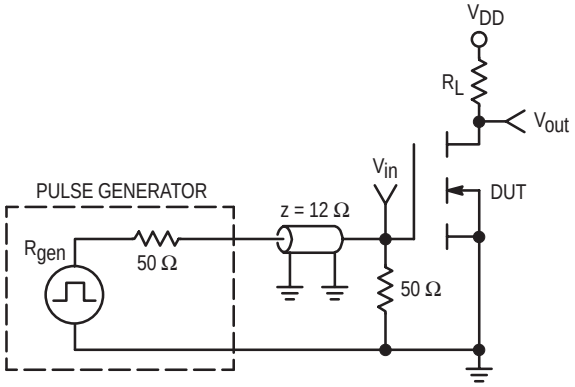


Figure 17. Unclamped Inductive Switching Waveforms

RESISTIVE SWITCHING



* Note: The Mirror is shorted to the Kelvin terminal for this test.

Figure 18. Switching Test Circuit

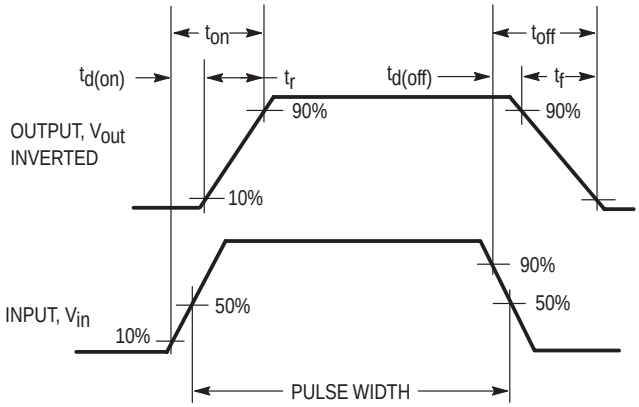
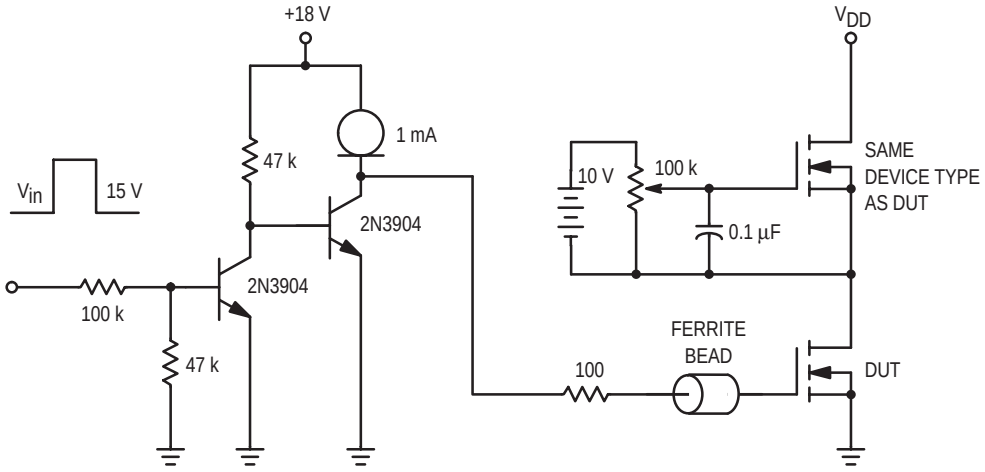


Figure 19. Switching Waveforms



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

Figure 20. Gate Charge Test Circuit

Designer's™ Data Sheet

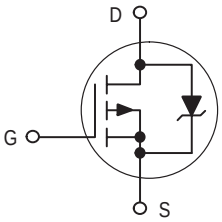
TMOS V
Power Field Effect Transistor
P–Channel Enhancement–Mode Silicon Gate

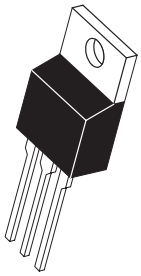
MTP5P06V

Motorola Preferred Device

TMOS POWER FET
5 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.450 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 221A–06, Style 5
TO–220AB

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	5 4 18	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	40 0.27	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, PEAK I_L = 5 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	125	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.75 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	61.2	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.8	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	4.7	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 2.5 Adc)		$R_{DS(on)}$	—	0.34	0.45	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 5 Adc)		$V_{DS(on)}$	—	—	2.7	Vdc
(V_{GS} = 10 Vdc, I_D = 2.5 Adc, T_J = 150°C)			—	—	2.6	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 2.5 Adc)		g_{FS}	1.5	3.6	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	367	510	pF
Output Capacitance		C_{oss}	—	140	200	
Transfer Capacitance		C_{rss}	—	29	60	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 5 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	11	20	ns
Rise Time		t_r	—	26	50	
Turn–Off Delay Time		$t_{d(off)}$	—	17	30	
Fall Time		t_f	—	19	40	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 5 Adc, V_{GS} = 10 Vdc)	Q_T	—	12	20	nC
		Q_1	—	3.0	—	
		Q_2	—	5.0	—	
		Q_3	—	5.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 5 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.72	3.5	Vdc
	(I_S = 5 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	1.34	—	
Reverse Recovery Time	(I_S = 5 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	97	—	ns
		t_a	—	73	—	
		t_b	—	24	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.42	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)				4.5		
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

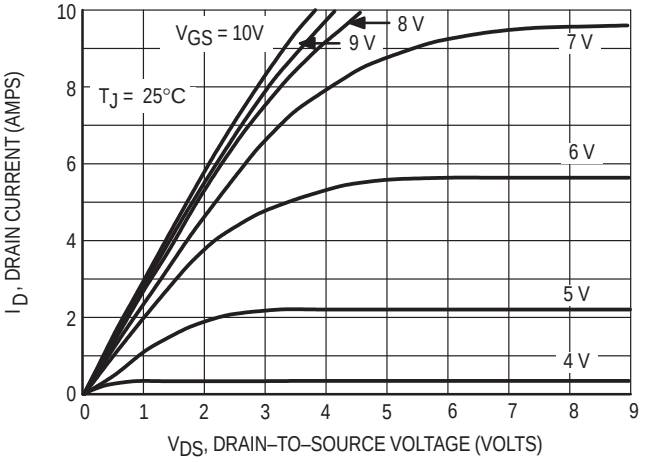


Figure 1. On–Region Characteristics

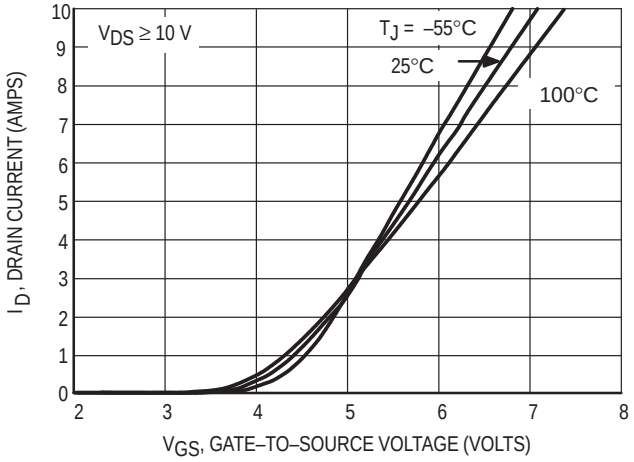


Figure 2. Transfer Characteristics

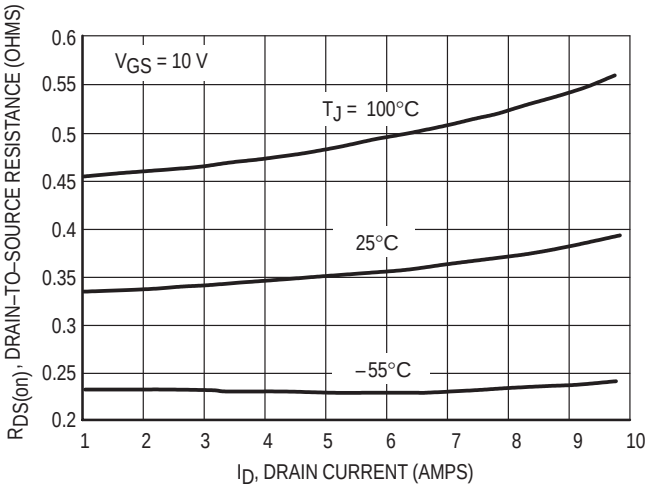


Figure 3. On–Resistance versus Drain Current and Temperature

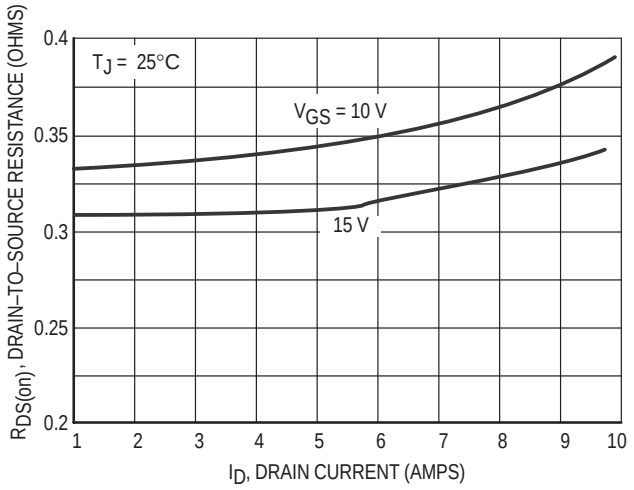


Figure 4. On–Resistance versus Drain Current and Gate Voltage

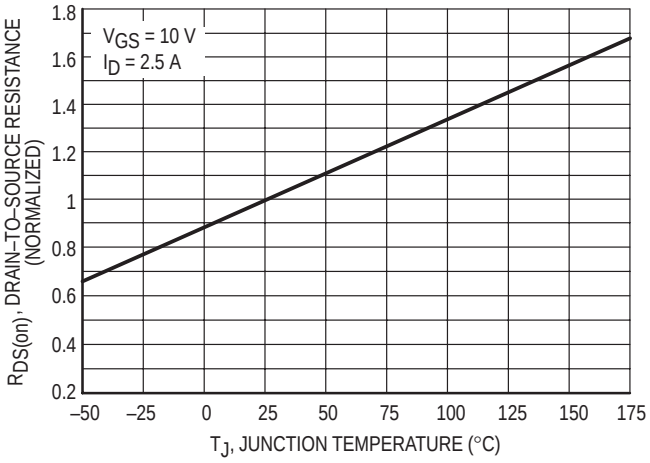


Figure 5. On–Resistance Variation with Temperature

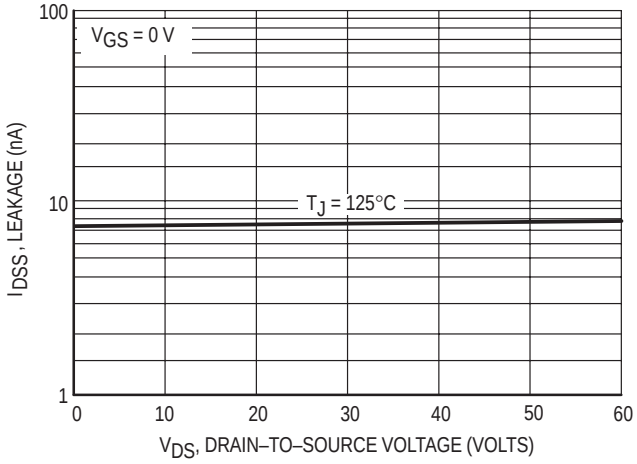


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

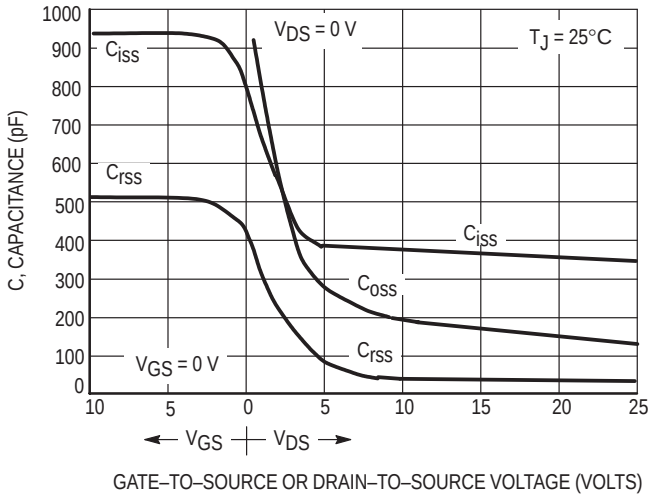


Figure 7. Capacitance Variation

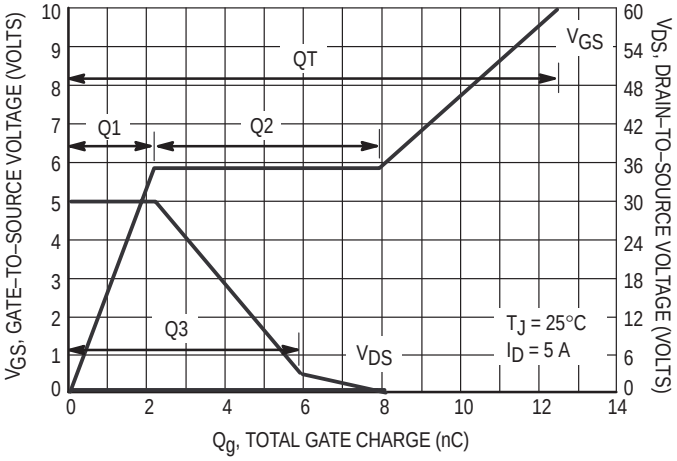


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

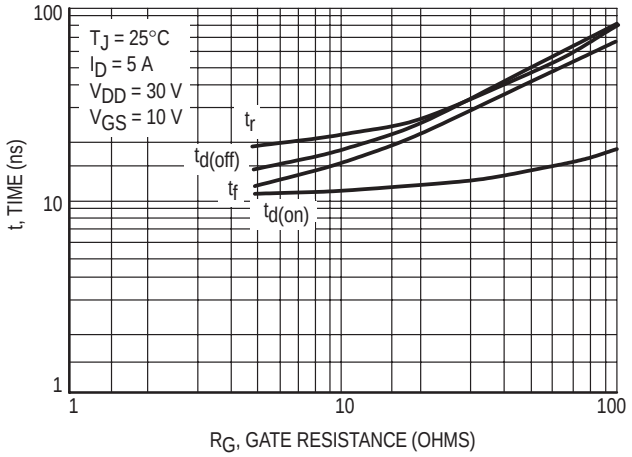


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

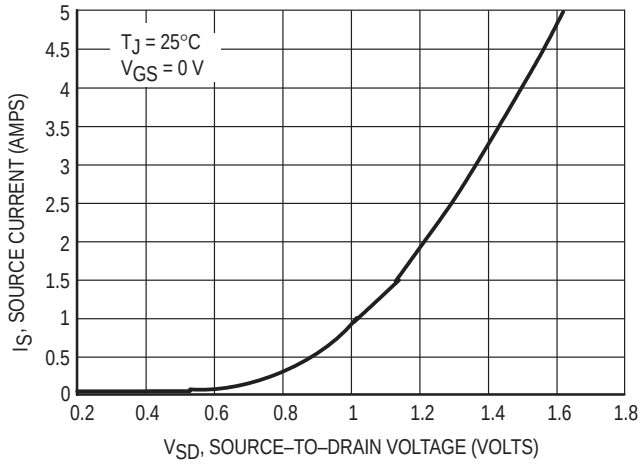


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

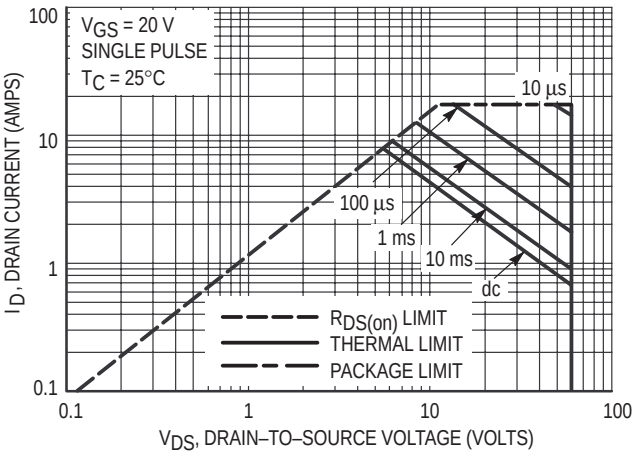


Figure 11. Maximum Rated Forward Biased Safe Operating Area

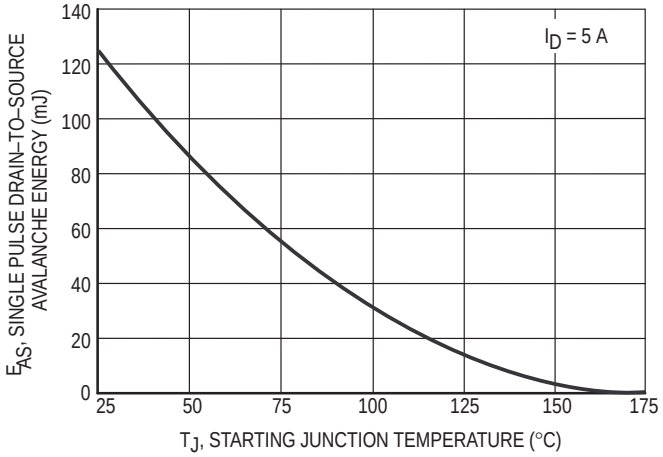


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

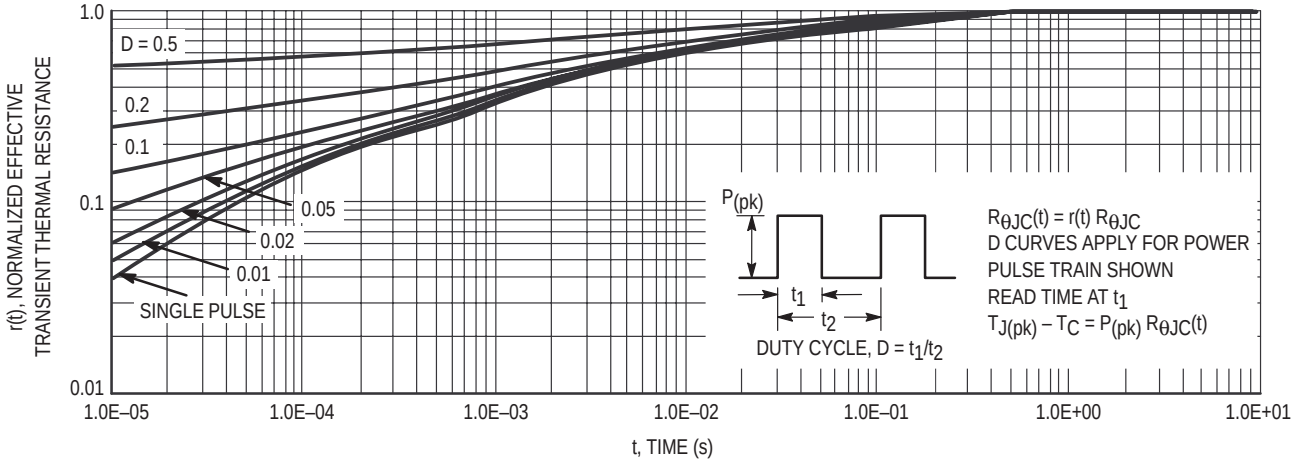


Figure 13. Thermal Response

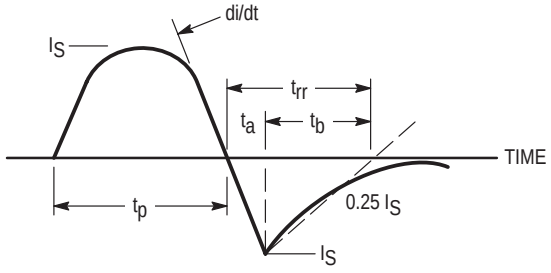


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

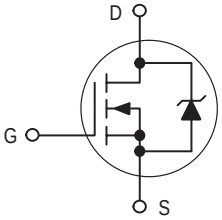
MTP6N60E

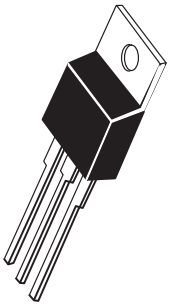
Motorola Preferred Device

TMOS POWER FET
6.0 AMPERES
600 VOLTS
$R_{DS(on)}$ = 1.2 OHMS

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	600	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	6.0 4.6 18	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 2.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	405	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 μAdc)		$V_{(BR)DSS}$	600	—	—	Vdc
Temperature Coefficient (Positive)			—	689	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 600 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	7.1	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	—	0.94	1.2	Ohms
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$V_{DS(on)}$	—	6.0	8.6	Vdc
(V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J = 125°C)			—	—	7.6	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 3.0 Adc)		g_{FS}	2.0	5.5	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1498	2100	pF
Output Capacitance		C_{oss}	—	158	220	
Reverse Transfer Capacitance		C_{rss}	—	29	60	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DS} = 300 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	14	30	ns
Rise Time		t_r	—	19	40	
Turn–Off Delay Time		$t_{d(off)}$	—	40	80	
Fall Time		t_f	—	26	55	
Gate Charge	(V_{DS} = 300 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	35.5	50	nC
		Q_1	—	8.1	—	
		Q_2	—	14.1	—	
		Q_3	—	15.8	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.83	1.2	Vdc
	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.72	—	
Reverse Recovery Time	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	266	—	ns
		t_a	—	166	—	
		t_b	—	100	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.5	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

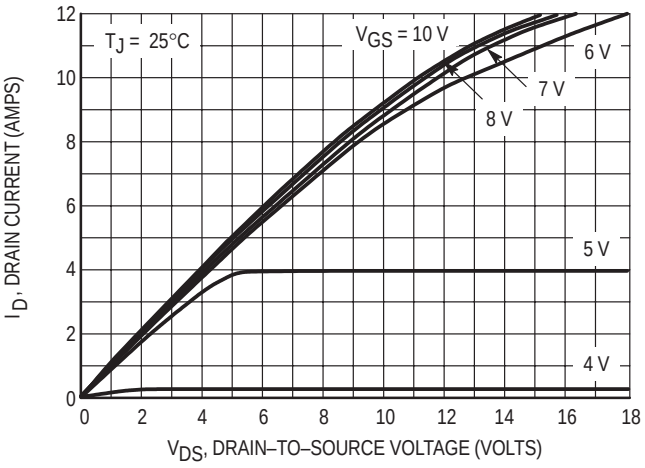


Figure 1. On–Region Characteristics

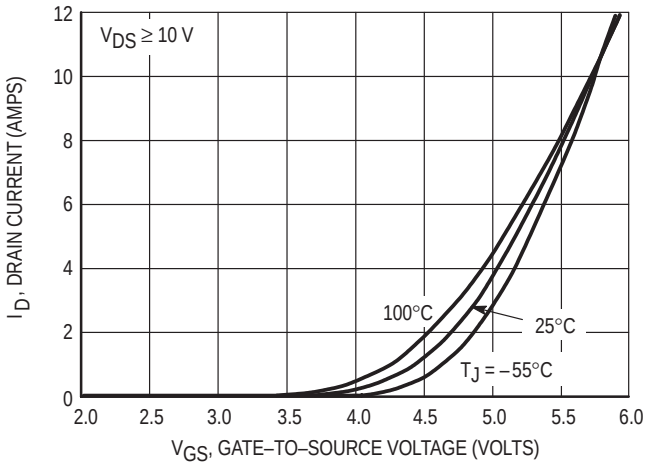


Figure 2. Transfer Characteristics

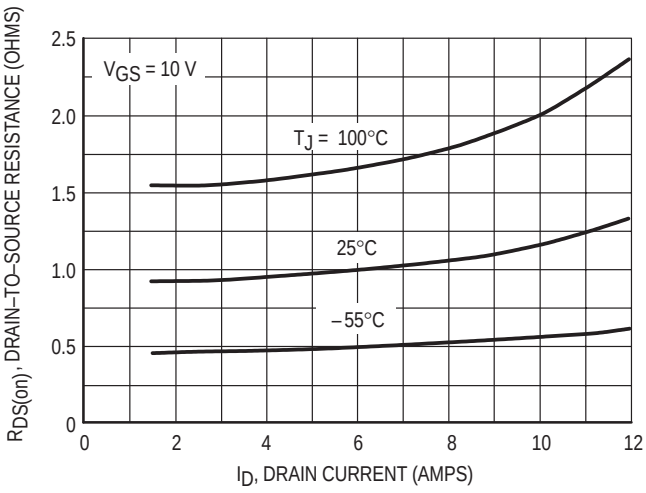


Figure 3. On–Resistance versus Drain Current and Temperature

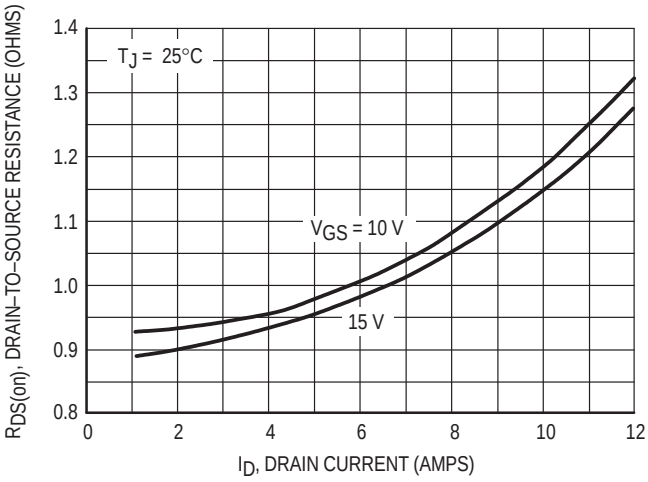


Figure 4. On–Resistance versus Drain Current and Gate Voltage

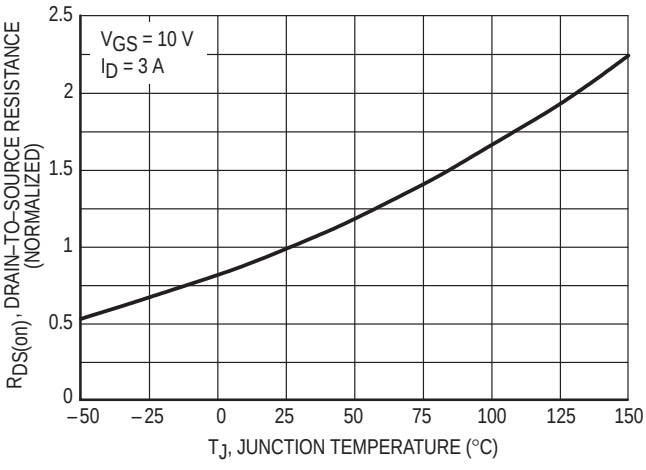


Figure 5. On–Resistance Variation with Temperature

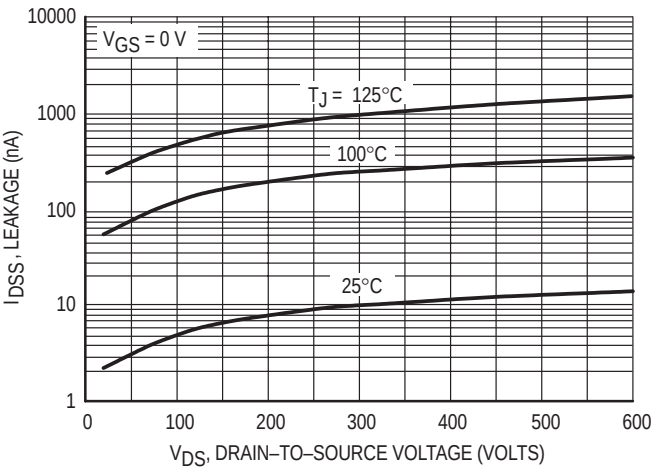


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

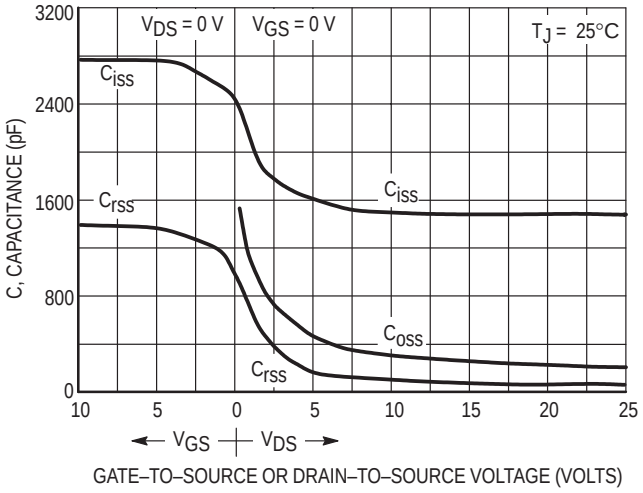


Figure 7a. Capacitance Variation

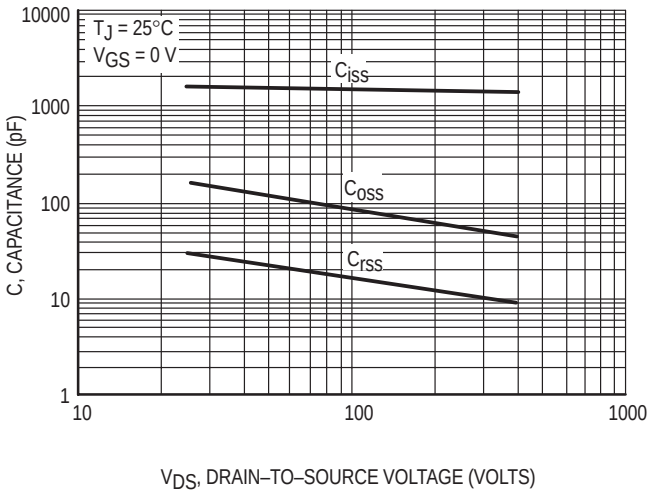


Figure 7b. High Voltage Capacitance Variation

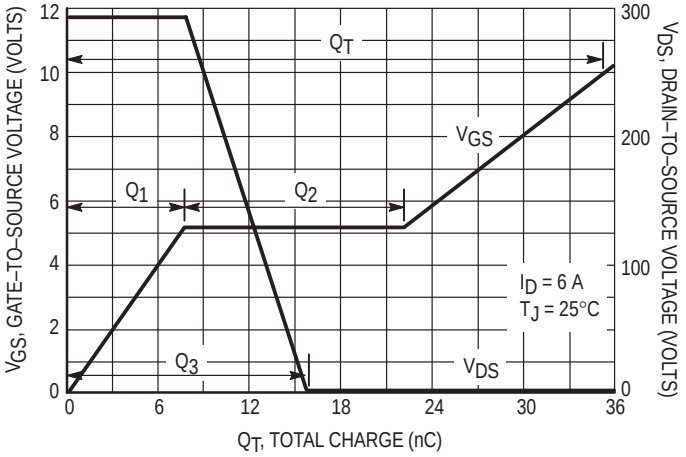


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

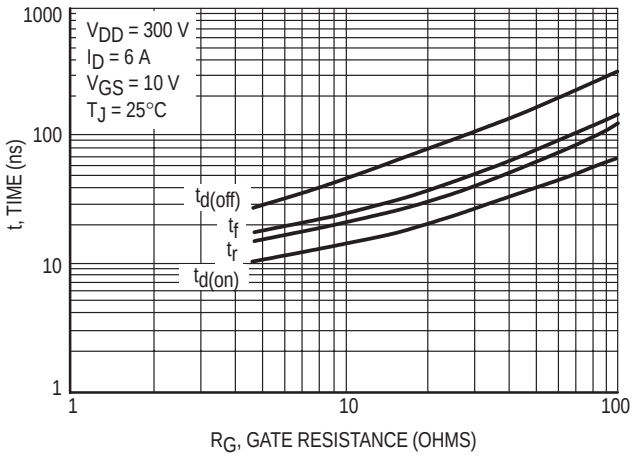


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

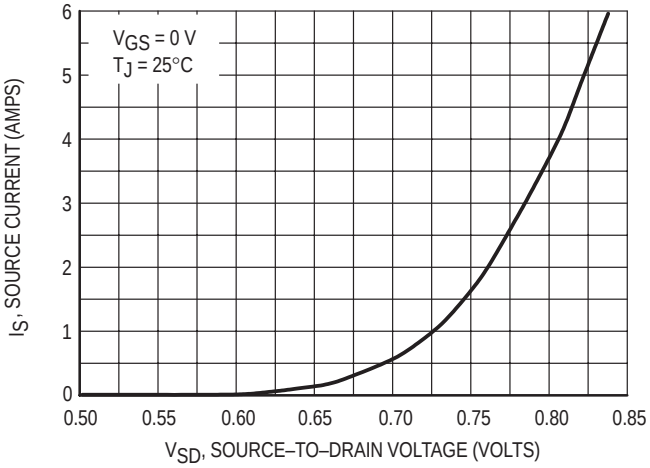


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

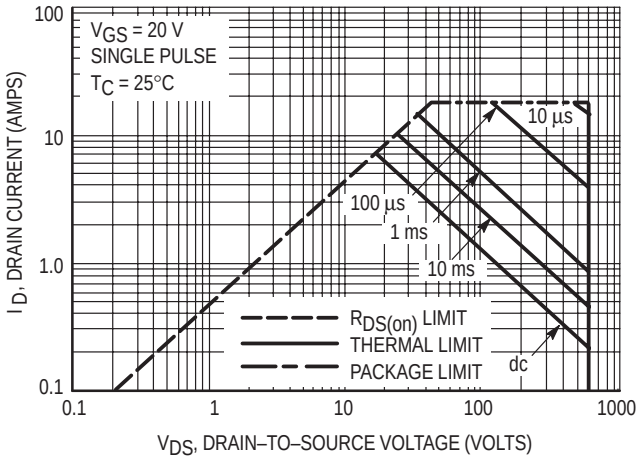


Figure 11. Maximum Rated Forward Biased Safe Operating Area

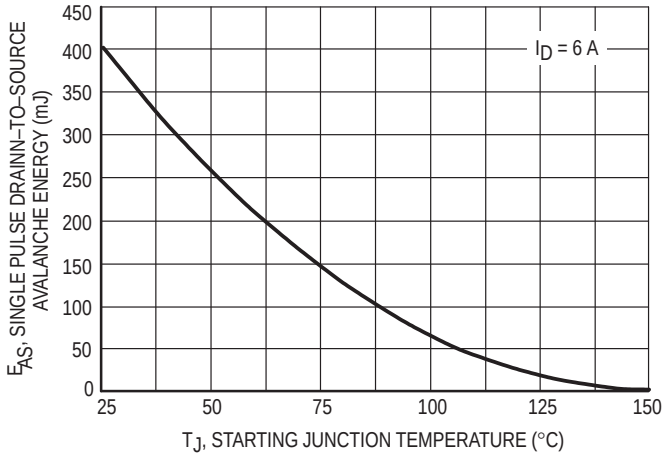


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

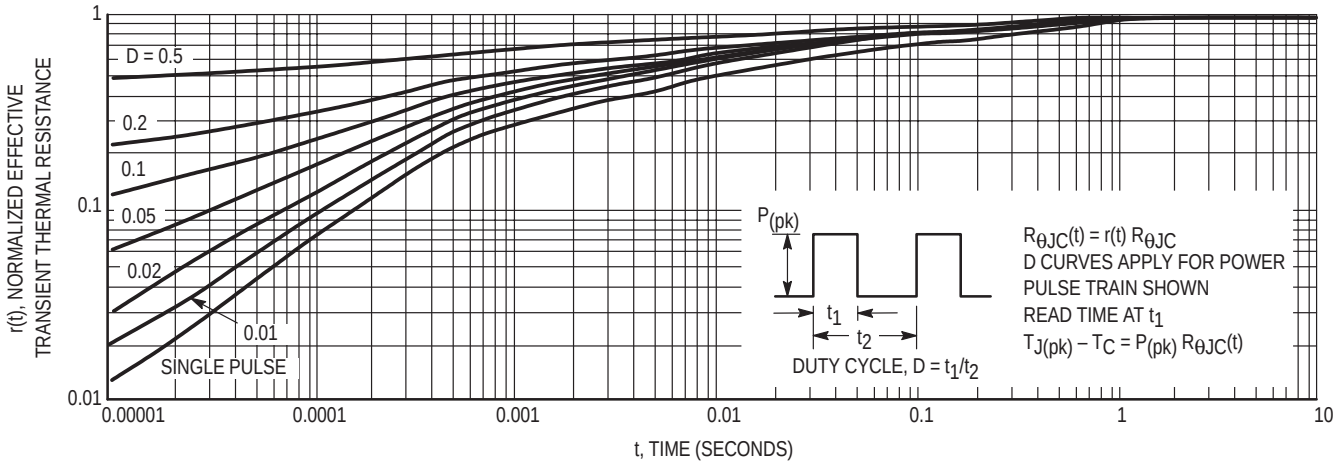


Figure 13. Thermal Response

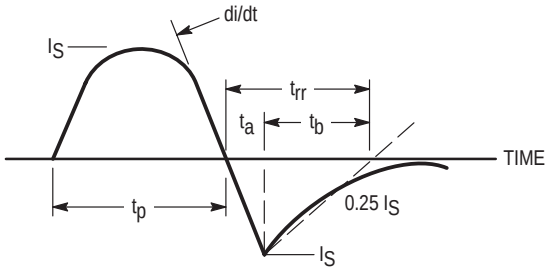


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
P–Channel Enhancement–Mode Silicon Gate

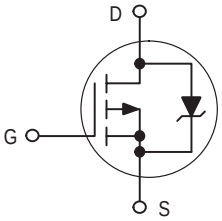
MTP6P20E

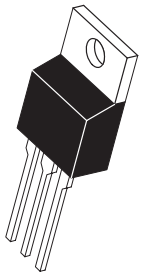
Motorola Preferred Device

TMOS POWER FET
6.0 AMPERES
200 VOLTS
$R_{DS(on)}$ = 1.0 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	200	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	6.0 3.9 21	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 6.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	180	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	200 —	— 211	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.1 4.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	—	0.81	1.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 6.0 Adc) (I_D = 3.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	6.0 —	7.2 6.3	Vdc
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 3.0 Adc)		g_{FS}	1.5	3.8	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	540	750	pF
Output Capacitance		C_{oss}	—	128	180	
Reverse Transfer Capacitance		C_{rss}	—	40	90	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 100 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	12	25	ns
Rise Time		t_r	—	32	65	
Turn–Off Delay Time		$t_{d(off)}$	—	24	50	
Fall Time		t_f	—	16	30	
Gate Charge (See Figure 8)	(V_{DS} = 160 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	22	30	nC
		Q_1	—	4.0	—	
		Q_2	—	11	—	
		Q_3	—	9.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc) (I_S = 6.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	2.8 2.6	4.0 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	188	—	ns
		t_a	—	152	—	
		t_b	—	36	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.595	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

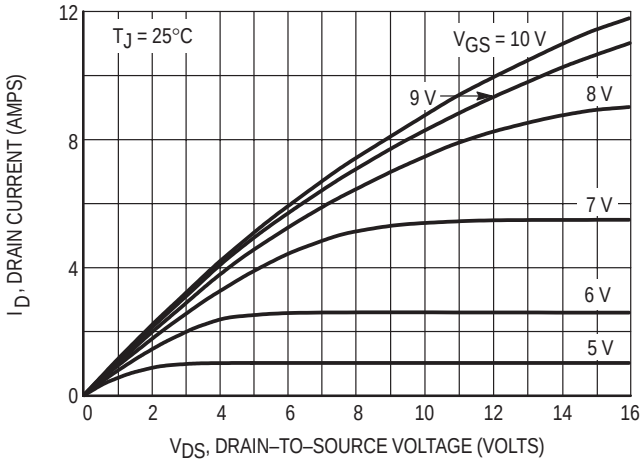


Figure 1. On–Region Characteristics

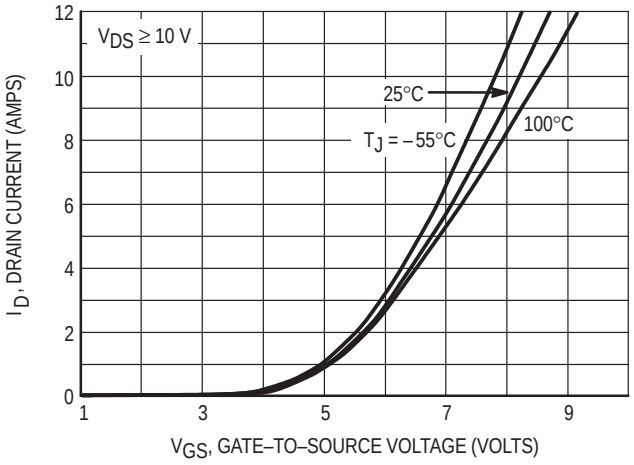


Figure 2. Transfer Characteristics

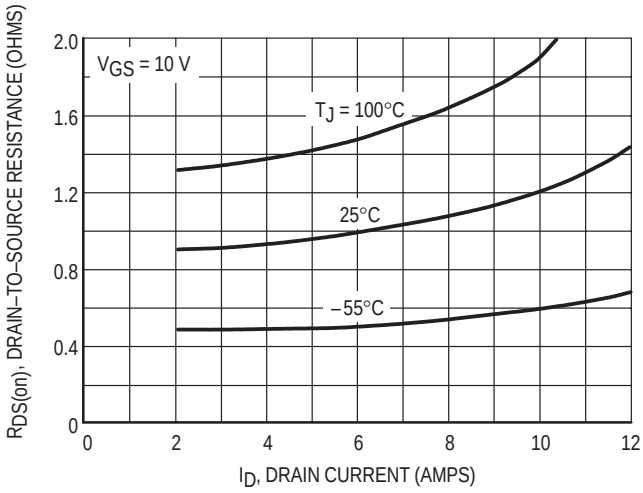


Figure 3. On–Resistance versus Drain Current and Temperature

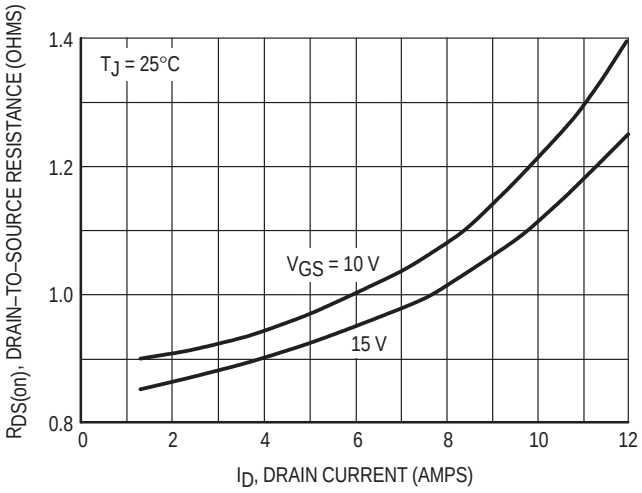


Figure 4. On–Resistance versus Drain Current and Gate Voltage

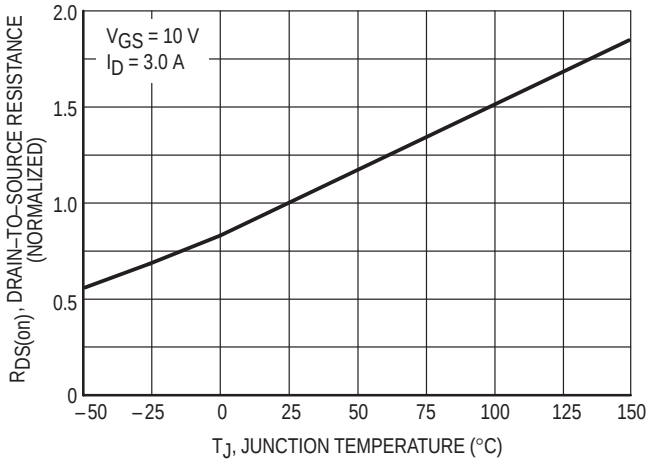


Figure 5. On–Resistance Variation with Temperature

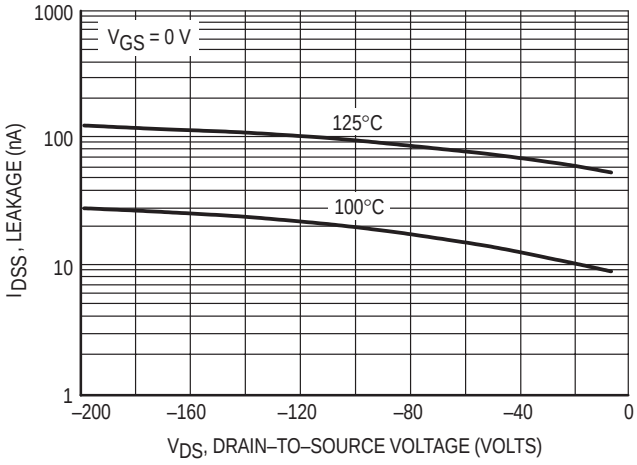


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

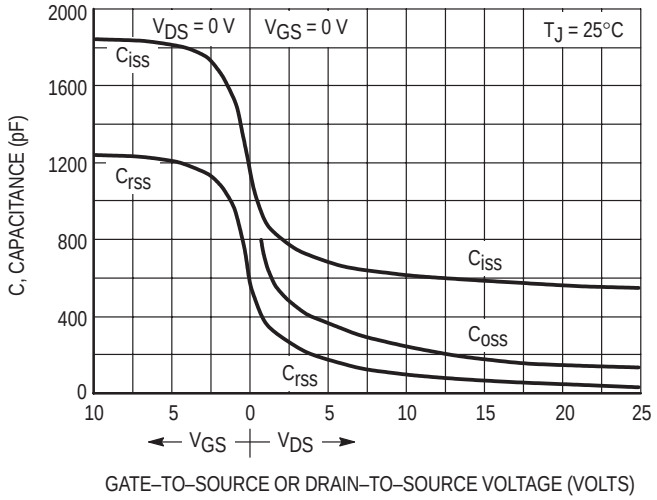


Figure 7. Capacitance Variation

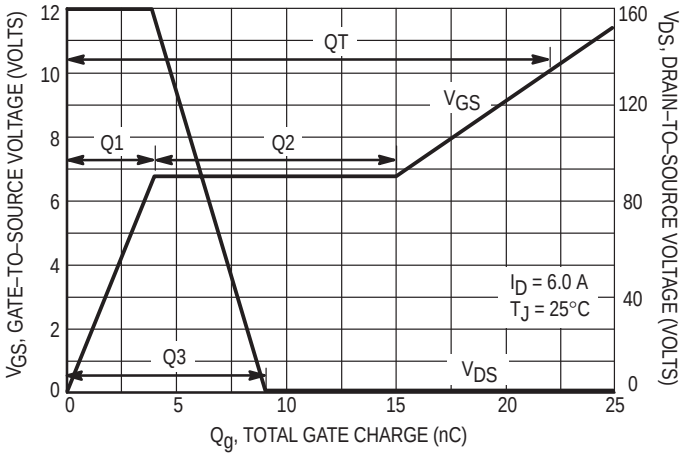


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

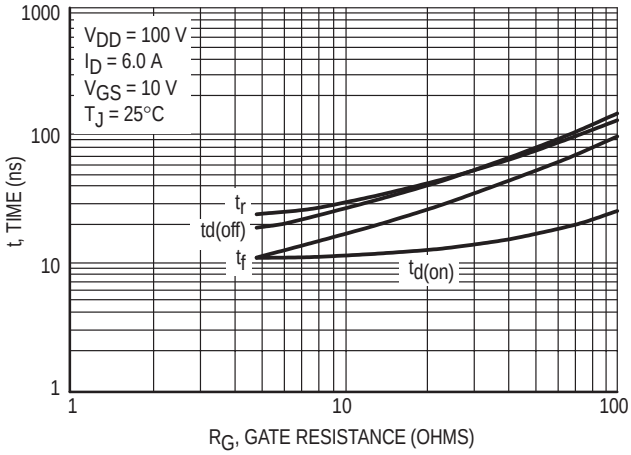


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

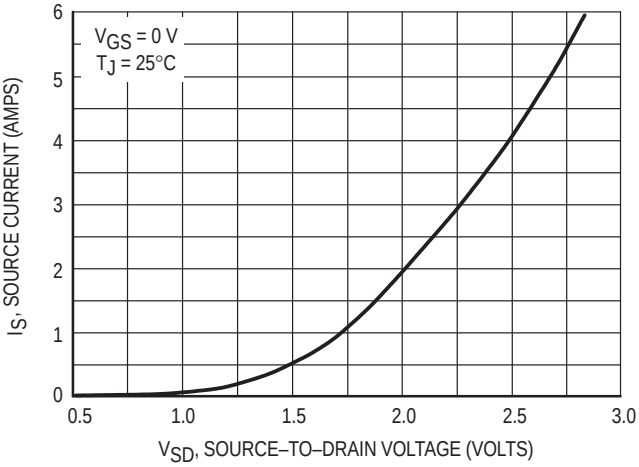


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

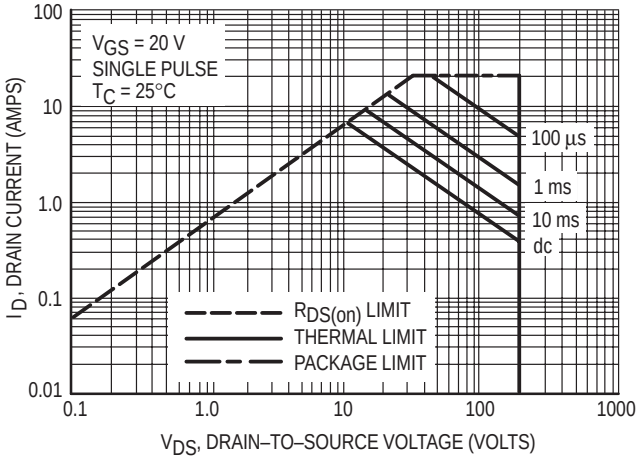


Figure 11. Maximum Rated Forward Biased Safe Operating Area

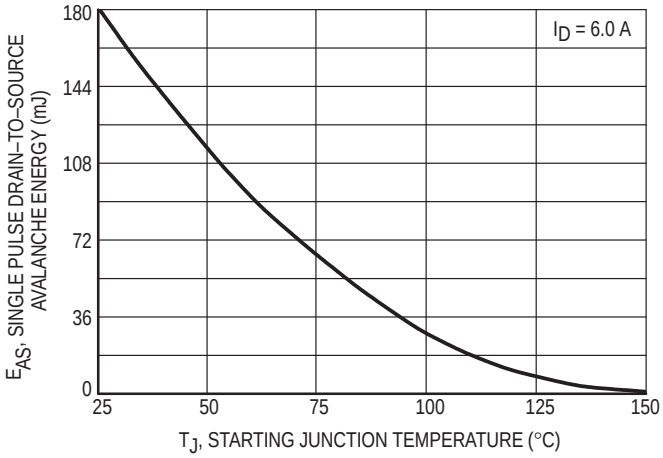


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

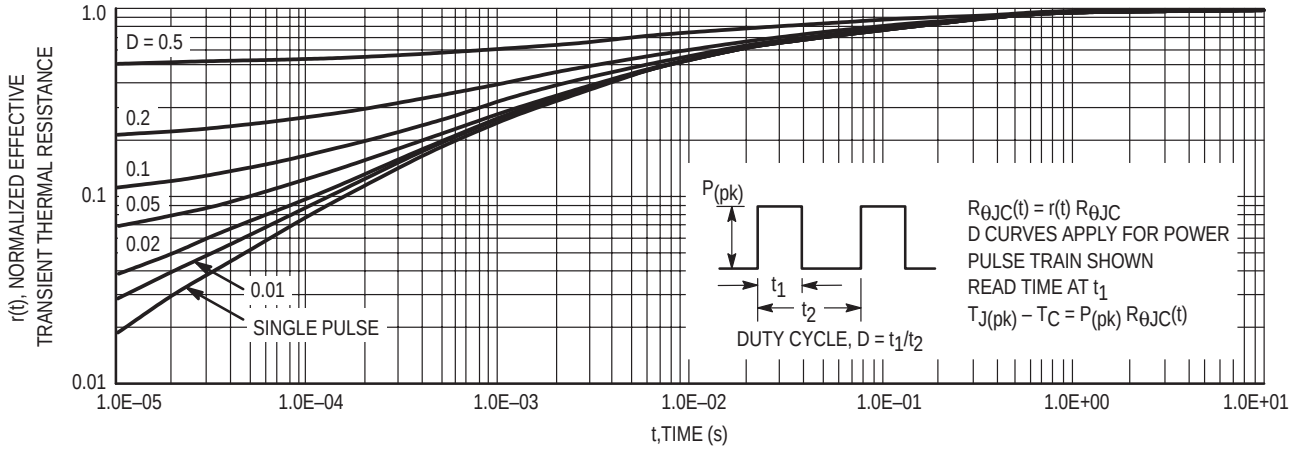


Figure 13. Thermal Response

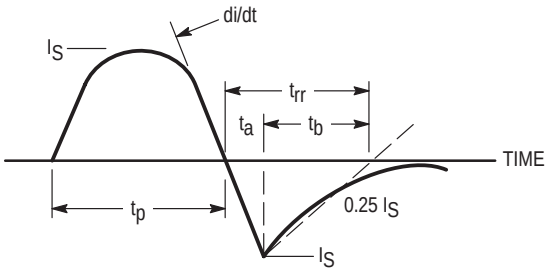


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

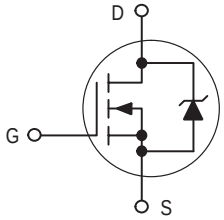
MTP7N20E

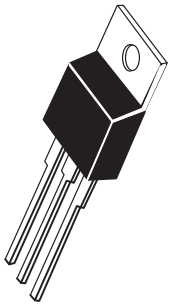
Motorola Preferred Device

TMOS POWER FET
7.0 AMPERES
200 VOLTS
$R_{DS(on)}$ = 0.70 OHMS

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	200	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	7.0 3.8 21	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	50 0.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, Peak I_L = 7.0 Adc, L = 10 mH, R_G = 25 Ω)	E_{AS}	74	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	200	—	—	Vdc
Temperature Coefficient (positive)			—	689	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 200 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.1	4.0	Vdc
Temperature Coefficient (negative)			—	7.1	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.5 Adc)		$R_{DS(on)}$	—	0.46	0.7	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 7.0 Adc)		$V_{DS(on)}$	—	3.4	5.9	Vdc
(V_{GS} = 10 Vdc, I_D = 3.5 Adc, T_J = 125°C)			—	—	5.1	
Forward Transconductance (V_{DS} = 14 Vdc, I_D = 3.5 Adc)		g_{FS}	1.5	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	342	480	pF
Output Capacitance		C_{oss}	—	92	130	
Reverse Transfer Capacitance		C_{rss}	—	27	55	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 100 Vdc, I_D = 7.0 Adc, V_{GS} = 10 Vdc, R_g = 9.1 Ω)	$t_{d(on)}$	—	8.8	17.6	ns
Rise Time		t_r	—	29	58	
Turn–Off Delay Time		$t_{d(off)}$	—	22	44	
Fall Time		t_f	—	20	40.8	
Gate Charge (See Figure 8)	(V_{DS} = 160 Vdc, I_D = 7.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	13.7	21	nC
		Q_1	—	3.3		
		Q_2	—	6.6	—	
		Q_3	—	5.9	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 7.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.02	1.2	Vdc
	(I_S = 7.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.9	—	
Reverse Recovery Time (See Figure 14)	(I_S = 7.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	138	—	ns
		t_a	—	93	—	
		t_b	—	45	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.74	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_d	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

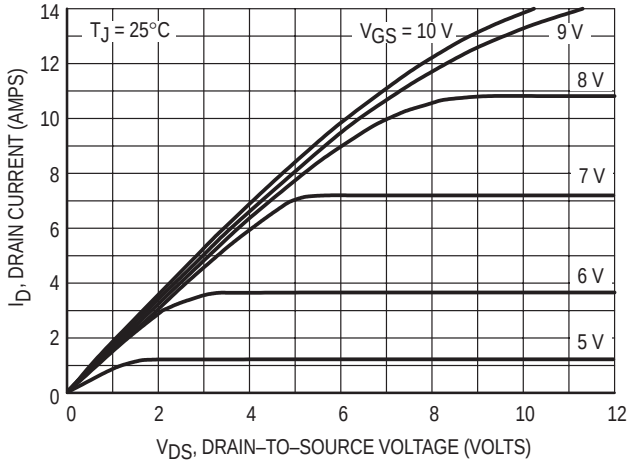


Figure 1. On–Region Characteristics

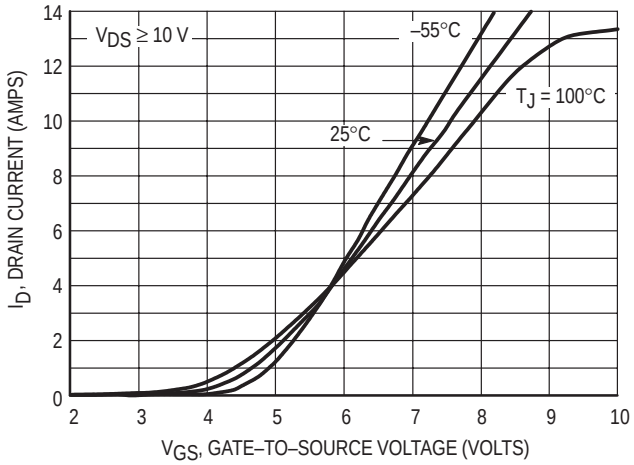


Figure 2. Transfer Characteristics

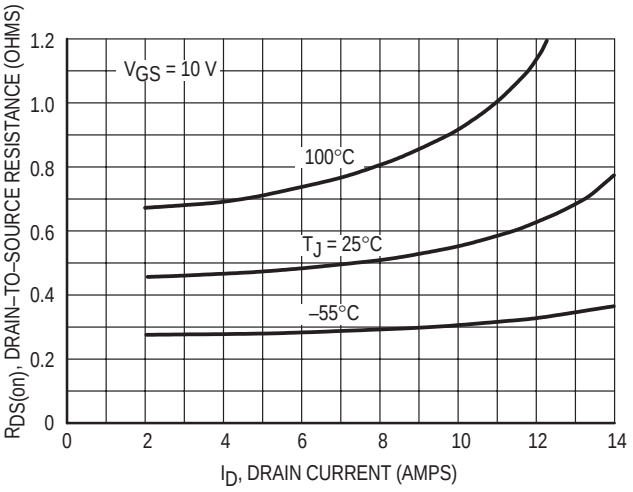


Figure 3. On–Resistance versus Drain Current and Temperature

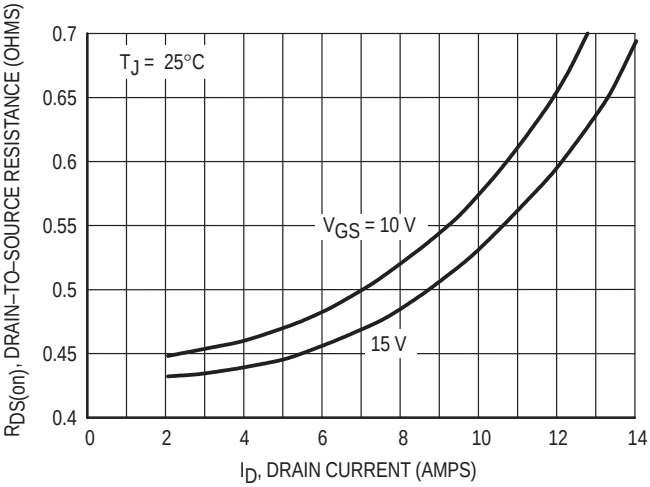


Figure 4. On–Resistance versus Drain Current and Gate Voltage

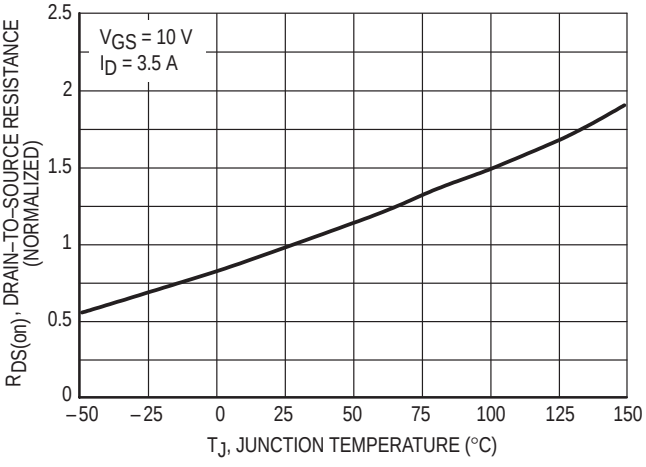


Figure 5. On–Resistance Variation with Temperature

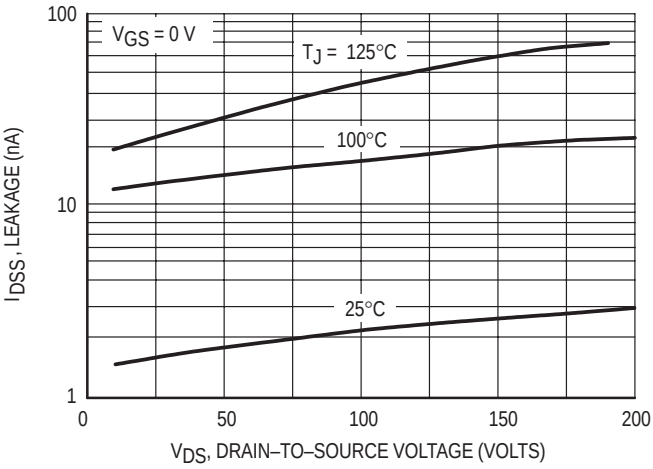


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

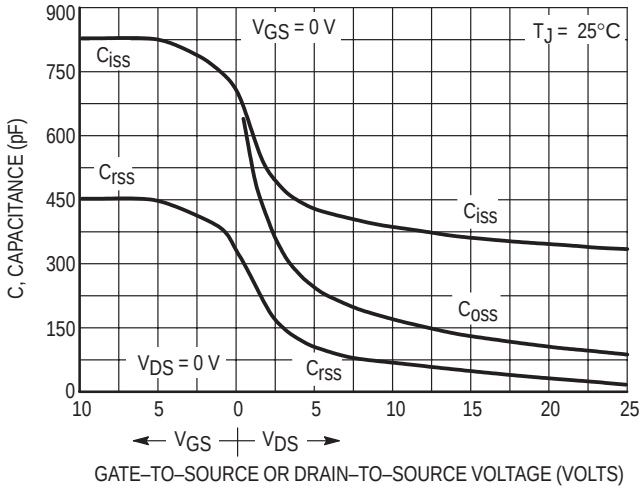


Figure 7. Capacitance Variation

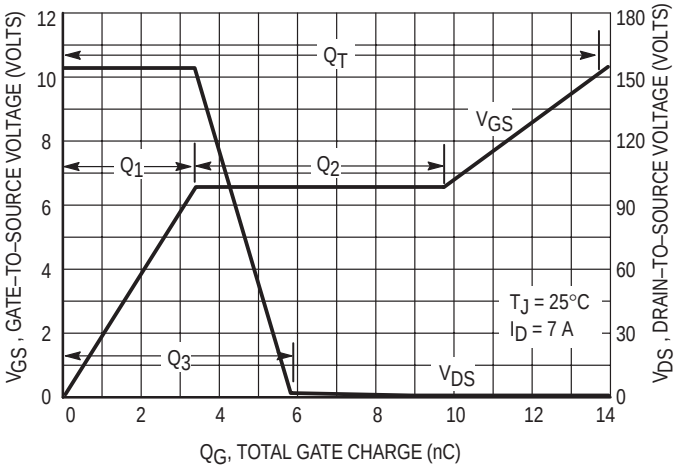


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

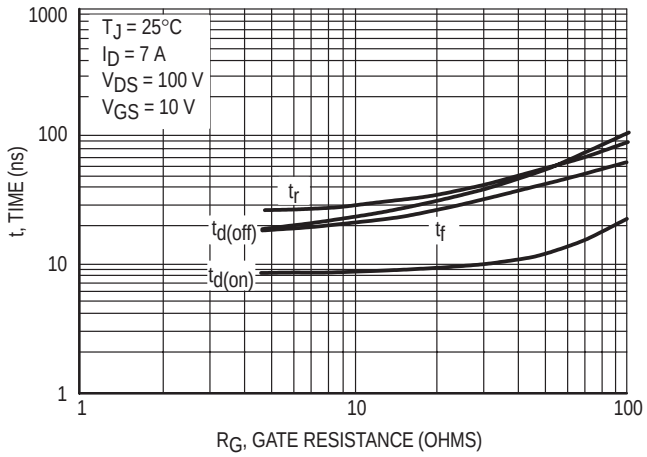


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

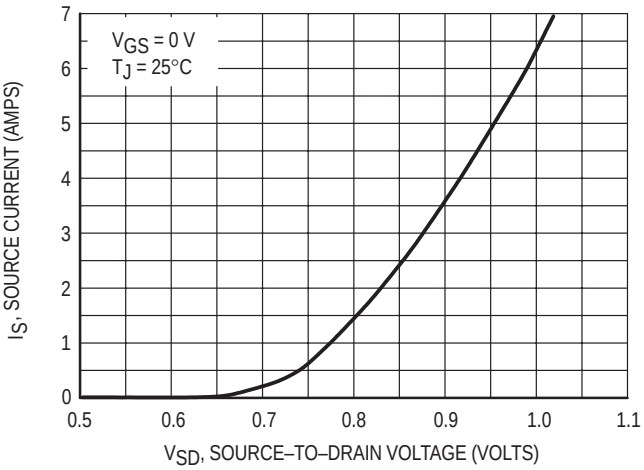


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

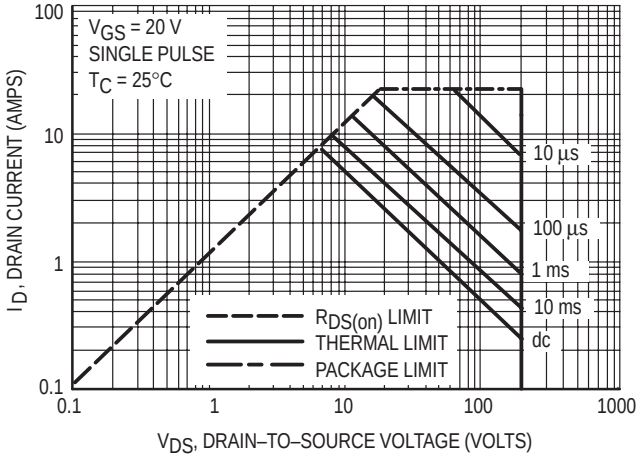


Figure 11. Maximum Rated Forward Biased Safe Operating Area

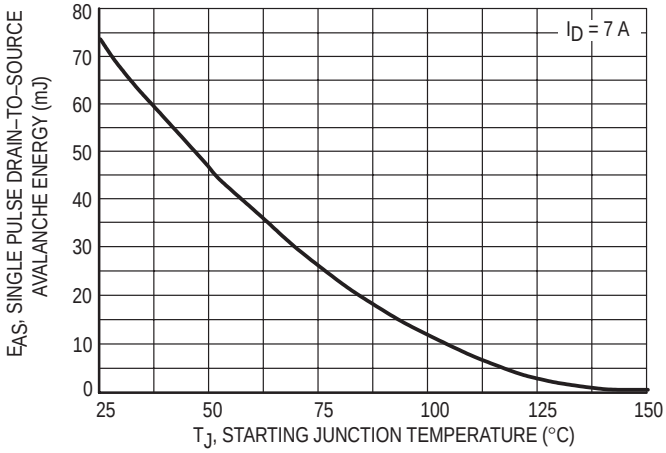


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

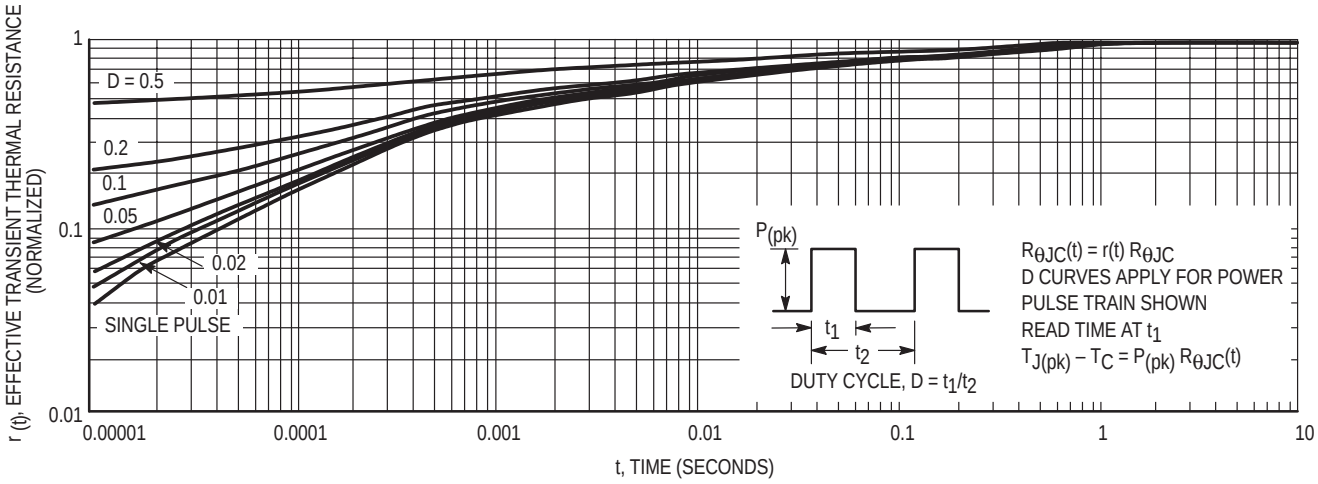


Figure 13. Thermal Response

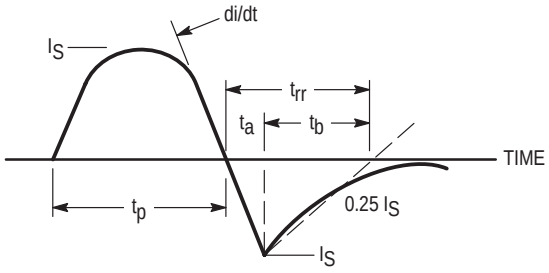


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

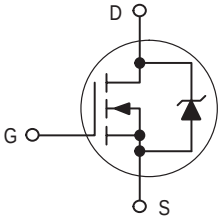
TMOS E-FET™
High Energy Power FET
N–Channel Enhancement–Mode Silicon Gate

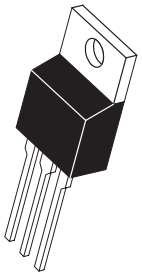
MTP8N50E

TMOS POWER FET
8.0 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.8 OHM

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode





CASE 221A–06, Style 5
TO-220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–repetitive	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	8.0 24	Adc
Total Power Dissipation Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain–to–Source Avalanche Energy — T_J = 25°C — T_J = 100°C Repetitive Pulse Drain–to–Source Avalanche Energy	$W_{DSR(1)}$ $W_{DSR(2)}$	510 82 13	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) V_{DD} = 50 V, I_D = 8.0 A
(2) Pulse Width and frequency is limited by T_J(max) and thermal response

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μAdc)	$V_{(BR)DSS}$	500	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 500 V, V_{GS} = 0) (V_{DS} = 400 V, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— —	— —	0.25 1.0	mAdc
Gate–Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) (T_J = 125°C)	$V_{GS(th)}$	2.0 1.5	— —	4.0 3.5	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)	$R_{DS(on)}$	—	0.67	0.8	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 8.0 Adc) (I_D = 4.0 Adc, T_J = 100°C)	$V_{DS(on)}$	— —	— —	7.2 6.4	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 4.0 Adc)	g_{FS}	4.0	—	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	—	1200	—	pF
Output Capacitance (V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{oss}	—	176	—	
Transfer Capacitance	C_{rss}	—	72	—	
SWITCHING CHARACTERISTICS*					
Turn–On Delay Time	$t_{d(on)}$	—	25	—	ns
Rise Time	t_r	—	36	—	
Turn–Off Delay Time (V_{DD} = 250 V, I_D = 8.0 A, R_D = 30 Ω, R_G = 9.1 Ω, $V_{GS(on)}$ = 10 V)	$t_{d(off)}$	—	75	—	
Fall Time	t_f	—	30	—	
Total Gate Charge	Q_g	—	46	63	nC
Gate–Source Charge (V_{DS} = 400 V, I_D = 8.0 A, V_{GS} = 10 V)	Q_{gs}	—	10	—	
Gate–Drain Charge	Q_{gd}	—	24	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage	V_{SD}	—	—	2.0	Vdc
Forward Turn–On Time (I_S = 8.0 A, di/dt = 100 A/μs)	t_{on}	—	**	—	ns
Reverse Recovery Time	t_{rr}	—	700	—	
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from screw on tab to center of die) (Measured from the drain lead 0.23″ from package to center of die)	L_D	— —	3.5 4.5	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_S	—	7.5	—	

* Indicates Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

** Limited by circuit inductance.

TYPICAL ELECTRICAL CHARACTERISTICS

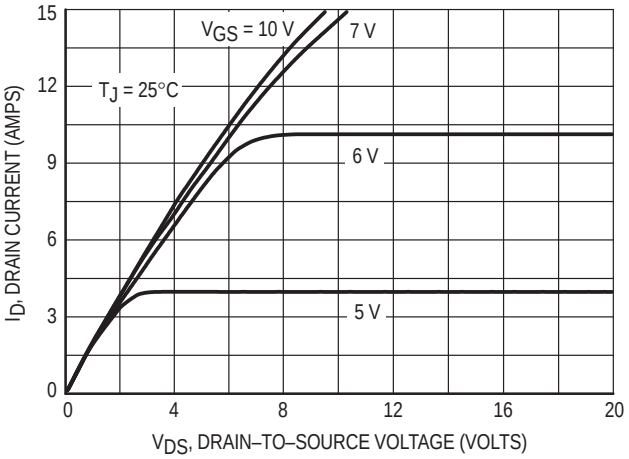


Figure 1. On–Region Characteristics

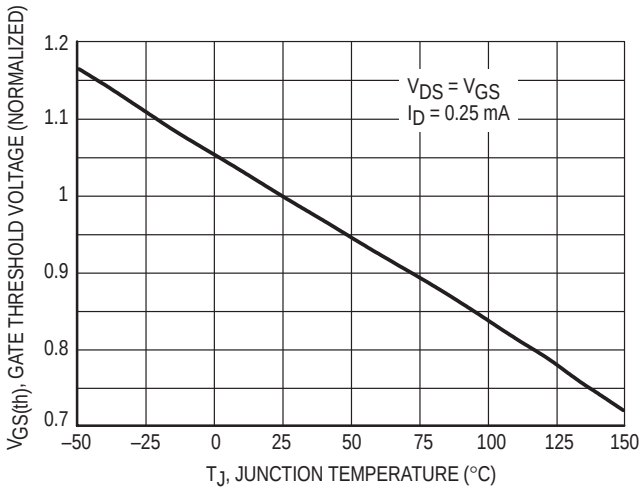


Figure 2. Gate–Threshold Voltage Variation With Temperature

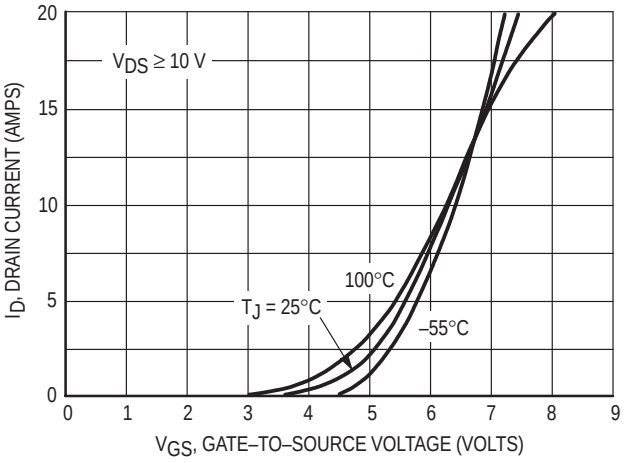


Figure 3. Transfer Characteristics

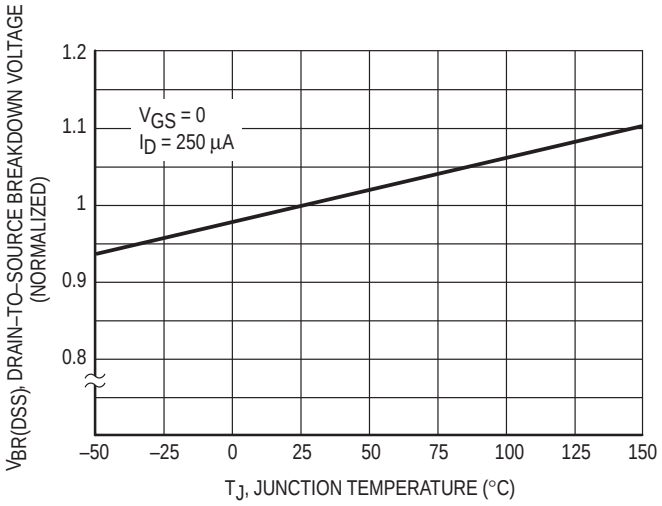


Figure 4. Breakdown Voltage Variation With Temperature

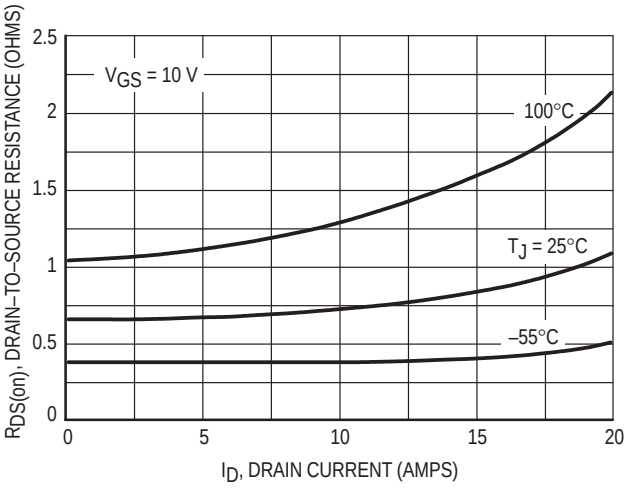


Figure 5. On–Resistance versus Drain Current

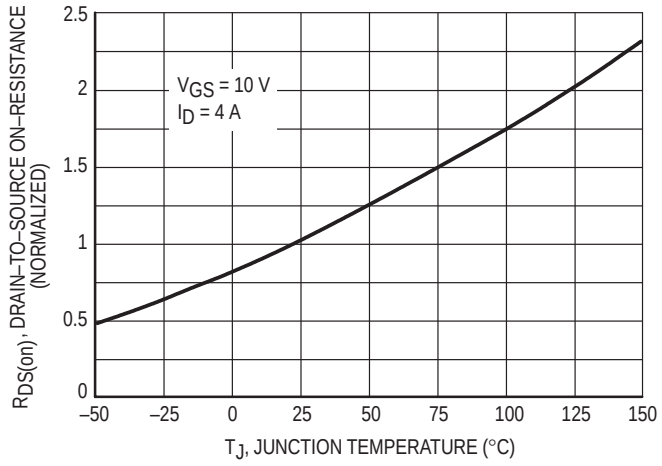


Figure 6. On–Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

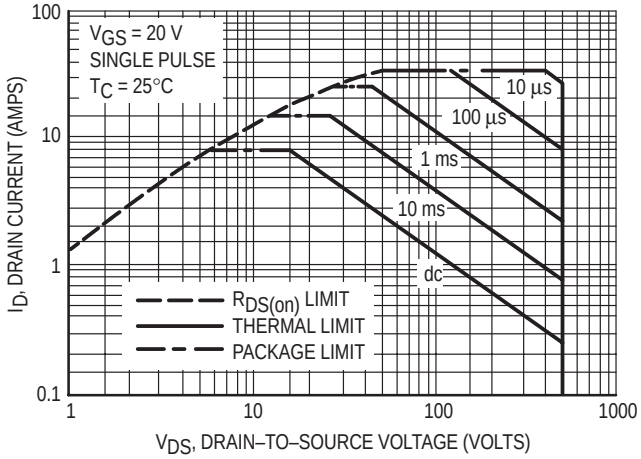


Figure 7. Maximum Rated Forward Biased Safe Operating Area

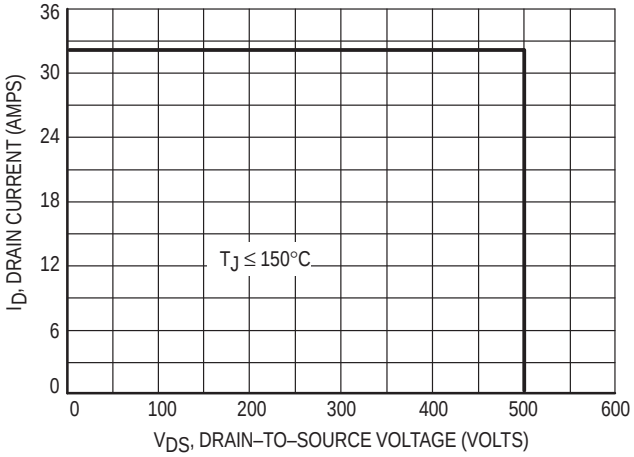


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

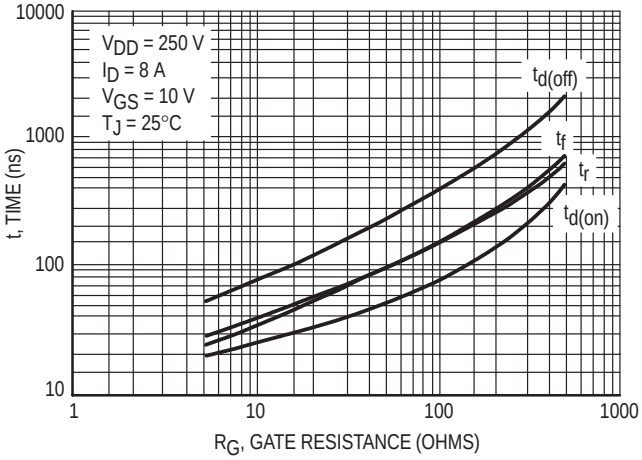


Figure 9. Resistive Switching Time Variation versus Gate Resistance

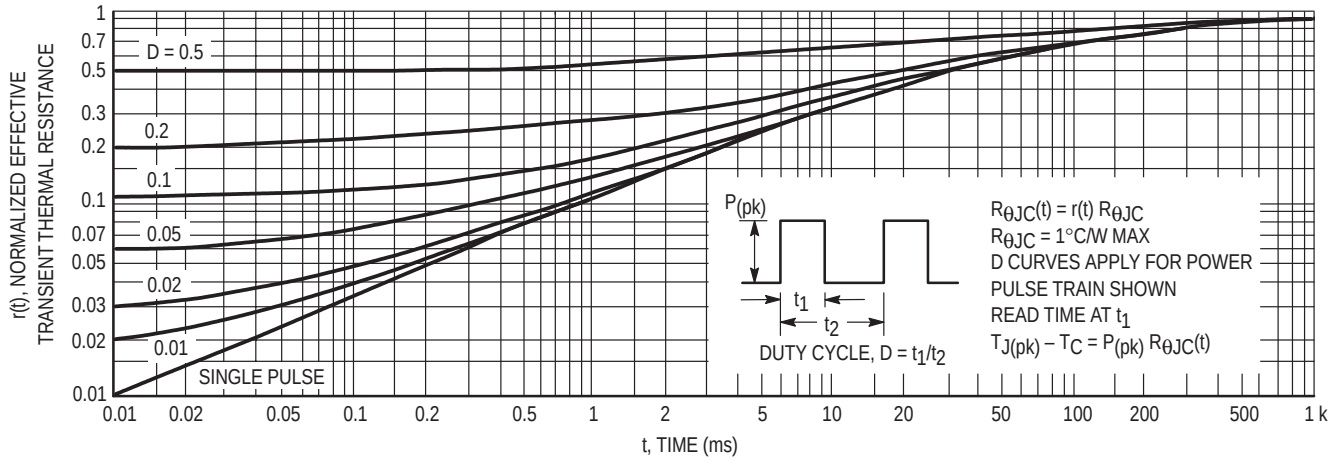


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

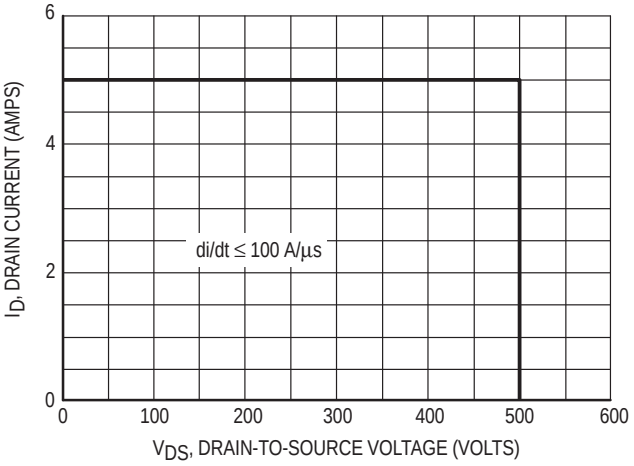


Figure 12. Commutating Safe Operating Area (CSOA)

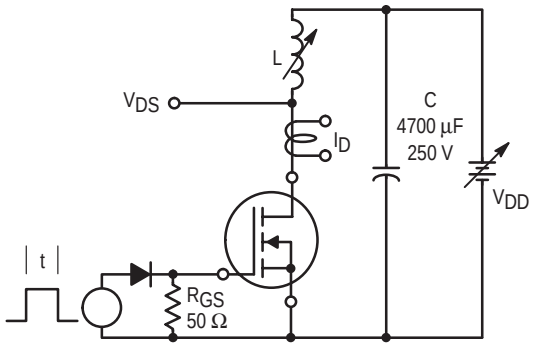


Figure 14. Unclamped Inductive Switching Test Circuit

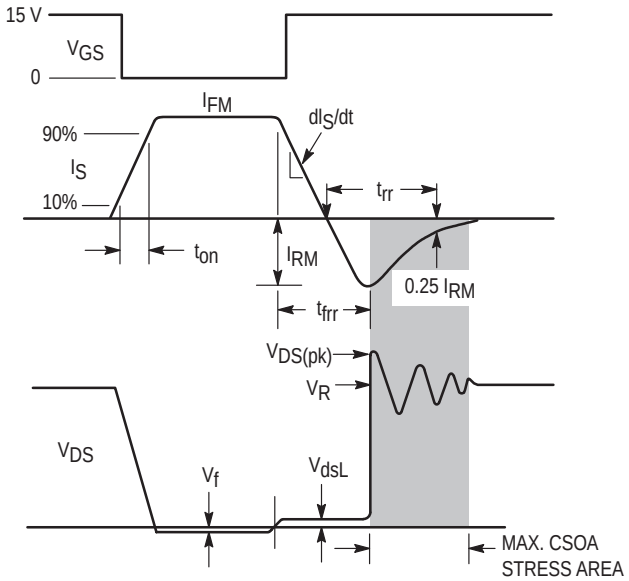


Figure 11. Commutating Waveforms

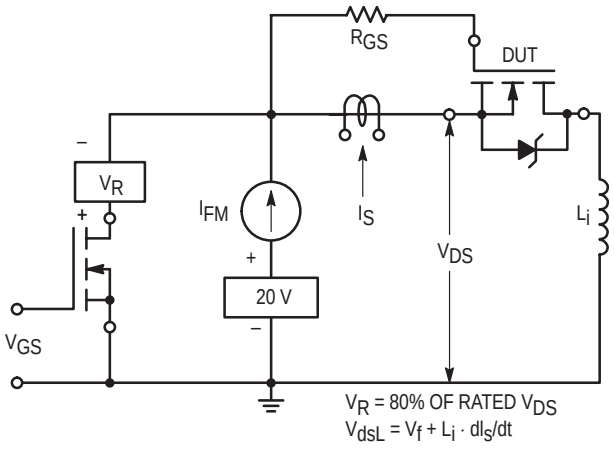


Figure 13. Commutating Safe Operating Area Test Circuit

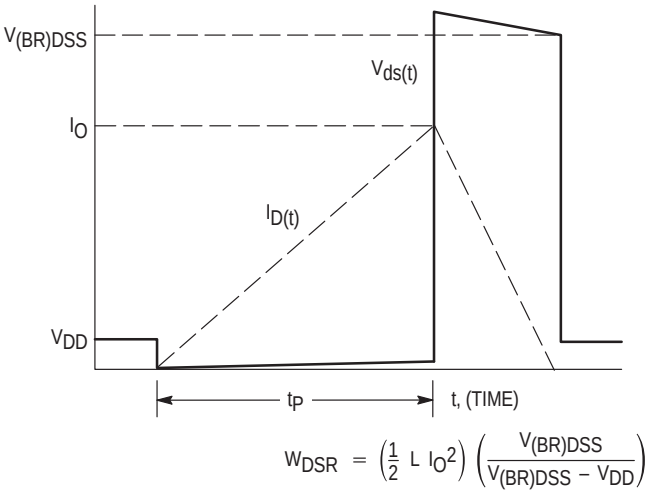


Figure 15. Unclamped Inductive Switching Waveforms

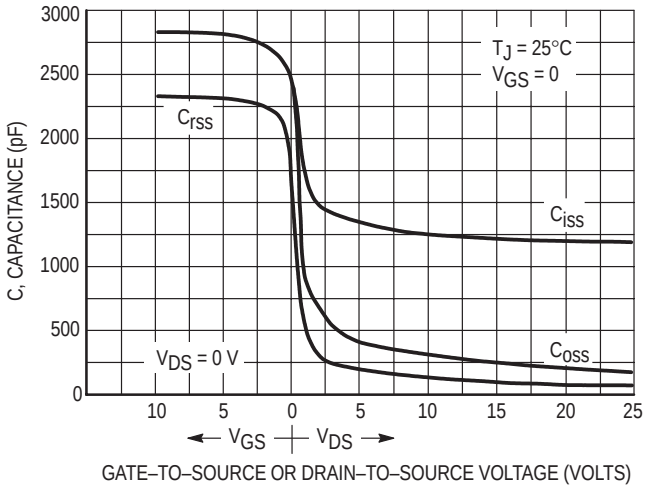


Figure 16. Capacitance Variation

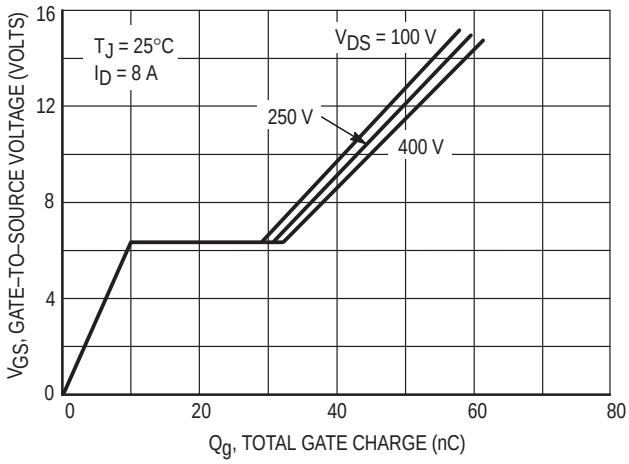
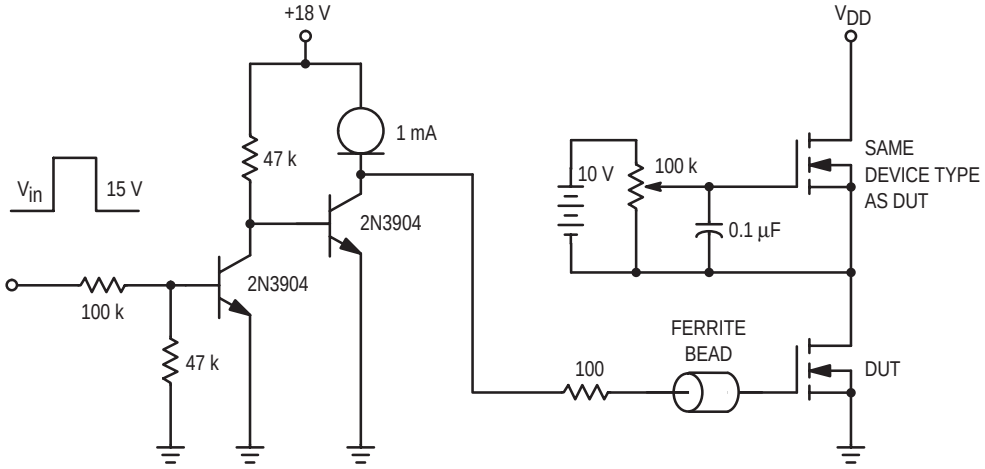


Figure 17. Gate Charge versus Gate–To–Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

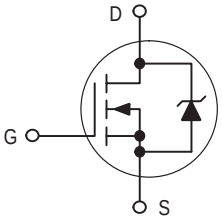
MTP9N25E

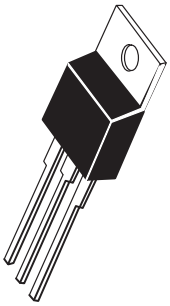
Motorola Preferred Device

TMOS POWER FET
9.0 AMPERES
250 VOLTS
$R_{DS(on)}$ = 0.45 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	250	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	250	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	9.0 5.7 32	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	80 0.64	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, Peak I_L = 9.0 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	122	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.56 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	250	—	—	Vdc
Temperature Coefficient (Positive)			—	328	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 250 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 250 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 4.5 Adc)		$R_{DS(on)}$	—	0.37	0.45	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 9.0 Adc)		$V_{DS(on)}$	—	3.5	5.4	Vdc
(V_{GS} = 10 Vdc, I_D = 4.5 Adc, T_J = 125°C)			—	—	4.7	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 4.5 Adc)		g_{FS}	3.0	5.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	783	1100	pF
Output Capacitance		C_{oss}	—	144	200	
Reverse Transfer Capacitance		C_{rss}	—	32	65	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 125 Vdc, I_D = 9.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	10	20	ns
Rise Time		t_r	—	36	70	
Turn–Off Delay Time		$t_{d(off)}$	—	27	55	
Fall Time		t_f	—	26	50	
Gate Charge (See Figure 8)	(V_{DS} = 200 Vdc, I_D = 9.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	26	40	nC
		Q_1	—	4.8	—	
		Q_2	—	12.7	—	
		Q_3	—	9.2	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 9.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.9	1.5	Vdc
	(I_S = 9.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.81	—	
Reverse Recovery Time (See Figure 14)	(I_S = 9.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	191	—	ns
		t_a	—	126	—	
		t_b	—	65	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.387	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

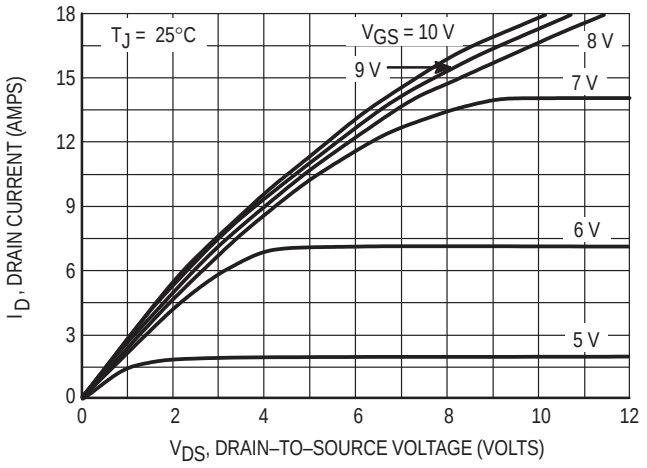


Figure 1. On–Region Characteristics

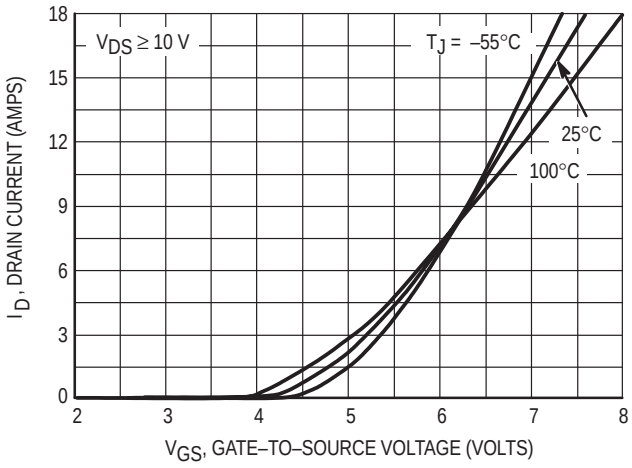


Figure 2. Transfer Characteristics

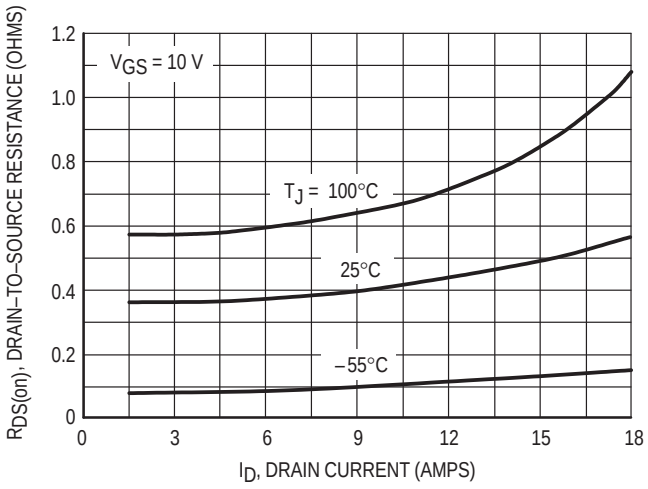


Figure 3. On–Resistance versus Drain Current and Temperature

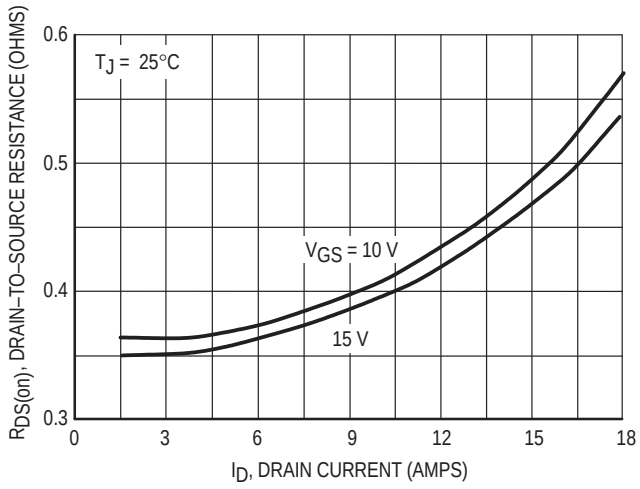


Figure 4. On–Resistance versus Drain Current and Gate Voltage

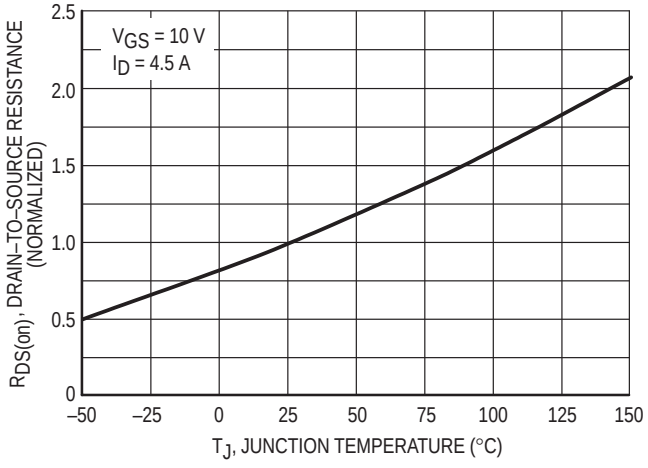


Figure 5. On–Resistance Variation with Temperature

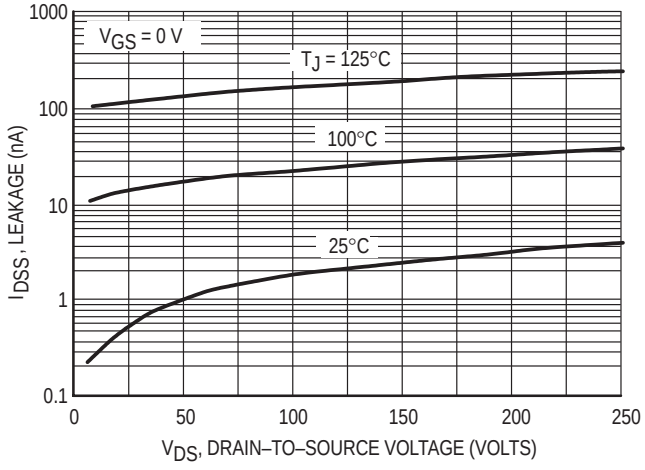


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

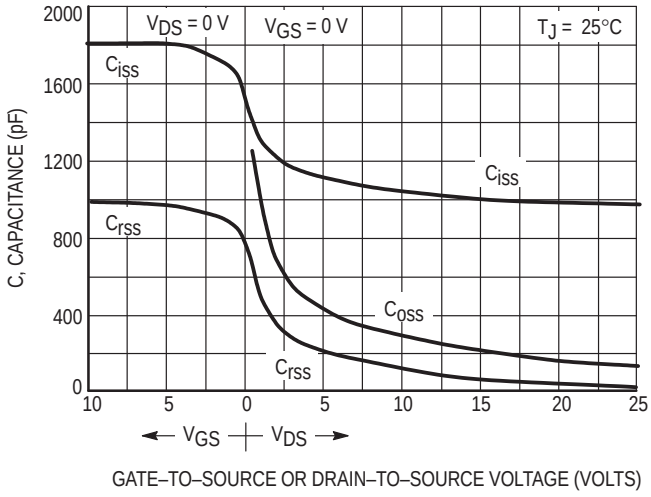


Figure 7. Capacitance Variation

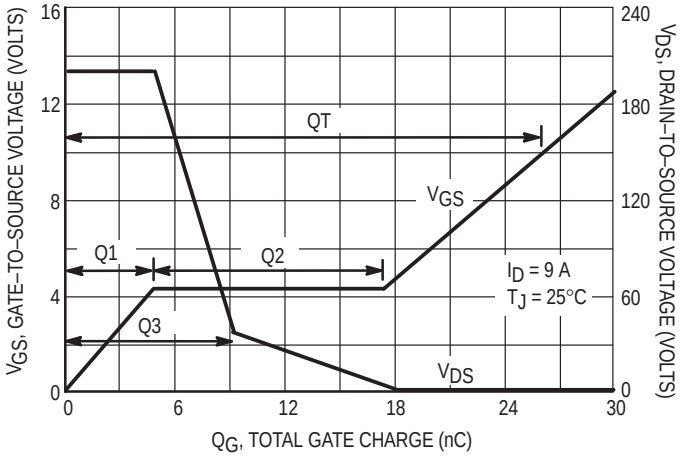


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

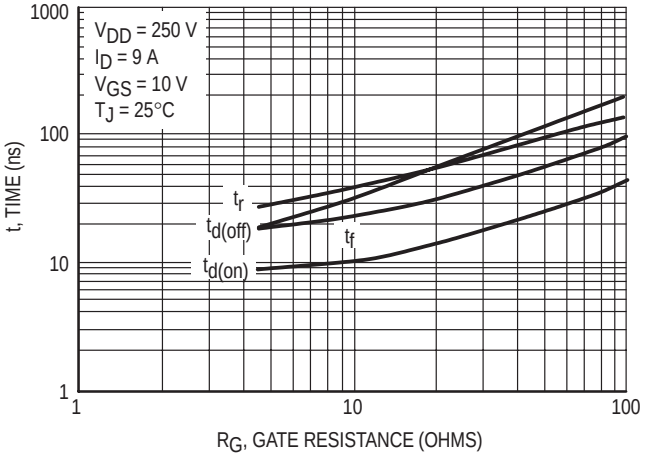


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

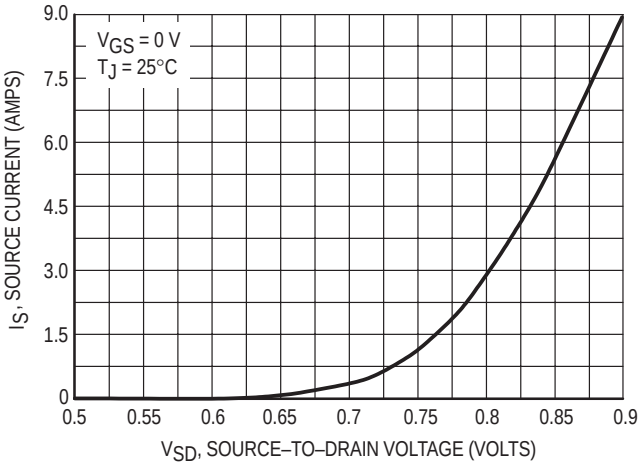


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

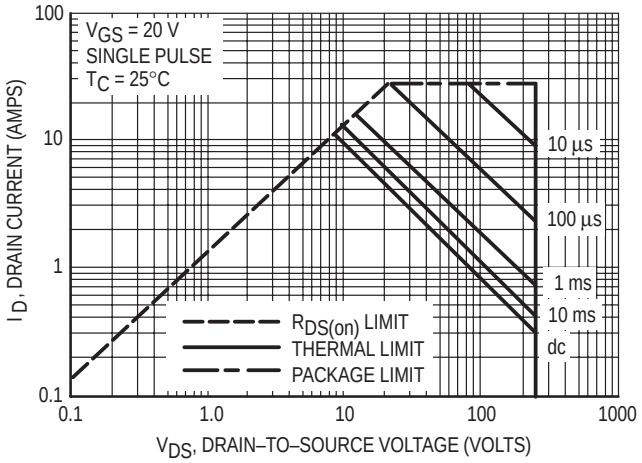


Figure 11. Maximum Rated Forward Biased Safe Operating Area

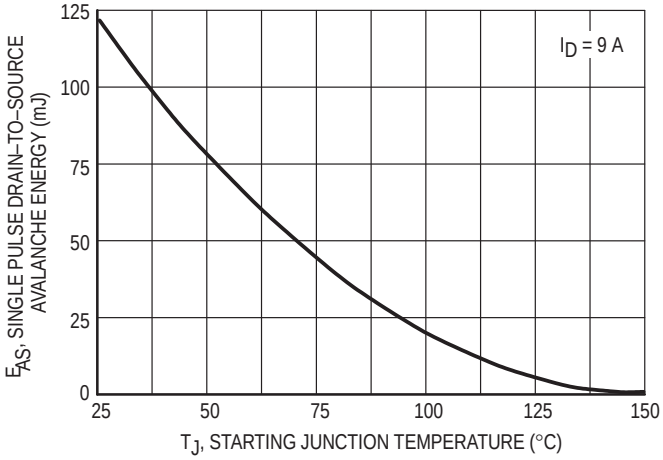


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

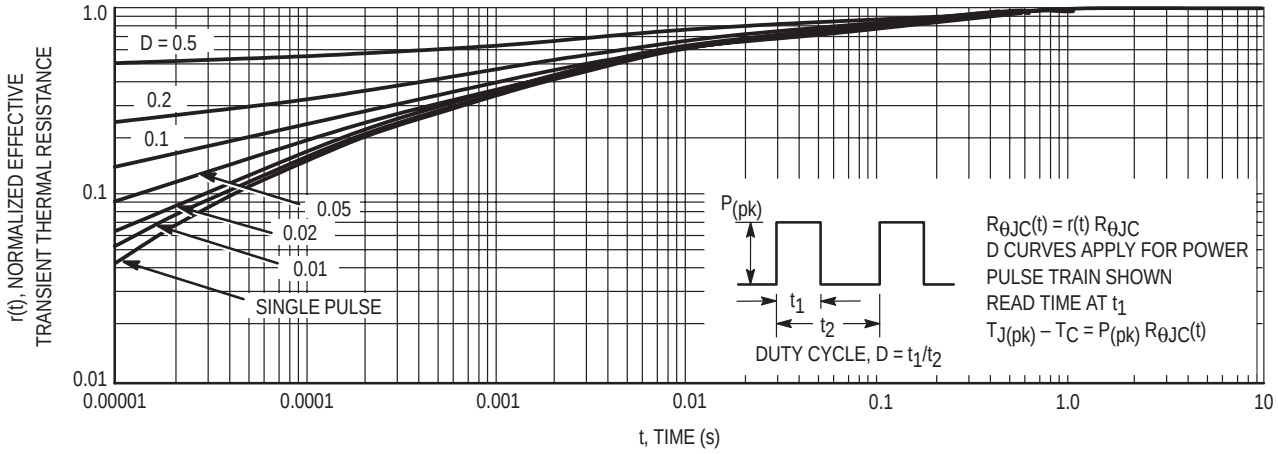


Figure 13. Thermal Response

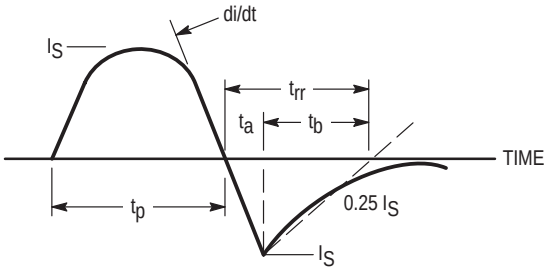


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

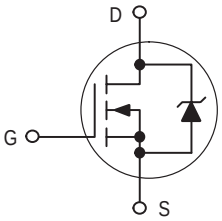
TMOS IV
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

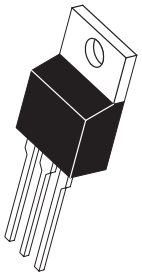
MTP10N10E

TMOS POWER FETs
10 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.25 OHM

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain–to–source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	100	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–Source Voltage	V_{GS}	±20	Vdc
Drain Current — Continuous — Pulsed	I_D I_{DM}	10 25	Adc
Total Power Dissipation Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = 0.8 Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 10 80	μA
Gate–Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate–Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA) T_J = 100°C		$V_{GS(th)}$	 2.0 1.5	 4.5 4.0	Vdc
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc)		$R_{DS(on)}$	—	0.25	Ohm
Drain–Source On–Voltage (V_{GS} = 10 V) (I_D = 10 Adc) (I_D = 5.0 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 2.7 2.4	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 5.0 A)		g_{FS}	4.0	—	mhos
DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS					
Unclamped Drain–to–Source Avalanche Energy See Figures 14 and 15 (I_D = 25 A, V_{DD} = 25 V, T_C = 25°C, Single Pulse, Non–repetitive) (I_D = 10 A, V_{DD} = 25 V, T_C = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%) (I_D = 4.0 A, V_{DD} = 25 V, T_C = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)		W_{DSR}	 — — —	 60 100 40	mJ
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz) See Figure 16	C_{iss}	—	600	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	100	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn–On Delay Time	(V_{DD} = 25 V, I_D = 5.0 A, R_G = 50 Ω) See Figure 9	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	80	
Turn–Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	80	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figures 17 and 18	Q_g	15 (Typ)	30	nC
Gate–Source Charge		Q_{gs}	8.0 (Typ)	—	
Gate–Drain Charge		Q_{gd}	7.0 (Typ)	—	
SOURCE–DRAIN DIODE CHARACTERISTICS*					
Forward On–Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	1.4 (Typ)	1.7	Vdc
Forward Turn–On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	70 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	7.5 (Typ)	—	

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

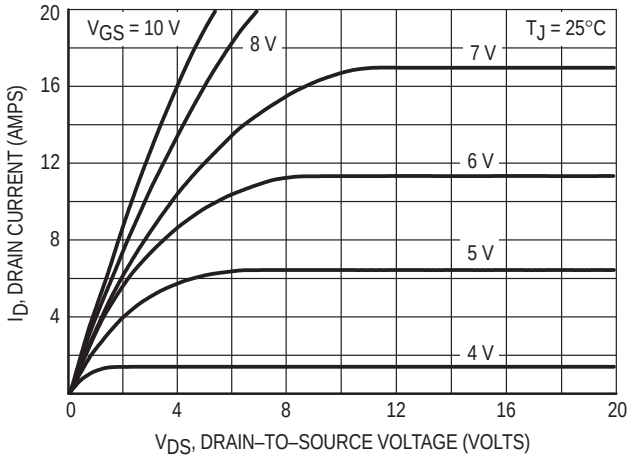


Figure 1. On–Region Characteristics

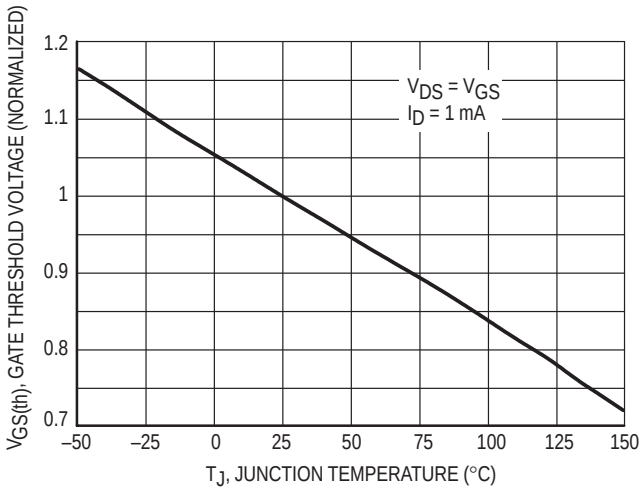


Figure 2. Gate–Threshold Voltage Variation With Temperature

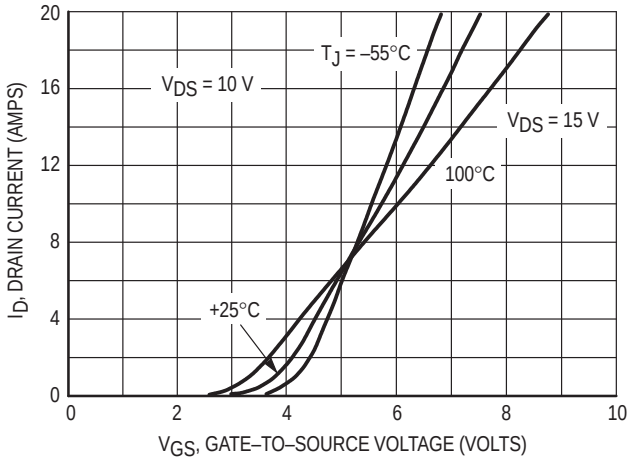


Figure 3. Transfer Characteristics

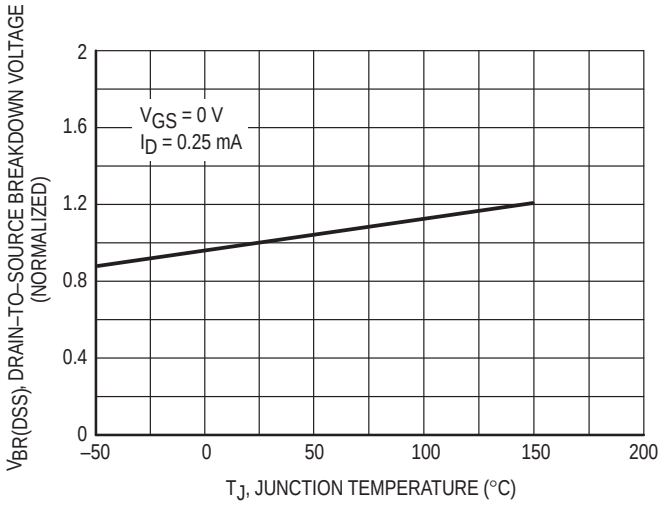


Figure 4. Breakdown Voltage Variation With Temperature

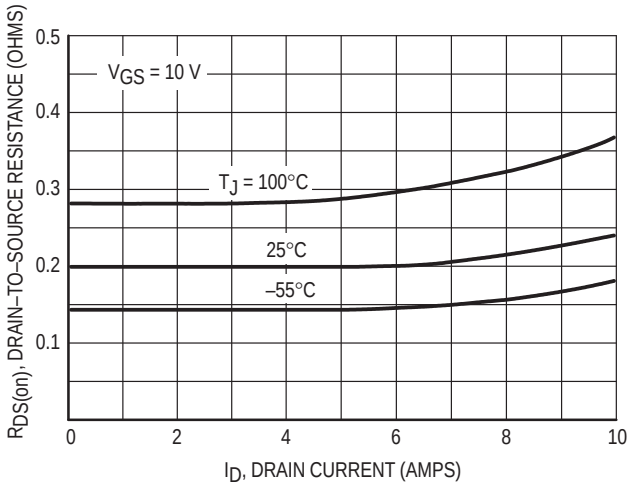


Figure 5. On–Resistance versus Drain Current

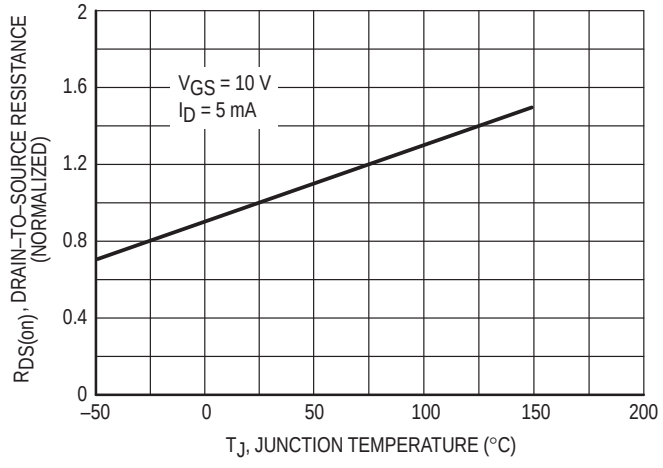


Figure 6. On–Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

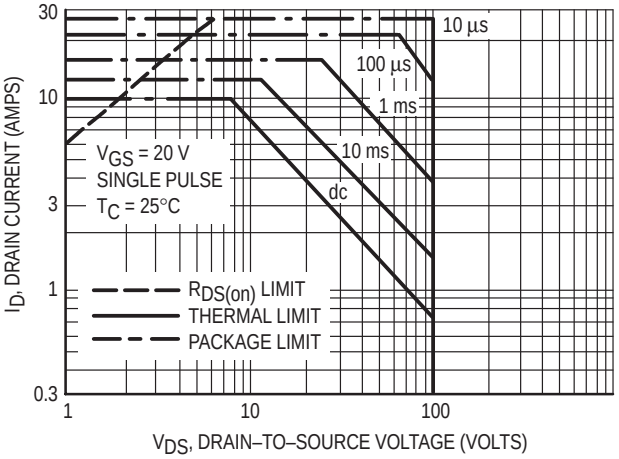


Figure 7. Maximum Rated Forward Biased Safe Operating Area

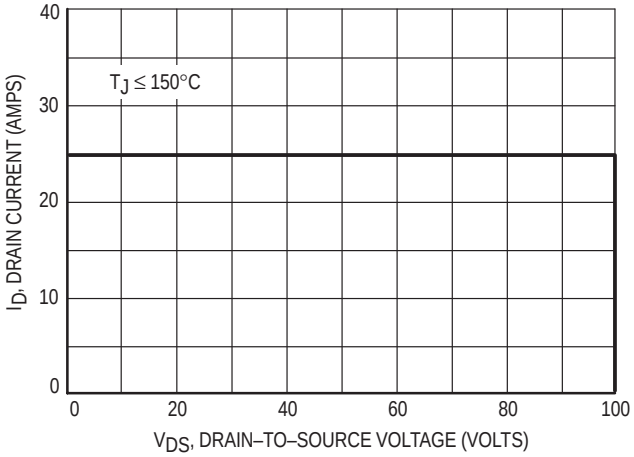


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

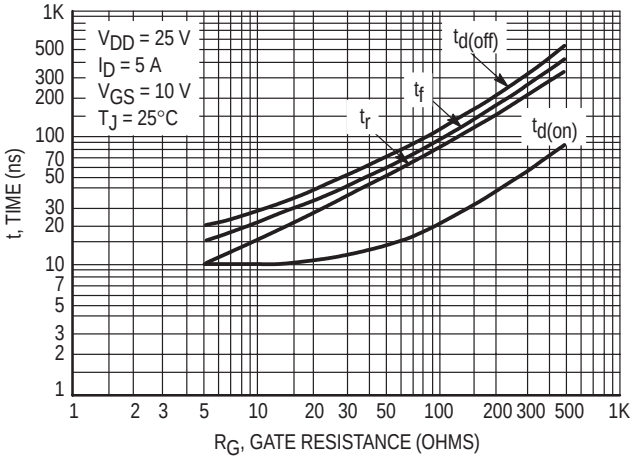


Figure 9. Resistive Switching Time versus Gate Resistance

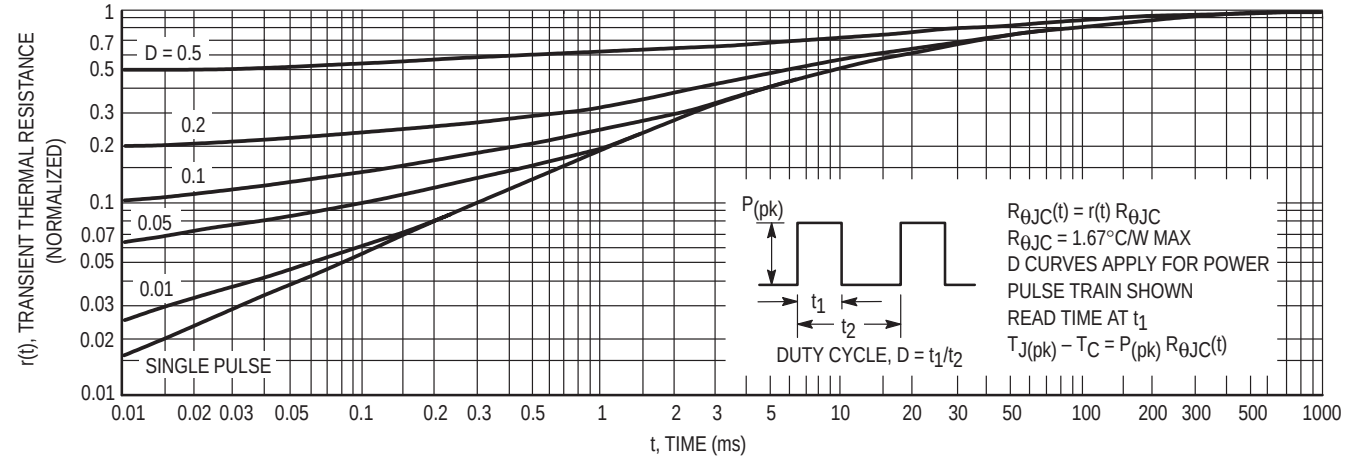


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with dI_S/dt of 400 A/μs.

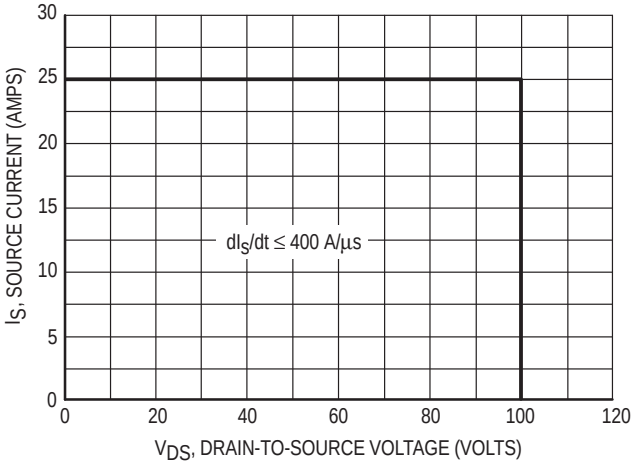


Figure 12. Commutating Safe Operating Area (CSOA)

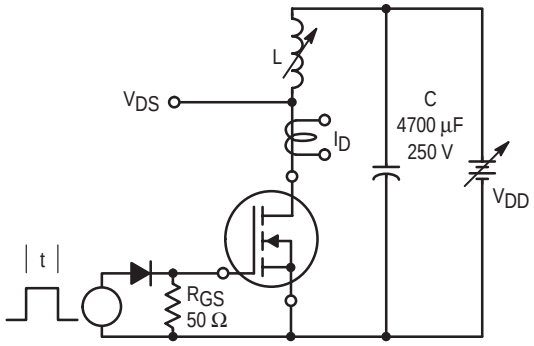


Figure 14. Unclamped Inductive Switching Test Circuit

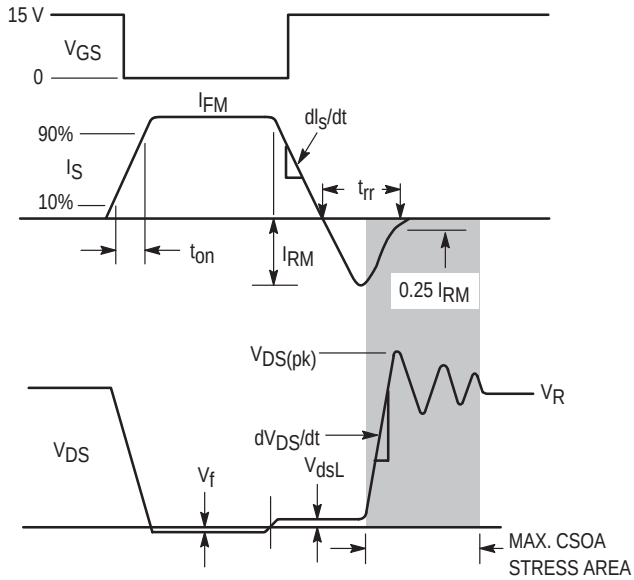


Figure 11. Commutating Waveforms

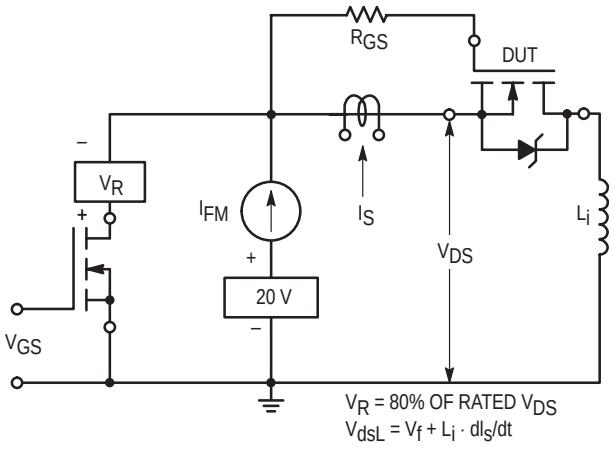


Figure 13. Commutating Safe Operating Area Test Circuit

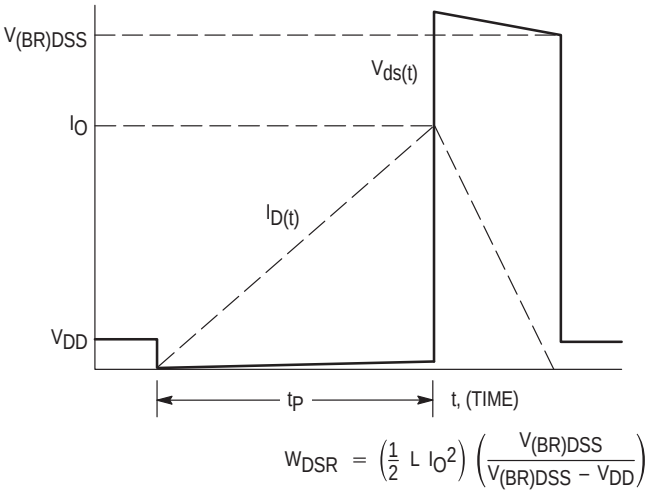


Figure 15. Unclamped Inductive Switching Waveforms

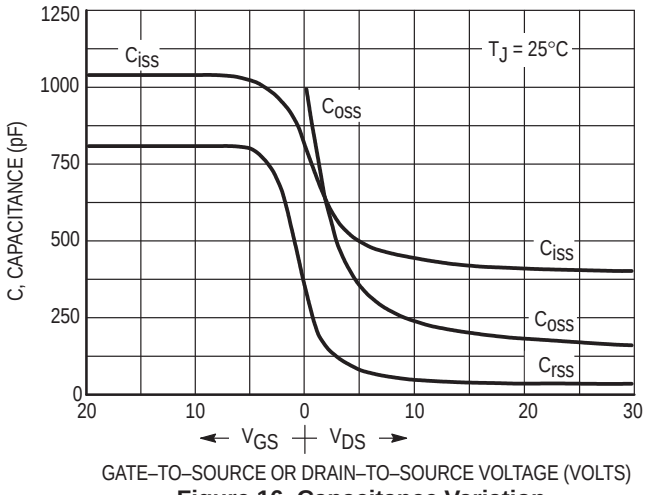


Figure 16. Capacitance Variation

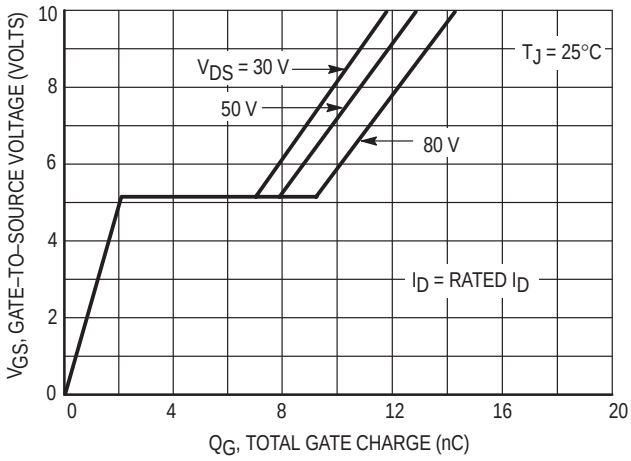
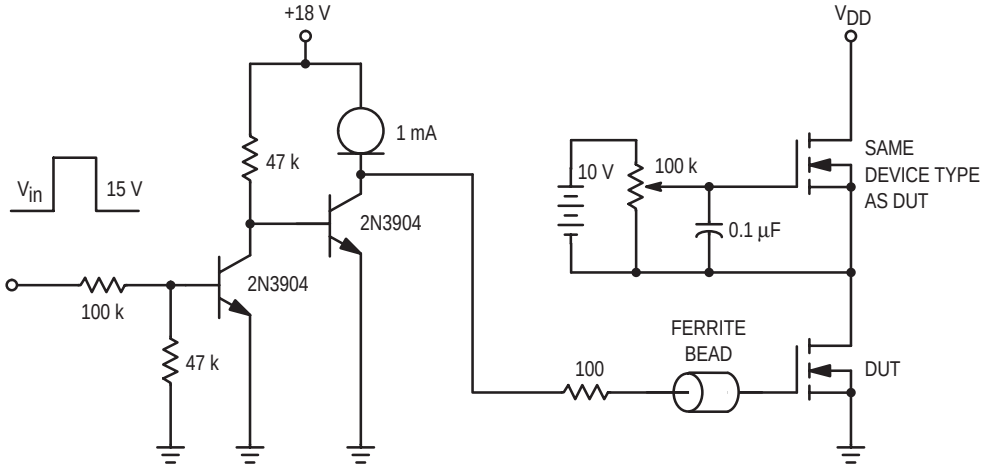


Figure 17. Gate Charge versus Gate–To–Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

Designer's™ Data Sheet

Logic Level TMOS E-FET™ Power Field Effect Transistor

N–Channel Enhancement–Mode Silicon Gate

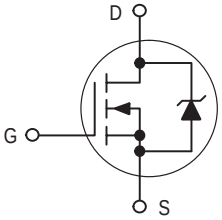
MTP10N10EL

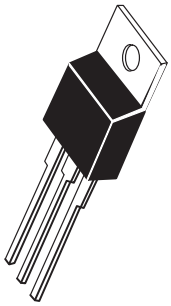
Motorola Preferred Device

TMOS POWER FET
10 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.22 OHMS

This advanced TMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	100	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±15 ±20	Vdc Vpk
Drain Current — Continuous @ T_C = 25°C — Continuous @ T_C = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	10 6.0 35	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C Total Power Dissipation @ T_C = 25°C (1)	P_D	40 0.32 1.75	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 10 Adc, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	 50	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.13 100 71.4	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	100	—	—	Vdc
Temperature Coefficient (Positive)			—	115	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.45	2.0	Vdc
Threshold Temperature Coefficient (Negative)			—	4.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 5.0 Adc)		$R_{DS(on)}$	—	0.17	0.22	Ohm
Drain–to–Source On–Voltage (V_{GS} = 5.0 Vdc, I_D = 10 Adc)		$V_{DS(on)}$	—	1.85	2.6	Vdc
(V_{GS} = 5.0 Vdc, I_D = 5.0 Adc, T_J = 125°C)			—	—	2.3	
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 5.0 Adc)		g_{FS}	5.0	7.9	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	741	1040	pF
Output Capacitance		C_{oss}	—	175	250	
Reverse Transfer Capacitance		C_{rss}	—	18.9	40	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 50 Vdc, I_D = 10 Adc, V_{GS} = 5.0 Vdc, R_g = 9.1 Ω)	$t_{d(on)}$	—	11	20	ns
Rise Time		t_r	—	74	150	
Turn–Off Delay Time		$t_{d(off)}$	—	17	30	
Fall Time		t_f	—	38	80	
Gate Charge (See Figure 8)	(V_{DS} = 80 Vdc, I_D = 10 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	9.3	15	nC
		Q_1	—	2.56		
		Q_2	—	4.4	—	
		Q_3	—	4.6	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 10 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.98	1.6	Vdc
	(I_S = 10 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.898	—	
Reverse Recovery Time	(I_S = 10 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	124.7	—	ns
		t_a	—	86	—	
		t_b	—	38.7	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.539	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_d	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.)		L_s	—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

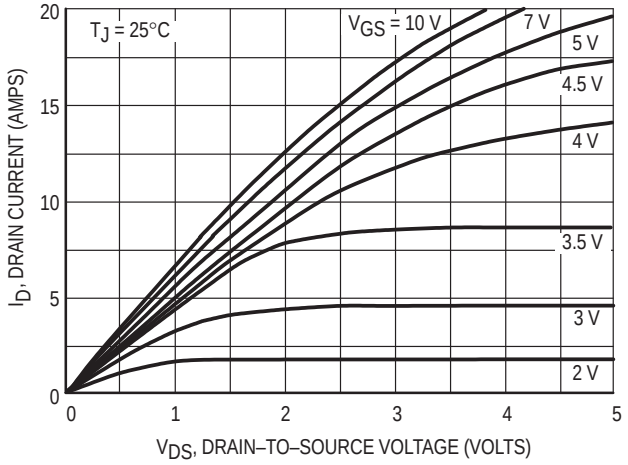


Figure 1. On–Region Characteristics

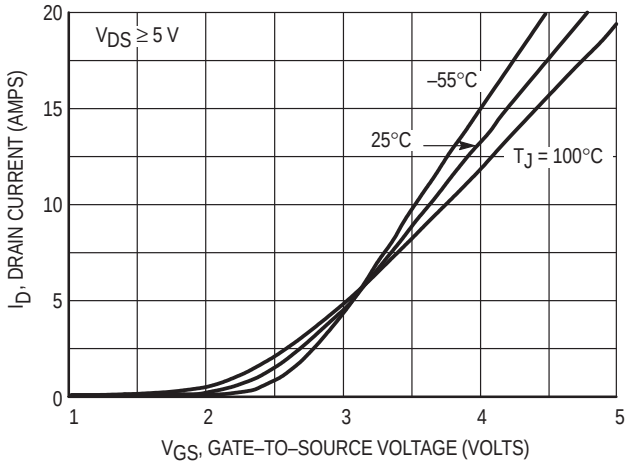


Figure 2. Transfer Characteristics

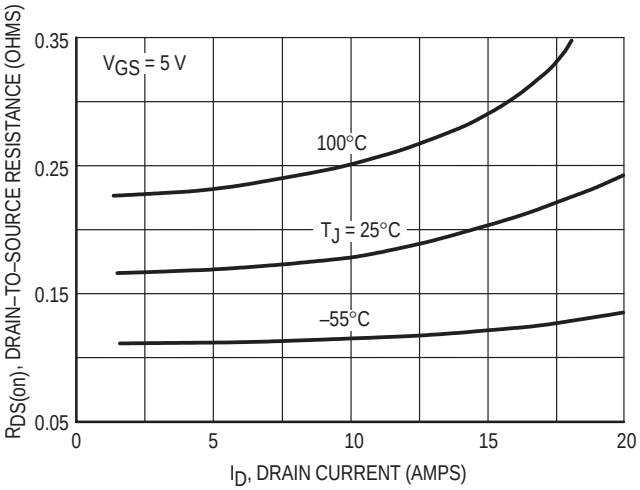


Figure 3. On–Resistance versus Drain Current and Temperature

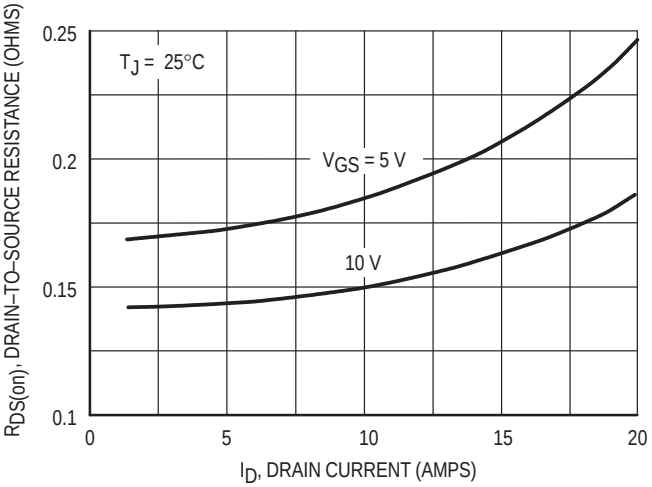


Figure 4. On–Resistance versus Drain Current and Gate Voltage

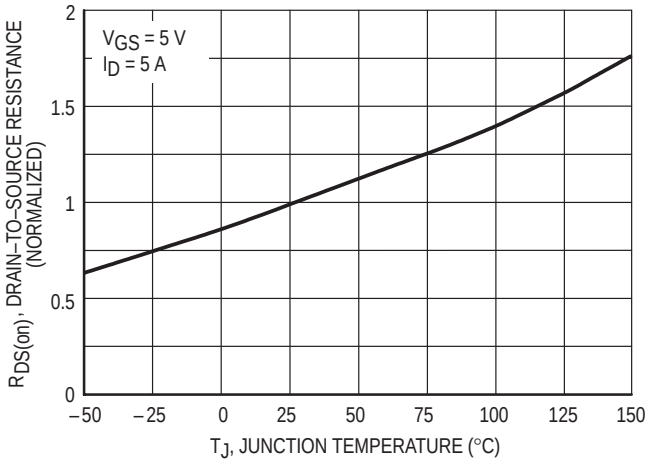


Figure 5. On–Resistance Variation with Temperature

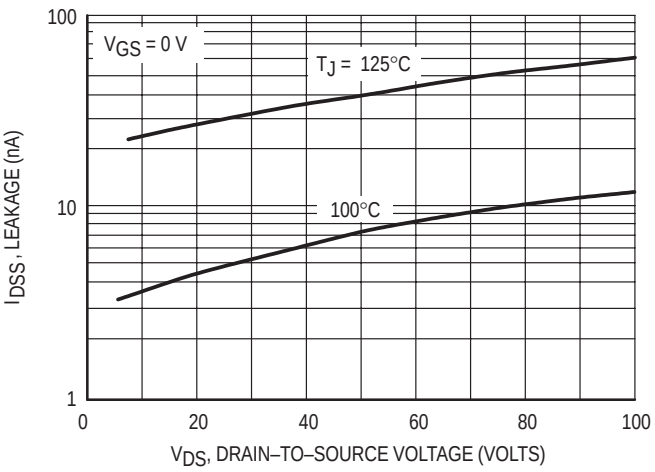


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

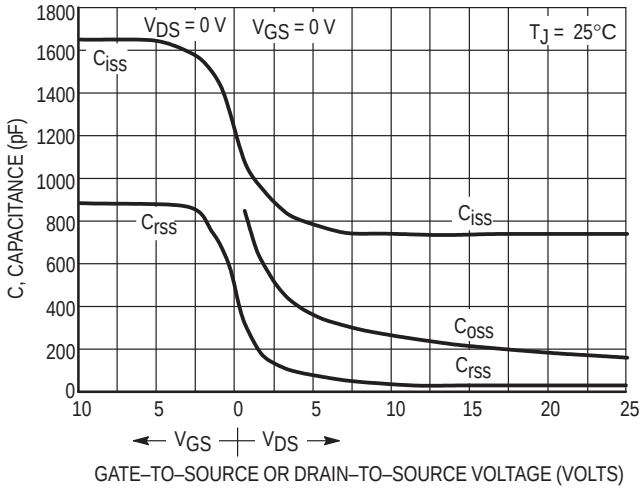


Figure 7. Capacitance Variation

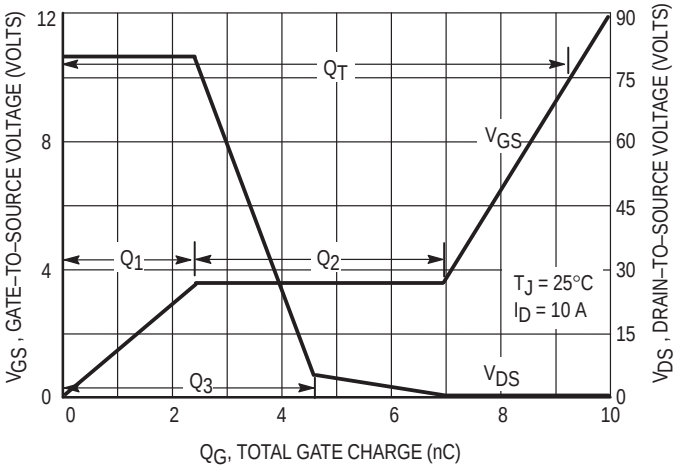


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

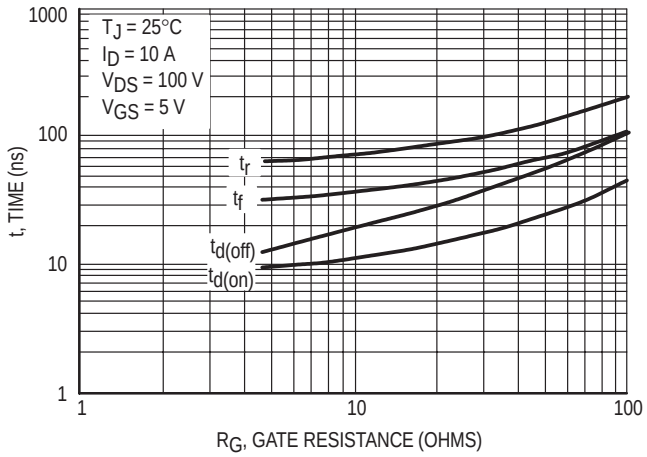


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

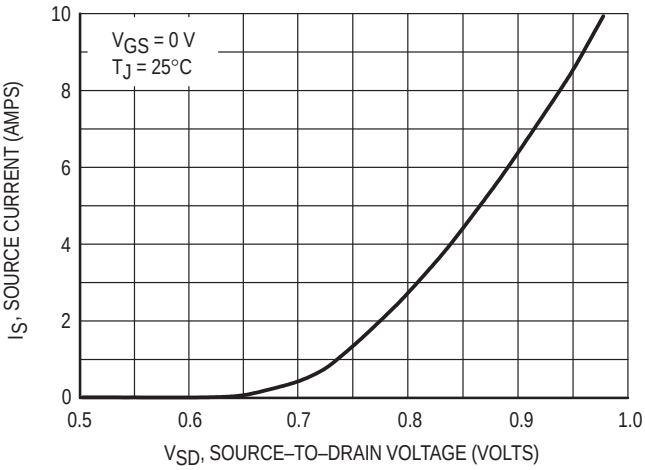


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

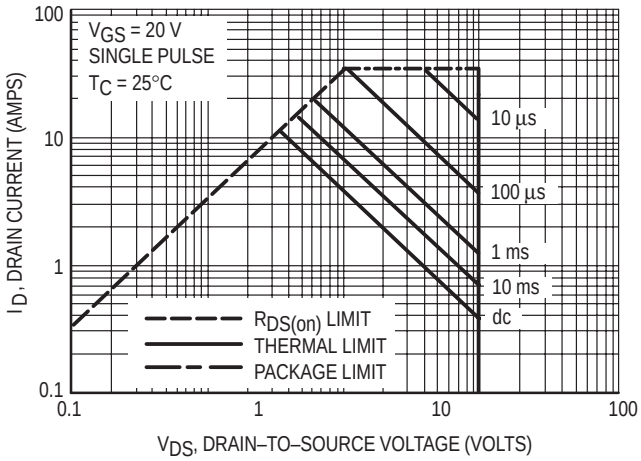


Figure 11. Maximum Rated Forward Biased Safe Operating Area

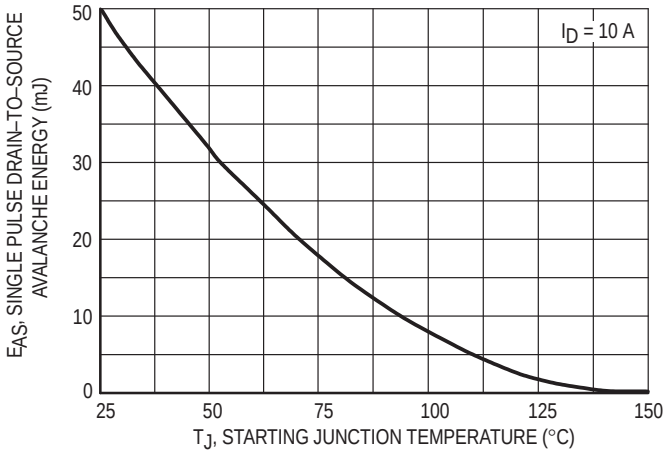


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

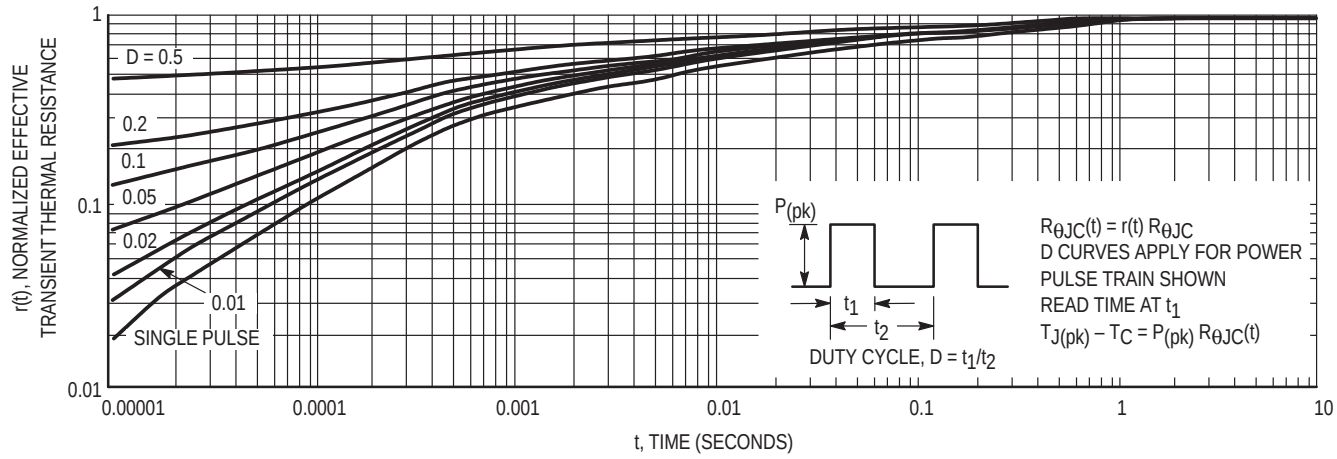


Figure 13. Thermal Response

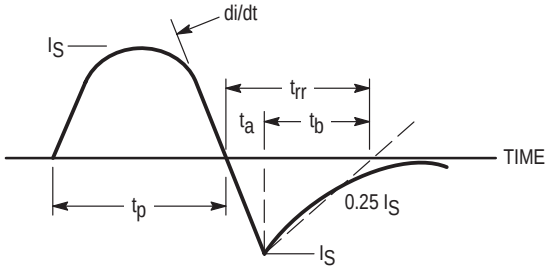


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

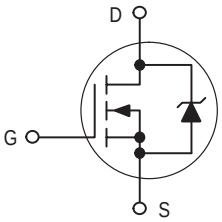
TMOS E-FET™
High Energy Power FET
N–Channel Enhancement–Mode Silicon Gate

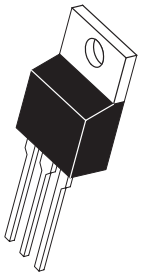
MTP10N40E

TMOS POWER FET
10 AMPERES
400 VOLTS
$R_{DS(on)}$ = 0.55 OHMS

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode





CASE 221A–06, Style 5
TO-220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	400	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate–Source Voltage — Continuous — Non–repetitive	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	10 40	Adc
Total Power Dissipation Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain–to–Source Avalanche Energy — T_J = 25°C — T_J = 100°C Repetitive Pulse Drain–to–Source Avalanche Energy	$W_{DSR(1)}$ $W_{DSR(2)}$	520 83 13	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

(1) V_{DD} = 50 V, I_D = 10 A
(2) Pulse Width and frequency is limited by T_J(max) and thermal response

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	400	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 400 V, V_{GS} = 0) (V_{DS} = 320 V, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 — —	 0.25 1.0	mAdc
Gate–Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mAdc) (T_J = 125°C)		$V_{GS(th)}$	 2.0 1.5	 — —	 4.0 3.5	Vdc
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 5.0 A)		$R_{DS(on)}$	—	0.4	0.55	Ohms
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 5.0 A) (I_D = 2.5 A, T_J = 100°C)		$V_{DS(on)}$	 — —	 — —	 6.0 4.75	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 5.0 A)		g_{FS}	4.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1570	—	pF
Output Capacitance		C_{oss}	—	230	—	
Transfer Capacitance		C_{rss}	—	55	—	
SWITCHING CHARACTERISTICS*						
Turn–On Delay Time	(V_{DD} = 200 V, $I_D \approx$ 10 A, R_L = 20 Ω, R_G = 9.1 Ω, $V_{GS(on)}$ = 10 V)	$t_{d(on)}$	—	25	—	ns
Rise Time		t_r	—	37	—	
Turn–Off Delay Time		$t_{d(off)}$	—	75	—	
Fall Time		t_f	—	31	—	
Total Gate Charge	(V_{DS} = 320 V, I_D = 10 A, V_{GS} = 10 V)	Q_g	—	46	63	nC
Gate–Source Charge		Q_{gs}	—	10	—	
Gate–Drain Charge		Q_{gd}	—	23	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 10 A, di/dt = 100 A/μs)	V_{SD}	—	—	2.0	Vdc
Forward Turn–On Time		t_{on}	—	**	—	ns
Reverse Recovery Time		t_{rr}	—	250	—	
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 — —	 3.5 4.5	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	—	7.5	—	nH

* Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

** Limited by circuit inductance.

TYPICAL ELECTRICAL CHARACTERISTICS

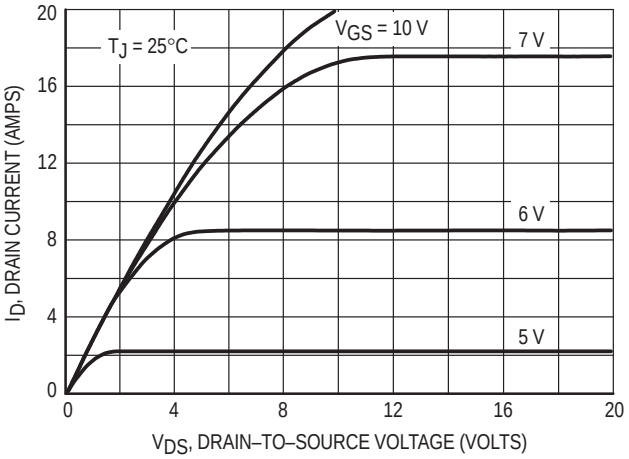


Figure 1. On–Region Characteristics

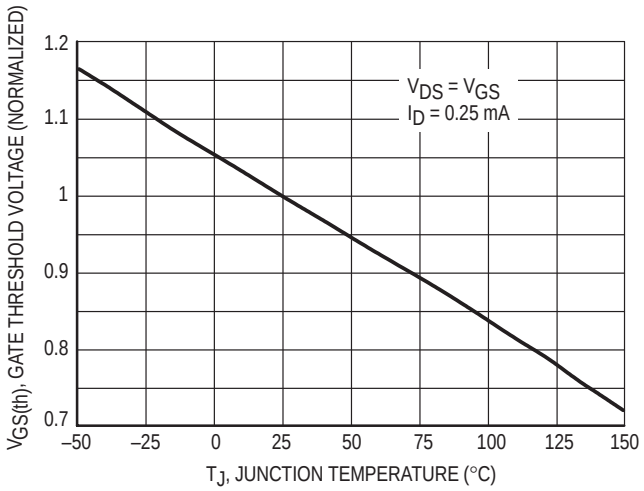


Figure 2. Gate–Threshold Voltage Variation With Temperature

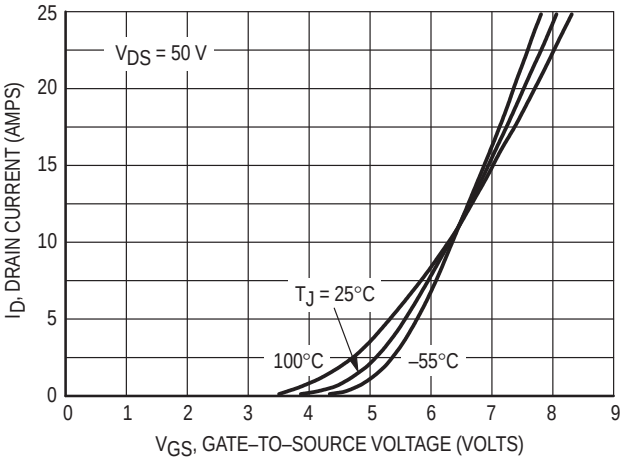


Figure 3. Transfer Characteristics

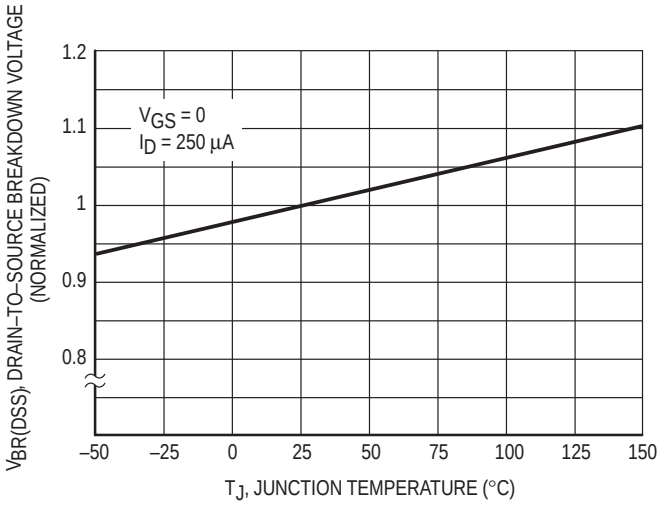


Figure 4. Breakdown Voltage Variation With Temperature

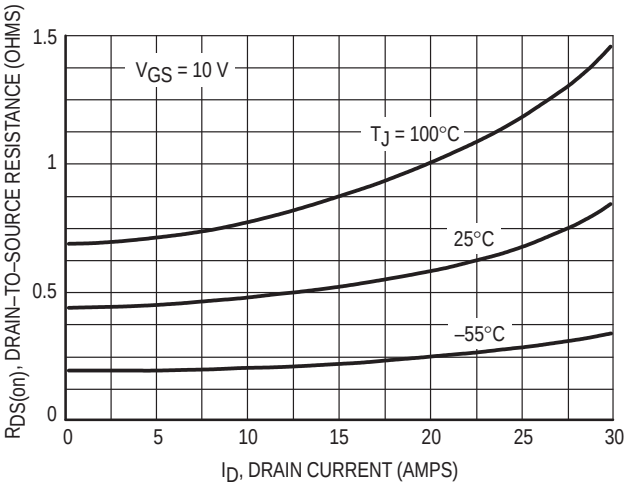


Figure 5. On–Resistance versus Drain Current

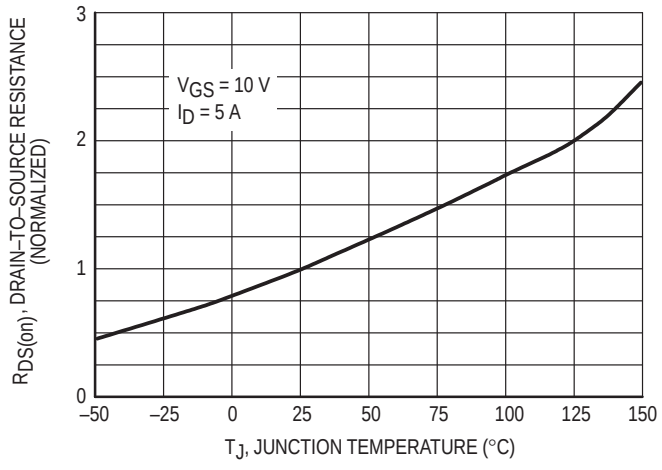


Figure 6. On–Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

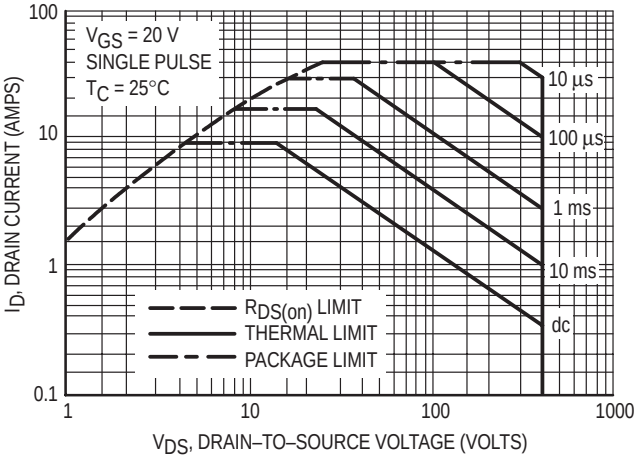


Figure 7. Maximum Rated Forward Biased Safe Operating Area

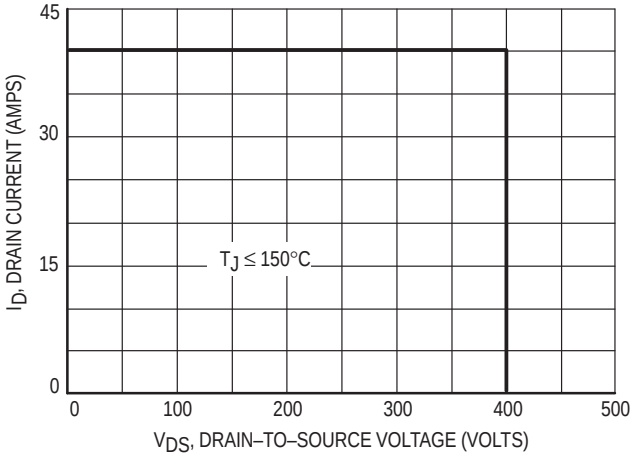


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

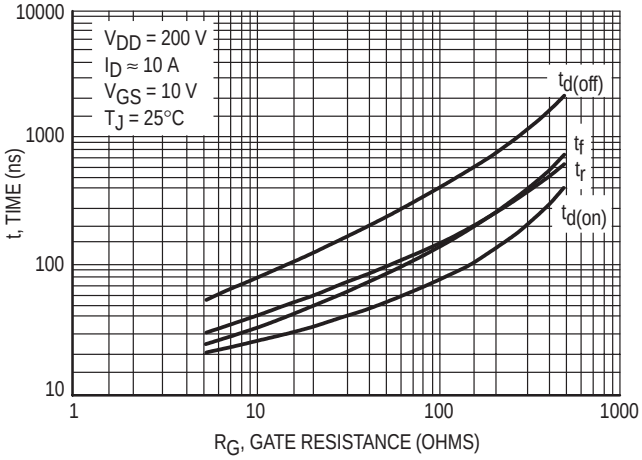


Figure 9. Resistive Switching Time Variation versus Gate Resistance

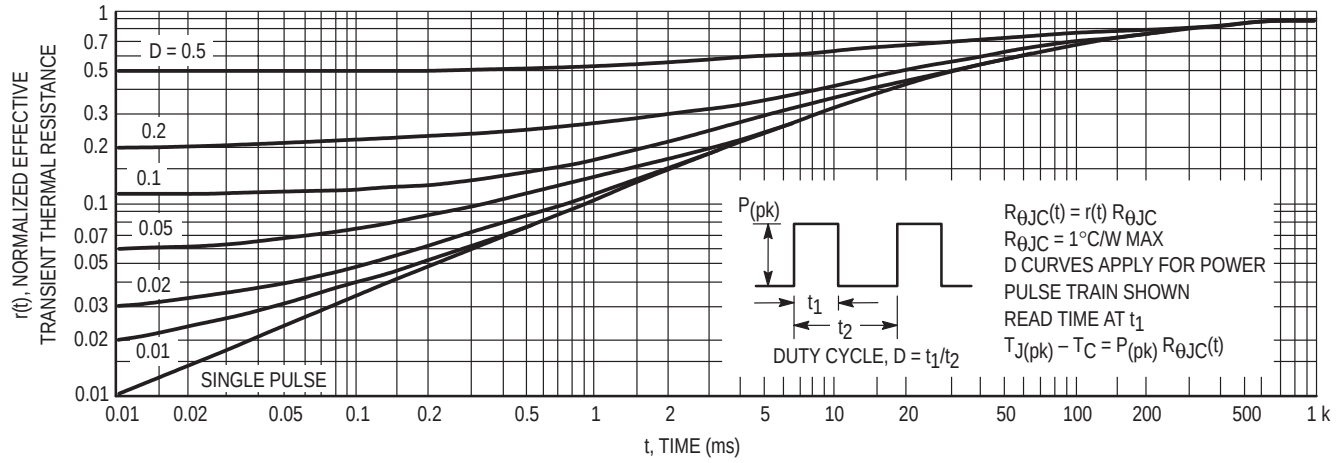


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

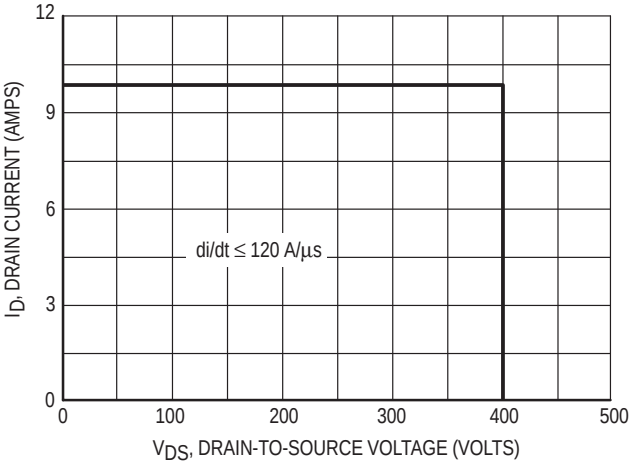


Figure 12. Commutating Safe Operating Area (CSOA)

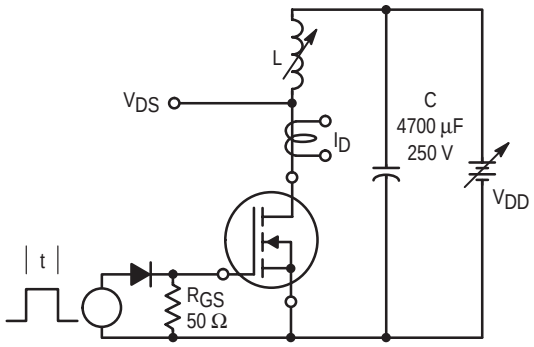


Figure 14. Unclamped Inductive Switching Test Circuit

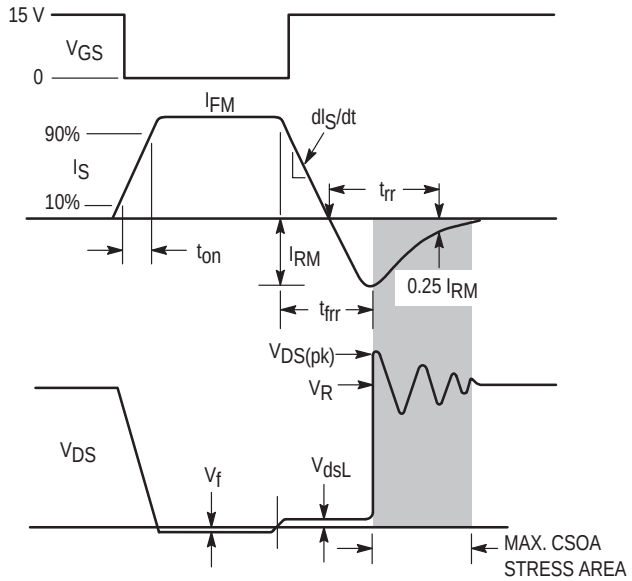


Figure 11. Commutating Waveforms

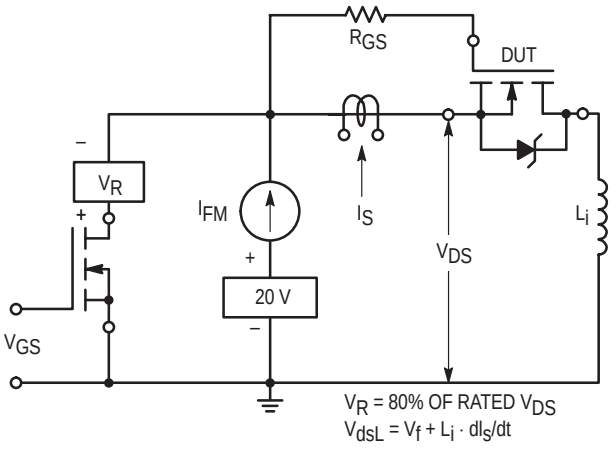


Figure 13. Commutating Safe Operating Area Test Circuit

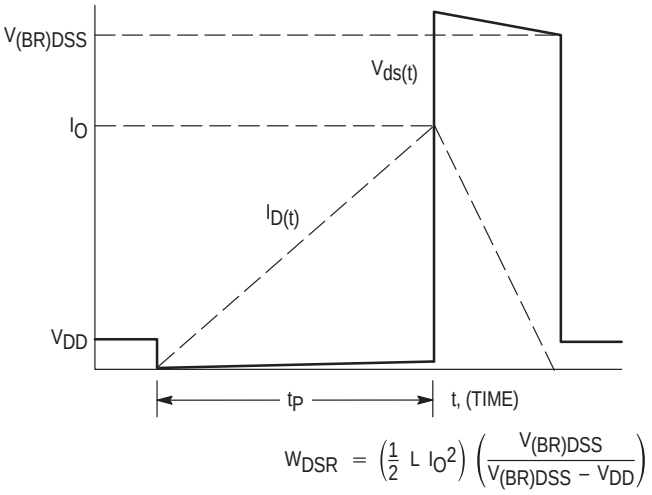


Figure 15. Unclamped Inductive Switching Waveforms

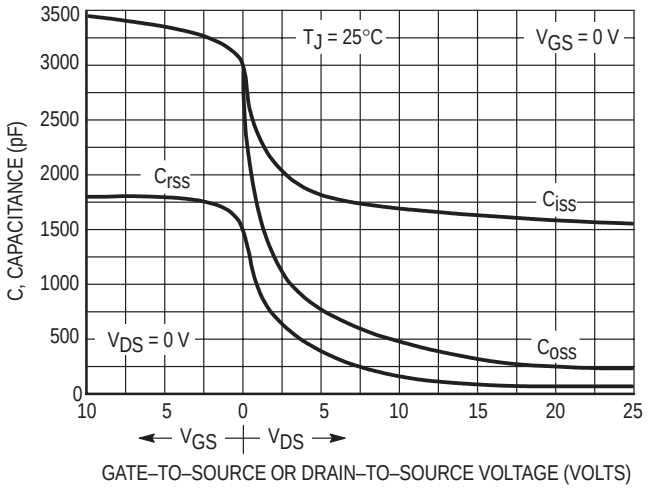


Figure 16. Capacitance Variation

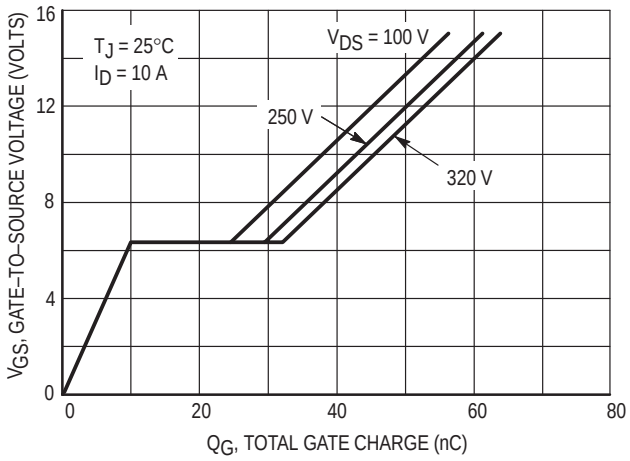
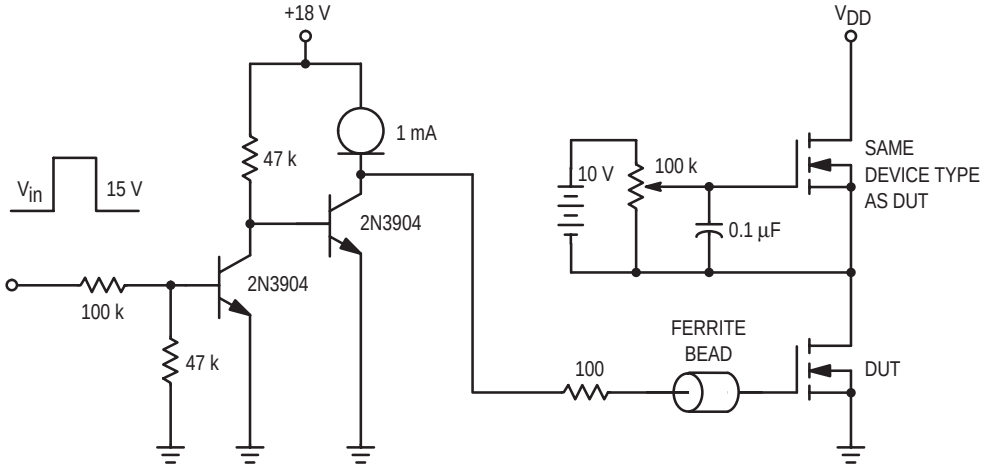


Figure 17. Gate Charge versus Gate–To–Source Voltage



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 µs, DUTY CYCLE ≤ 10%

Figure 18. Gate Charge Test Circuit

Designer's™ Data Sheet
TMOS E-FET ™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

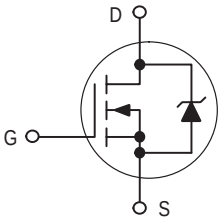
MTP12N10E

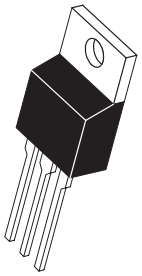
Motorola Preferred Device

TMOS POWER FET
12 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.16 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Designed to Eliminate the Need for External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	100	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–Source Voltage — Continuous — Single Pulse ($t_p \le 50$ μs)	V_{GS}	±20 ±40	Vdc
Drain Current — Continuous — Single Pulse ($t_p \le 10$ μs)	I_D I_{DM}	12 30	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	79 0.53	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS ($T_J \le 175$°C)

Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 V, V_{GS} = 10 V, L = 4.03 mH, R_G = 25 Ω, Peak I_L = 12 A) (See Figures 15, 16 and 17)	E_{AS}	290	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.9 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μAdc)		$V_{(BR)DSS}$	100	—	—	Vdc
Temperature Coefficient (positive)			—	110	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 V, V_{GS} = 0)		I_{DSS}	—	—	10	μA
(V_{DS} = 100 V, V_{GS} = 0, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Gate–Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (negative)			—	6.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	—	0.125	0.16	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 12 Adc)		$V_{DS(on)}$	—	1.5	2.4	Vdc
(I_D = 6.0 Adc, T_J = 150°C)			—	1.4	1.92	
Forward Transconductance (V_{DS} ≥ 15 V, I_D = 6.0 A)		g_{FS}	4.0	5.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz) See Figure 14	C_{iss}	—	600	—	pF
Reverse Transfer Capacitance		C_{rss}	—	70	—	
Output Capacitance		C_{oss}	—	230	—	
SWITCHING CHARACTERISTICS (T_J = 100°C)						
Turn–On Delay Time	(V_{DD} = 50 V, I_D = 12 A, V_{GS} = 10 V, R_G = 12 Ω) See Figure 7	$t_{d(on)}$	—	10	—	ns
Rise Time		t_r	—	64	—	
Turn–Off Delay Time		$t_{d(off)}$	—	21	—	
Fall Time		t_f	—	30	—	
Gate Charge	(V_{DS} = 80 V, I_D = 12 A, V_{GS} = 10 Vdc) See Figures 5 and 6	Q_T	—	18	26	nC
		Q_1	—	4.0	—	
		Q_2	—	10	—	
		Q_3	—	8.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS*						
Forward On–Voltage	(I_S = 12 A, V_{GS} = 0)	V_{SD}	—	1.0	2.5	Vdc
	(I_S = 12 A, V_{GS} = 0, T_J = 150°C)		—	0.83	—	
Reverse Recovery Time	(I_S = 12 A, V_{GS} = 0, dI_S/dt = 100 A/μs, V_R = 50 V)	t_{rr}	—	110	—	ns
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on tab to center of die)		L_d	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

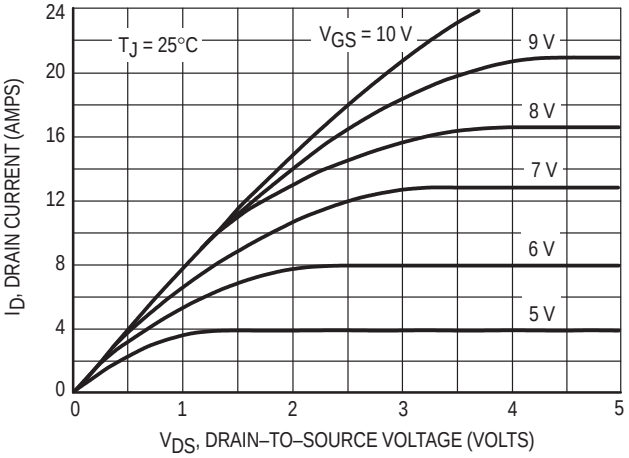


Figure 1. On–Region Characteristics

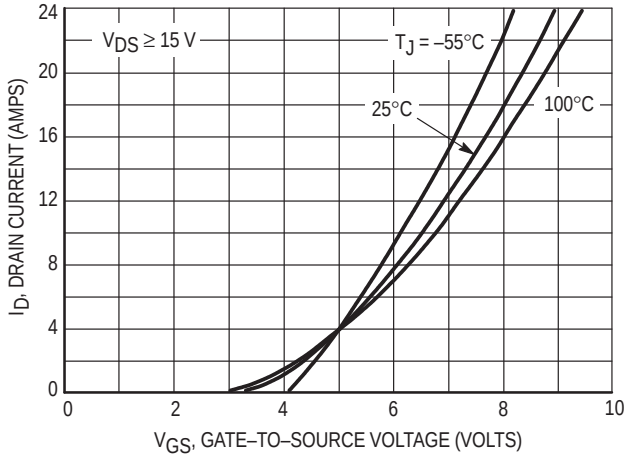


Figure 2. Transfer Characteristics

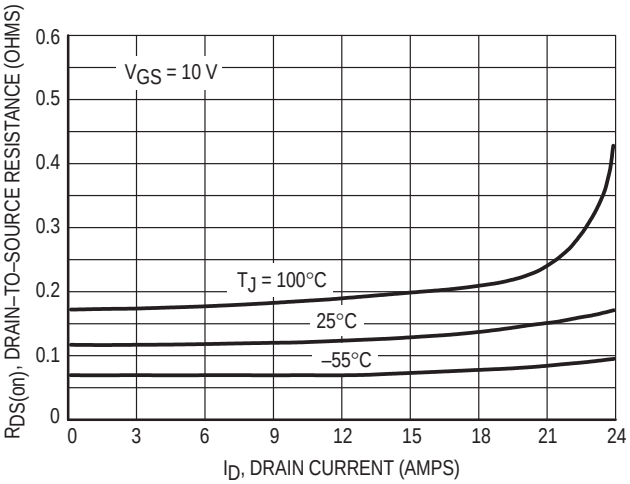


Figure 3. On–Resistance versus Drain Current

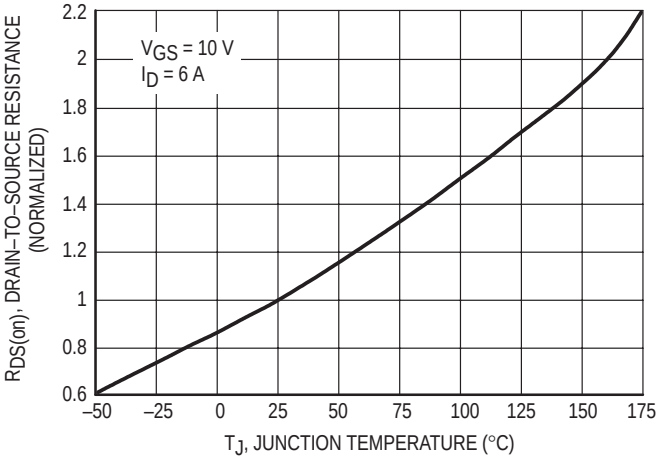


Figure 4. On–Resistance Variation with Temperature

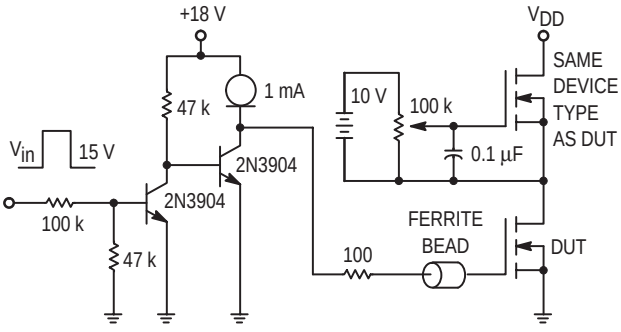


Figure 5. Gate Charge Test Circuit

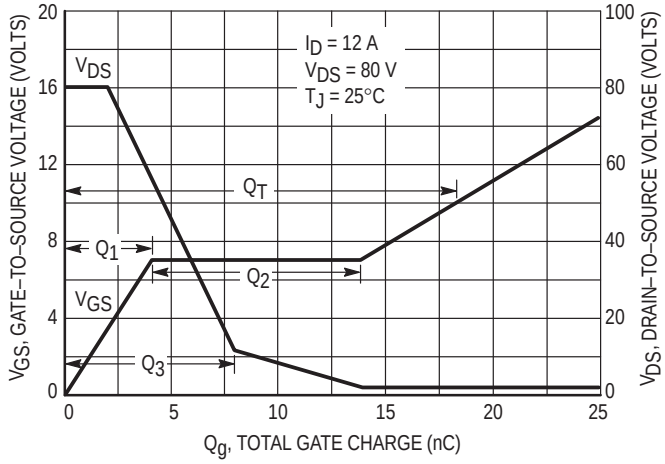


Figure 6. Gate–To–Source and Drain–To–Source Voltage versus Gate Charge

SAFE OPERATING AREA INFORMATION

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 175°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, BV_{DSS}. The switching SOA shown in Figure 9 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

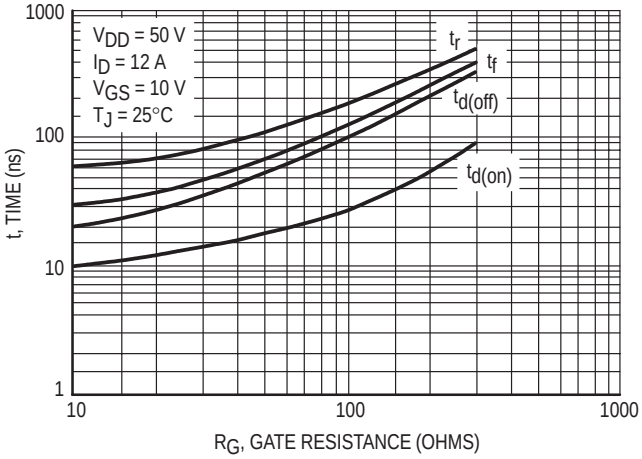


Figure 7. Resistive Switching Time versus Gate Resistance

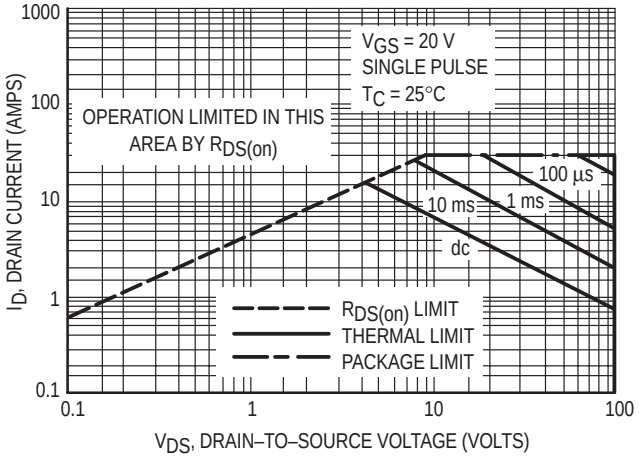


Figure 8. Maximum Rated Forward Biased Safe Operating Area

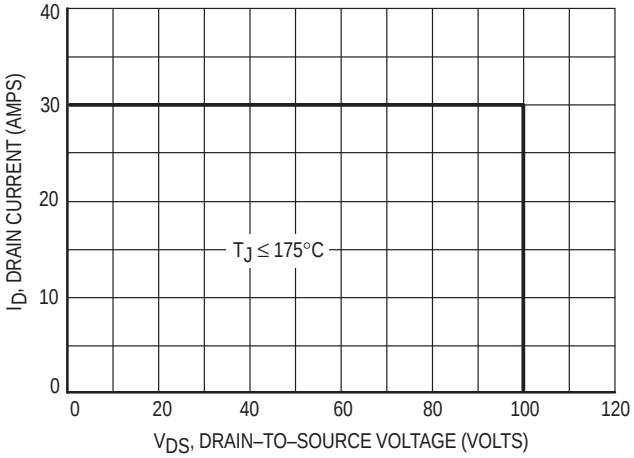


Figure 9. Maximum Rated Switching Safe Operating Area

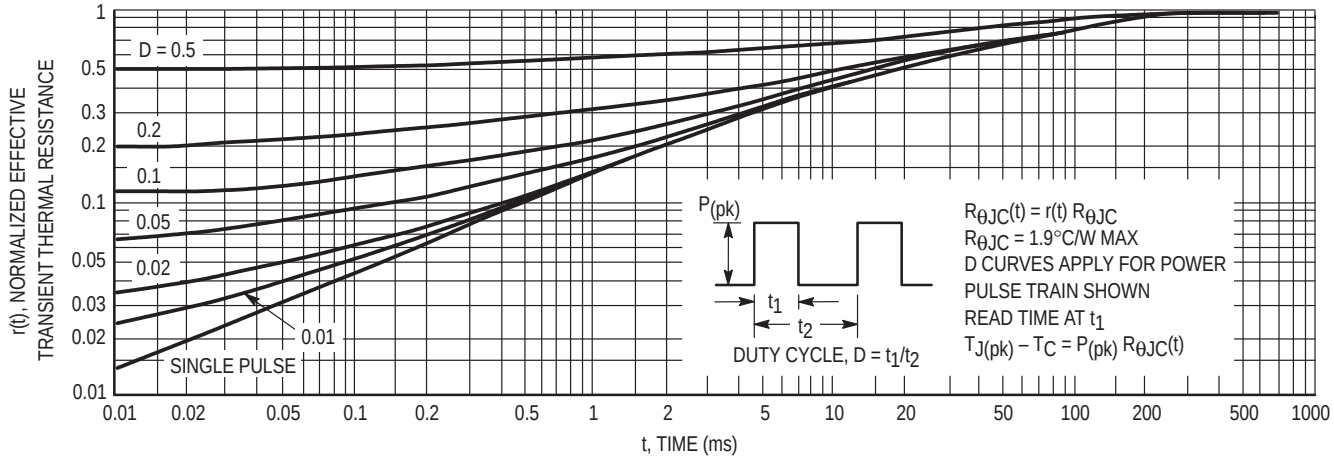


Figure 10. Thermal Response

COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so dI_S/dt is specified with a maximum value. Higher values of dI_S/dt require an appropriate derating of I_{FM}, peak V_{DS} or both. Ultimately dI_S/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at rated BV_{DSS} to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums.

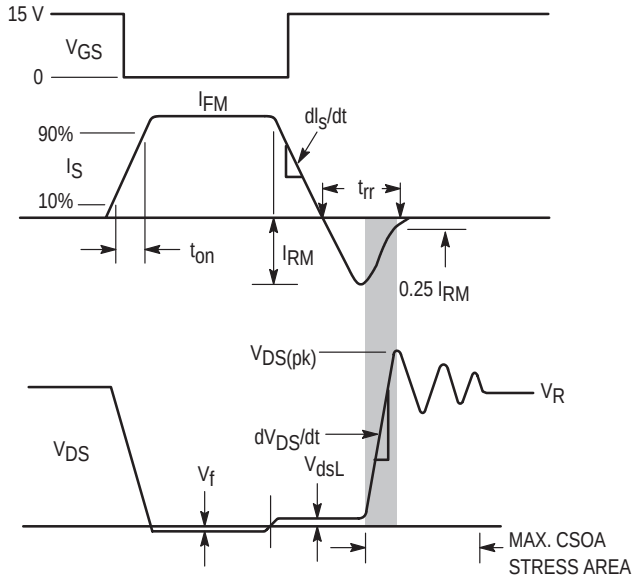


Figure 11. Commutating Waveforms

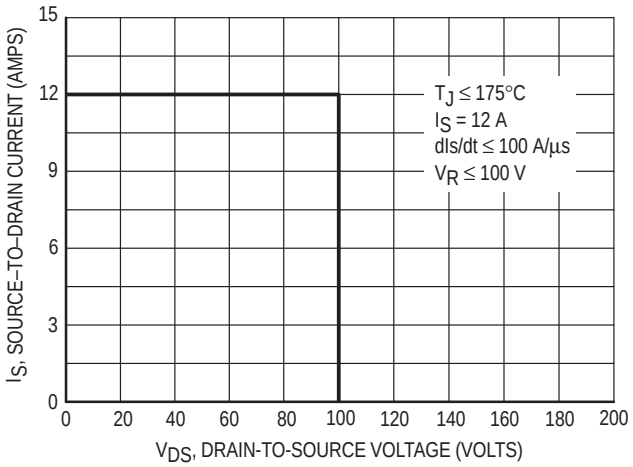


Figure 12. Commutating Safe Operating Area (CSOA)

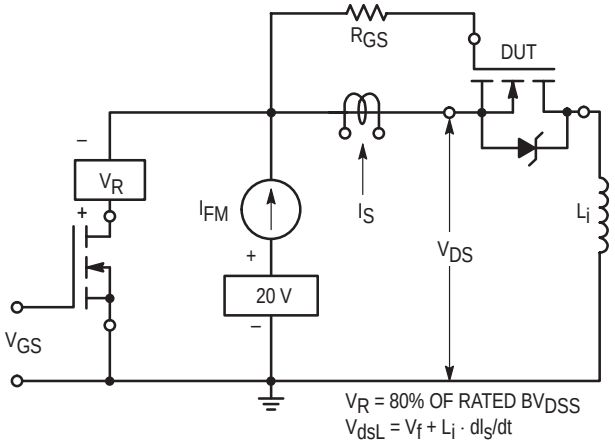


Figure 13. Commutating Safe Operating Area Test Circuit

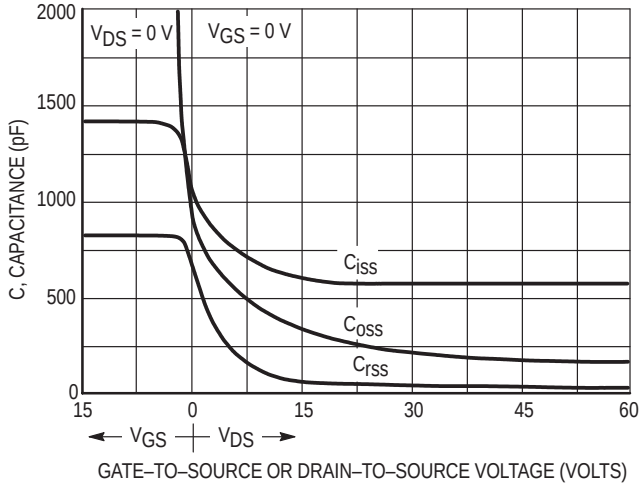


Figure 14. Capacitance Variation

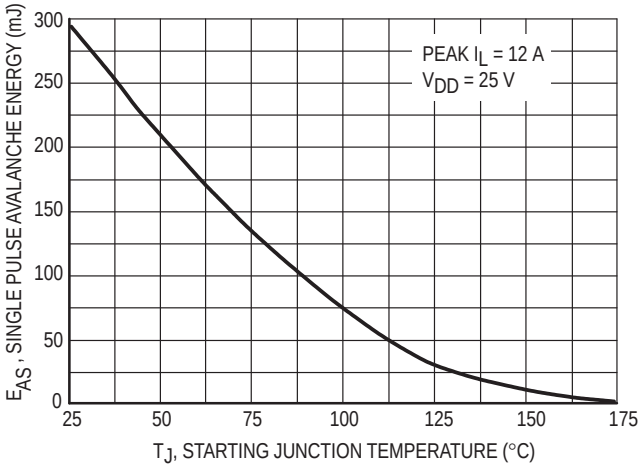


Figure 15. Maximum Avalanche Energy versus Starting Junction Temperature

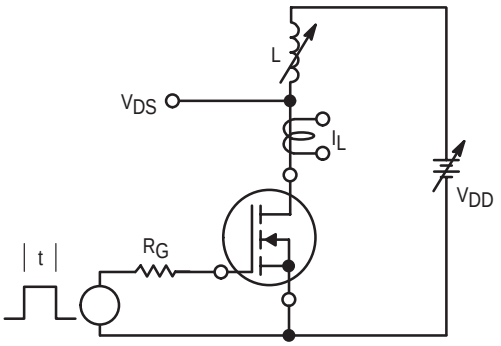


Figure 16. Unclamped Inductive Switching Test Circuit

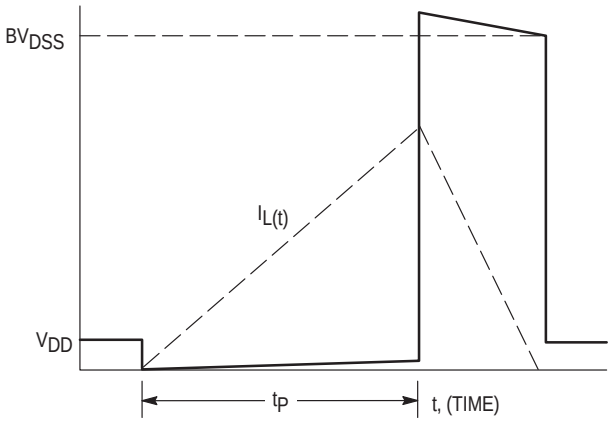


Figure 17. Unclamped Inductive Switching Waveforms

Designer's™ Data Sheet

Power Field Effect Transistor

P–Channel Enhancement–Mode Silicon Gate

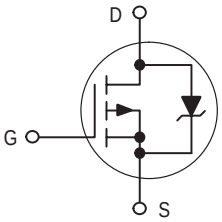
MTP12P10

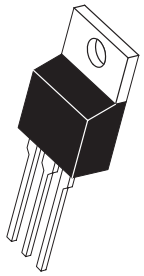
This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source–to–Drain Diode Characterized for Use With Inductive Loads

TMOS®

TMOS POWER FET
12 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.3 OHM





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	100	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–Source Voltage — Continuous — Non–repetitive ($t_p \leq 50$ μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	12 28	Adc
Total Power Dissipation Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 10 100	μAdc
Gate–Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate–Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA) T_J = 100°C		$V_{GS(th)}$	2.0 1.5	4.5 4.0	Vdc
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	—	0.3	Ohm
Drain–Source On–Voltage (V_{GS} = 10 V) (I_D = 12 Adc) (I_D = 6.0 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 4.2 3.8	Vdc
Forward Transconductance (V_{DS} = 15 V, I_D = 6.0 A)		g_{FS}	2.0	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz) See Figure 10	C_{iss}	—	920	pF
Output Capacitance		C_{oss}	—	575	
Reverse Transfer Capacitance		C_{rss}	—	200	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn–On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_G = 50 Ω) See Figures 12 and 13	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	150	
Turn–Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	150	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 11	Q_g	33 (Typ)	50	nC
Gate–Source Charge		Q_{gs}	16 (Typ)	—	
Gate–Drain Charge		Q_{gd}	17 (Typ)	—	
SOURCE–DRAIN DIODE CHARACTERISTICS*					
Forward On–Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	4.0 (Typ)	5.5	Vdc
Forward Turn–On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns
INTERNAL PACKAGE INDUCTANCE (TO–204)					
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die)		L_d	5.0 (Typ)	—	nH
Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad)		L_s	12.5 (Typ)	—	
INTERNAL PACKAGE INDUCTANCE (TO–220)					
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_d	 3.5 (Typ) 4.5 (Typ)	 — —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_s	7.5 (Typ)	—	

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

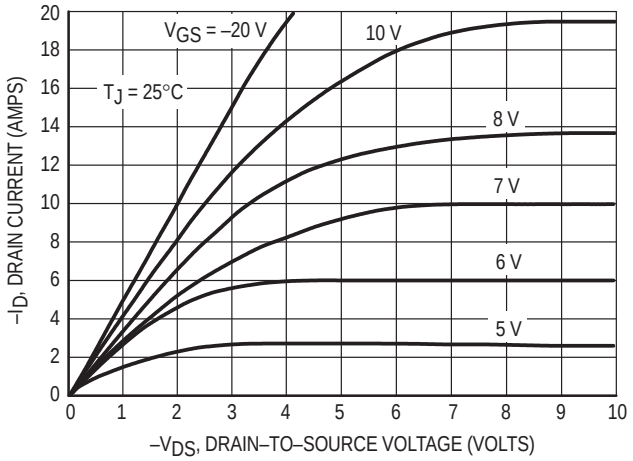


Figure 1. On–Region Characteristics

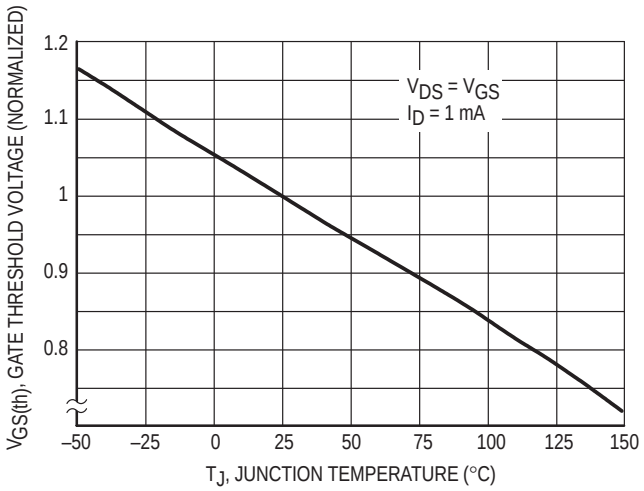


Figure 2. Gate–Threshold Voltage Variation With Temperature

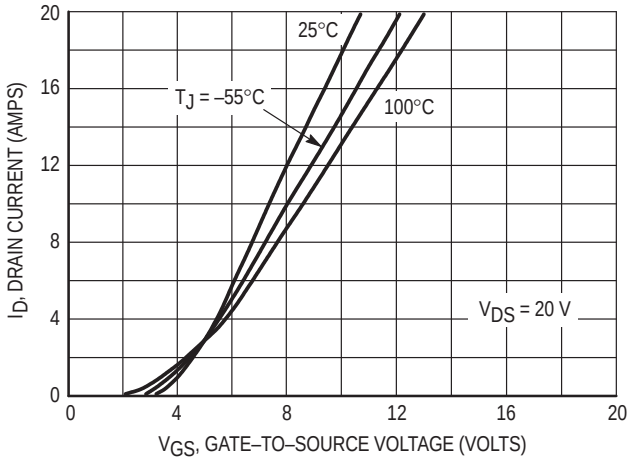


Figure 3. Transfer Characteristics

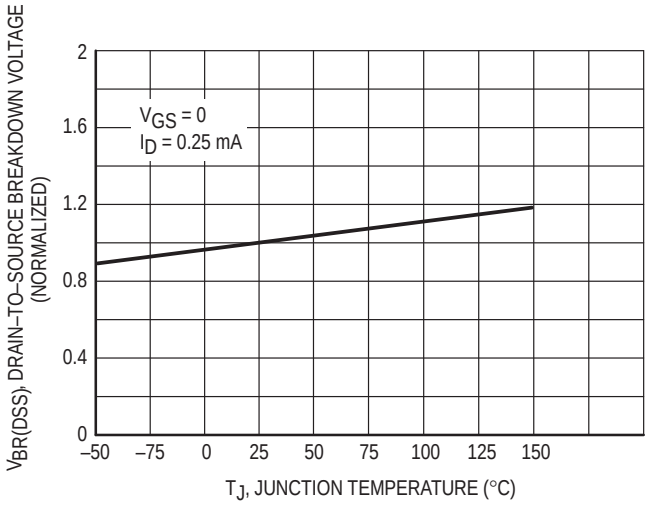


Figure 4. Normalized Breakdown Voltage versus Temperature

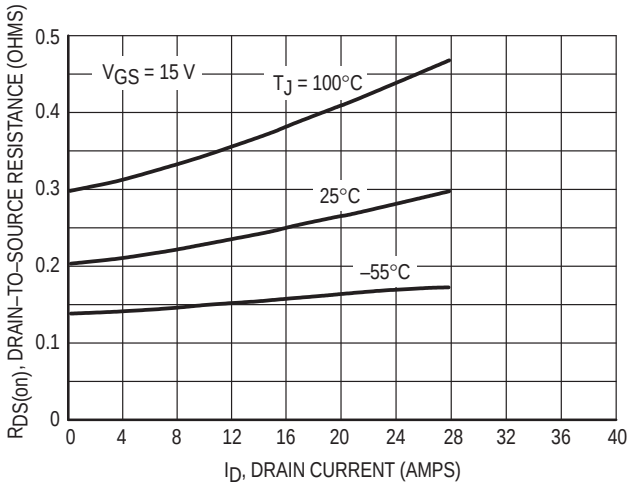


Figure 5. On–Resistance versus Drain Current

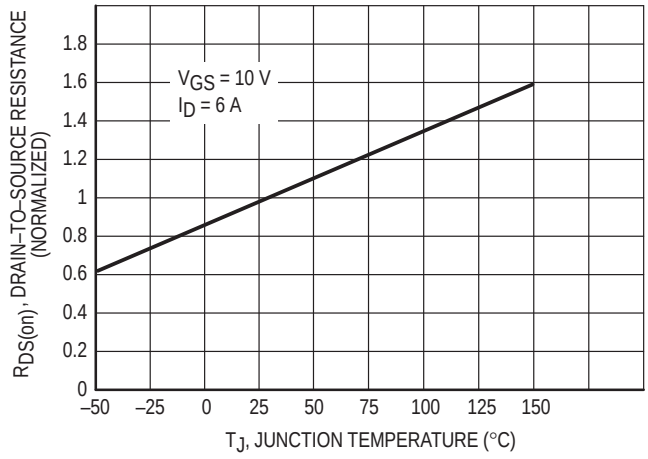


Figure 6. On–Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

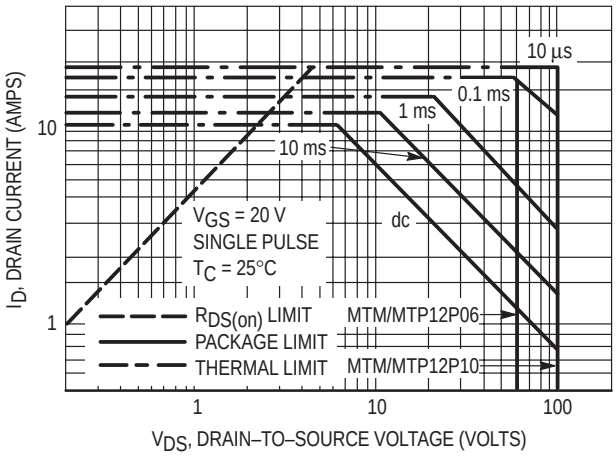


Figure 7. Maximum Rated Forward Biased Safe Operating Area

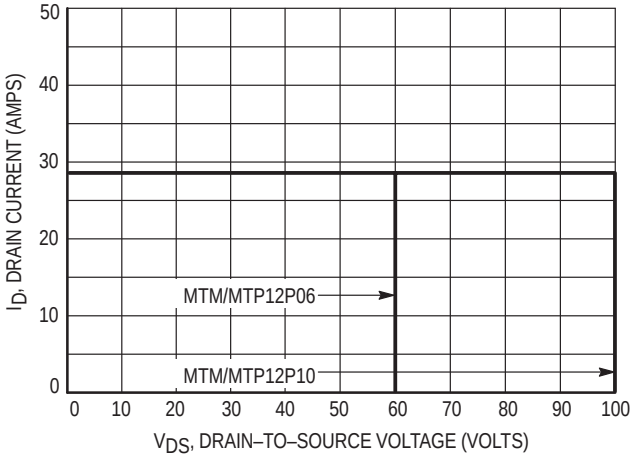


Figure 8. Maximum Rated Switching Safe Operating Area

FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

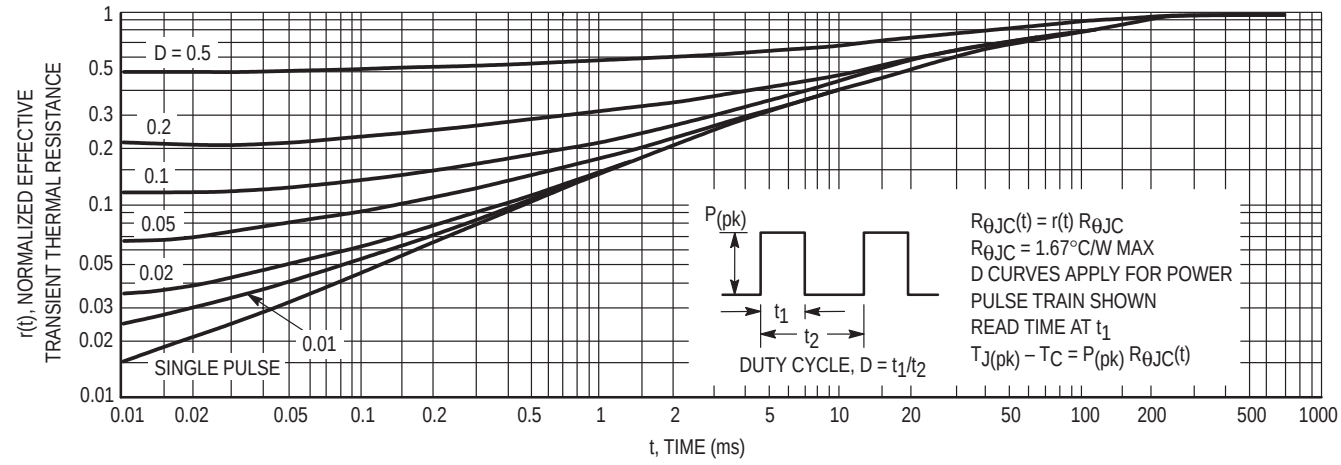


Figure 9. Thermal Response

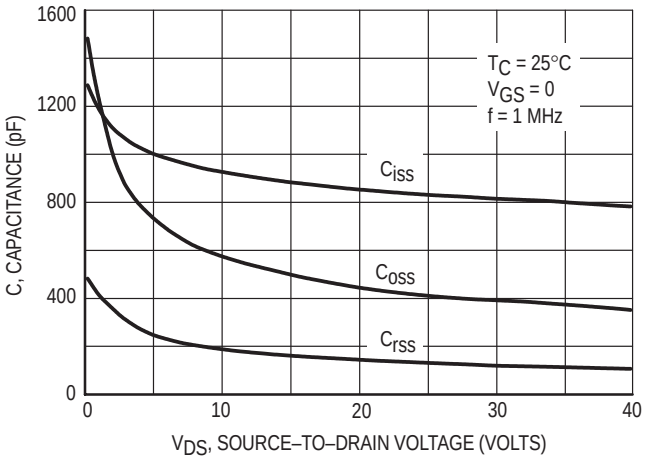


Figure 10. Capacitance Variation

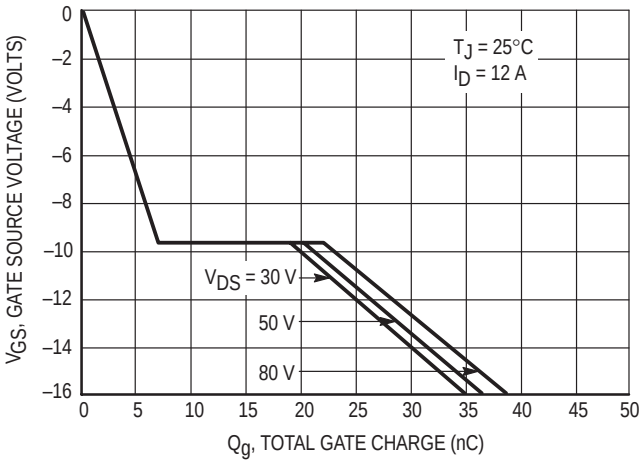


Figure 11. Gate Charge versus Gate–To–Source Voltage

RESISTIVE SWITCHING

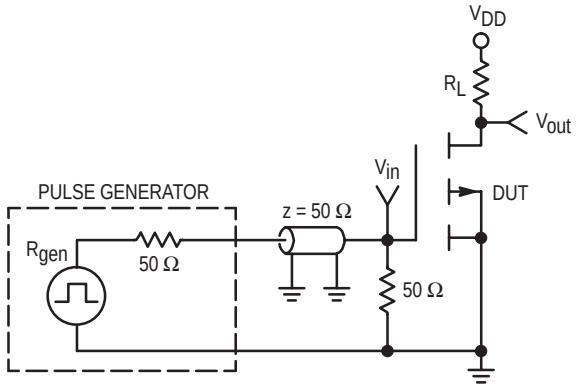


Figure 12. Switching Test Circuit

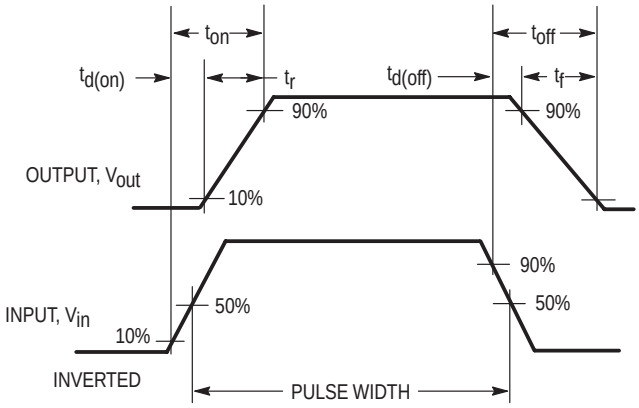


Figure 13. Switching Waveforms

Designer's™ Data Sheet

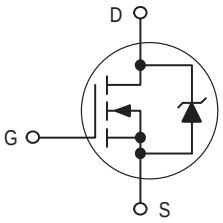
TMOS V
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

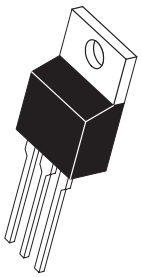
MTP15N06V

Motorola Preferred Device

TMOS POWER FET
15 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.12 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 221A–06, Style 5
TO–220AB

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Single Pulse ($t_p \le 50$ μs)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	15 8.7 45	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C	P_D	55 0.5	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 15 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	113	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.73 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	60 —	— 67	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	2.7 5.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 7.5 Adc)		$R_{DS(on)}$	—	0.08	0.12	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 15 Adc) (I_D = 7.5 Adc, T_J = 150°C)		$V_{DS(on)}$	— —	2.0 —	2.2 1.9	Vdc
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 7.5 Adc)		g_{FS}	4.0	6.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	469	660	pF
Output Capacitance		C_{oss}	—	148	200	
Reverse Transfer Capacitance		C_{rss}	—	35	60	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 15 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	7.6	20	ns
Rise Time		t_r	—	51	100	
Turn–Off Delay Time		$t_{d(off)}$	—	18	40	
Fall Time		t_f	—	33	70	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 15 Adc, V_{GS} = 10 Vdc)	Q_T	—	14.4	20	nC
		Q_1	—	2.8	—	
		Q_2	—	6.4	—	
		Q_3	—	6.1	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 15 Adc, V_{GS} = 0 Vdc) (I_S = 15 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	— —	1.05 1.5	1.6 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 15 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	59.3	—	ns
		t_a	—	46	—	
		t_b	—	13.3	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.165	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

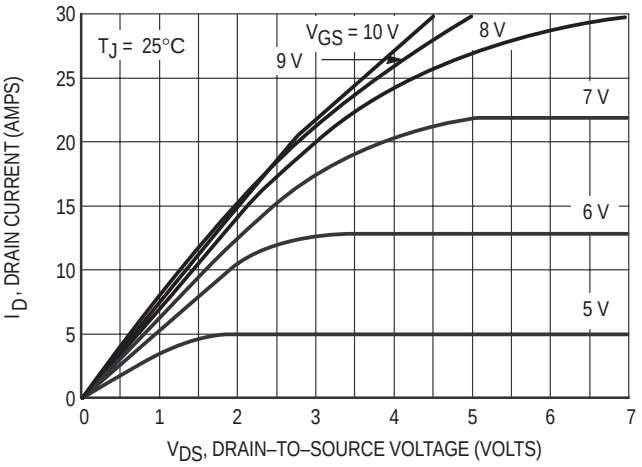


Figure 1. On–Region Characteristics

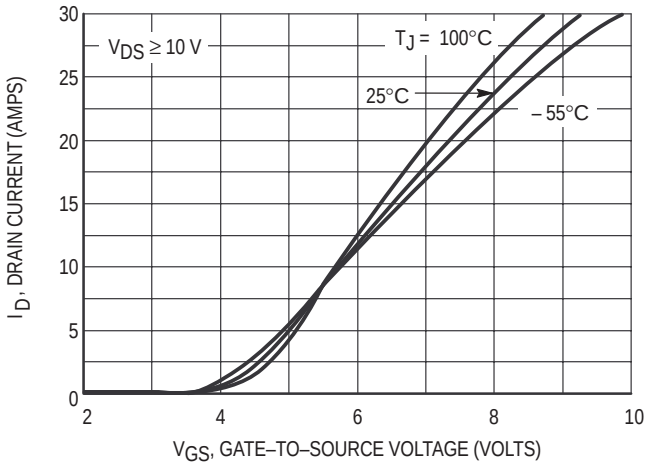


Figure 2. Transfer Characteristics

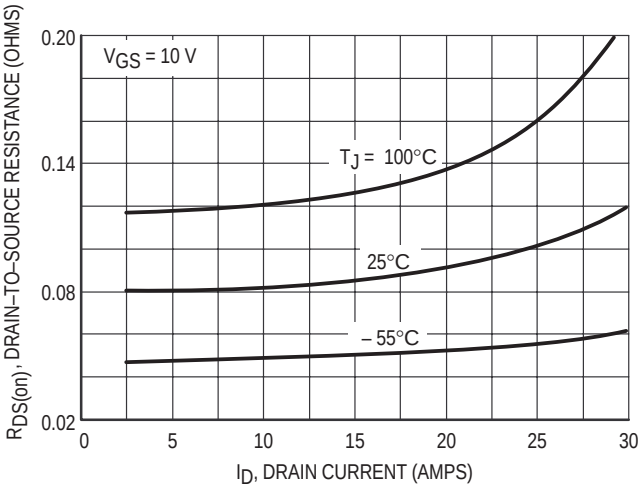


Figure 3. On–Resistance versus Drain Current and Temperature

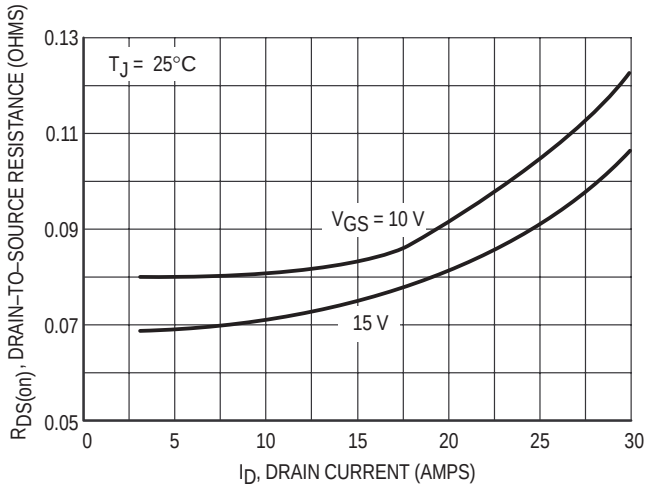


Figure 4. On–Resistance versus Drain Current and Gate Voltage

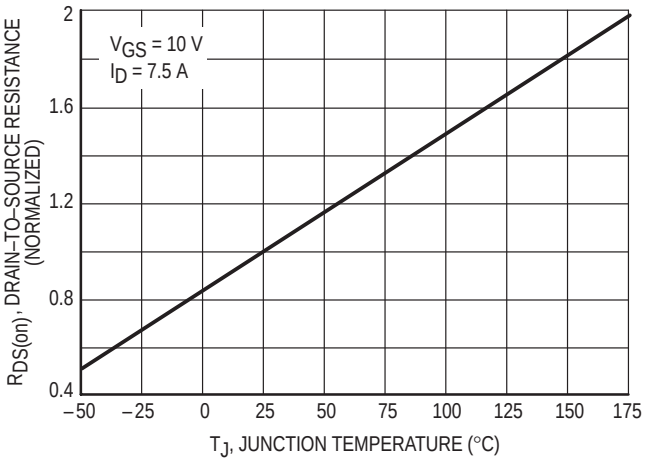


Figure 5. On–Resistance Variation with Temperature

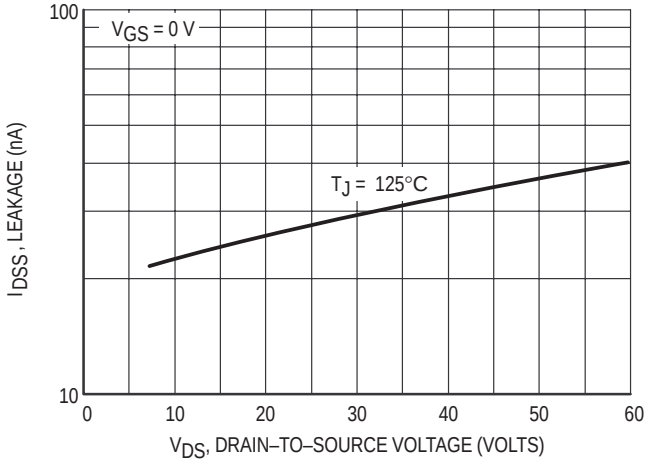


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

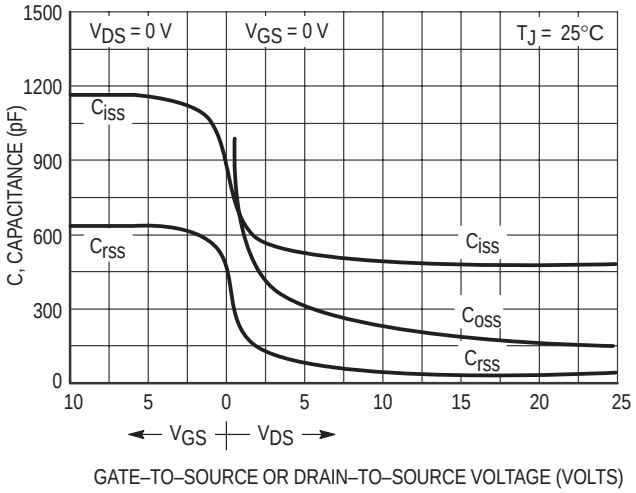


Figure 7. Capacitance Variation

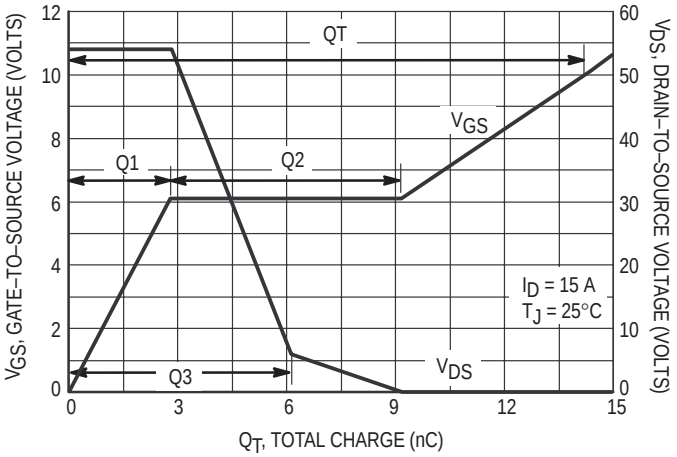


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

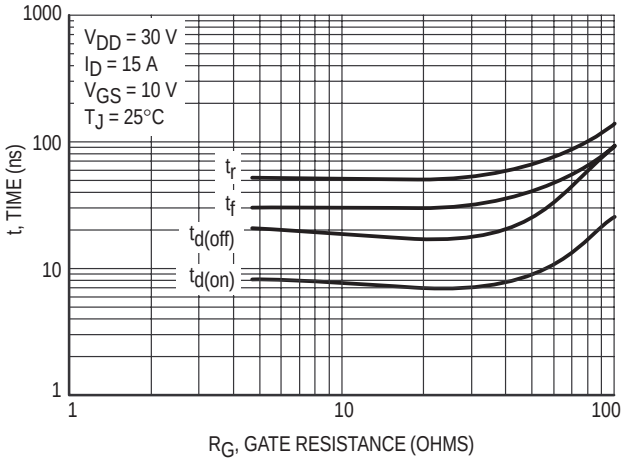


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

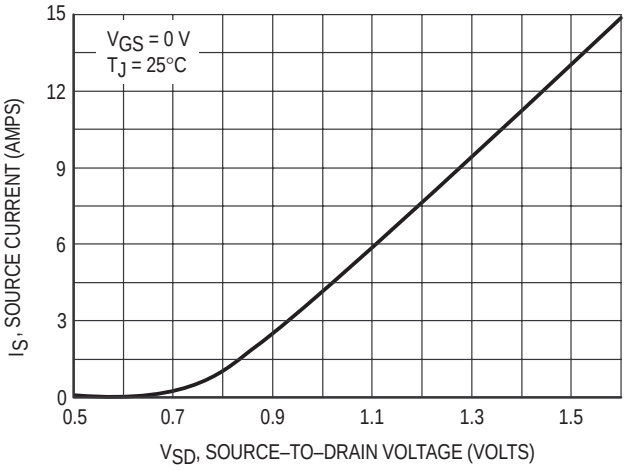


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

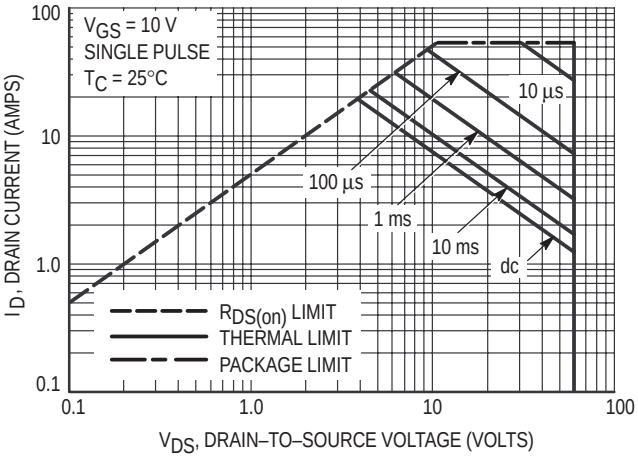


Figure 11. Maximum Rated Forward Biased Safe Operating Area

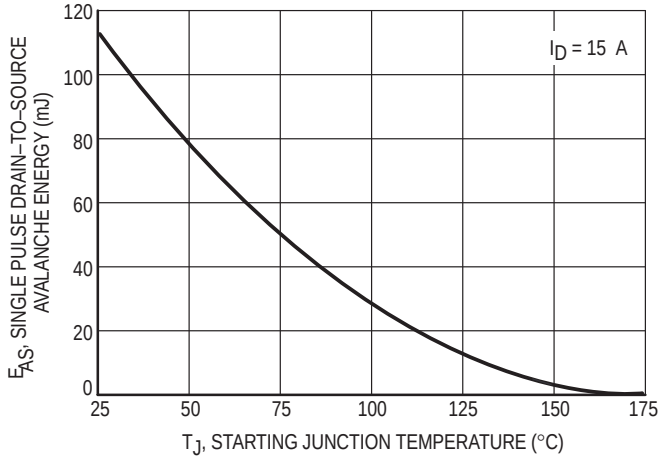


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

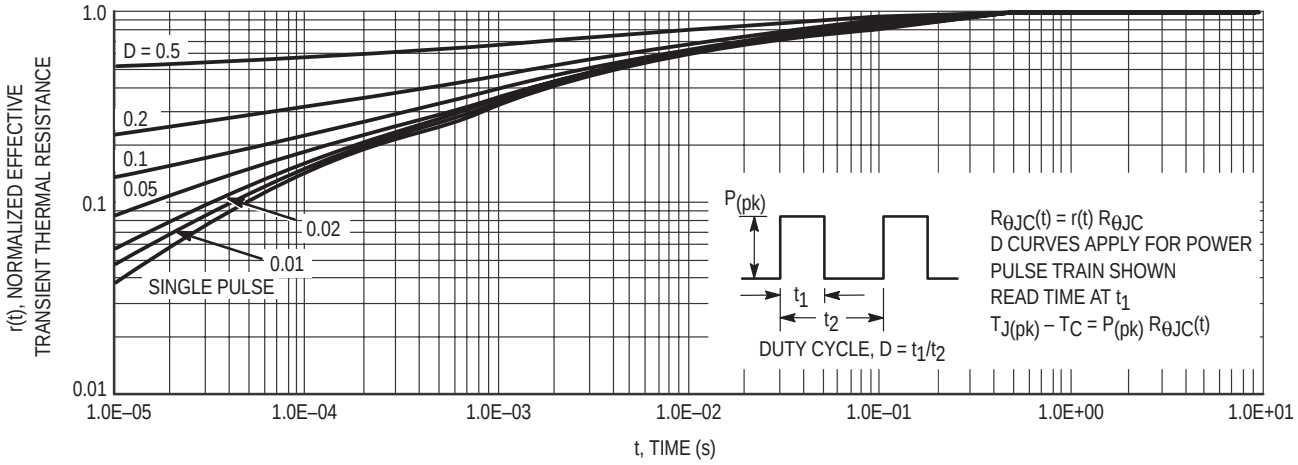


Figure 13. Thermal Response

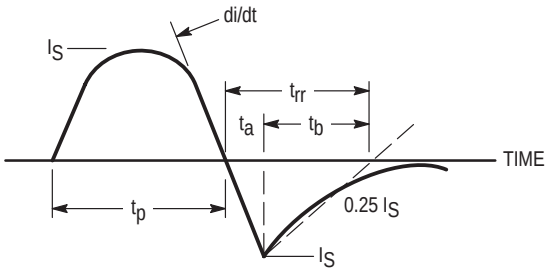


Figure 14. Diode Reverse Recovery Waveform

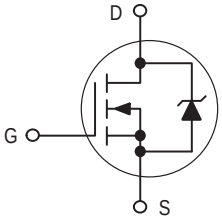
Product Preview

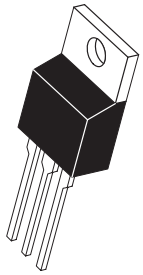
TMOS V™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

MTP15N06VL

TMOS POWER FET
15 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.085 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 221A–06, Style 5
TO–220AB

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 25	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	15 12 53	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	60 0.40	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 15 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	113	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			1.0	1.5	2.0	
Threshold Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 7.5 Adc)		$R_{DS(on)}$	—	0.075	0.085	Ohm
Drain–to–Source On–Voltage		$V_{DS(on)}$				Vdc
(V_{GS} = 5.0 Vdc, I_D = 15 Adc)			—	—	1.5	
(V_{GS} = 5.0 Vdc, I_D = 7.5 Adc, T_J = 150°C)			—	—	1.3	
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 7.5 Adc)		g_{FS}	8.0	10	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	630	880	pF
Output Capacitance		C_{oss}	—	270	380	
Reverse Transfer Capacitance		C_{rss}	—	56	110	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 15 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	26	50	ns
Rise Time		t_r	—	105	210	
Turn–Off Delay Time		$t_{d(off)}$	—	80	160	
Fall Time		t_f	—	70	140	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 15 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	12	20	nC
		Q_1	—	3.0	—	
		Q_2	—	8.0	—	
		Q_3	—	10	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 15 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.6	Vdc
	(I_S = 15 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.9	—	
Reverse Recovery Time	(I_S = 15 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	100	—	ns
		t_a	—	55	—	
		t_b	—	45	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.345	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die.)			—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance		L_S				nH
(Measured from the source lead 0.25″ from package to source bond pad)			—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

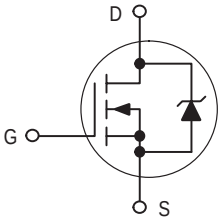
MTP16N25E

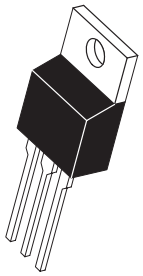
Motorola Preferred Device

TMOS POWER FET
16 AMPERES
250 VOLTS
$R_{DS(on)}$ = 0.25 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	250	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	250	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	16 10 56	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, I_L = 16 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	384	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	250	—	—	Vdc
Temperature Coefficient (Positive)			—	333	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 250 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 250 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 8.0 Adc)		$R_{DS(on)}$	—	0.17	0.25	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 16 Adc)		$V_{DS(on)}$	—	3.6	4.8	Vdc
(I_D = 8.0 Adc, T_J = 125°C)			—	—	4.2	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 8.0 Adc)		g_{FS}	3.0	7.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1558	2180	pF
Output Capacitance		C_{oss}	—	281	390	
Reverse Transfer Capacitance		C_{rss}	—	130	260	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 125 Vdc, I_D = 16 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	15	30	ns
Rise Time		t_r	—	64	130	
Turn–Off Delay Time		$t_{d(off)}$	—	56	110	
Fall Time		t_f	—	44	90	
Gate Charge (See Figure 8)	(V_{DS} = 200 Vdc, I_D = 16 Adc, V_{GS} = 10 Vdc)	Q_T	—	53.4	70	nC
		Q_1	—	9.3	—	
		Q_2	—	27.5	—	
		Q_3	—	17.1	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 16 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.915	1.5	Vdc
	(I_S = 16 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.39	—	
Reverse Recovery Time (See Figure 14)	(I_S = 16 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	234	—	ns
		t_a	—	170	—	
		t_b	—	64	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.165	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

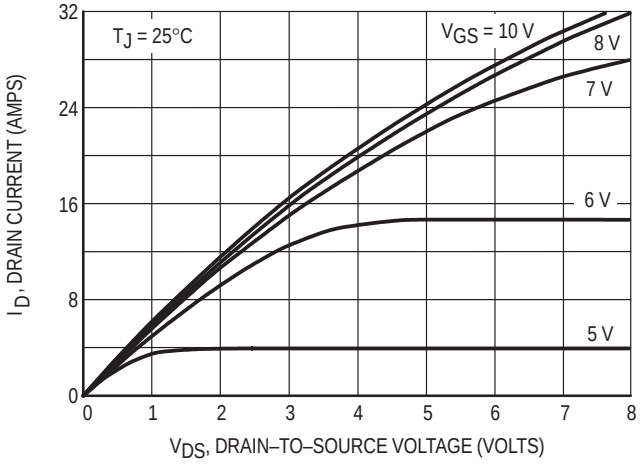


Figure 1. On–Region Characteristics

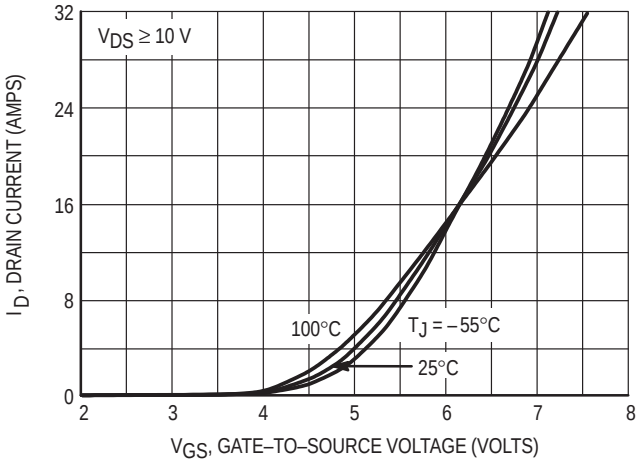


Figure 2. Transfer Characteristics

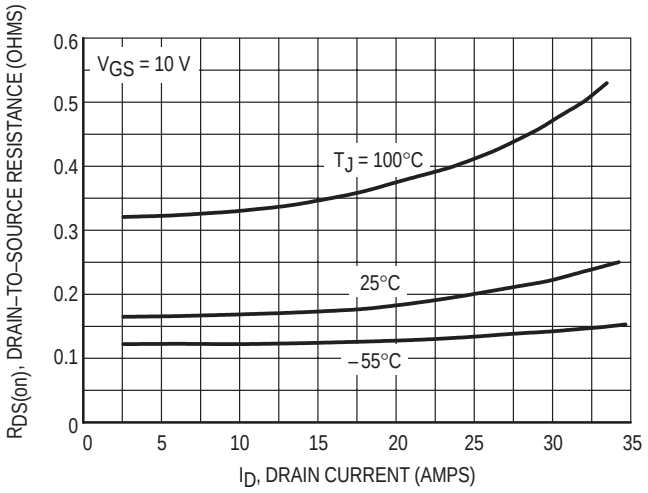


Figure 3. On–Resistance versus Drain Current and Temperature

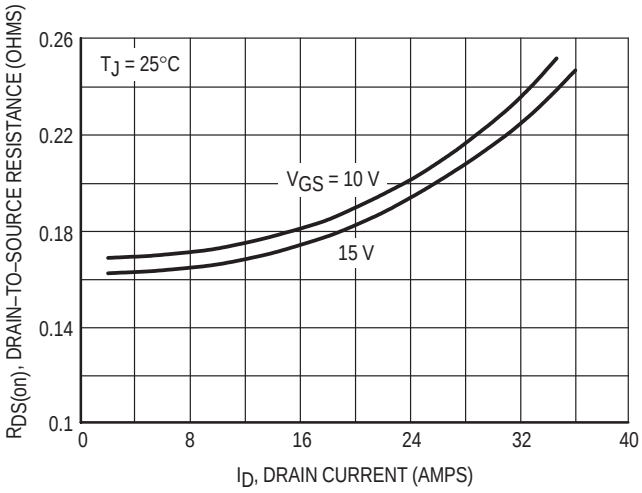


Figure 4. On–Resistance versus Drain Current and Gate Voltage

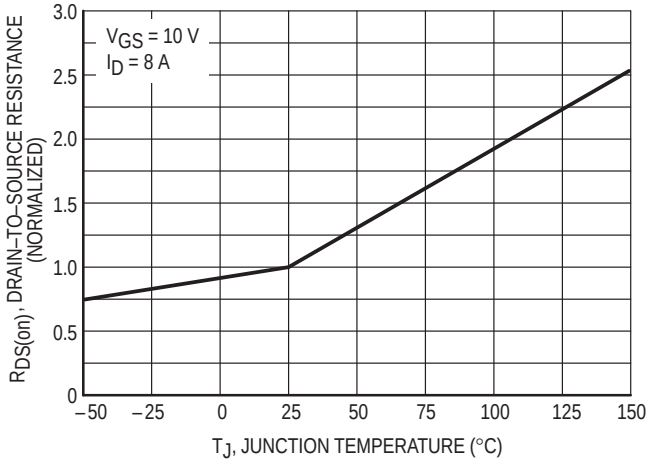


Figure 5. On–Resistance Variation with Temperature

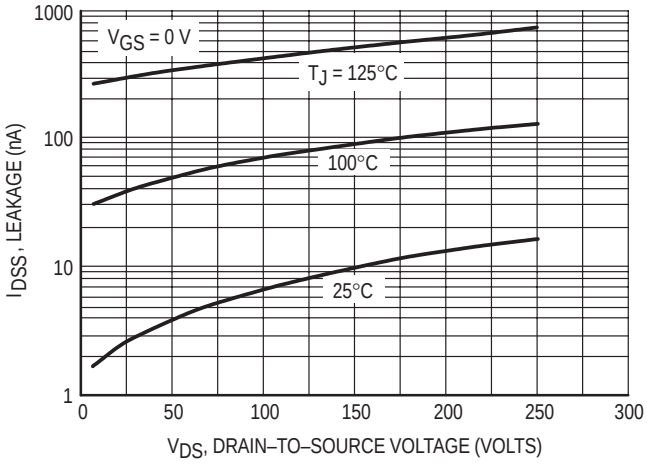


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

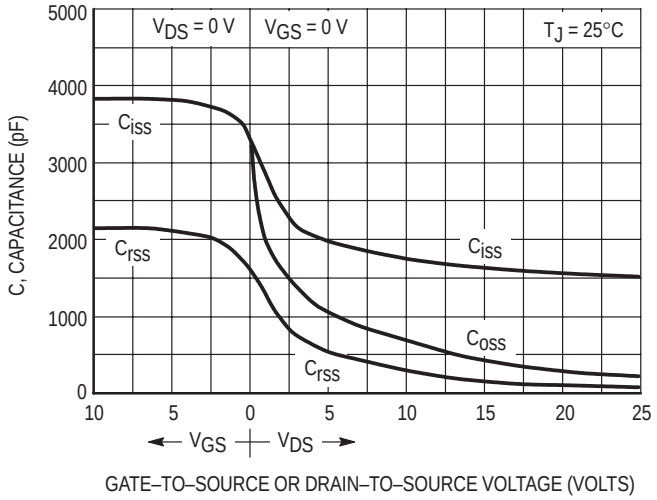


Figure 7. Capacitance Variation

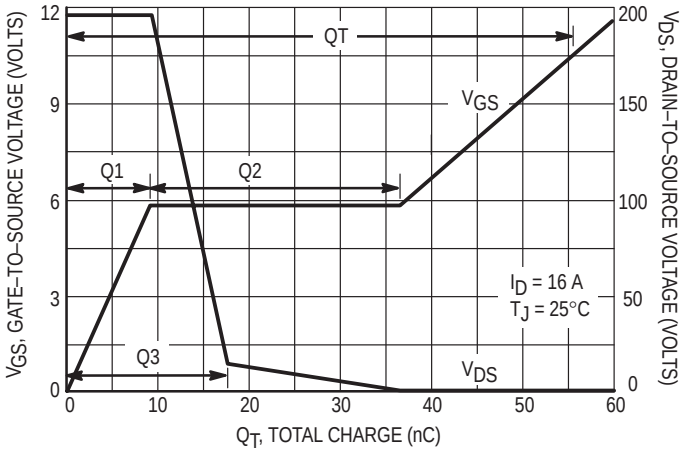


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

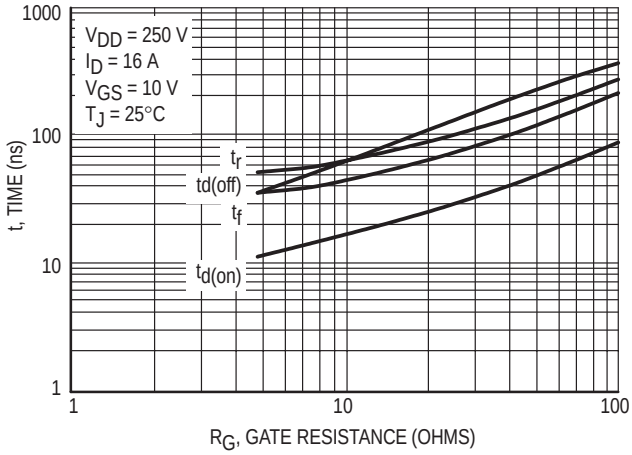


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

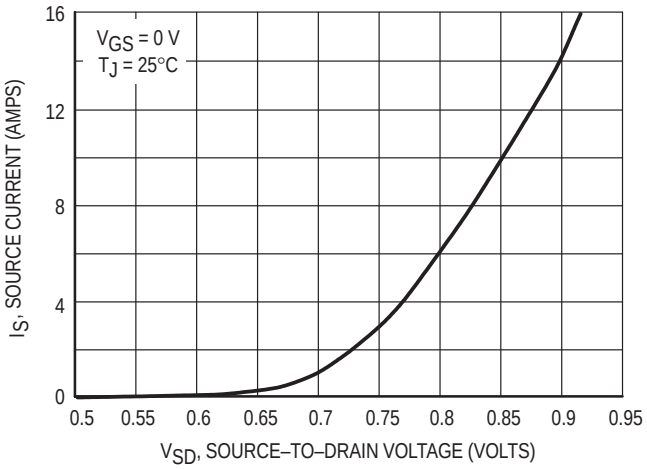


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

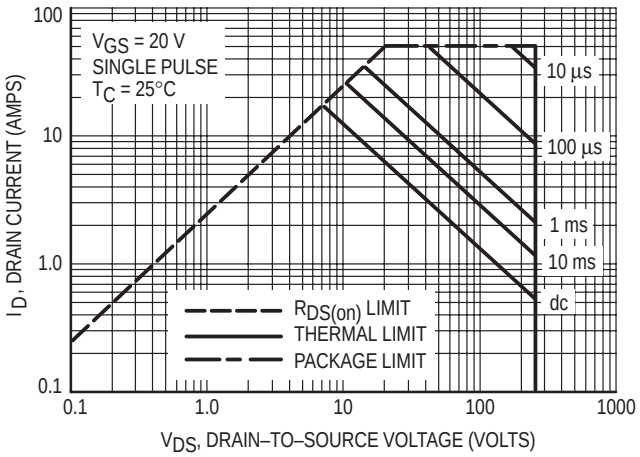


Figure 11. Maximum Rated Forward Biased Safe Operating Area

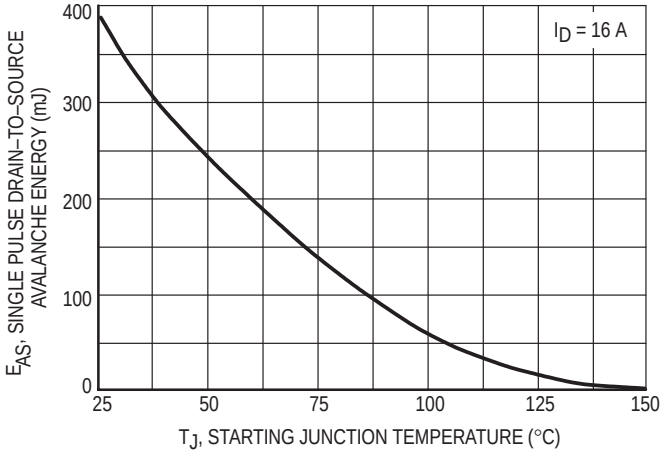


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

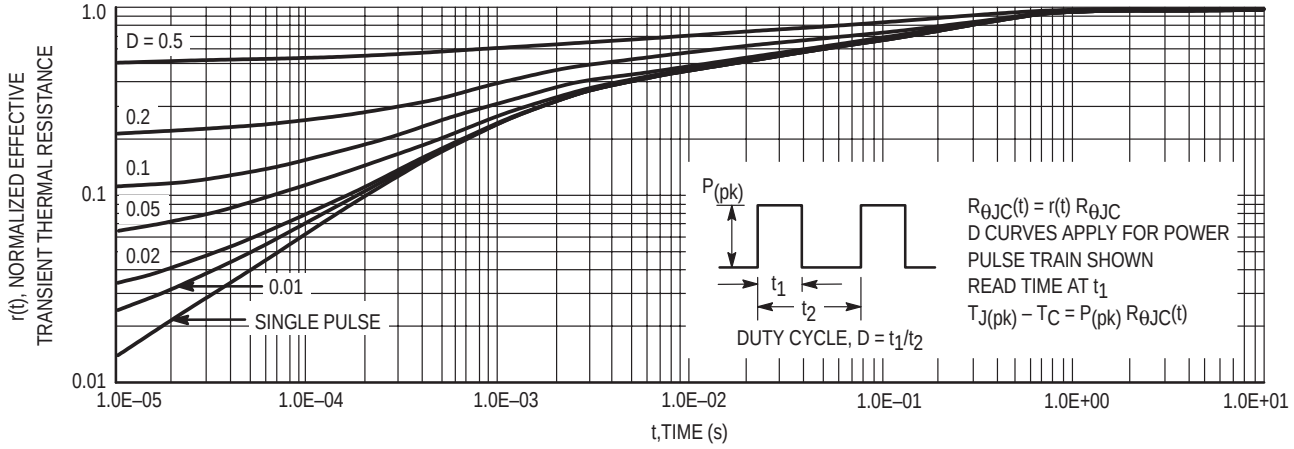


Figure 13. Thermal Response

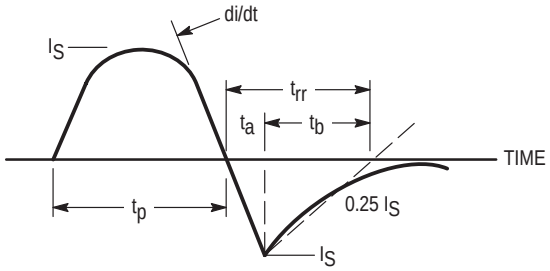


Figure 14. Diode Reverse Recovery Waveform

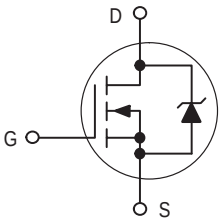
Product Preview

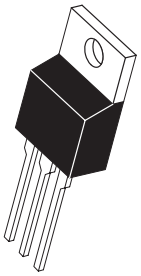
TMOS V™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

MTP20N06V

TMOS POWER FET
20 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.085 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 221A–06, Style 5
TO–220AB

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	20 13 70	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	60 0.40	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 20 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	200	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.8	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$R_{DS(on)}$	—	0.065	0.085	Ohm
Drain–to–Source On–Voltage		$V_{DS(on)}$				Vdc
(V_{GS} = 10 Vdc, I_D = 20 Adc)			—	—	2.0	
(V_{GS} = 10 Vdc, I_D = 10 Adc, T_J = 150°C)			—	—	1.9	
Forward Transconductance (V_{DS} = 6.0 Vdc, I_D = 10 Adc)		g_{FS}	6.0	8.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	590	830	pF
Output Capacitance		C_{oss}	—	180	250	
Reverse Transfer Capacitance		C_{rss}	—	40	80	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	8.7	20	ns
Rise Time		t_r	—	77	150	
Turn–Off Delay Time		$t_{d(off)}$	—	26	50	
Fall Time		t_f	—	46	90	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc)	Q_T	—	28	40	nC
		Q_1	—	4.0	—	
		Q_2	—	9.0	—	
		Q_3	—	8.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 20 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.6	Vdc
	(I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.96	—	
Reverse Recovery Time	(I_S = 20 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	60	—	ns
		t_a	—	52	—	
		t_b	—	8.0	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.172	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance		L_S				nH
(Measured from the source lead 0.25″ from package to source bond pad)			—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

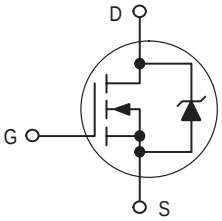
MTP20N20E

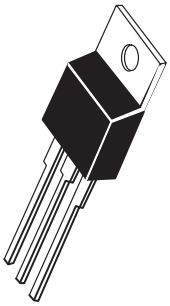
Motorola Preferred Device

TMOS POWER FET
20 AMPERES
200 VOLTS
$R_{DS(on)}$ = 0.16 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	200	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	20 12 60	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 20 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	600	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.00 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	200	—	—	Vdc
Temperature Coefficient (Positive)			—	263	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 200 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			2.0	—	4.0	
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$R_{DS(on)}$	—	0.12	0.16	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 20 Adc)			—	—	3.84	
(I_D = 10 Adc, T_J = 125°C)			—	—	3.36	
Forward Transconductance (V_{DS} = 13 Vdc, I_D = 10 Adc)		g_{FS}	8.0	11	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1880	2700	pF
Output Capacitance		C_{oss}	—	378	535	
Reverse Transfer Capacitance		C_{rss}	—	68	100	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 100 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	17	40	ns
Rise Time		t_r	—	86	180	
Turn–Off Delay Time		$t_{d(off)}$	—	50	100	
Fall Time		t_f	—	60	120	
Gate Charge (See Figure 8)	(V_{DS} = 160 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc)	Q_T	—	54	75	nC
		Q_1	—	12	—	
		Q_2	—	24	—	
		Q_3	—	22	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 20 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.35	Vdc
	(I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.82	—	
Reverse Recovery Time (See Figure 14)	(I_S = 20 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	239	—	ns
		t_a	—	136	—	
		t_b	—	103	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.09	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

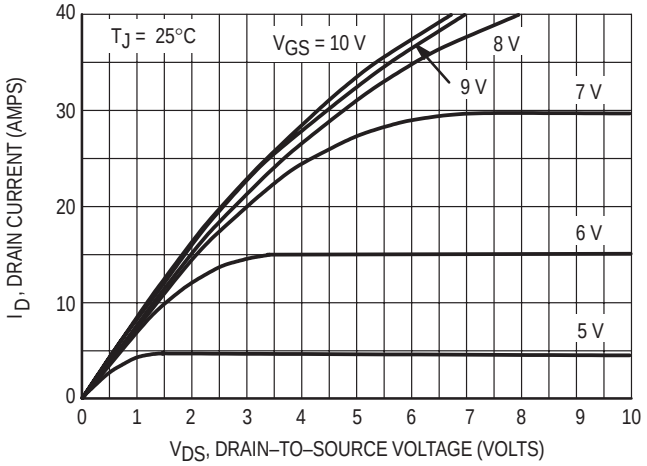


Figure 1. On–Region Characteristics

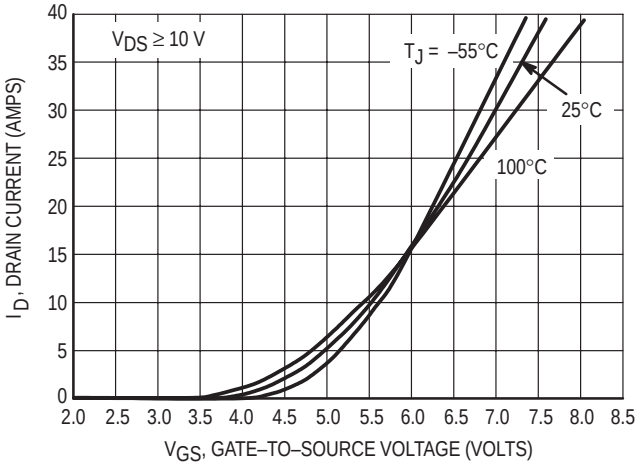


Figure 2. Transfer Characteristics

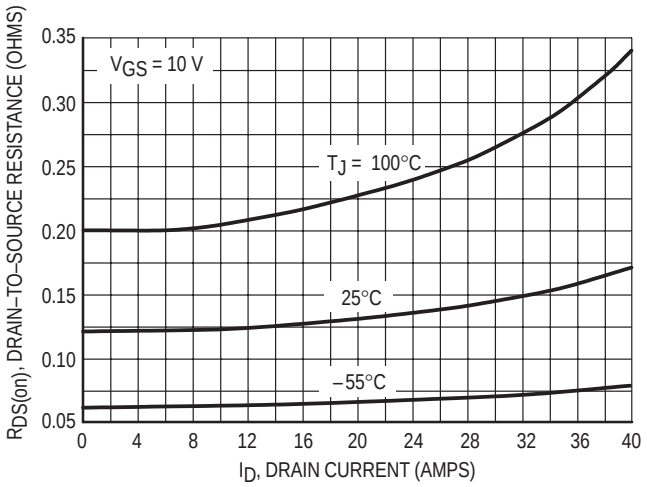


Figure 3. On–Resistance versus Drain Current and Temperature

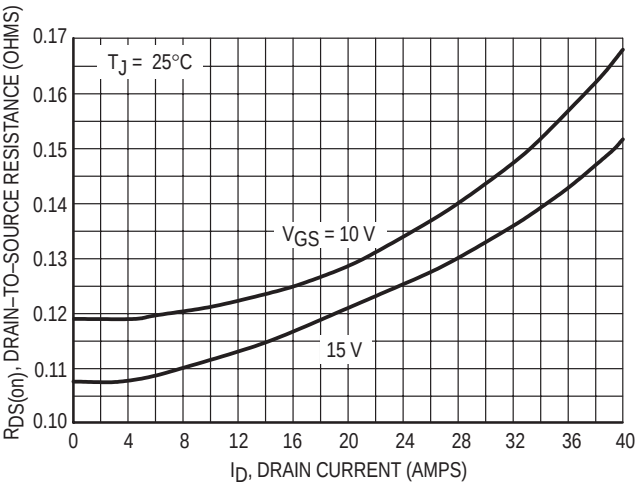


Figure 4. On–Resistance versus Drain Current and Gate Voltage

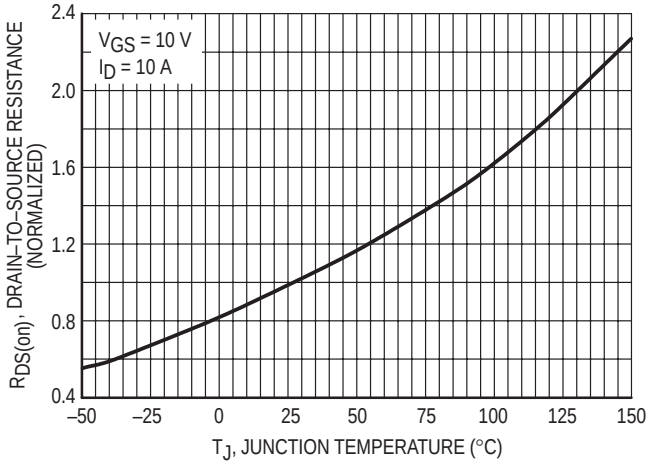


Figure 5. On–Resistance Variation with Temperature

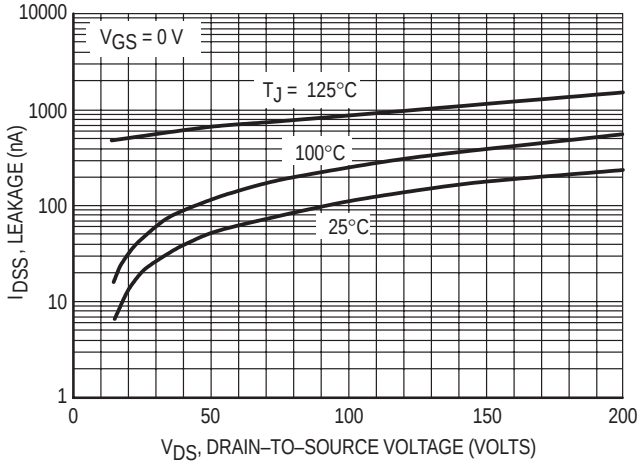


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

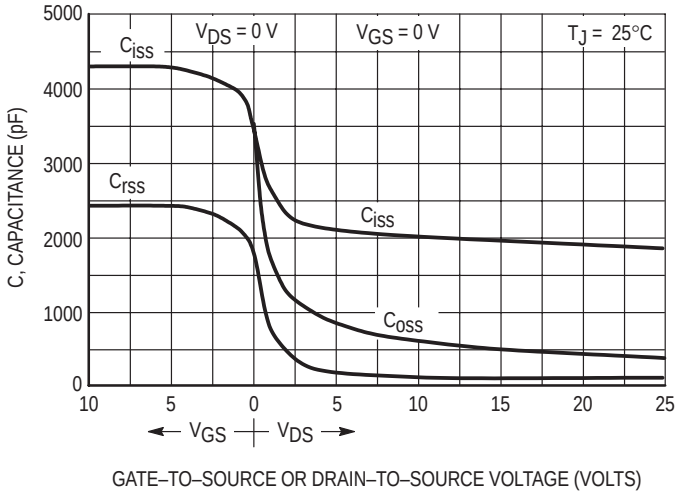


Figure 7. Capacitance Variation

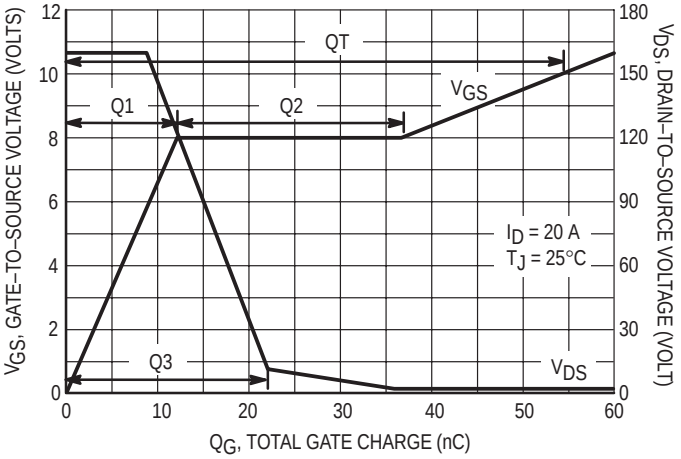


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

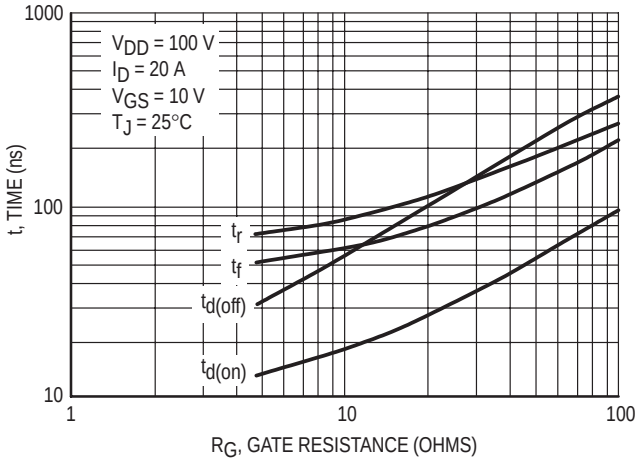


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

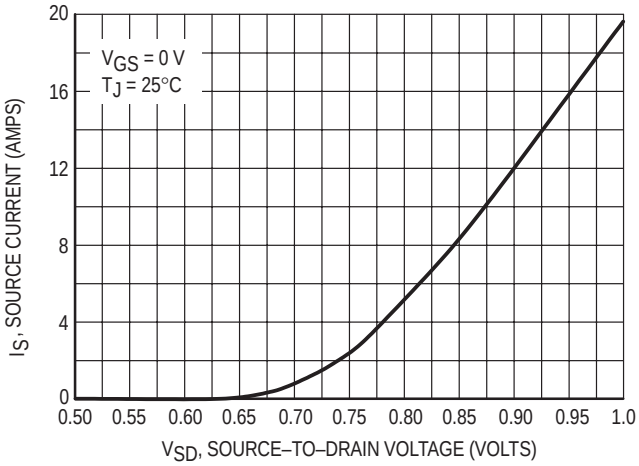


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

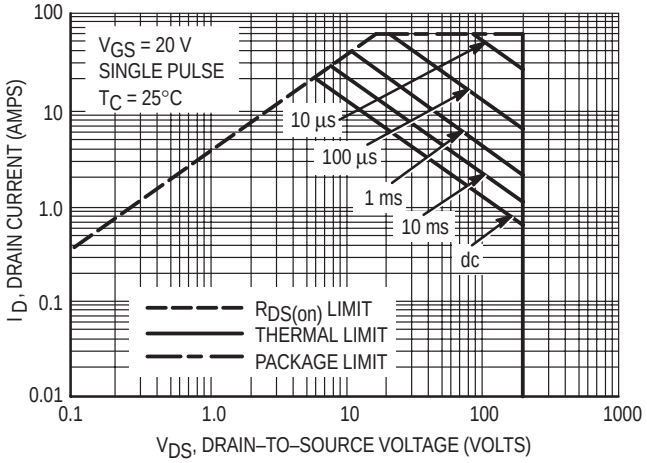


Figure 11. Maximum Rated Forward Biased Safe Operating Area

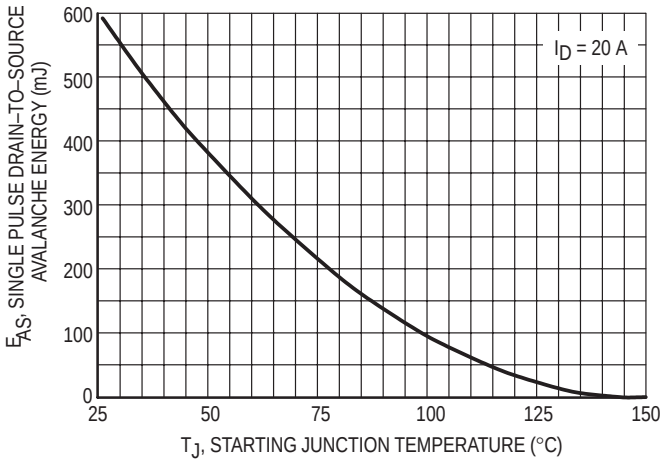


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

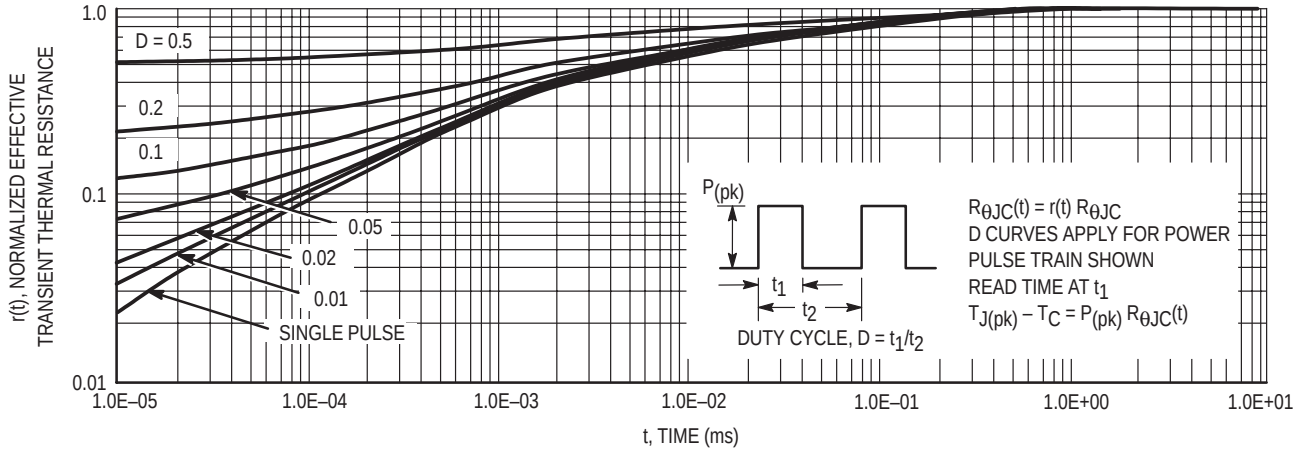


Figure 13. Thermal Response

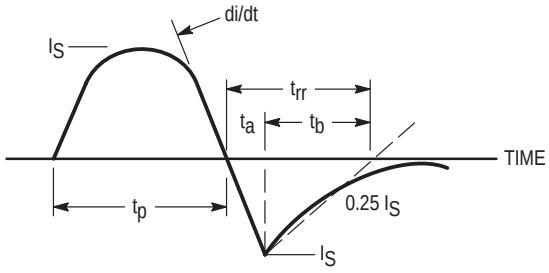


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

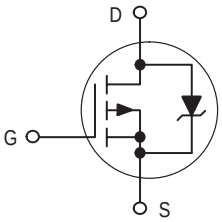
TMOS V™
Power Field Effect Transistor
P–Channel Enhancement–Mode Silicon Gate

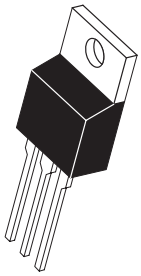
MTP23P06V

Motorola Preferred Device

TMOS POWER FET
23 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.120 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 221A–06, Style 5
TO–220AB

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	23 15 81	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C	P_D	90 0.60	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, PEAK I_L = 23 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	794	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	60.5	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.8	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	5.3	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 11.5 Adc)		$R_{DS(on)}$	—	0.093	0.12	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 23 Adc)		$V_{DS(on)}$	—	—	3.3	Vdc
(V_{GS} = 10 Vdc, I_D = 11.5 Adc, T_J = 150°C)			—	—	3.2	
Forward Transconductance (V_{DS} = 10.9 Vdc, I_D = 11.5 Adc)		g_{FS}	5.0	11.5	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1160	1620	pF
Output Capacitance		C_{oss}	—	380	530	
Transfer Capacitance		C_{rss}	—	105	210	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 23 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	13.8	30	ns
Rise Time		t_r	—	98.3	200	
Turn–Off Delay Time		$t_{d(off)}$	—	41	80	
Fall Time		t_f	—	62	120	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 23 Adc, V_{GS} = 10 Vdc)	Q_T	—	38	50	nC
		Q_1	—	7.0	—	
		Q_2	—	18	—	
		Q_3	—	14	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 23 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	2.2	3.5	Vdc
	(I_S = 23 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	1.8	—	
Reverse Recovery Time	(I_S = 23 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	142.2	—	ns
		t_a	—	100.5	—	
		t_b	—	41.7	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.804	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)				4.5		
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

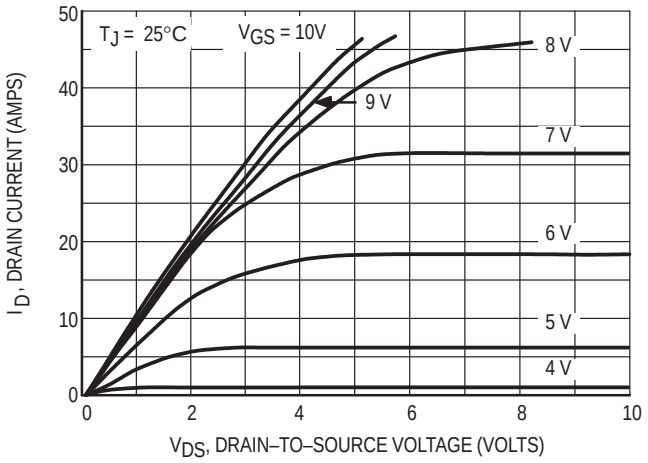


Figure 1. On–Region Characteristics

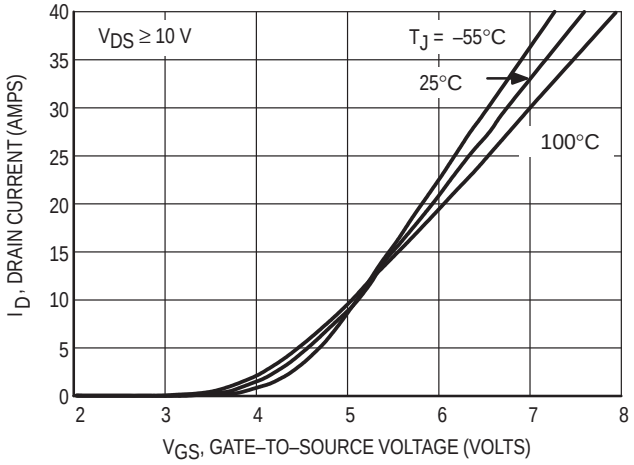


Figure 2. Transfer Characteristics

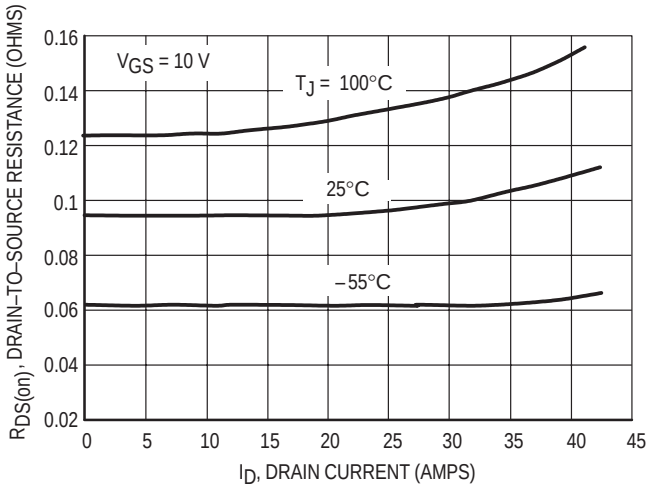


Figure 3. On–Resistance versus Drain Current and Temperature

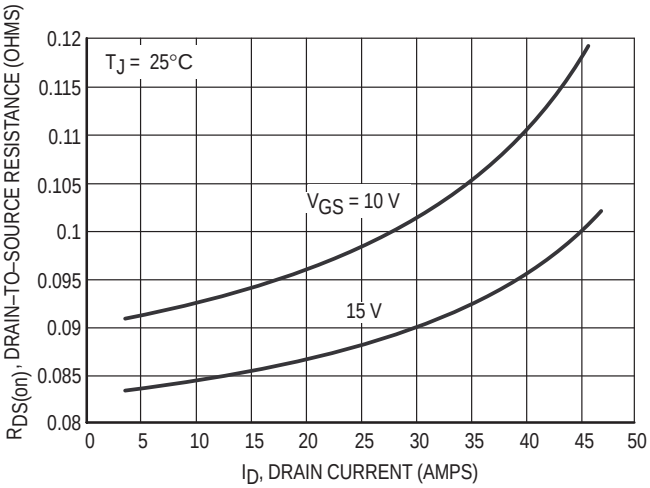


Figure 4. On–Resistance versus Drain Current and Gate Voltage

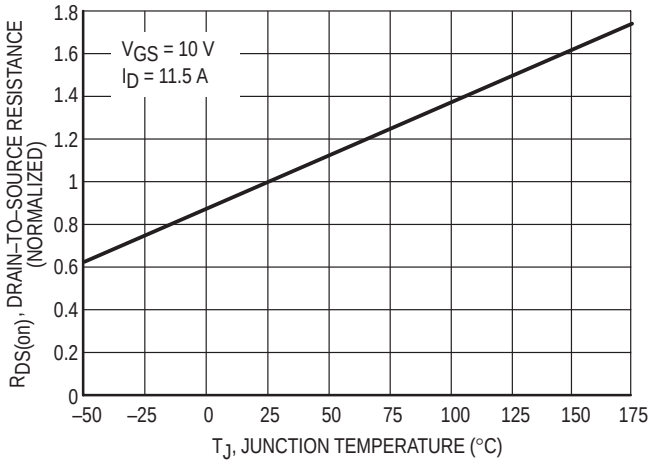


Figure 5. On–Resistance Variation with Temperature

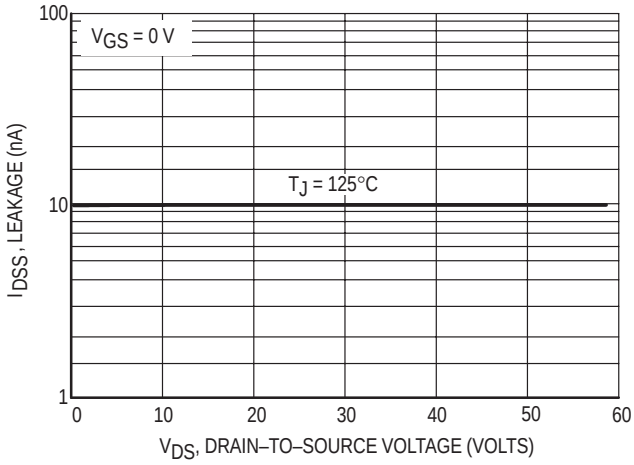


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

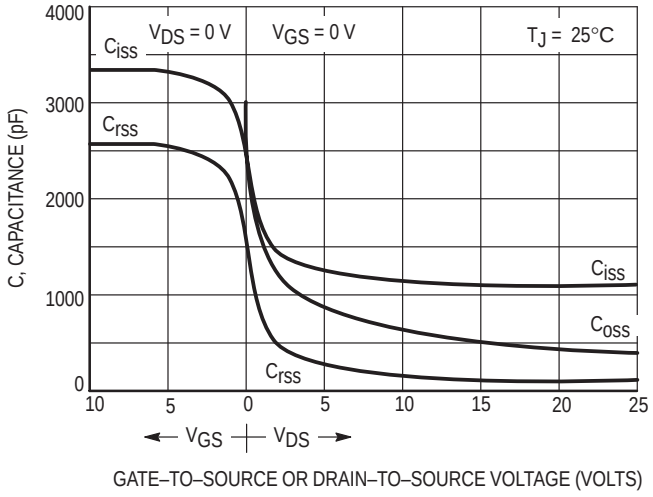


Figure 7. Capacitance Variation

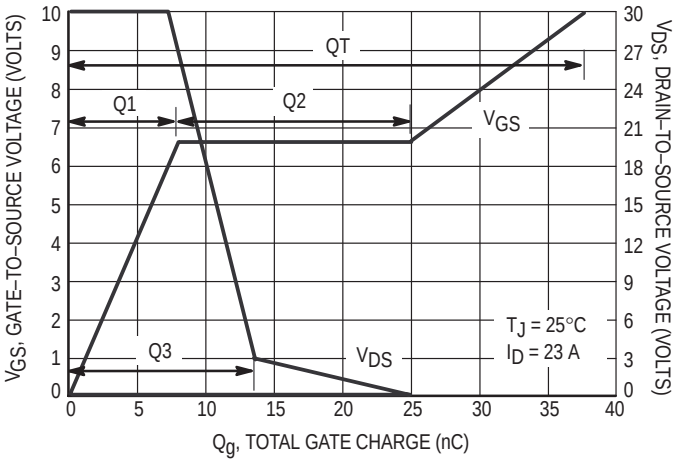


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

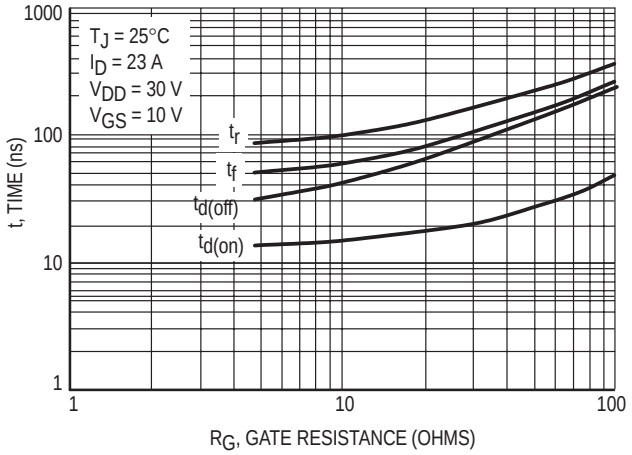


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

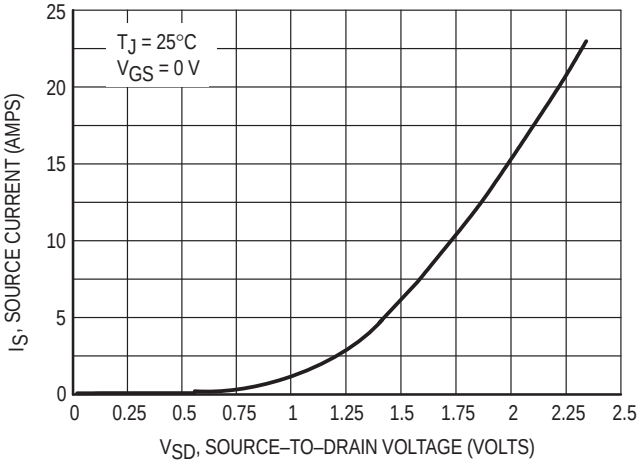


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

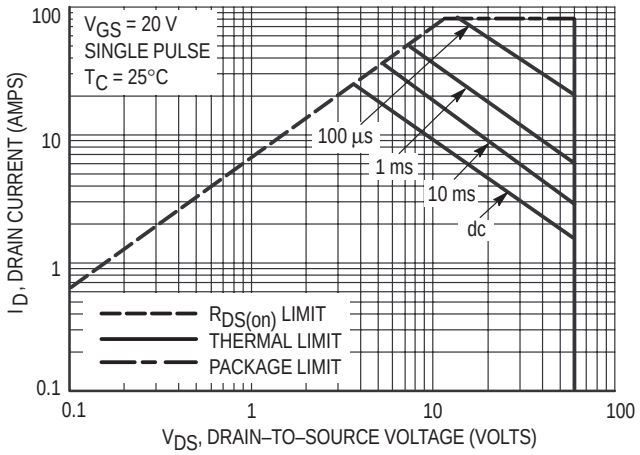


Figure 11. Maximum Rated Forward Biased Safe Operating Area

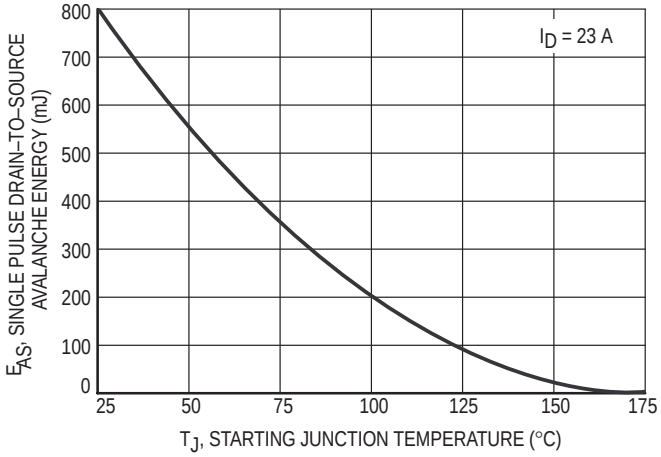


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

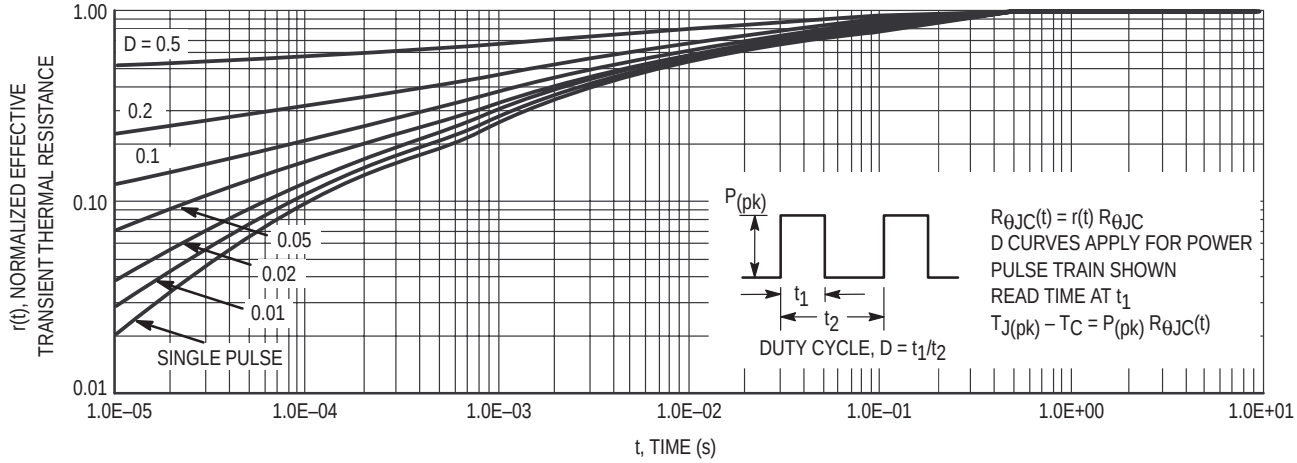


Figure 13. Thermal Response

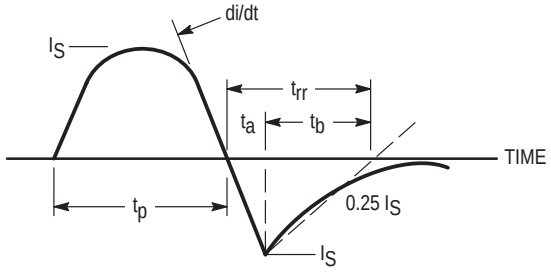


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

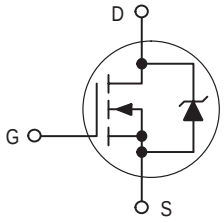
MTP27N10E

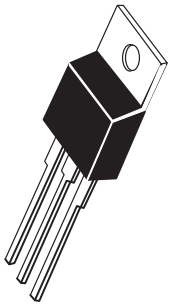
Motorola Preferred Device

TMOS POWER FET
27 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.07 OHM

This advanced TMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Device Marking: MTP27N10E





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	100	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	27 17 95	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C	P_D	104 0.83	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 75 Vdc, V_{GS} = 10 Vdc, I_L = 27 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	109	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (3) (V_{GS} = 0 Vdc, I_D = 0.25 mAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 100 —	 — 120	 — —	 Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 10 100	µAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (3) (V_{DS} = V_{GS}, I_D = 250 µAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 2.0 —	 3.1 7.0	 4.0 —	 Vdc mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (3) (V_{GS} = 10 Vdc, I_D = 13.5 Adc)		$R_{DS(on)}$	 —	 0.058	 0.07	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 27 Adc) (V_{GS} = 10 Vdc, I_D = 13.5 Adc, T_J = 125°C)		$V_{DS(on)}$	 — —	 — —	 2.3 2.0	Vdc
Forward Transconductance (V_{DS} = 7.7 Vdc, I_D = 13.5 Adc)		g_{FS}	6.0	11	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1131	1580	pF
Output Capacitance		C_{oss}	—	468	660	
Transfer Capacitance		C_{rss}	—	186	370	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 50 Vdc, I_D = 27 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	13	30	ns
Rise Time		t_r	—	142	280	
Turn–Off Delay Time		$t_{d(off)}$	—	29	60	
Fall Time		t_f	—	59	120	
Gate Charge (See Figure 8)	(V_{DS} = 80 Vdc, I_D = 27 Adc, V_{GS} = 10 Vdc)	Q_T	—	41	60	nC
		Q_1	—	9.0	—	
		Q_2	—	25	—	
		Q_3	—	22	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 27 Adc, V_{GS} = 0 Vdc) (I_S = 27 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 1.0 0.94	 1.5 —	Vdc
Reverse Recovery Time	(I_S = 27 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/µs)	t_{rr}	—	126	—	ns
		t_a	—	98	—	
		t_b	—	28	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.685	—	µC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	 3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

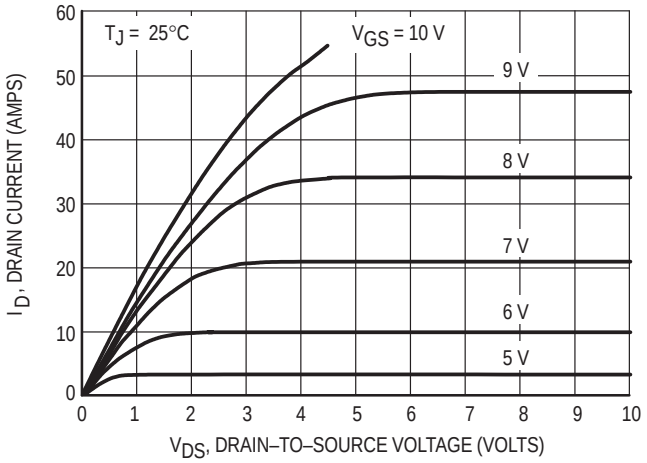


Figure 1. On–Region Characteristics

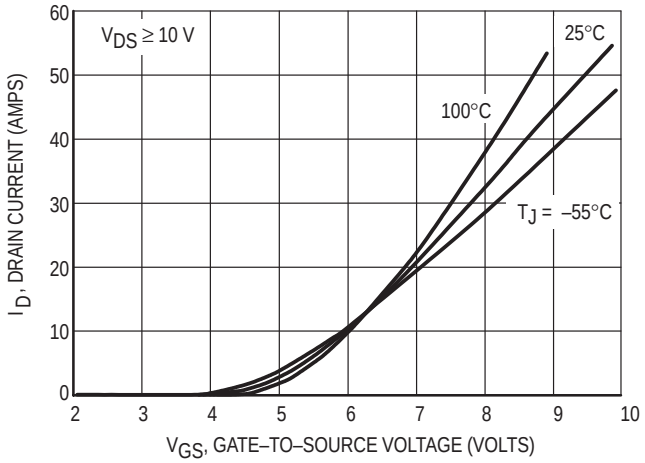


Figure 2. Transfer Characteristics

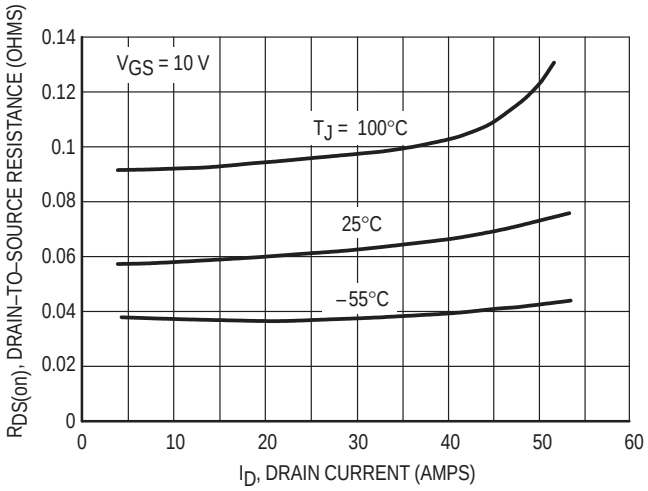


Figure 3. On–Resistance versus Drain Current and Temperature

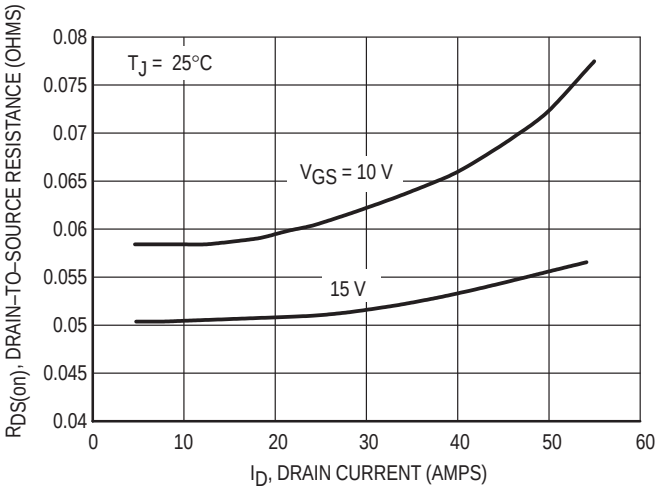


Figure 4. On–Resistance versus Drain Current and Gate Voltage

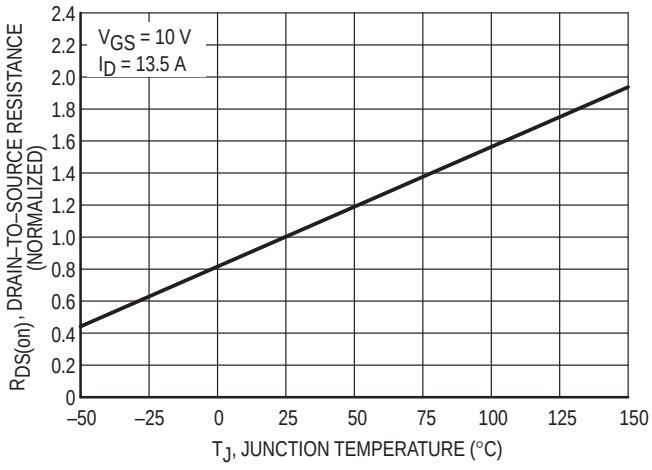
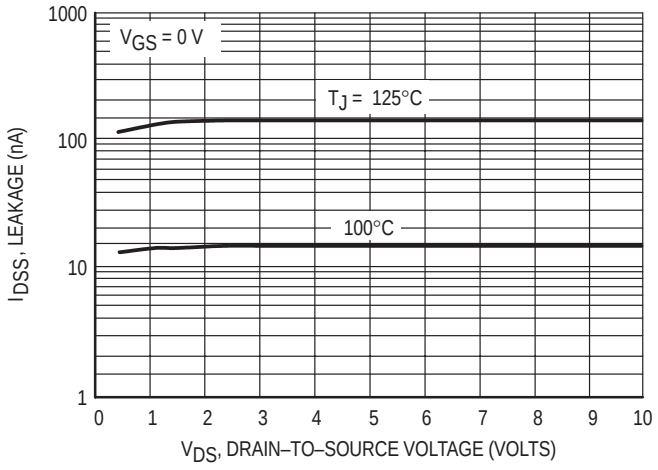


Figure 5. On–Resistance Variation with Temperature



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POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

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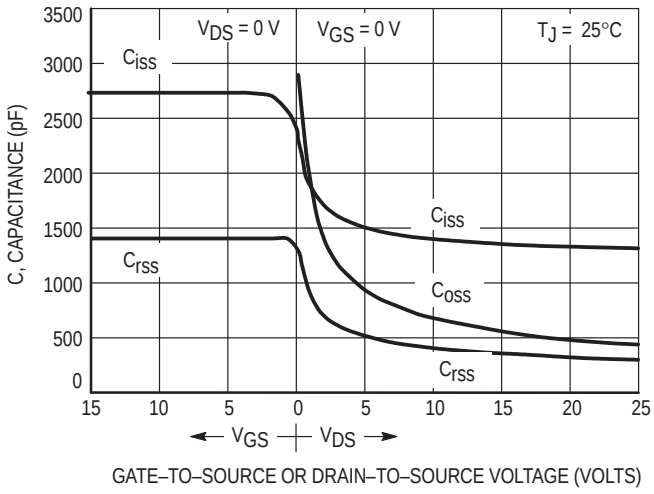


Figure 7. Capacitance Variation

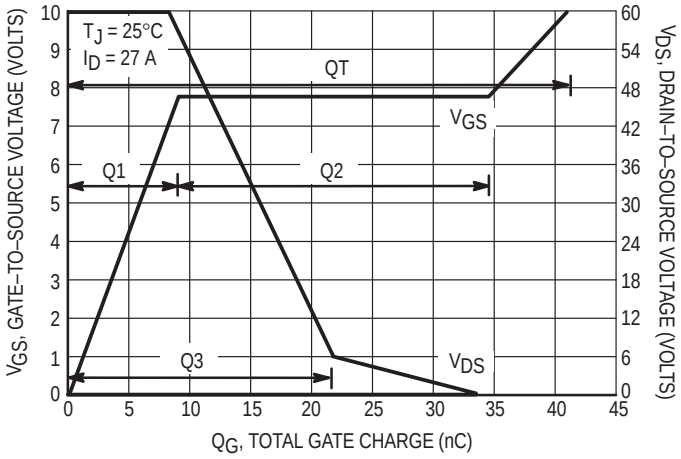


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

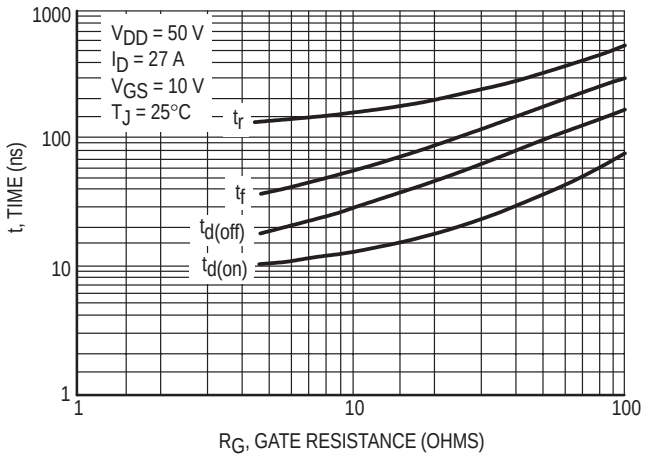


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

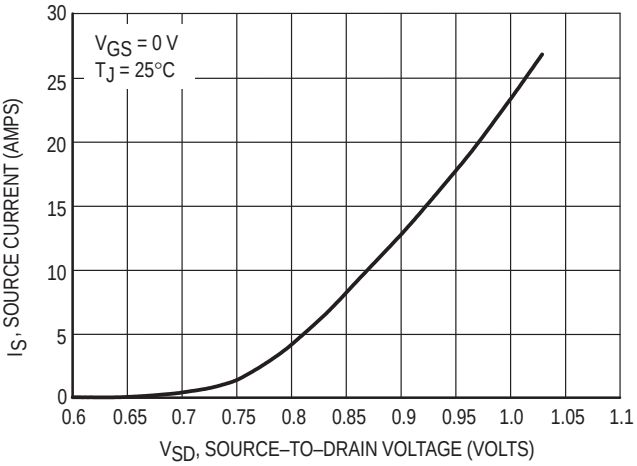


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

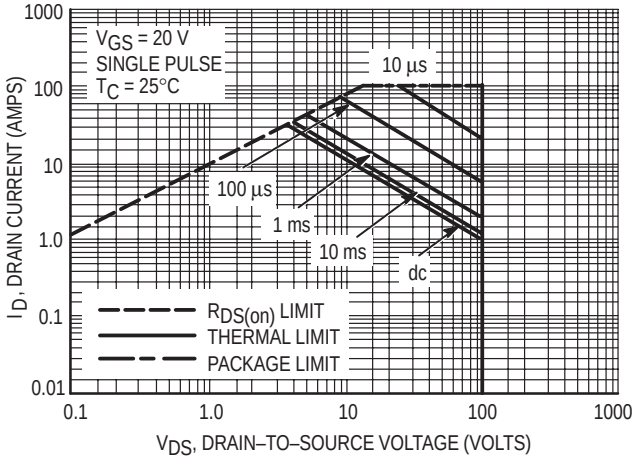


Figure 11. Maximum Rated Forward Biased Safe Operating Area

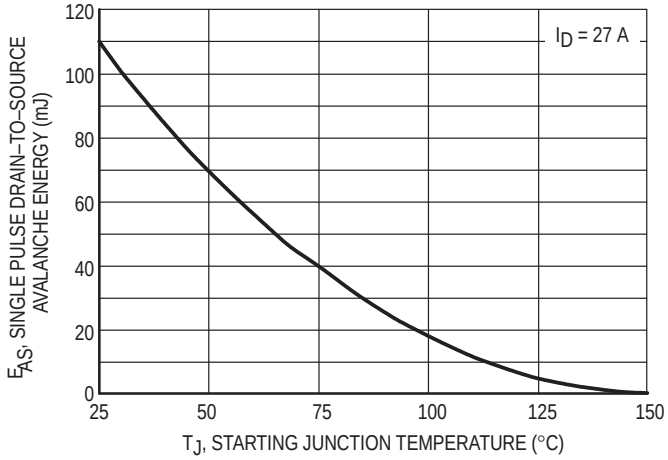


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

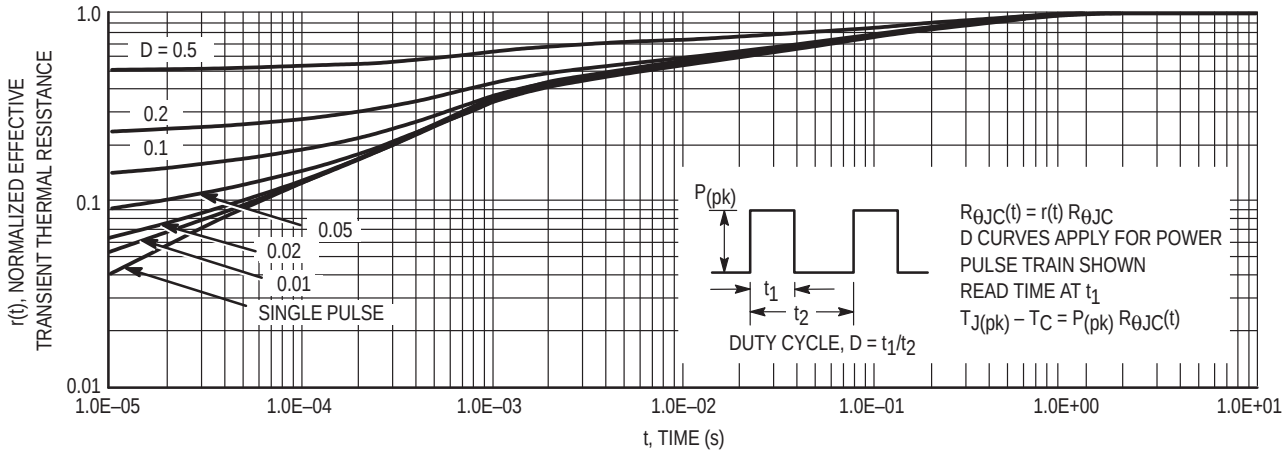


Figure 13. Thermal Response

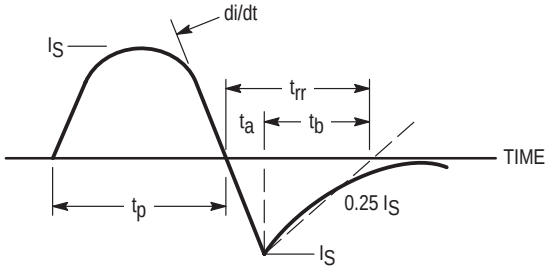


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

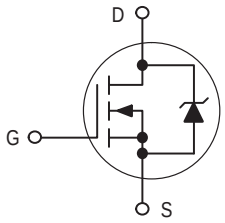
TMOS V
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

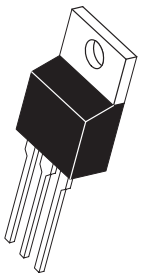
MTP30N06VL

Motorola Preferred Device

TMOS POWER FET
30 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.050 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 221A–06, Style 5
TO–220AB

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	30 20 105	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	90 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5 Vdc, PEAK I_L = 30 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	154	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

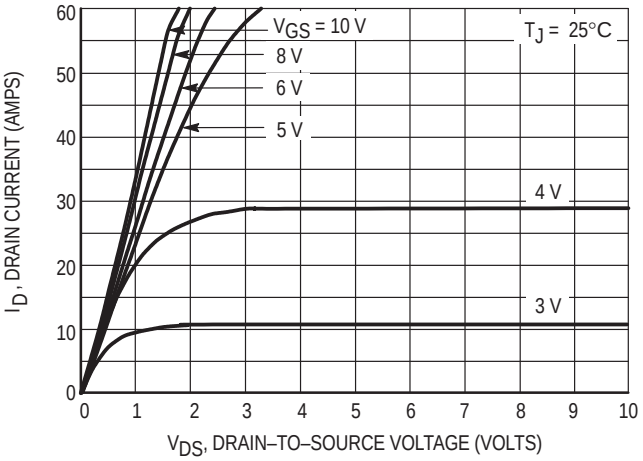
REV 3

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	63	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150 °C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Threshold Temperature Coefficient (Negative)			—	4.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 5 Vdc, I_D = 15 Adc)		$R_{DS(on)}$	—	0.033	0.05	Ohm
Drain–to–Source On–Voltage (V_{GS} = 5 Vdc, I_D = 30 Adc)		$V_{DS(on)}$	—	—	1.8	Vdc
(V_{GS} = 5 Vdc, I_D = 15 Adc, T_J = 150 °C)			—	—	1.73	
Forward Transconductance (V_{DS} = 6.25 Vdc, I_D = 15 Adc)		g_{FS}	13	21	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1130	1580	pF
Output Capacitance		C_{oss}	—	360	500	
Transfer Capacitance		C_{rss}	—	95	190	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 30 Adc, V_{GS} = 5 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	14	30	ns
Rise Time		t_r	—	260	520	
Turn–Off Delay Time		$t_{d(off)}$	—	54	110	
Fall Time		t_f	—	108	220	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 30 Adc, V_{GS} = 5 Vdc)	Q_T	—	27	40	nC
		Q_1	—	5	—	
		Q_2	—	17	—	
		Q_3	—	15	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 30 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.98	1.6	Vdc
	(I_S = 30 Adc, V_{GS} = 0 Vdc, T_J = 150 °C)		—	0.89	—	
Reverse Recovery Time	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	86.4	—	ns
		t_a	—	49.6	—	
		t_b	—	36.8	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.228	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS



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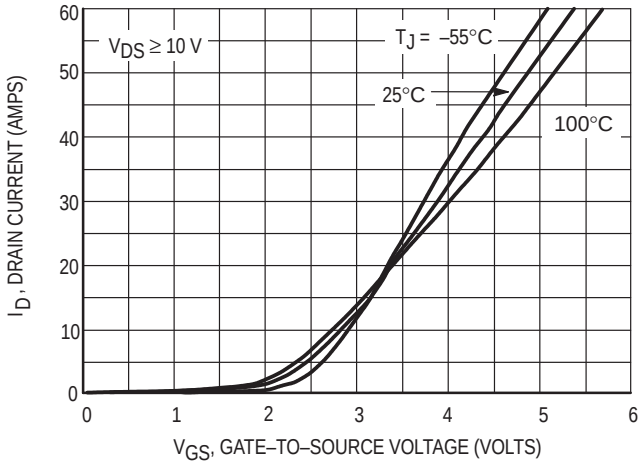

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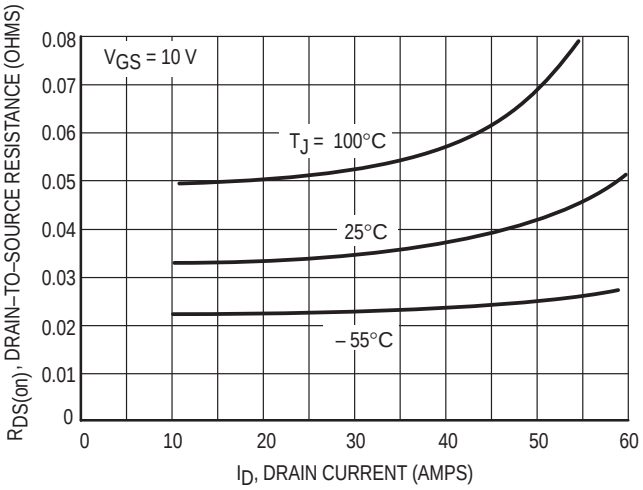

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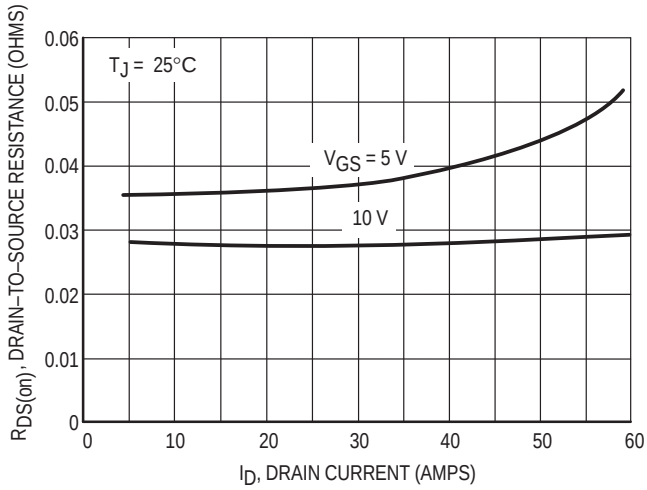

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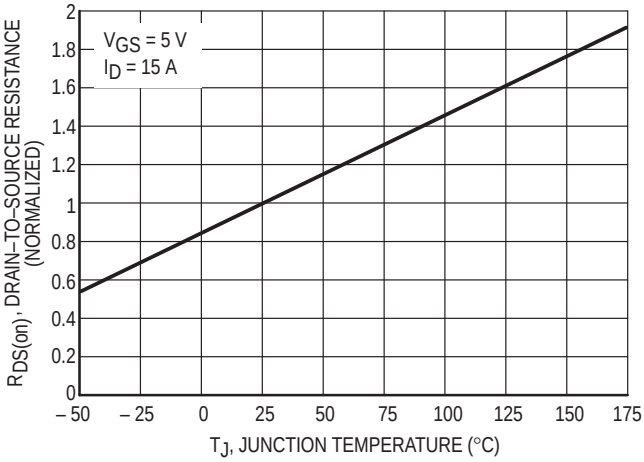

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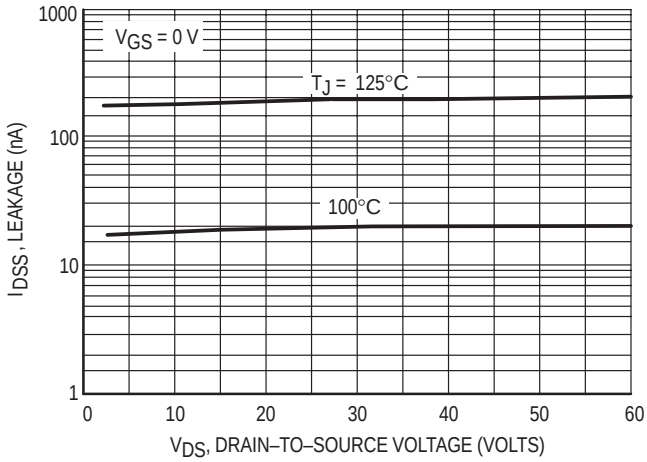

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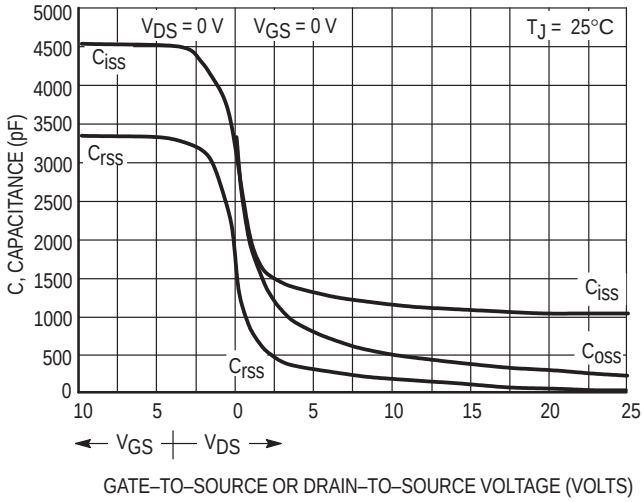

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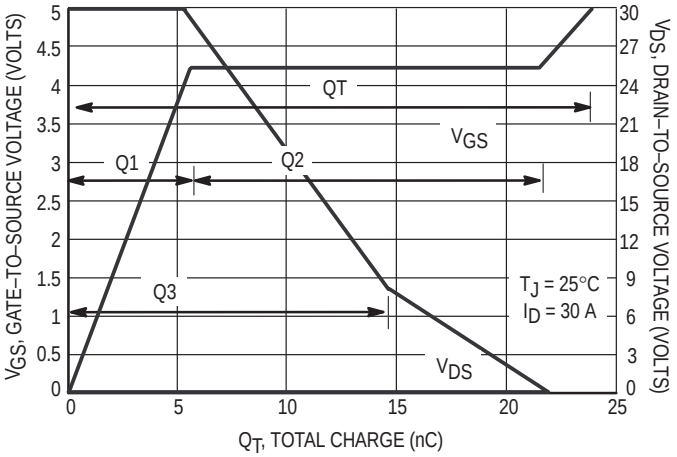

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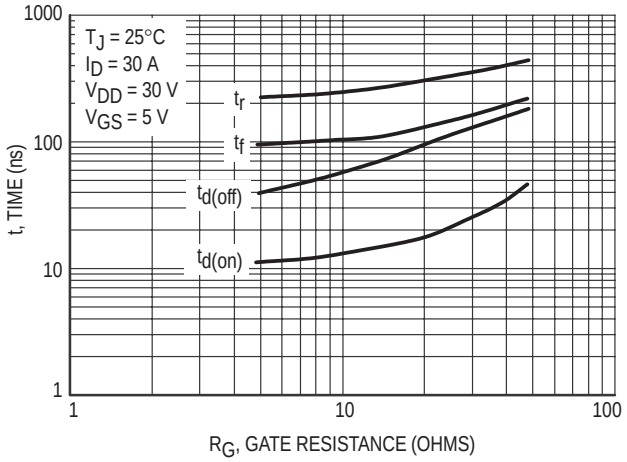


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

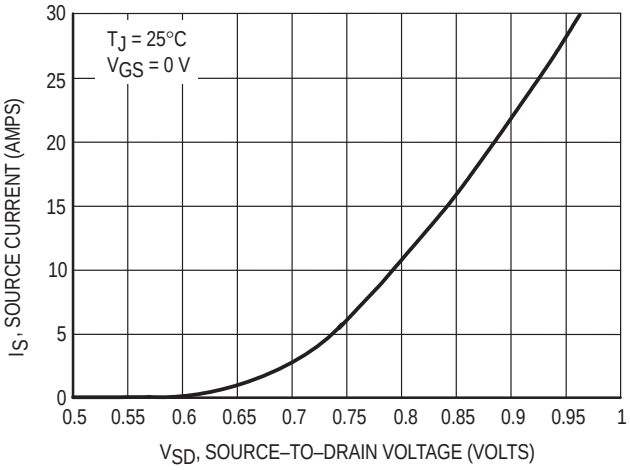


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

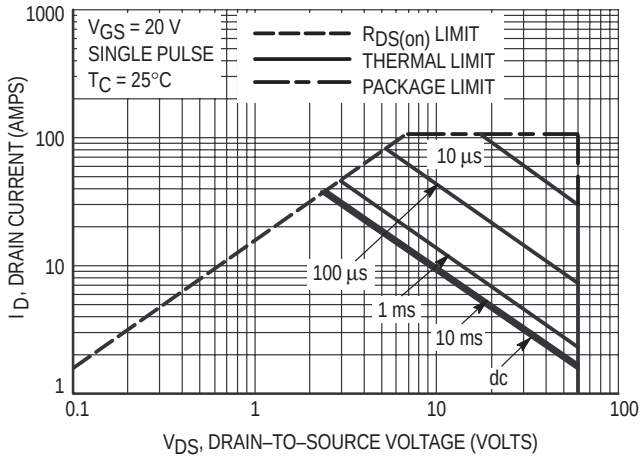


Figure 11. Maximum Rated Forward Biased Safe Operating Area

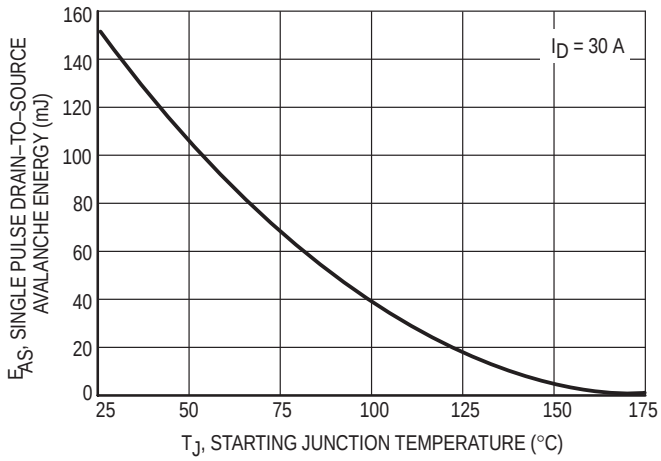


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

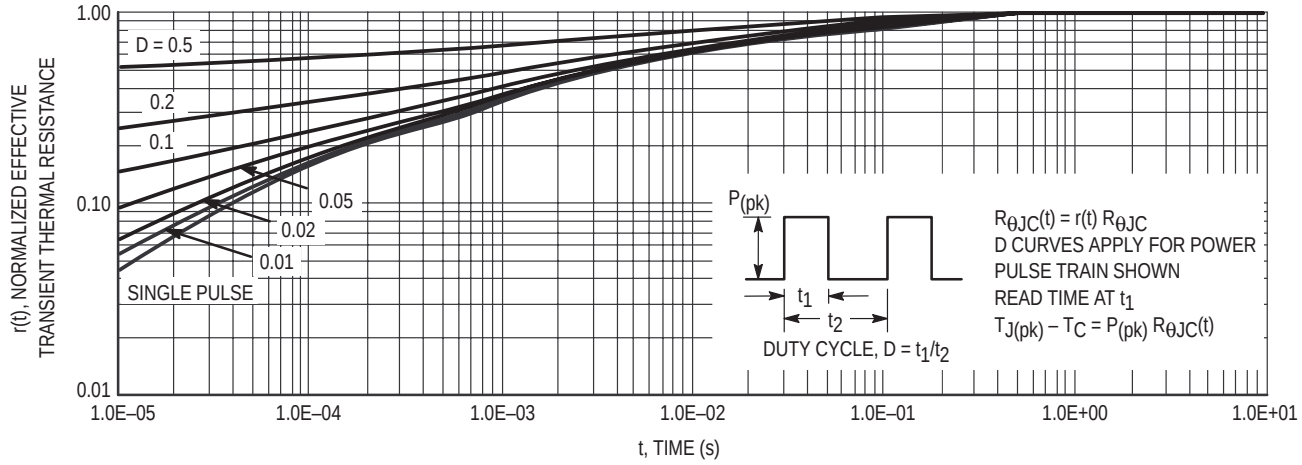


Figure 13. Thermal Response

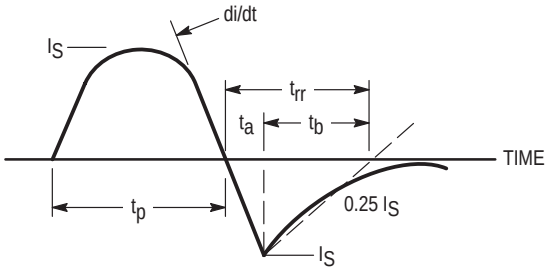


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

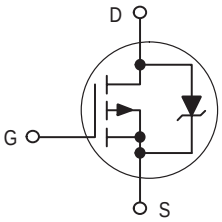
TMOS V
Power Field Effect Transistor
P–Channel Enhancement–Mode Silicon Gate

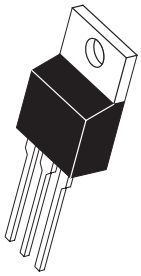
MTP30P06V

Motorola Preferred Device

TMOS POWER FET
30 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.080 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 221A–06, Style 5
TO–220AB

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	30 19 105	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C	P_D	125 0.83	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, PEAK I_L = 30 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	450	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	62	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.6	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	5.3	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)		$R_{DS(on)}$	—	0.067	0.08	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 30 Adc)		$V_{DS(on)}$	—	2.0	2.9	Vdc
(V_{GS} = 10 Vdc, I_D = 15 Adc, T_J = 150°C)			—	—	2.8	
Forward Transconductance (V_{DS} = 8.3 Vdc, I_D = 15 Adc)		g_{FS}	5.0	7.9	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1562	2190	pF
Output Capacitance		C_{oss}	—	524	730	
Transfer Capacitance		C_{rss}	—	154	310	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 30 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	14.7	30	ns
Rise Time		t_r	—	25.9	50	
Turn–Off Delay Time		$t_{d(off)}$	—	98	200	
Fall Time		t_f	—	52.4	100	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 30 Adc, V_{GS} = 10 Vdc)	Q_T	—	54	80	nC
		Q_1	—	9.0	—	
		Q_2	—	26	—	
		Q_3	—	20	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 30 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	2.3	3.0	Vdc
	(I_S = 30 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	1.9	—	
Reverse Recovery Time	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	175	—	ns
		t_a	—	107	—	
		t_b	—	68	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.965	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)				4.5		
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

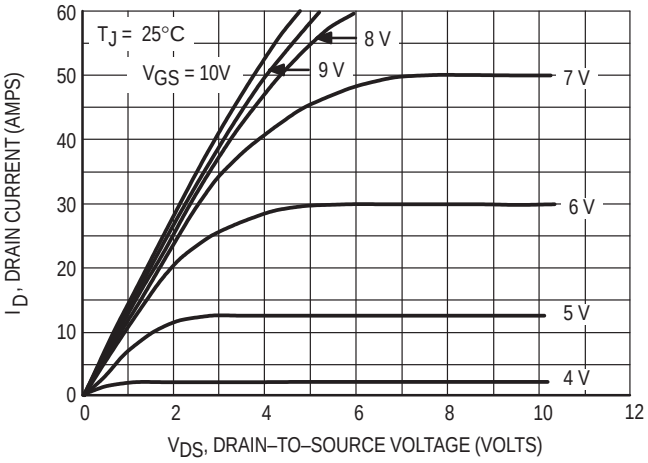


Figure 1. On–Region Characteristics

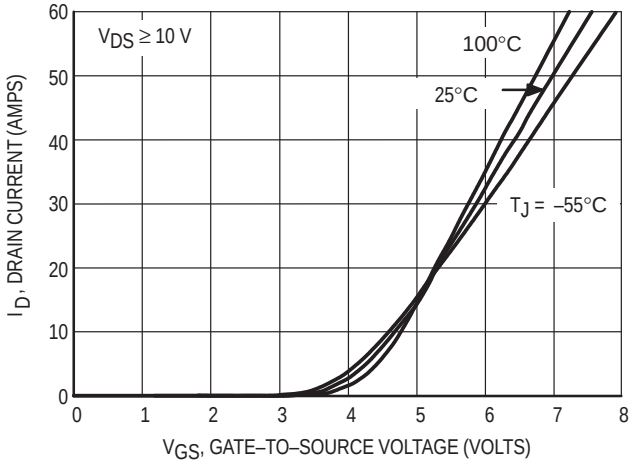


Figure 2. Transfer Characteristics

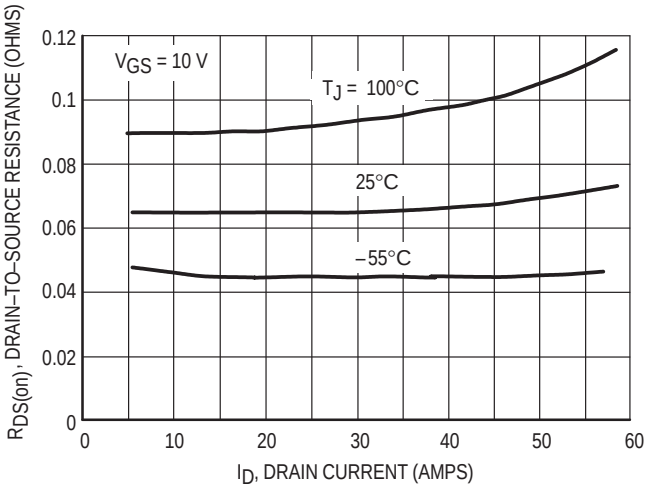


Figure 3. On–Resistance versus Drain Current and Temperature

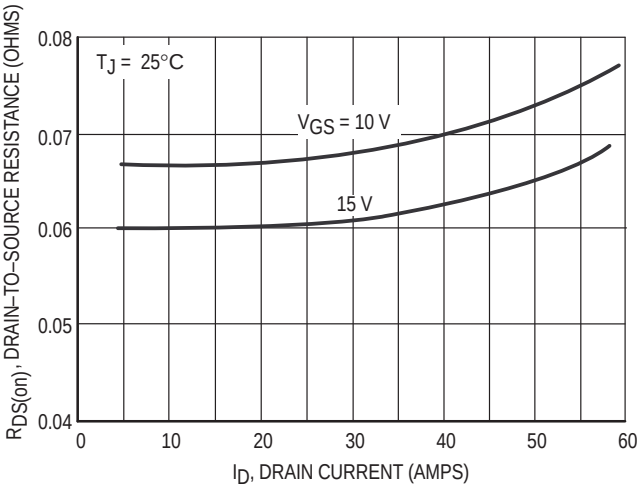


Figure 4. On–Resistance versus Drain Current and Gate Voltage

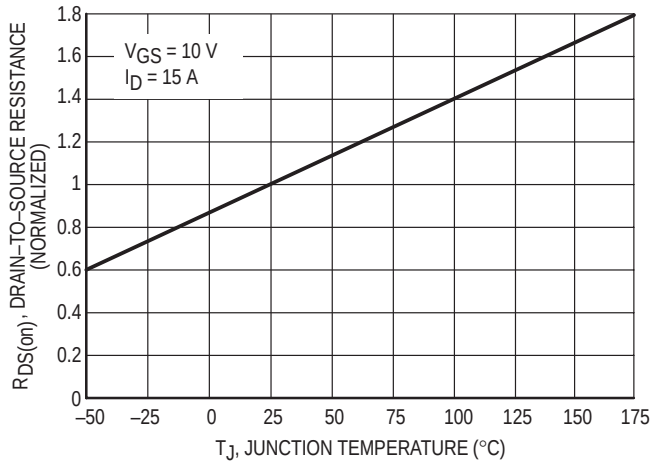


Figure 5. On–Resistance Variation with Temperature

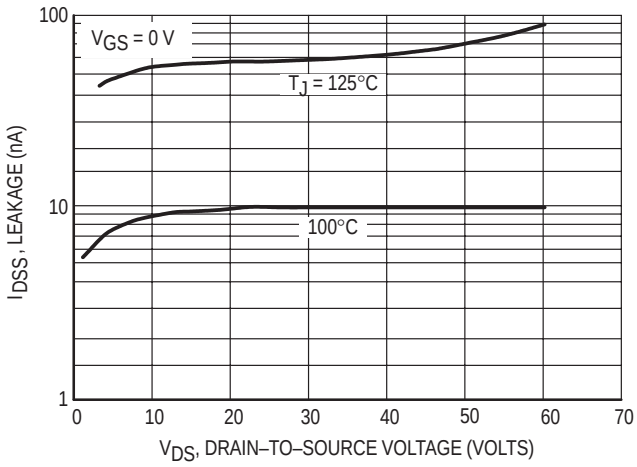


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

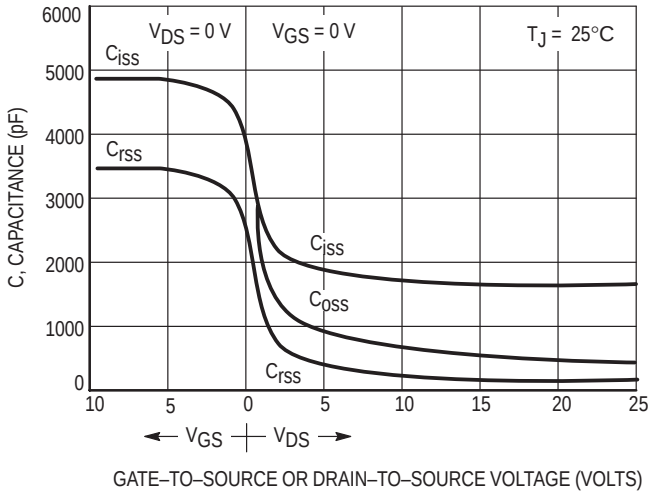


Figure 7. Capacitance Variation

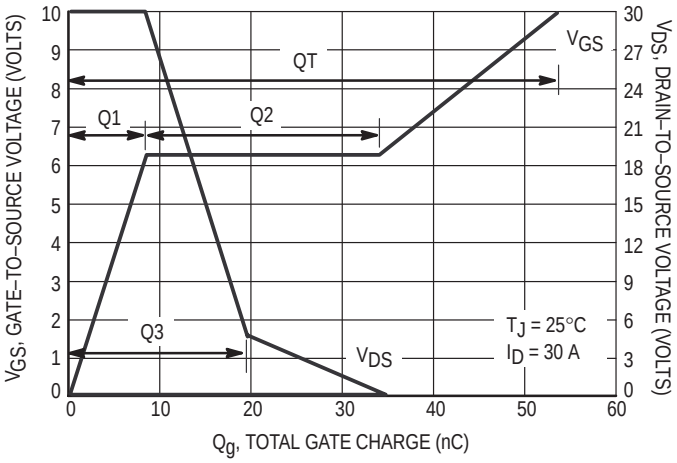


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

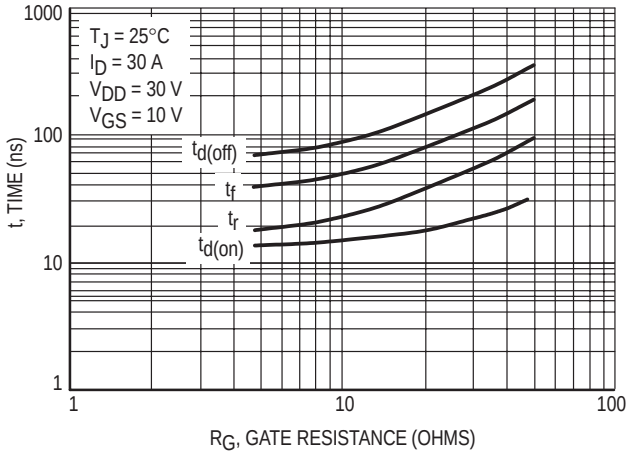


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

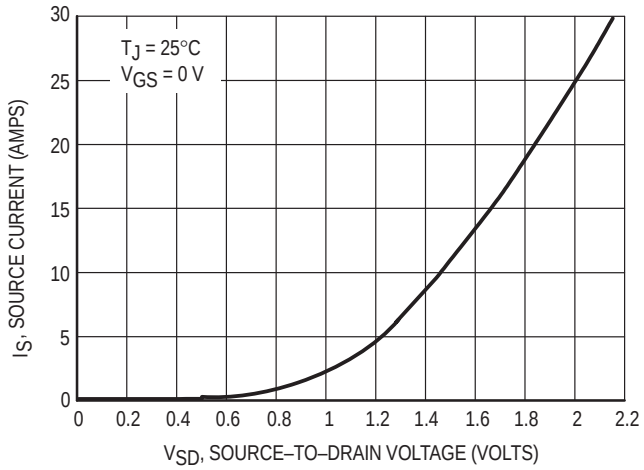


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

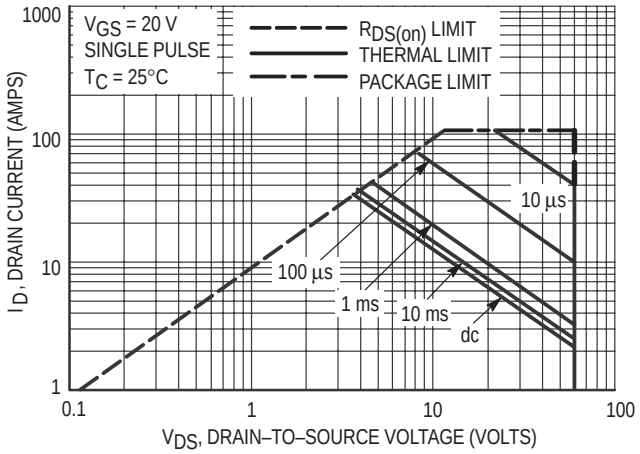
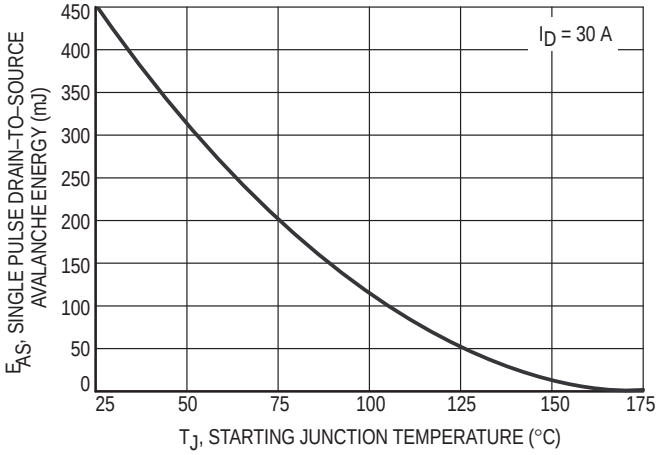


Figure 11. Maximum Rated Forward Biased Safe Operating Area



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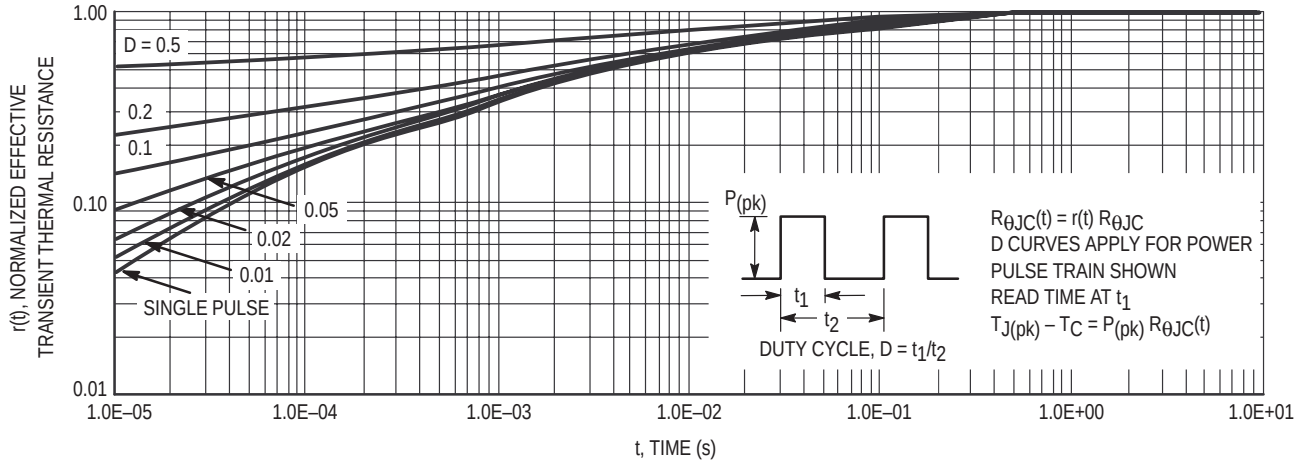


Figure 13. Thermal Response

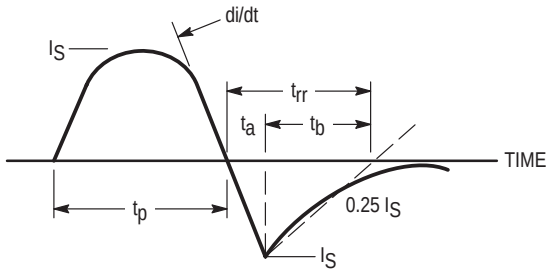


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet
TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

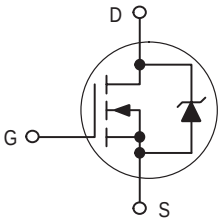
MTP33N10E

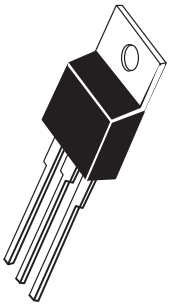
Motorola Preferred Device

TMOS POWER FET
33 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.06 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	100	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–Source — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Voltage — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	33 20 99	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 33 Apk, L = 1.000 mH, R_G = 25 Ω)	E_{AS}	545	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.00 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)	$V_{(BR)DSS}$	100	—	—	Vdc
Temperature Coefficient (Positive)		—	118	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
(V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = – 25°C)		—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)	$V_{GS(th)}$	2.0	—	4.0	Vdc
Temperature Coefficient (Negative)		—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 16.5 Adc)	$R_{DS(on)}$	—	0.04	0.06	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 33 Adc)	$V_{DS(on)}$	—	1.6	2.4	Vdc
(I_D = 16.5 Adc, T_J = – 25°C)		—	—	2.1	
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 16.5 Adc)	g_{FS}	8.0	—	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	—	1830	2500	pF
Output Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{oss}	—	678	1200	
Reverse Transfer Capacitance	C_{rss}	—	559	1100	
SWITCHING CHARACTERISTICS (2)					
Turn–On Delay Time	$t_{d(on)}$	—	18	40	ns
Rise Time (V_{DD} = 50 Vdc, I_D = 33 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	t_r	—	164	330	
Turn–Off Delay Time	$t_{d(off)}$	—	48	100	
Fall Time	t_f	—	83	170	
Gate Charge (See Figure 8)	Q_T	—	52	110	nC
(V_{DS} = 80 Vdc, I_D = 33 Adc, V_{GS} = 10 Vdc)	Q_1	—	12	—	
	Q_2	—	32	—	
	Q_3	—	24	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (1) (I_S = 33 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	2.0	Vdc
(I_S = 33 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.98	—	
Reverse Recovery Time (See Figure 14)	t_{rr}	—	144	—	ns
(I_S = 33 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_a	—	108	—	
	t_b	—	36	—	
Reverse Recovery Stored Charge	Q_{RR}	—	0.93	—	μC
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from contact screw on tab to center of die)	L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			4.5		
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

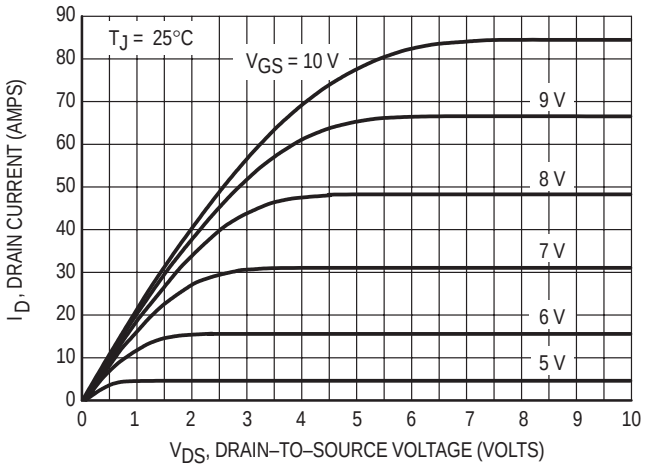


Figure 1. On–Region Characteristics

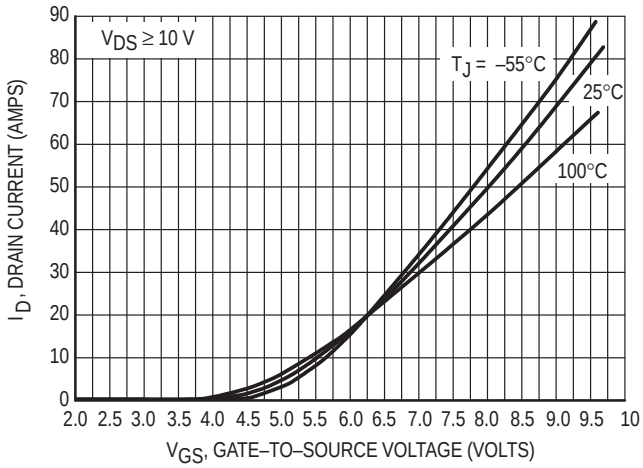


Figure 2. Transfer Characteristics

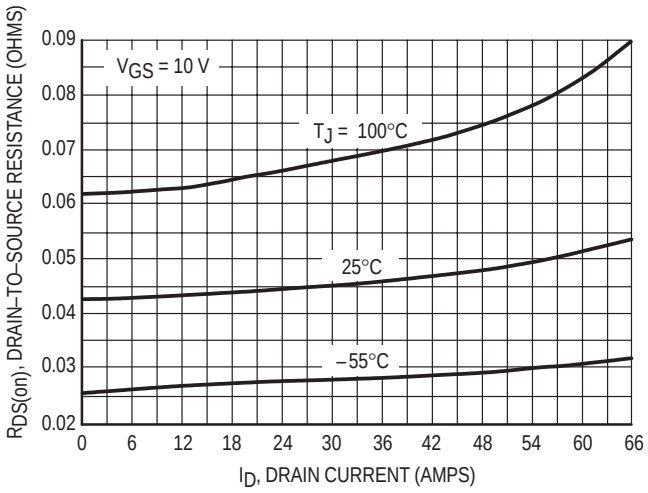


Figure 3. On–Resistance versus Drain Current and Temperature

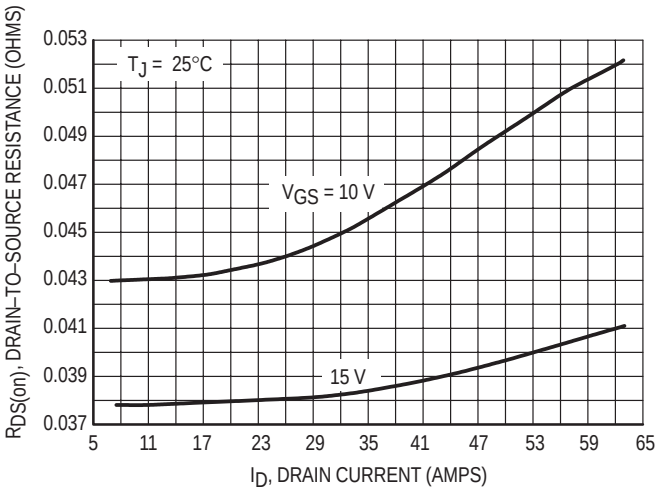


Figure 4. On–Resistance versus Drain Current and Gate Voltage

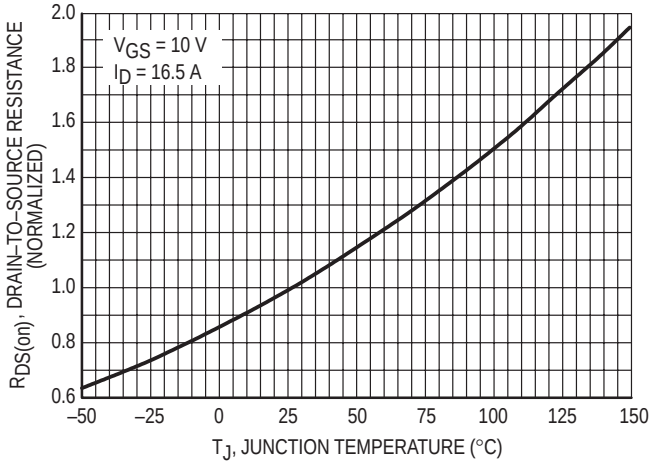


Figure 5. On–Resistance Variation with Temperature

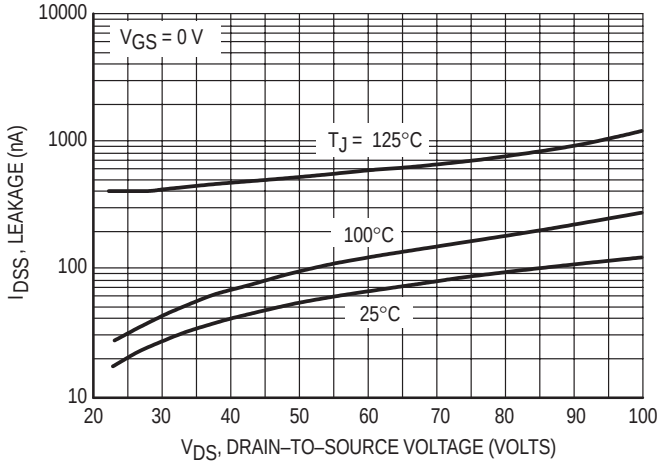


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

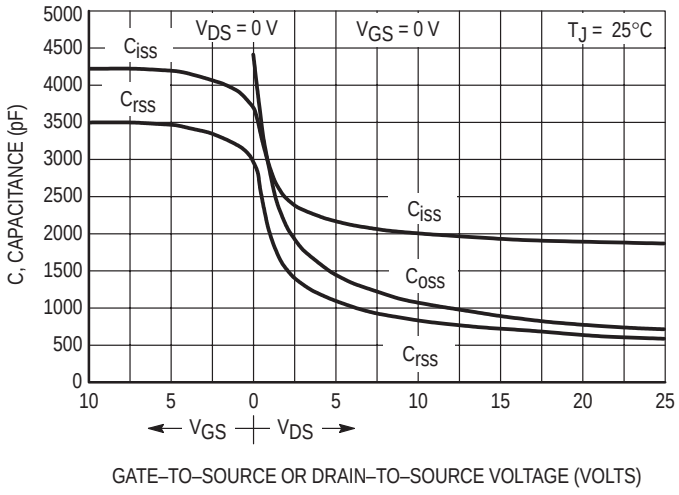


Figure 7. Capacitance Variation

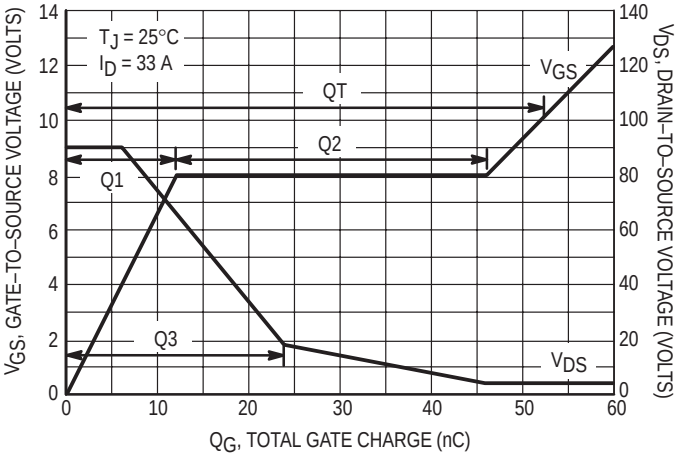


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

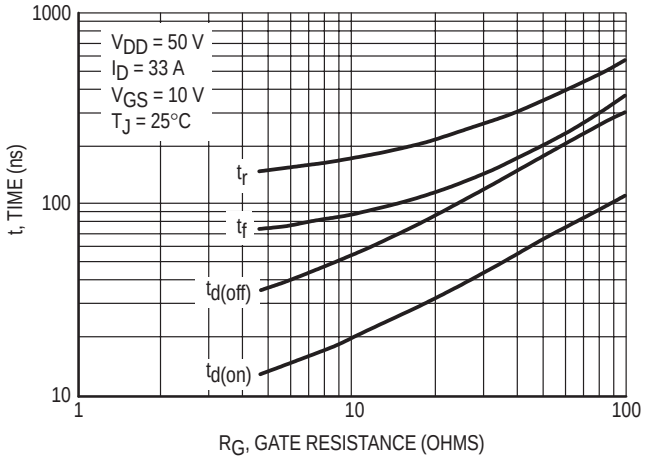


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

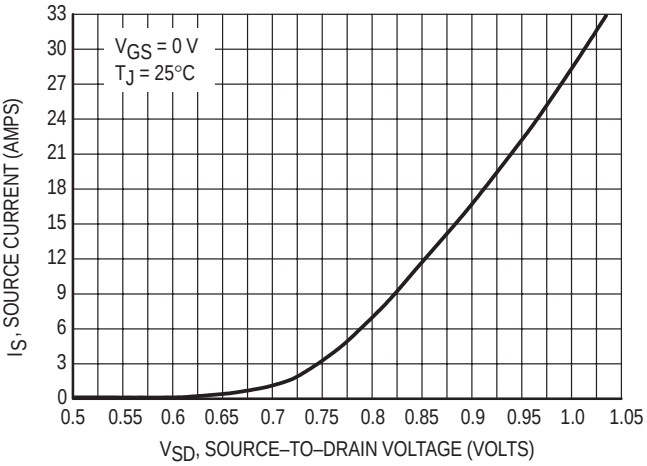


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

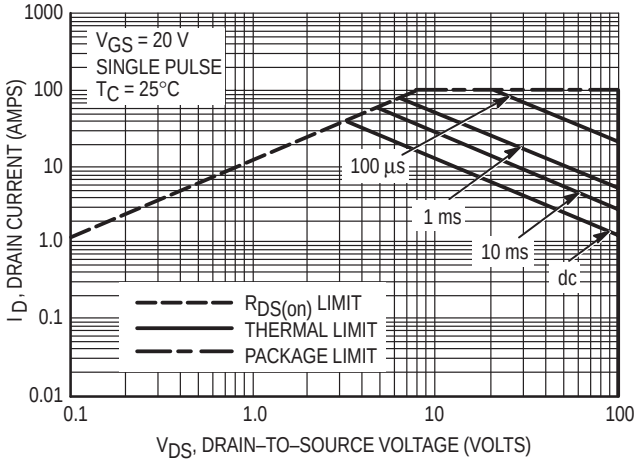


Figure 11. Maximum Rated Forward Biased Safe Operating Area

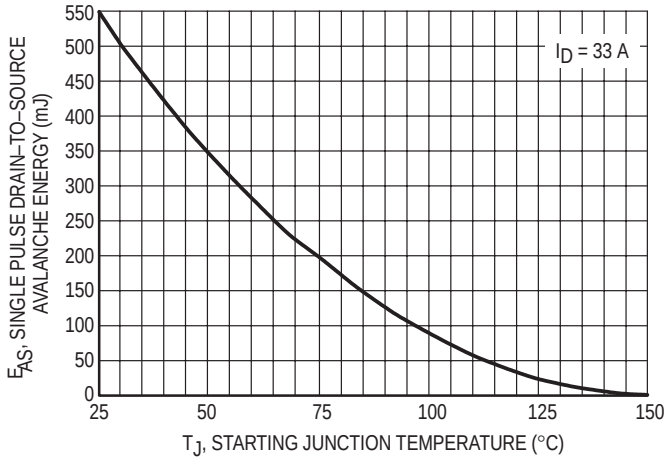


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

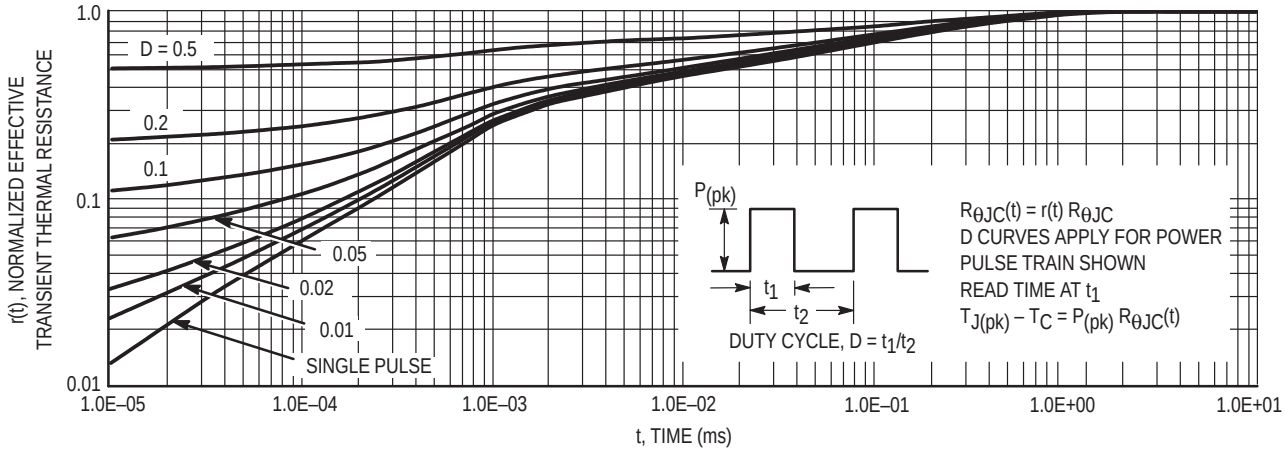


Figure 13. Thermal Response

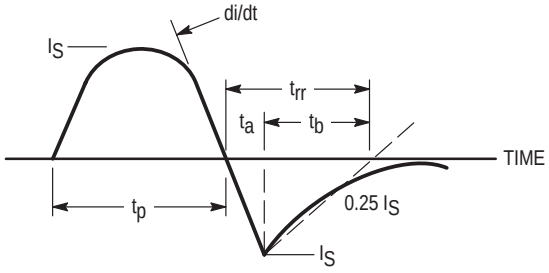


Figure 14. Diode Reverse Recovery Waveform

Product Preview

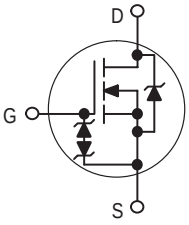
HDTMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

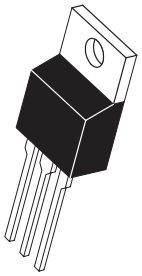
MTP35N06ZL

TMOS POWER FET
35 AMPERES
60 VOLTS
$R_{DS(on)}$ = 26 mΩ

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor–Absorbs High Energy in the Avalanche Mode
- ESD Protected. 400 V Machine Model Level and 4000 V Human Body Model Level.





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±15 ±20	Vdc Vpk
Drain Current — Continuous @ T_C = 25°C — Continuous @ T_C = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	35 22.8 105	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	94 0.63	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{DS} = 60 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 35 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	184	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.6 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (Cpk ≥ 3.0) (V_{GS} = 0 Vdc, I_D = 250 μAdc)	$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)		—	52	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		—	—	100	
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0)	I_{GSS}	—	—	5.0	μAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (Cpk ≥ 3.0) (V_{DS} = V_{GS}, I_D = 250 μAdc)	$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Threshold Temperature Coefficient (Negative)		—	4.0	—	mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (V_{GS} = 5.0 Vdc, I_D = 11.5 Adc)	$R_{DS(on)}$	—	22	26	mΩ
Drain–to–Source On–Voltage (V_{GS} = 5.0 Vdc) (I_D = 23 Adc)	$V_{DS(on)}$	—	0.78	1.1	Vdc
(I_D = 11.5 Adc, T_J = 125°C)		—	0.7	1.0	
Forward Transconductance (V_{DS} = 4.0 Vdc, I_D = 11.5 Adc)	g_{FS}	10	12	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	C_{iss}	—	1600	—	pF
Output Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{oss}	—	560	—	
Transfer Capacitance	C_{rss}	—	140	—	
SWITCHING CHARACTERISTICS (2)					
Turn–On Delay Time	$t_{d(on)}$	—	40	—	ns
Rise Time (V_{DD} = 30 Vdc, I_D = 23 Adc, $V_{GS(on)}$ = 5.0 Vdc, R_G = 9.1 Ω)	t_r	—	250	—	
Turn–Off Delay Time	$t_{d(off)}$	—	130	—	
Fall Time	t_f	—	170	—	
Gate Charge (See Figure 8)	Q_T	—	45	—	nC
(V_{DS} = 48 Vdc, I_D = 23 Adc, V_{GS} = 5.0 Vdc)	Q_1	—	8.0	—	
	Q_2	—	22	—	
	Q_3	—	19	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (I_S = 23 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.92	1.1	Vdc
(I_S = 23 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.81	—	
Reverse Recovery Time	t_{rr}	—	43	—	ns
(I_S = 23 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_a	—	24	—	
	t_b	—	20	—	
Reverse Recovery Stored Charge	Q_{RR}	—	0.055	—	μC
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from contact screw on tab to center of die)	L_D	—	3.5	—	nH
(Measured from drain lead 0.25″ from package to center of die)			4.5		
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)	L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

Designer's™ Data Sheet

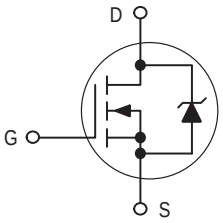
TMOS V
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

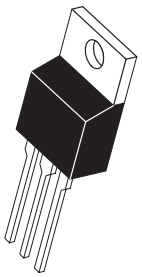
MTP36N06V

Motorola Preferred Device

TMOS POWER FET
32 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.04 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 221A–06, Style 5
TO–220AB

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current — Continuous @ 25 °C — Continuous @ 100 °C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	32 22.6 112	Adc Apk
Total Power Dissipation @ 25 °C Derate above 25 °C	P_D	90 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, PEAK I_L = 32 Apk, L = 0.1 mH, R_G = 25 Ω)	E_{AS}	205	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	61	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150 °C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.6	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	6.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc)		$R_{DS(on)}$	—	0.034	0.04	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 32 Adc)		$V_{DS(on)}$	—	1.25	1.54	Vdc
(V_{GS} = 10 Vdc, I_D = 16 Adc, T_J = 150 °C)			—	—	1.47	
Forward Transconductance (V_{DS} = 7.6 Vdc, I_D = 16 Adc)		g_{FS}	5.0	7.83	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1220	1700	pF
Output Capacitance		C_{oss}	—	337	470	
Reverse Transfer Capacitance		C_{rss}	—	74.8	150	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	14	30	ns
Rise Time		t_r	—	138	270	
Turn–Off Delay Time		$t_{d(off)}$	—	54	100	
Fall Time		t_f	—	91	180	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc)	Q_T	—	39	50	nC
		Q_1	—	7.0	—	
		Q_2	—	17	—	
		Q_3	—	13	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 32 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.03	2.0	Vdc
	(I_S = 32 Adc, V_{GS} = 0 Vdc, T_J = 150 °C)		—	0.94	—	
Reverse Recovery Time	(I_S = 32 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	92	—	ns
		t_a	—	64	—	
		t_b	—	28	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.332	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

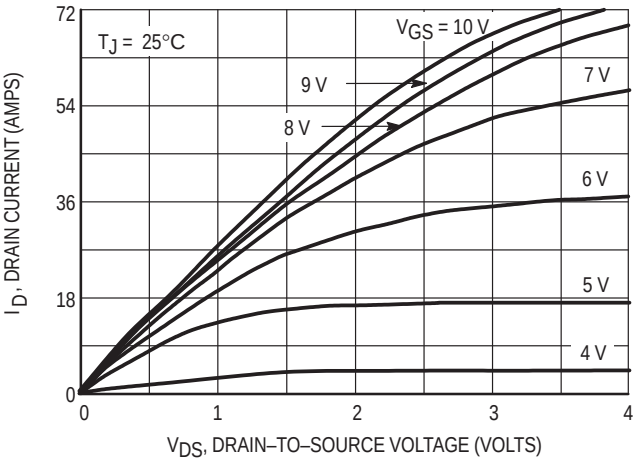


Figure 1. On–Region Characteristics

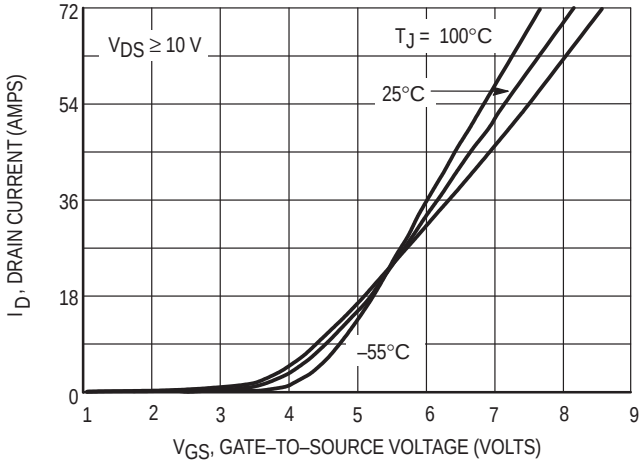


Figure 2. Transfer Characteristics

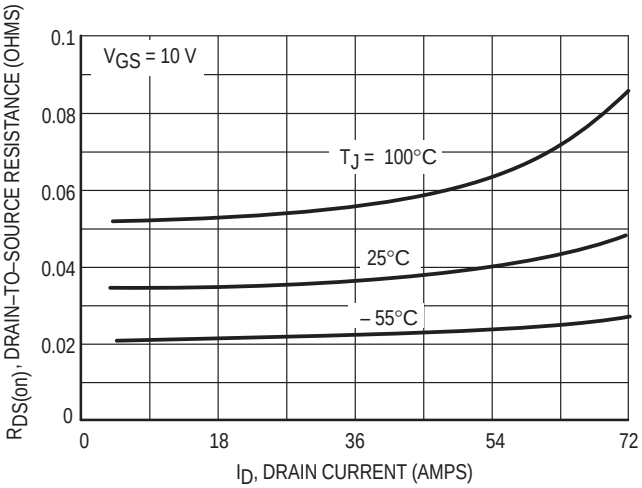


Figure 3. On–Resistance versus Drain Current and Temperature

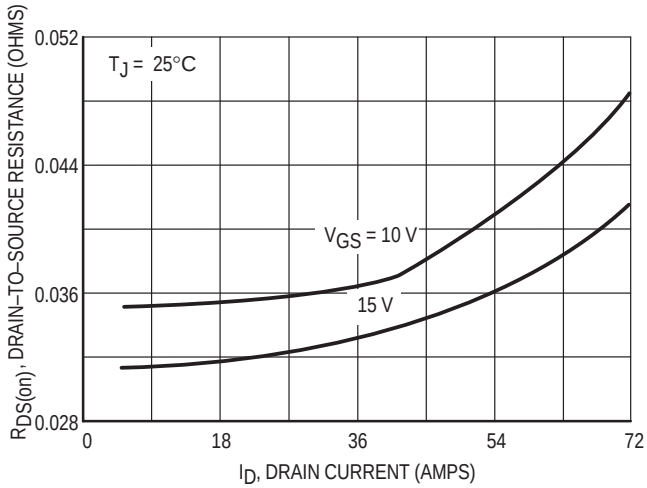


Figure 4. On–Resistance versus Drain Current and Gate Voltage

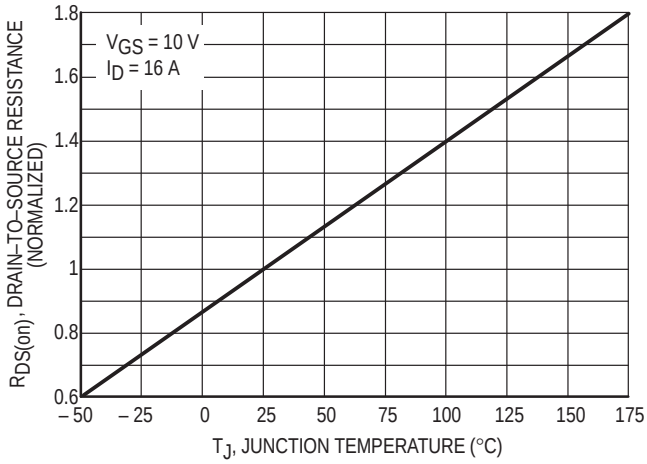


Figure 5. On–Resistance Variation with Temperature

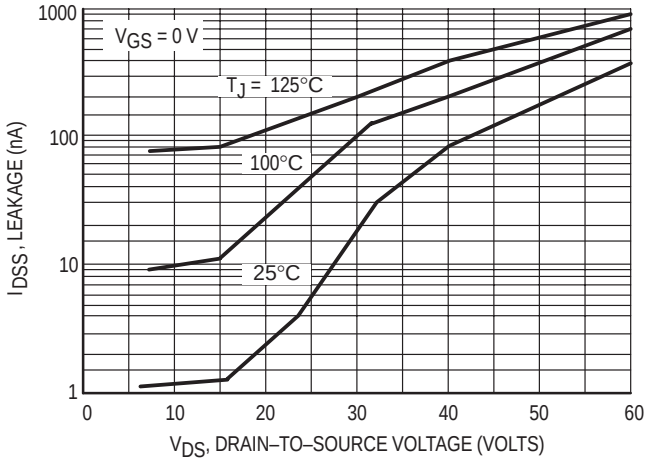


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

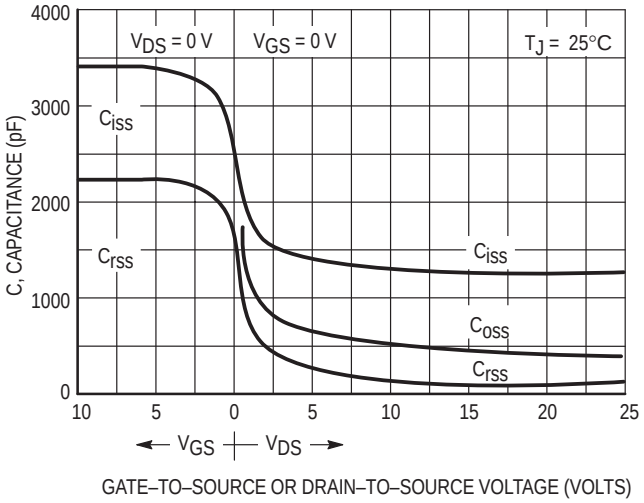


Figure 7. Capacitance Variation

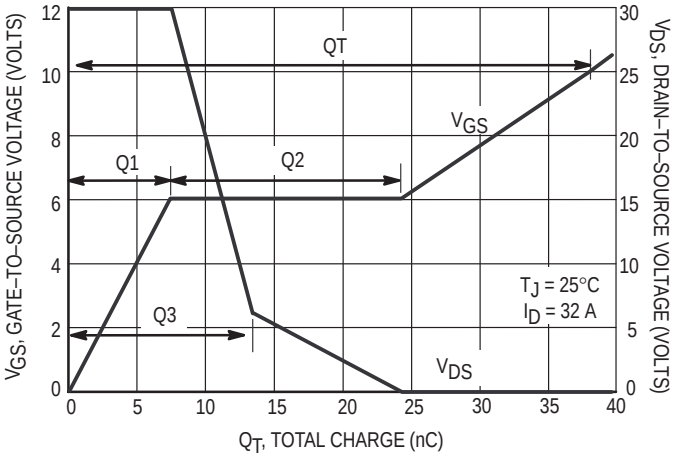


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

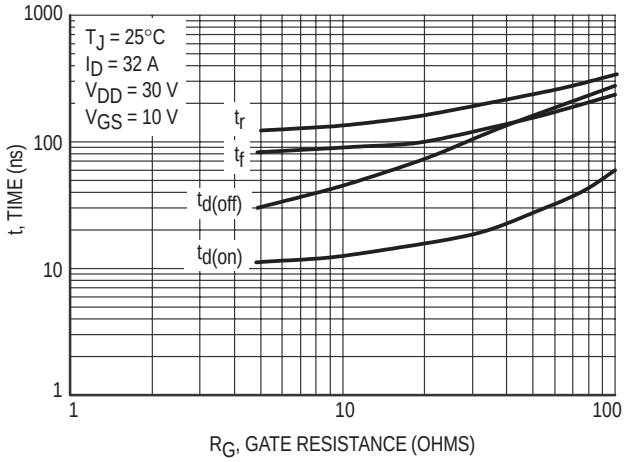


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

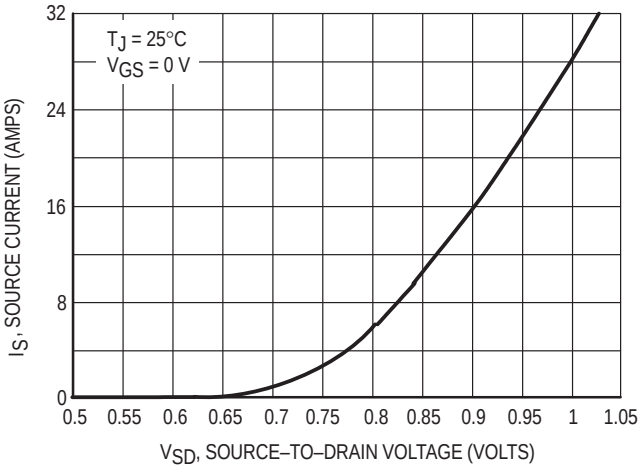


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

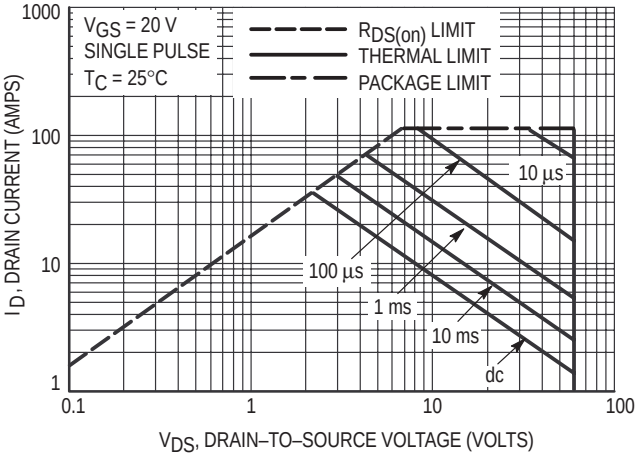


Figure 11. Maximum Rated Forward Biased Safe Operating Area

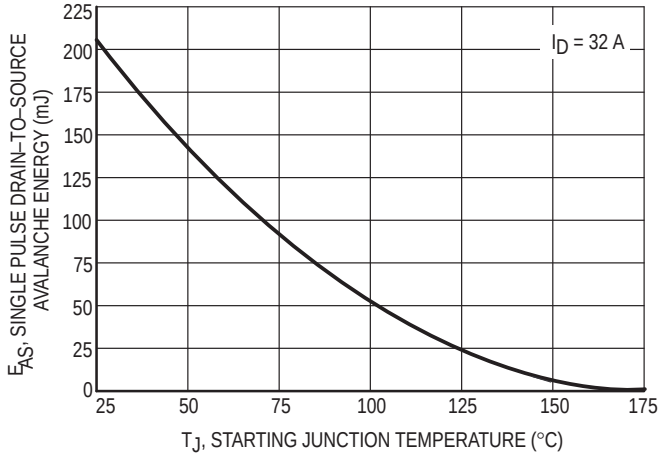


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

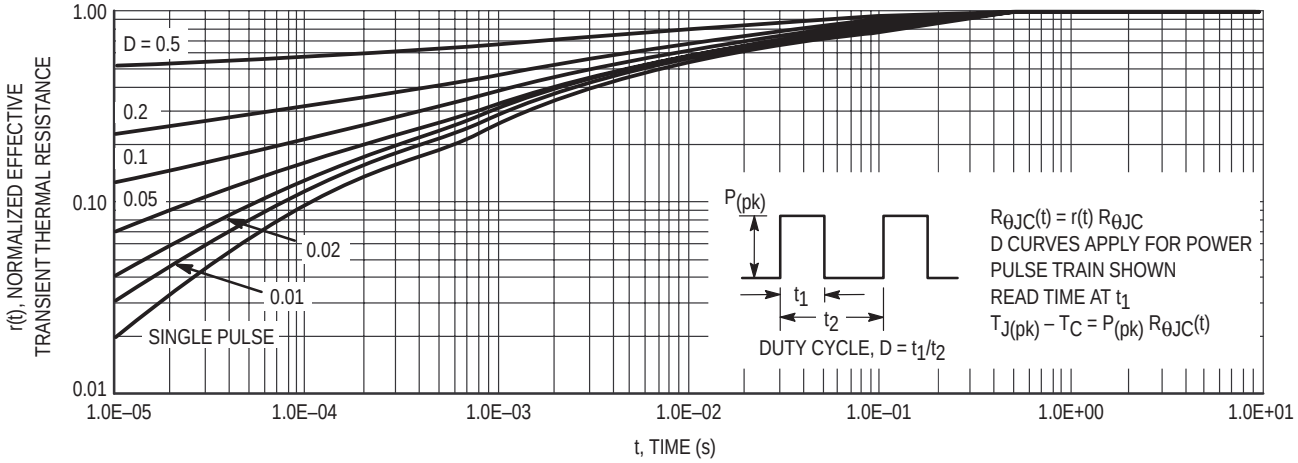


Figure 13. Thermal Response

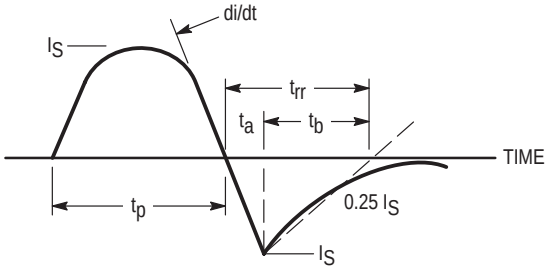


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

HDTMOS E-FET ™
Power Field Effect Transistor
P–Channel Enhancement–Mode Silicon Gate

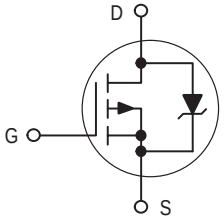
MTP50P03HDL

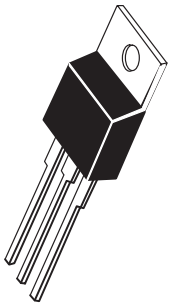
Motorola Preferred Device

TMOS POWER FET
LOGIC LEVEL
50 AMPERES
30 VOLTS
$R_{DS(on)}$ = 0.025 OHM

This advanced high–cell density HDTMOS power FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	30	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	50 31 150	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, Peak I_L = 50 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	1250	mJ
Thermal Resistance — Junction to Case — Junction to Ambient, when mounted with the minimum recommended pad size	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage ($C_{pk} \geq 2.0$) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			30	—	—	
Temperature Coefficient (Positive)			—	26	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 30 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 30 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current		I_{GSS}				nAdc
(V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)			—	—	100	
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($C_{pk} \geq 3.0$) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			1.0	1.5	2.0	
Threshold Temperature Coefficient (Negative)			—	4.0	—	mV/°C
Static Drain–to–Source On–Resistance ($C_{pk} \geq 3.0$) (3)		$R_{DS(on)}$				Ohm
(V_{GS} = 5.0 Vdc, I_D = 25 Adc)			—	0.020	0.025	
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 50 Adc)			—	0.83	1.5	
(I_D = 25 Adc, T_J = 125°C)			—	—	1.3	
Forward Transconductance		g_{FS}				mhos
(V_{DS} = 5.0 Vdc, I_D = 25 Adc)			15	20	—	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3500	4900	pF
Output Capacitance		C_{oss}	—	1550	2170	
Transfer Capacitance		C_{rss}	—	550	770	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 50 Adc, V_{GS} = 5.0 Vdc, R_G = 2.3 Ω)	$t_{d(on)}$	—	22	30	ns
Rise Time		t_r	—	340	466	
Turn–Off Delay Time		$t_{d(off)}$	—	90	117	
Fall Time		t_f	—	218	300	
Gate Charge (See Figure 8)	(V_{DS} = 24 Vdc, I_D = 50 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	74	100	nC
		Q_1	—	13.6	—	
		Q_2	—	44.8	—	
		Q_3	—	35	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S =50 Adc, V_{GS} = 0 Vdc)	V_{SD}				Vdc
	(I_S = 50 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	2.39	3.0	
			—	1.84	—	
Reverse Recovery Time (See Figure 15)	(I_S = 50 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	106	—	ns
		t_a	—	58	—	
		t_b	—	48	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.246	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance		L_S				nH
(Measured from the source lead 0.25″ from package to source bond pad)			—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

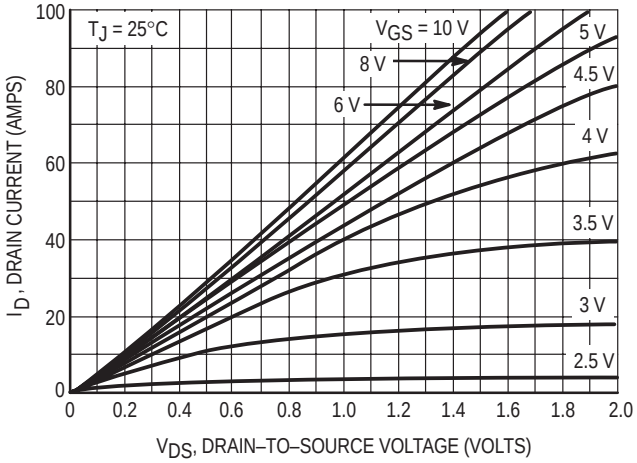


Figure 1. On–Region Characteristics

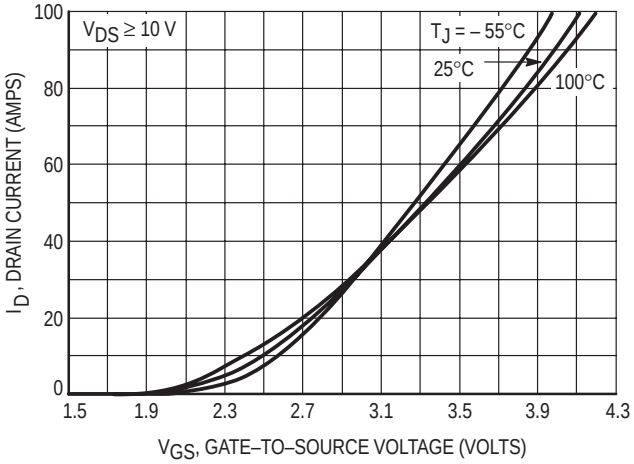


Figure 2. Transfer Characteristics

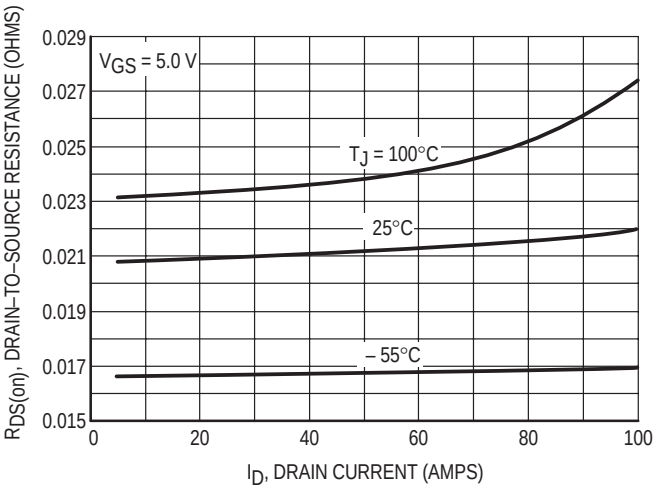


Figure 3. On–Resistance versus Drain Current and Temperature

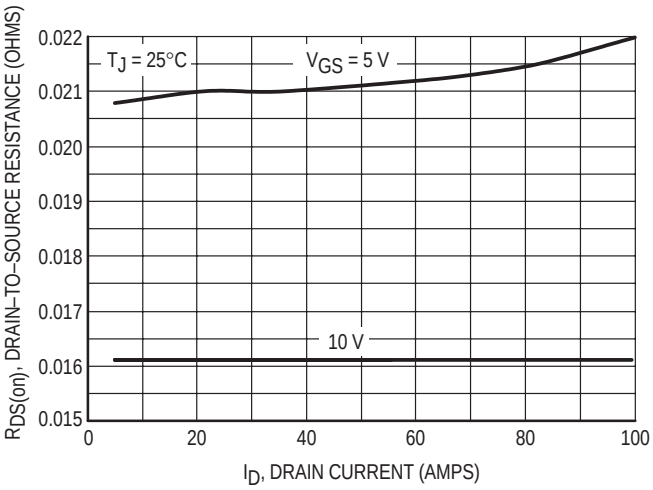


Figure 4. On–Resistance versus Drain Current and Gate Voltage

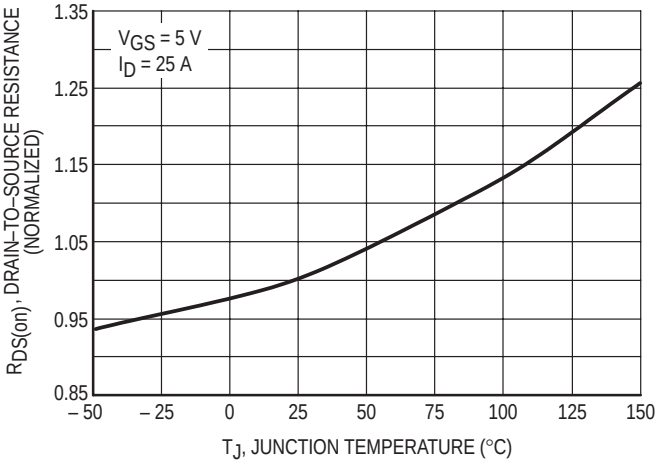


Figure 5. On–Resistance Variation with Temperature

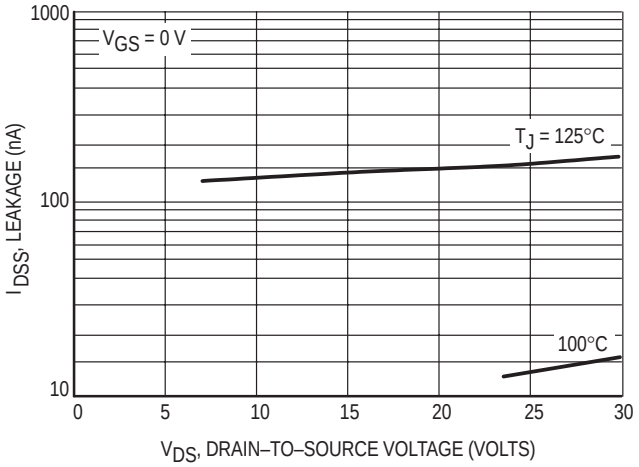


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

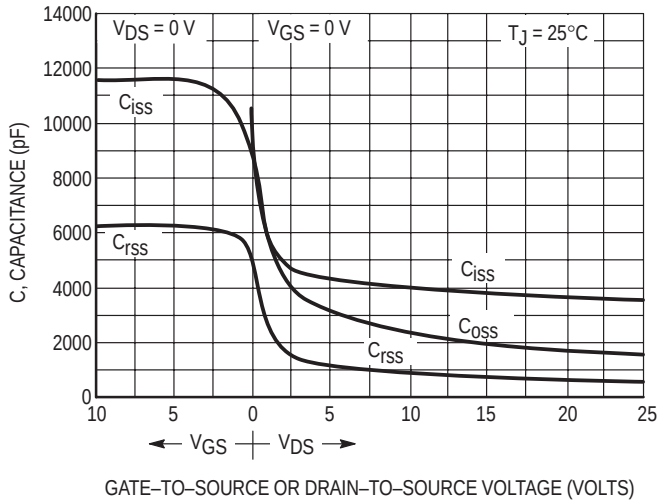


Figure 7. Capacitance Variation

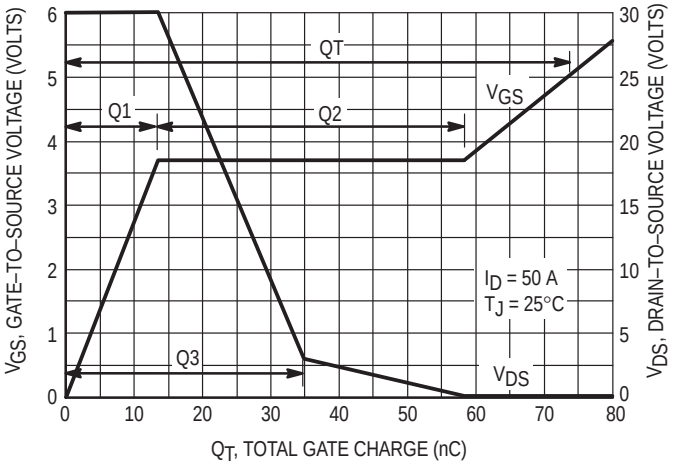


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

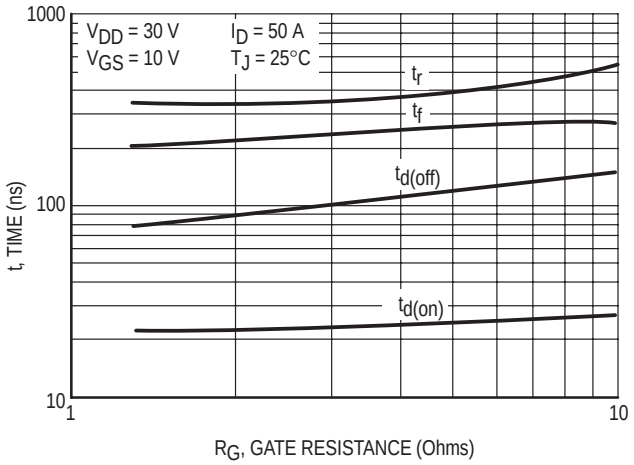


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

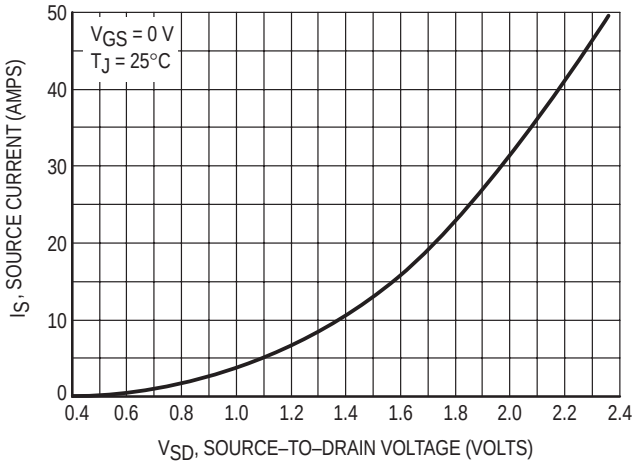


Figure 10. Diode Forward Voltage versus Current

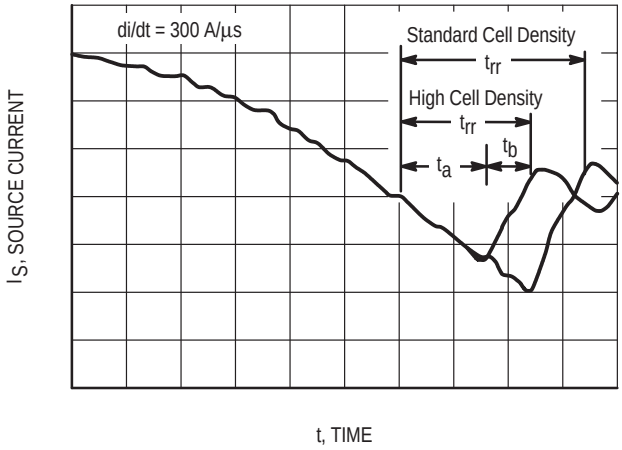


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance — General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

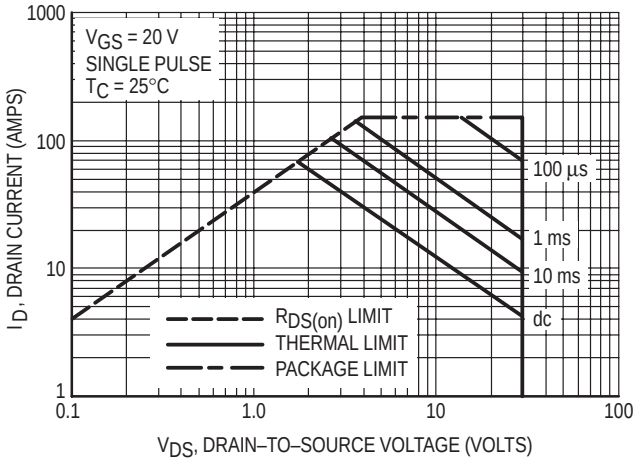


Figure 12. Maximum Rated Forward Biased Safe Operating Area

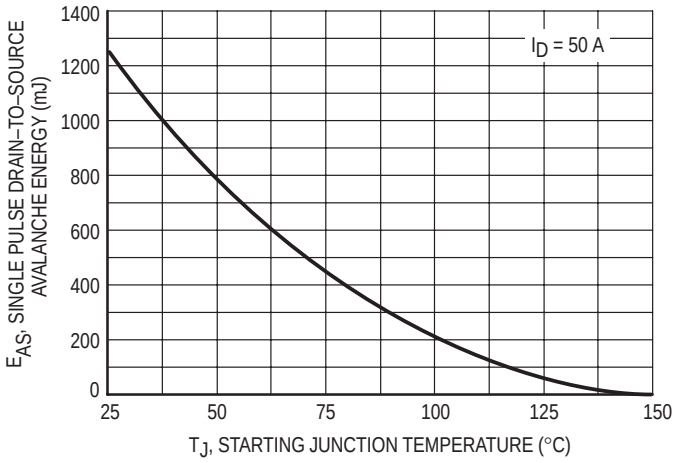


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

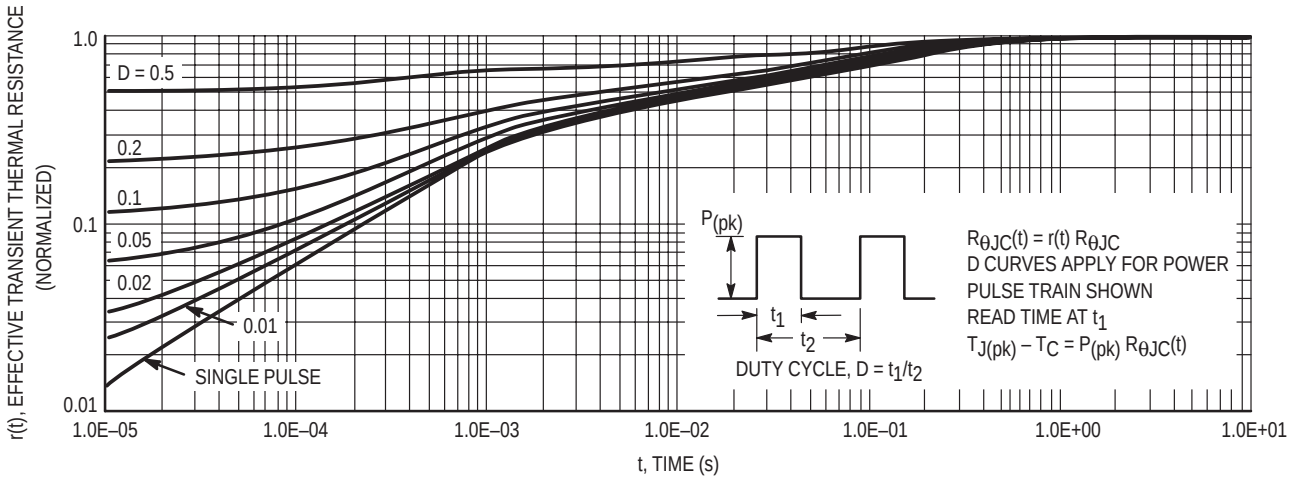


Figure 14. Thermal Response

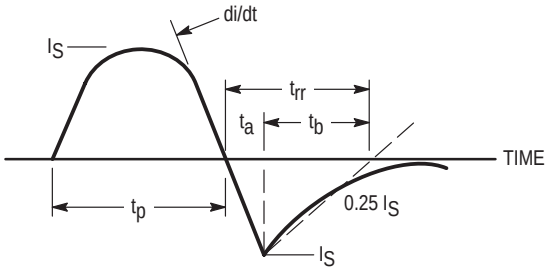


Figure 15. Diode Reverse Recovery Waveform

Product Preview

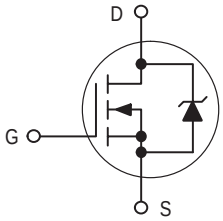
TMOS V™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

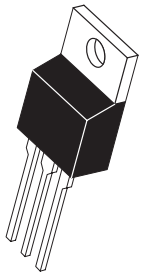
MTP52N06V

Motorola Preferred Device

TMOS POWER FET
52 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.022 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 221A–06, Style 5
TO–220AB

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	52 41 182	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	165 1.10	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 52 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	406	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.91 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 26 Adc)		$R_{DS(on)}$	—	0.019	0.022	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 52 Adc)		$V_{DS(on)}$	—	—	1.4	Vdc
(V_{GS} = 10 Vdc, I_D = 26 Adc, T_J = 150°C)			—	—	1.2	
Forward Transconductance (V_{DS} = 6.3 Vdc, I_D = 20 Adc)		g_{FS}	17	25	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1700	2380	pF
Output Capacitance		C_{oss}	—	500	700	
Reverse Transfer Capacitance		C_{rss}	—	150	300	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 52 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	15	30	ns
Rise Time		t_r	—	130	260	
Turn–Off Delay Time		$t_{d(off)}$	—	68	140	
Fall Time		t_f	—	70	140	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 52 Adc, V_{GS} = 10 Vdc)	Q_T	—	70	80	nC
		Q_1	—	10	—	
		Q_2	—	30	—	
		Q_3	—	20	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 52 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.5	Vdc
	(I_S = 52 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.9	—	
Reverse Recovery Time (See Figure 14)	(I_S = 52 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	90	—	ns
		t_a	—	80	—	
		t_b	—	10	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.3	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

Product Preview

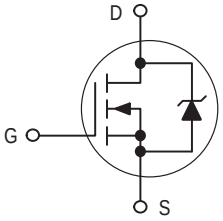
TMOS V™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

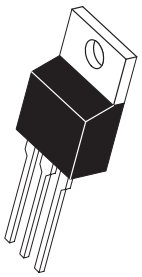
MTP52N06VL

Motorola Preferred Device

TMOS POWER FET
52 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.025 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





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Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 25	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	52 41 182	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	165 1.10	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5 Vdc, PEAK I_L = 52 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	406	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.91 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds	T_L	260	°C

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Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = .25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage		$V_{GS(th)}$				
(V_{DS} = V_{GS}, I_D = 250 μAdc)			1.0	1.5	2.0	Vdc
Threshold Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 5 Vdc, I_D = 26 Adc)		$R_{DS(on)}$	—	0.022	0.025	Ohm
Drain–to–Source On–Voltage		$V_{DS(on)}$				Vdc
(V_{GS} = 5 Vdc, I_D = 52 Adc)			—	—	1.5	
(V_{GS} = 5 Vdc, I_D = 26 Adc, T_J = 150°C)			—	—	1.3	
Forward Transconductance (V_{DS} = 6.3 Vdc, I_D = 20 Adc)		g_{FS}	17	30	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1600	2240	pF
Output Capacitance		C_{oss}	—	550	770	
Transfer Capacitance		C_{rss}	—	170	340	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 52 Adc, V_{GS} = 5 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	18	40	ns
Rise Time		t_r	—	370	740	
Turn–Off Delay Time		$t_{d(off)}$	—	90	180	
Fall Time		t_f	—	170	340	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 52 Adc, V_{GS} = 5 Vdc)	Q_T	—	45	60	nC
		Q_1	—	12	—	
		Q_2	—	22	—	
		Q_3	—	18	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 52 Adc, V_{GS} = 0 Vdc)	V_{SD}				Vdc
	(I_S = 52 Adc, V_{GS} = 0 Vdc, T_J = 150 °C)		—	1.0	1.5	
			—	0.9	—	
Reverse Recovery Time	(I_S = 52 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	93	—	ns
		t_a	—	65	—	
		t_b	—	28	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.3	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance		L_S				nH
(Measured from the source lead 0.25″ from package to source bond pad)			—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

Product Preview

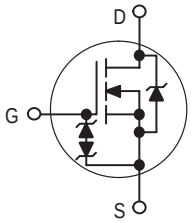
TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

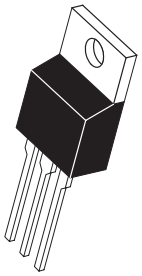
MTP55N06Z

TMOS POWER FET
55 AMPERES
60 VOLTS
$R_{DS(on)}$ = 16 mΩ

This advanced high voltage TMOS E–FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor–Absorbs High Energy in the Avalanche Mode
- ESD Protected. 400 V Machine Model Level and 4000 V Human Body Model Level.





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±30	Vdc Vpk
Drain Current — Continuous @ T_C = 25°C — Continuous @ T_C = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	55 35.5 165	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	136 0.91	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{DS} = 60 Vdc, V_{GS} = 10 Vdc, Peak I_L = 55 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	454	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.1 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 —	 — 53	 — —	 Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	5.0	μAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 2.0 —	 3.0 6.0	 4.0 —	 Vdc mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (V_{GS} = 10 Vdc, I_D = 15 Adc)		$R_{DS(on)}$	—	14	16	mΩ
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 30 Adc) (I_D = 15 Adc, T_J = 125°C)		$V_{DS(on)}$	 — —	 0.825 0.74	 1.2 1.0	Vdc
Forward Transconductance (V_{DS} = 4.0 Vdc, I_D = 15 Adc)		g_{FS}	12	15	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1390	1950	pF
Output Capacitance		C_{oss}	—	520	730	
Transfer Capacitance		C_{rss}	—	119	238	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 30 Adc, $V_{GS(on)}$ = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	27	54	ns
Rise Time		t_r	—	157	314	
Turn–Off Delay Time		$t_{d(off)}$	—	116	232	
Fall Time		t_f	—	126	252	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 30 Adc, V_{GS} = 10 Vdc)	Q_T	—	40	56	nC
		Q_1	—	7.0	—	
		Q_2	—	18	—	
		Q_3	—	15	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 30 Adc, V_{GS} = 0 Vdc) (I_S = 30 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 0.93 0.82	 1.1 —	Vdc
Reverse Recovery Time	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	57	—	ns
		t_a	—	32	—	
		t_b	—	25	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.11	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from drain lead 0.25″ from package to center of die)		L_D	 —	 3.5 4.5	 —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

Designer's™ Data Sheet

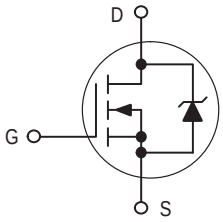
HDTMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

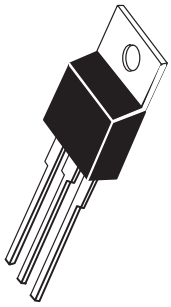
MTP60N06HD
Motorola Preferred Device

TMOS POWER FET
60 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.014 OHM

This advanced high–cell density HDTMOS power FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 30	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	60 42.3 180	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 60 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	540	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage ($C_{pk} \geq 2.0$) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			60	—	—	
Temperature Coefficient (Positive)			—	71	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current		I_{GSS}				nAdc
(V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)			—	—	100	
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($C_{pk} \geq 3.0$) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			2.0	3.0	4.0	
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance ($C_{pk} \geq 3.0$) (3)		$R_{DS(on)}$				Ohm
(V_{GS} = 10 Vdc, I_D = 30 Adc)			—	0.011	0.014	
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 60 Adc)			—	—	1.0	
(I_D = 30 Adc, T_J = 125°C)			—	—	0.9	
Forward Transconductance		g_{FS}				mhos
(V_{DS} = 5.0 Vdc, I_D = 30 Adc)			15	20	—	
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	1950	2800	pF
Output Capacitance		C_{oss}	—	660	924	
Transfer Capacitance		C_{rss}	—	147	300	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 60 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	14	26	ns
Rise Time		t_r	—	197	394	
Turn–Off Delay Time		$t_{d(off)}$	—	50	102	
Fall Time		t_f	—	124	246	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 60 Adc, V_{GS} = 10 Vdc)	Q_T	—	51	71	nC
		Q_1	—	12	—	
		Q_2	—	24	—	
		Q_3	—	21	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 60 Adc, V_{GS} = 0 Vdc)	V_{SD}				Vdc
	(I_S = 60 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.99	1.2	
			—	0.89	—	
Reverse Recovery Time (See Figure 15)	(I_S = 60 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	60	—	ns
		t_a	—	36	—	
		t_b	—	24	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.143	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance		L_S				nH
(Measured from the source lead 0.25″ from package to source bond pad)			—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

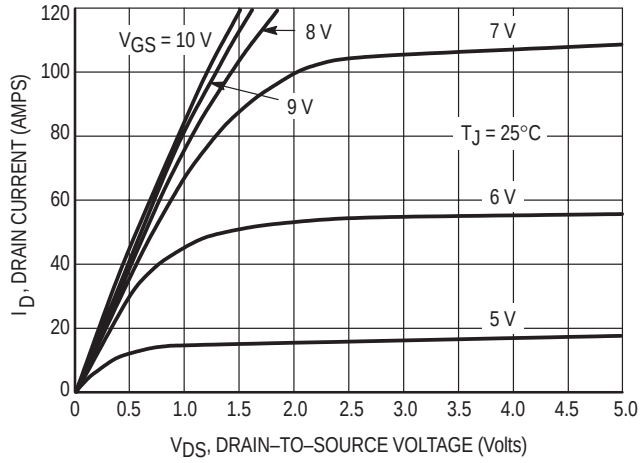


Figure 1. On–Region Characteristics

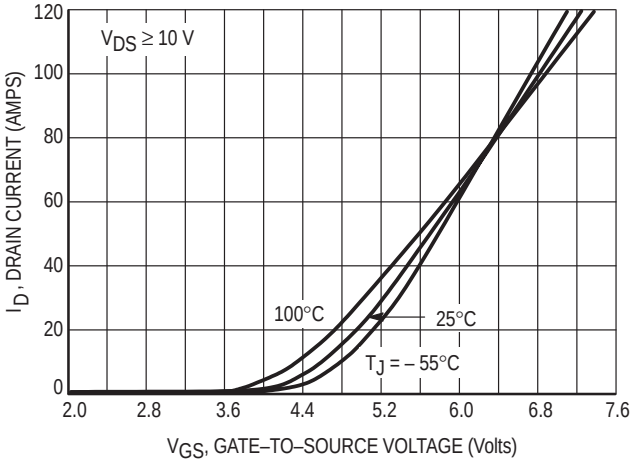


Figure 2. Transfer Characteristics

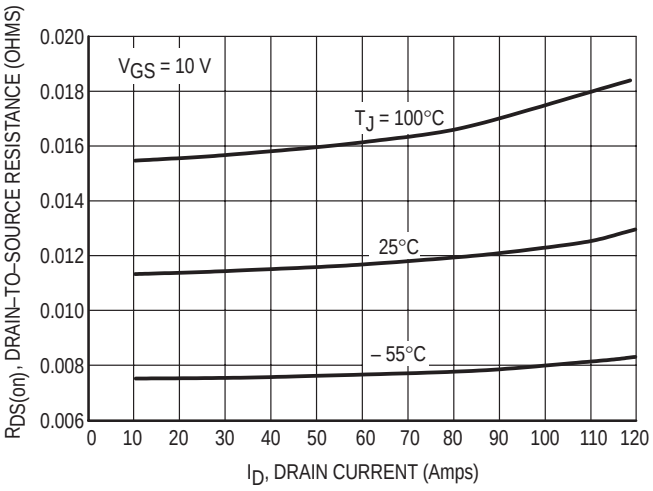


Figure 3. On–Resistance versus Drain Current and Temperature

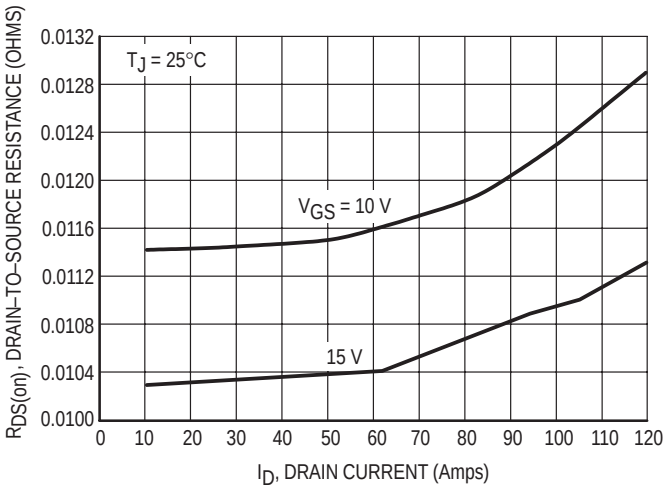


Figure 4. On–Resistance versus Drain Current and Gate Voltage

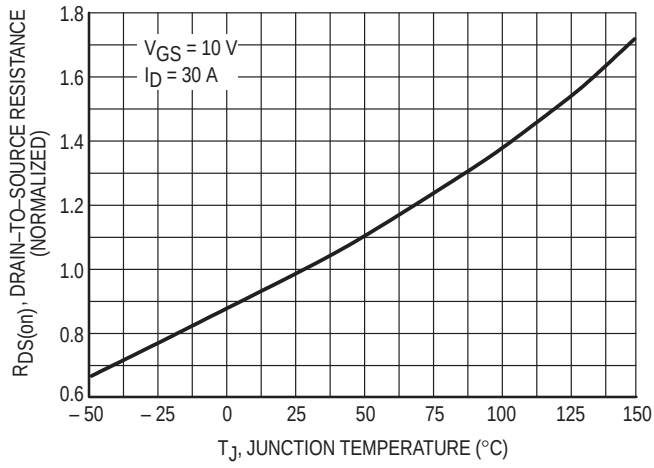


Figure 5. On–Resistance Variation with Temperature

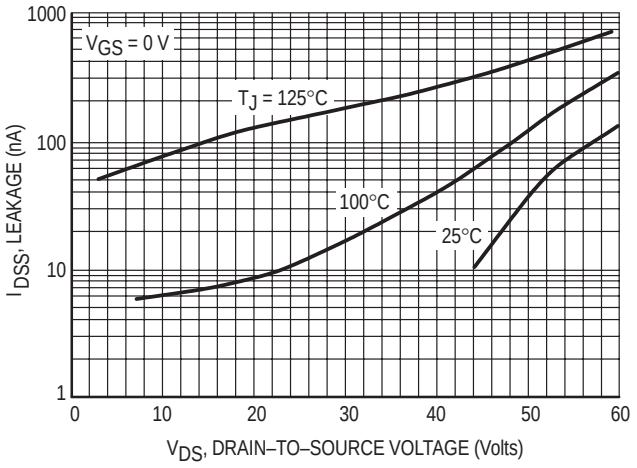


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

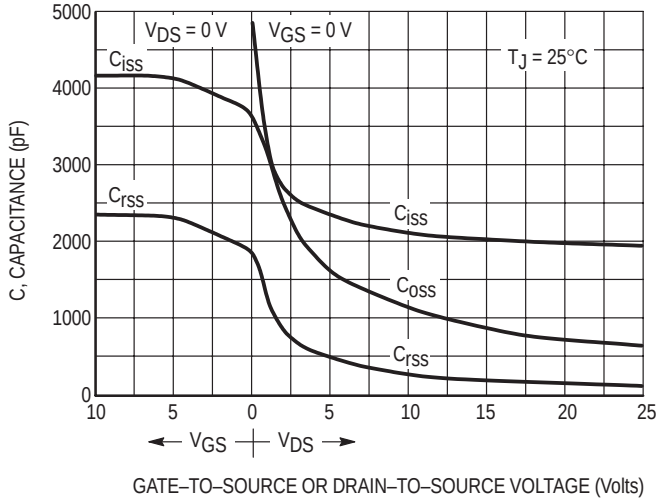


Figure 7. Capacitance Variation

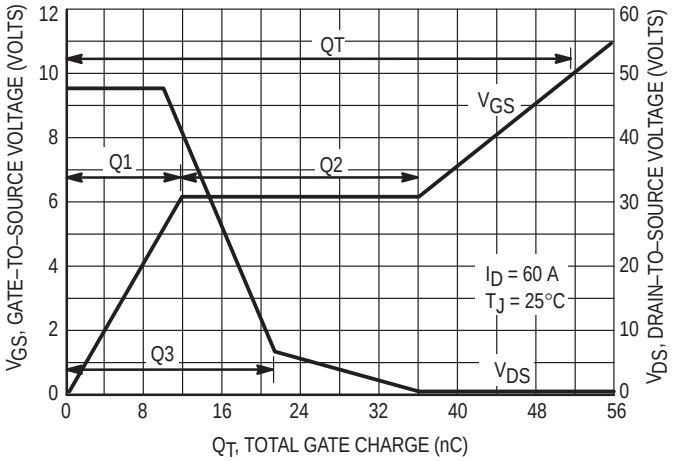


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

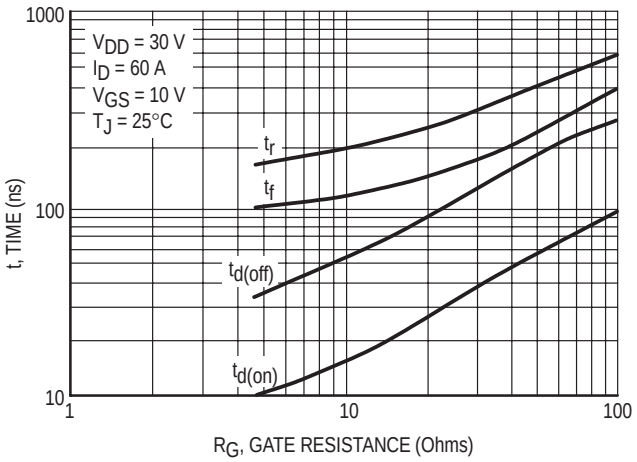


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

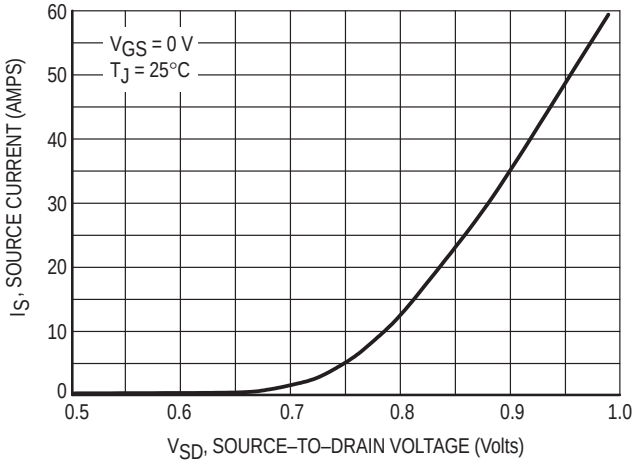


Figure 10. Diode Forward Voltage versus Current

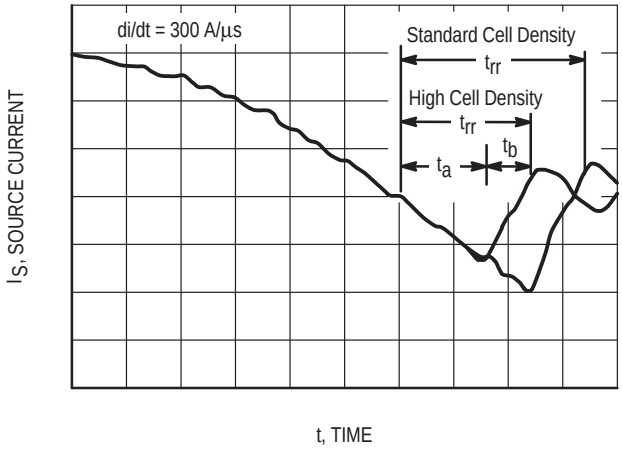


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

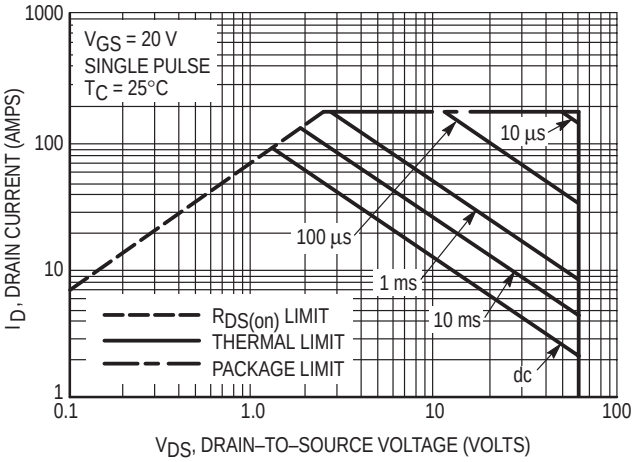


Figure 12. Maximum Rated Forward Biased Safe Operating Area

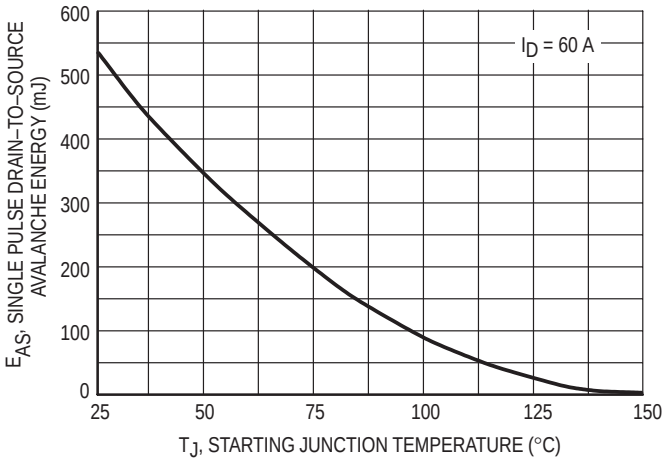


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

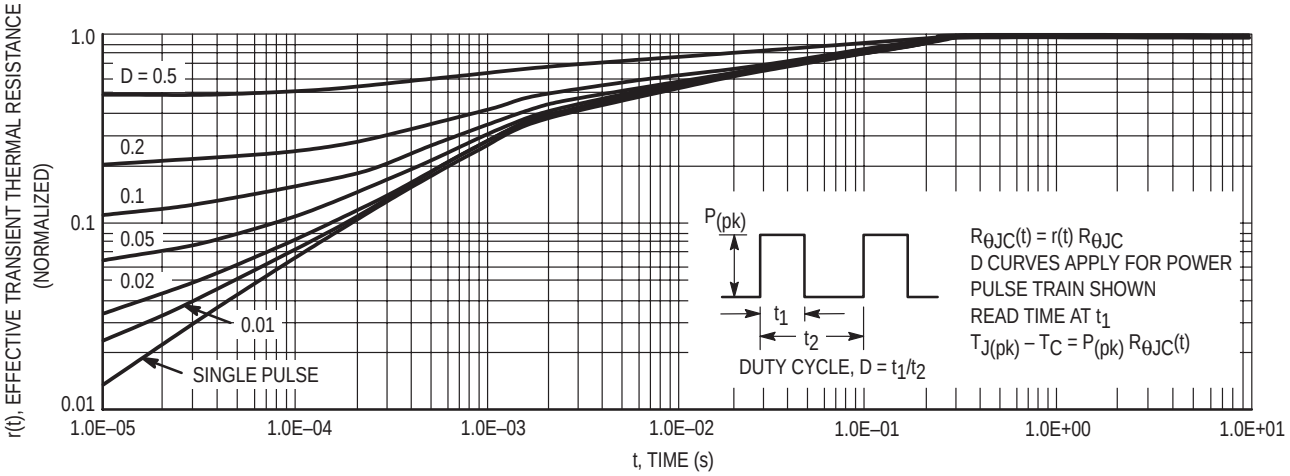


Figure 14. Thermal Response

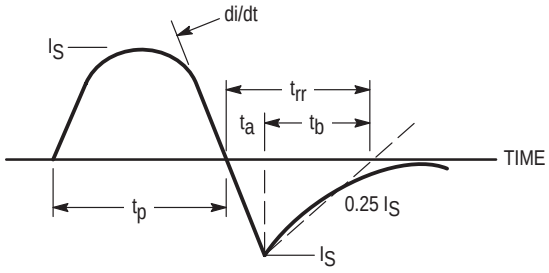


Figure 15. Diode Reverse Recovery Waveform

Advanced Information

HDTMOS E-FET™
High Density Power FET
N–Channel Enhancement–Mode Silicon Gate

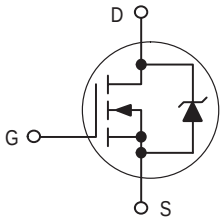
MTP75N03HDL

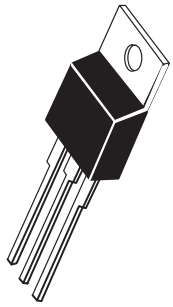
Motorola Preferred Device

TMOS POWER FET
LOGIC LEVEL
75 AMPERES
$R_{DS(on)}$ = 9.0 mOHM
25 VOLTS

This advanced high–cell density HDTMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low–voltage, high–speed switching applications in power supplies, converters and PWM motor controls, and inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched, and to offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$, High–Cell Density, HDTMOS
- SPICE Parameters Available
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Avalanche Energy Specified





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	25	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	25	Vdc
Gate–Source Voltage — Continuous — Single Pulse ($t_p \le 10$ ms)	V_{GS}	± 15 ± 20	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	75 59 225	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 75 Apk, L = 0.1 mH, R_G = 25 Ω)	E_{AS}	280	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage ($C_{pk} \geq 2.0$) (3) (V_{GS} = 0 Vdc, I_D = 0.25 mA)		$V_{(BR)DSS}$	25	—	—	Vdc
Temperature Coefficient (Positive)						mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	100	μAdc
(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	500	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 V)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($C_{pk} \geq 3.0$) (3) (V_{DS} = V_{GS}, I_D = 0.25 mA)		$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Temperature Coefficient (Negative)						mV/°C
Static Drain–Source On–Resistance ($C_{pk} \geq 2.0$) (3) (V_{GS} = 5.0 Vdc, I_D = 37.5 Adc)		$R_{DS(on)}$	—	6.0	9.0	mΩ
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 75 Adc)		$V_{DS(on)}$	—		0.68	Vdc
(I_D = 37.5 Adc, T_J = 125°C)			—	—	0.6	
Forward Transconductance (V_{DS} = 3.0 Vdc, I_D = 20 Adc)		g_{FS}	15	55	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	4025	5635	pF
Output Capacitance		C_{oss}	—	1353	1894	
Reverse Transfer Capacitance		C_{rss}	—	307	430	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DS} = 15 Vdc, I_D = 75 Adc, V_{GS} = 5.0 Vdc, R_g = 4.7 Ω)	$t_{d(on)}$	—	24	48	ns
Rise Time		t_r	—	493	986	
Turn–Off Delay Time		$t_{d(off)}$	—	60	120	
Fall Time		t_f	—	149	300	
Gate Charge	(V_{DS} = 24 Vdc, I_D = 75 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	61	122	nC
		Q_1	—	14	28	
		Q_2	—	33	66	
		Q_3	—	27	54	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 75 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.97	1.1	Vdc
	(I_S = 75 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.87	—	
Reverse Recovery Time	(I_S = 75 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	58	—	ns
		t_a	—	27	—	
		t_b	—	30	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.088	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

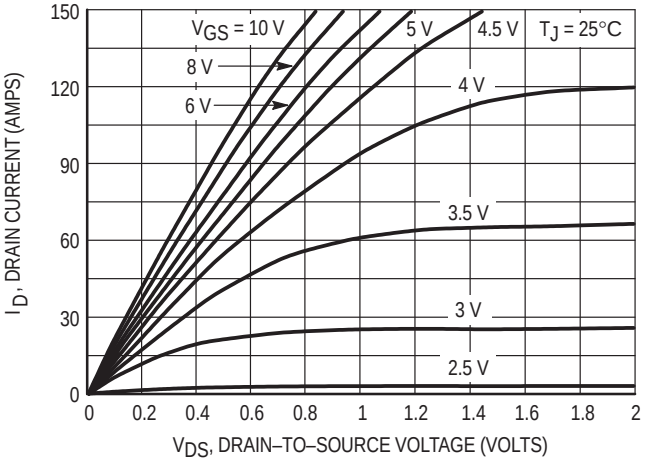


Figure 1. On–Region Characteristics

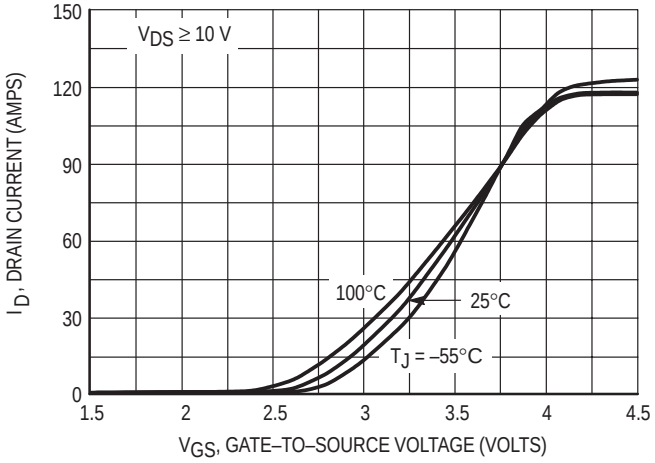


Figure 2. Transfer Characteristics

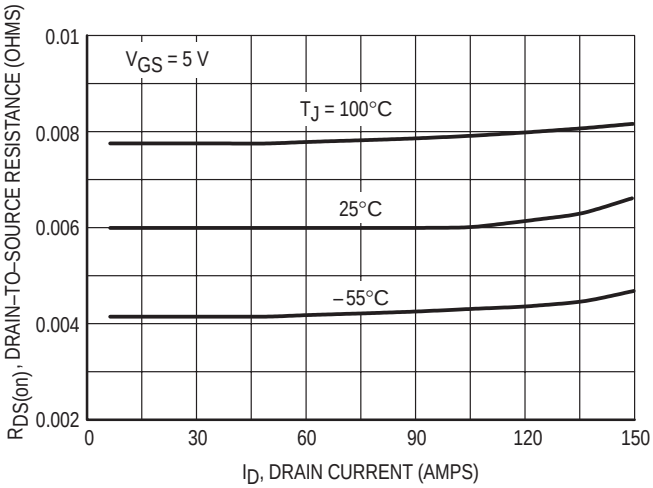


Figure 3. On–Resistance versus Drain Current and Temperature

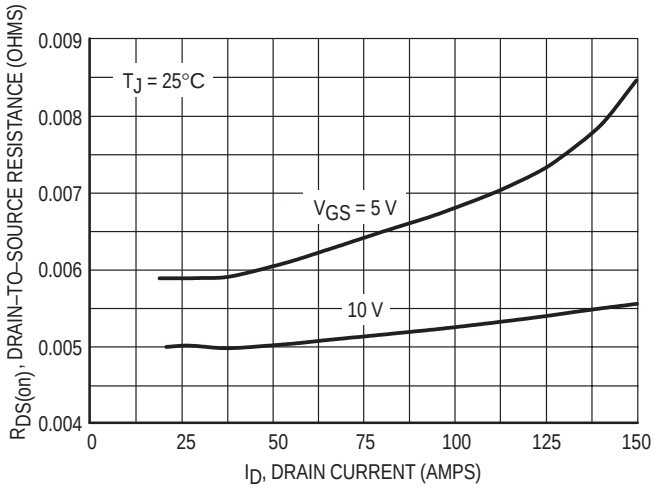


Figure 4. On–Resistance versus Drain Current and Gate Voltage

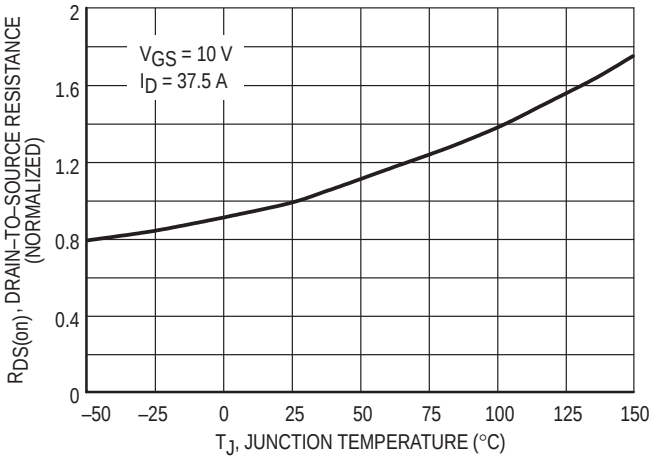


Figure 5. On–Resistance Variation with Temperature

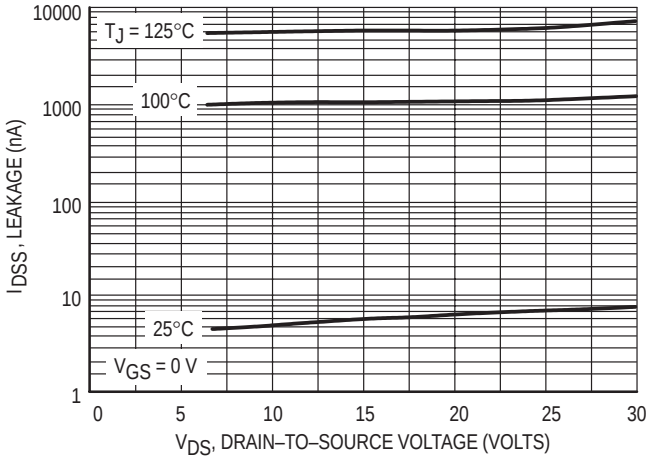


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

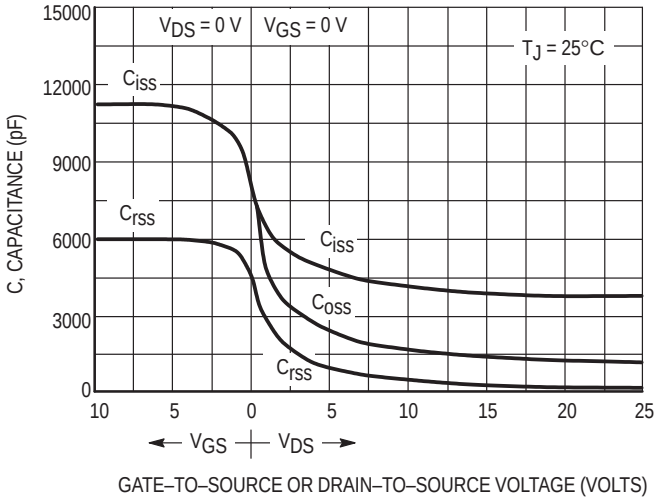


Figure 7. Capacitance Variation

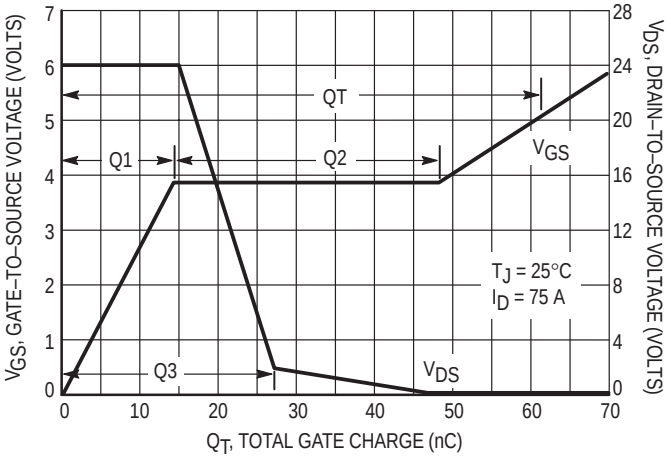


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

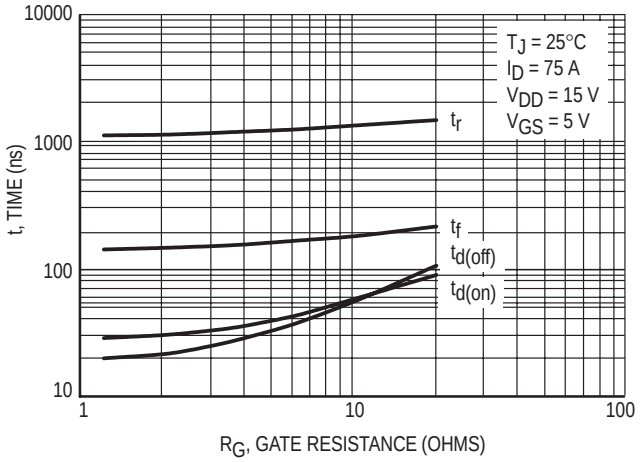


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

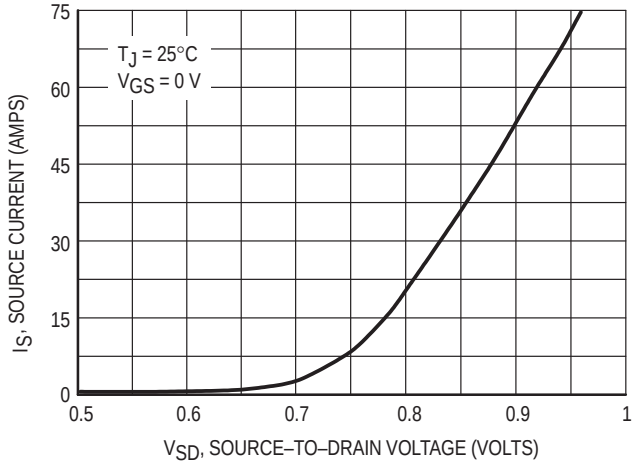


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (VDSS) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

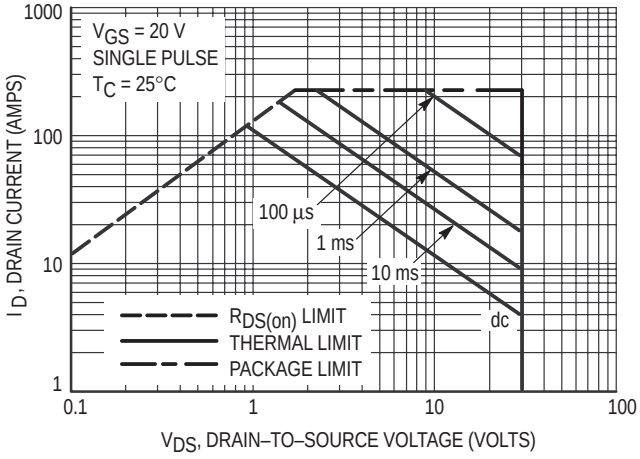


Figure 11. Maximum Rated Forward Biased Safe Operating Area

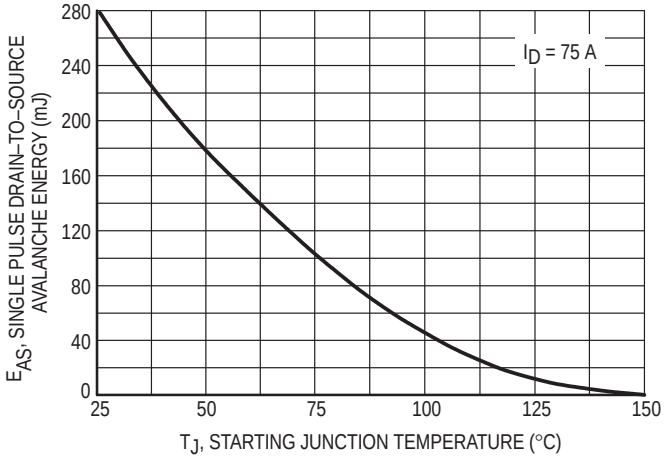


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

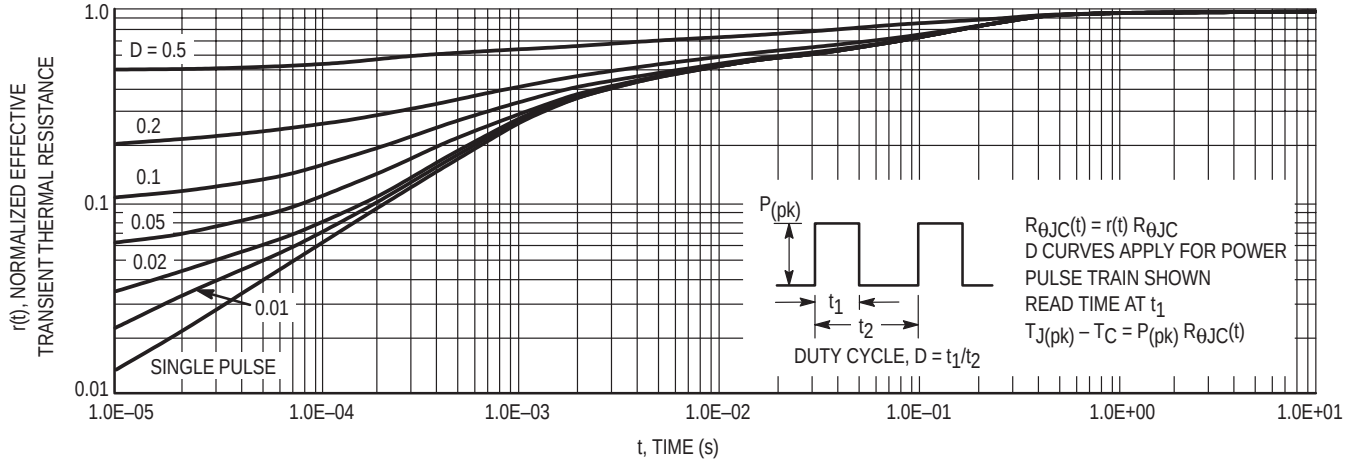


Figure 13. Thermal Response

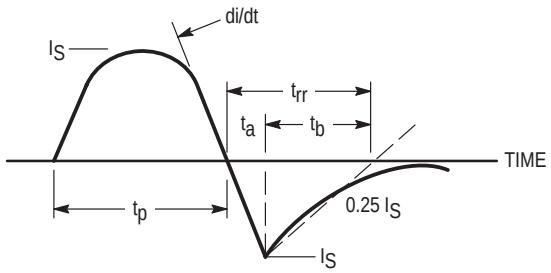


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

HDTMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

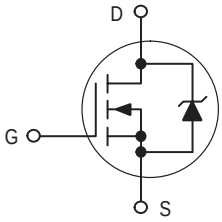
MTP75N05HD

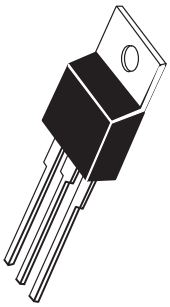
Motorola Preferred Device

TMOS POWER FET
75 AMPERES
$R_{DS(on)}$ = 9.5 mΩ
50 VOLTS

This advanced high–cell density HDTMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. This new energy–efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low–voltage, high–speed switching applications in power supplies, converters and PWM motor controls, and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched, and to offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$, High–Cell Density, HDTMOS
- SPICE Parameters Available
- Diode is Characterized for Use in Bridge Circuits
- Diode Exhibits High Speed, Yet Soft Recovery
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Avalanche Energy Specified





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	50	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	50	Vdc
Gate–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	75 65 225	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	150 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vpk, I_L = 75 Apk, L = 0.177 mH, R_G = 25 Ω)	E_{AS}	500	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.00 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage ($C_{pk} \geq 2.0$)(3)		$V_{(BR)DSS}$				
(V_{GS} = 0 V, I_D = 250 μAdc)			50	—	—	Vdc
Temperature Coefficient (Positive)			—	54.9	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 50 Vdc, V_{GS} = 0)			—	—	10	
(V_{DS} = 50 Vdc, V_{GS} = 0, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage ($C_{pk} \geq 1.5$)(3)		$V_{GS(th)}$				
(V_{DS} = V_{GS}, I_D = 250 μAdc)			2.0	—	4.0	Vdc
Temperature Coefficient (Negative)			—	6.3	—	mV/°C
Static Drain–Source On–Resistance ($C_{pk} \geq 3.0$)(3)		$R_{DS(on)}$				mW
(V_{GS} = 10 Vdc, I_D = 37.5 Adc)			—	7.0	9.5	
Drain–Source On–Voltage (V_{GS} = 10 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 75 Adc)			—	—	0.86	
(I_D = 37.5 Adc, T_J = 150°C)			—	—	0.64	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 20 Adc)		g_{FS}	15	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz) ($C_{pk} \geq 2.0$)(2)	C_{iss}	—	2600	2900	pF
Output Capacitance		C_{oss}	—	1000	1100	
Transfer Capacitance		C_{rss}	—	230	275	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DD} = 25 Vdc, I_D = 75 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	15	30	ns
Rise Time		t_r	—	170	340	
Turn–Off Delay Time		$t_{d(off)}$	—	70	140	
Fall Time		t_f	—	100	200	
Gate Charge	(V_{DS} = 40 Vdc, I_D = 75 Adc, V_{GS} = 10 Vdc)	Q_T	—	71	100	nC
		Q_1	—	13	—	
		Q_2	—	33	—	
		Q_3	—	26	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 75 Adc, V_{GS} = 0)	V_{SD}				Vdc
	(I_S = 75 Adc, V_{GS} = 0, T_J = 150°C)		—	0.97	1.1	
	($C_{pk} \geq 10$)(2)		—	0.88	—	
Reverse Recovery Time	(I_S = 37.5 Adc, V_{GS} = 0, dI_S/dt = 100 A/μs)	t_{rr}	—	57	—	ns
		t_a	—	40	—	
		t_b	—	17	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.17	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance		L_S				nH
(Measured from the source lead 0.25″ from package to source bond pad)			—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS(1)

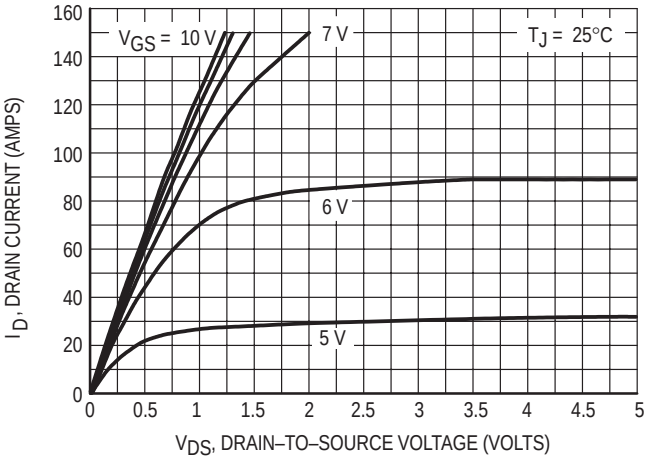


Figure 1. On–Region Characteristics

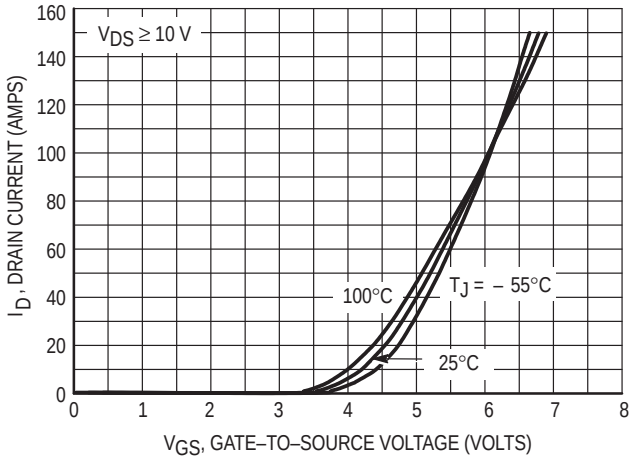


Figure 2. Transfer Characteristics

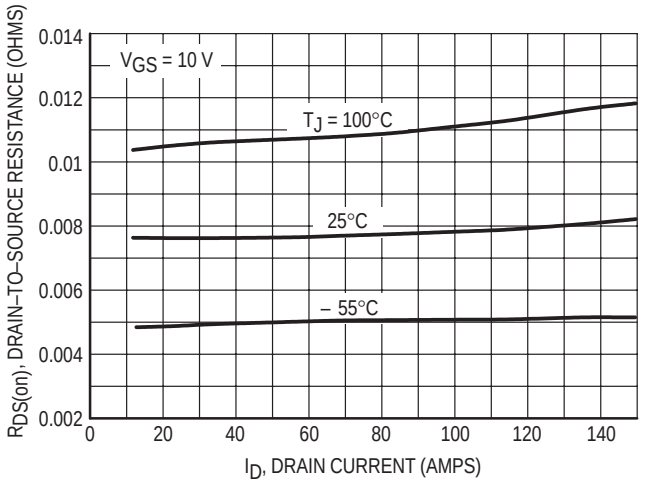


Figure 3. On–Resistance versus Drain Current and Temperature

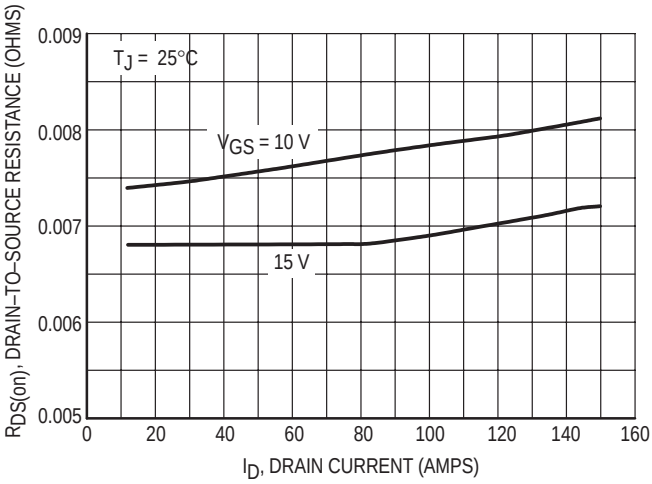


Figure 4. On–Resistance versus Drain Current and Gate Voltage

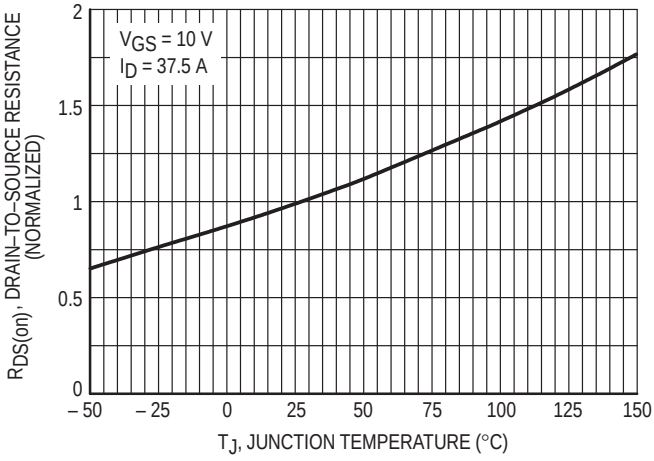


Figure 5. On–Resistance Variation with Temperature

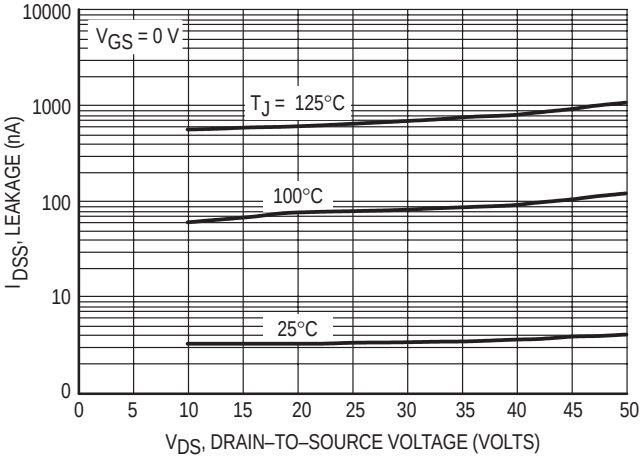


Figure 6. Drain–To–Source Leakage Current versus Voltage

(1)Pulse Tests: Pulse Width ≤ 250 μs, Duty Cycle ≤ 2%.

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board–mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

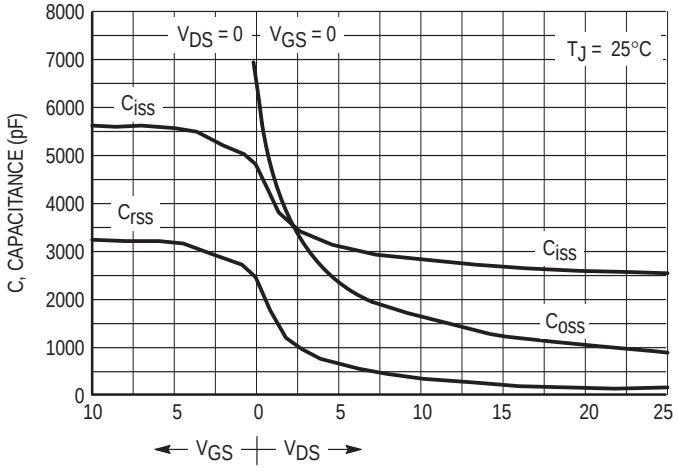


Figure 7. Capacitance Variation

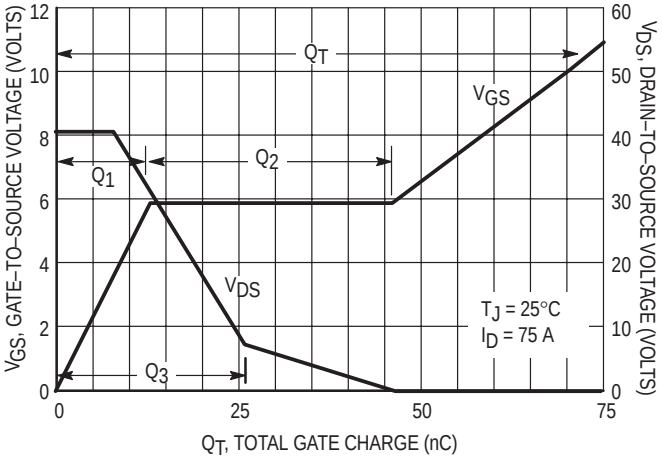


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

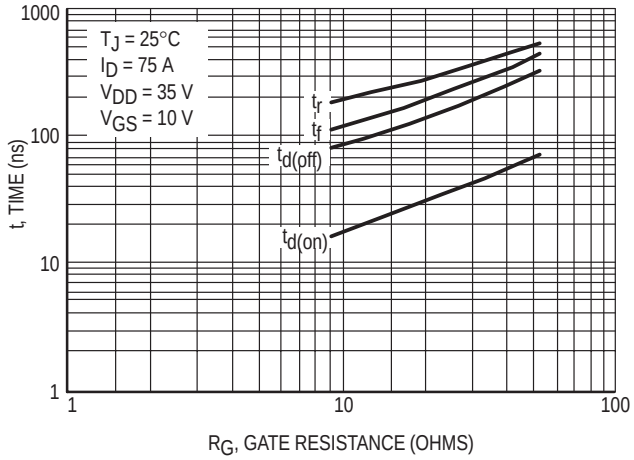


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

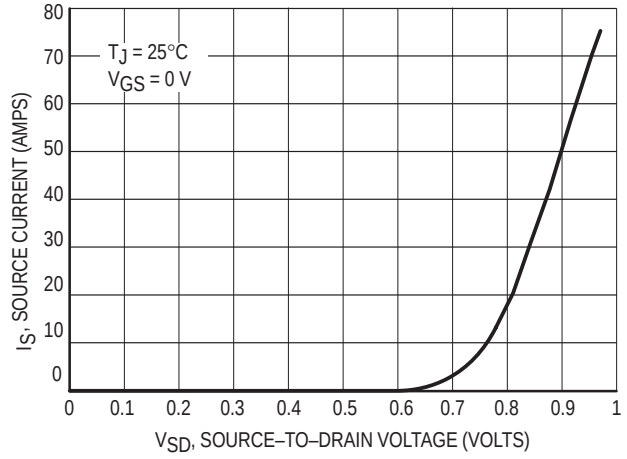


Figure 10. Diode Forward Voltage versus Current

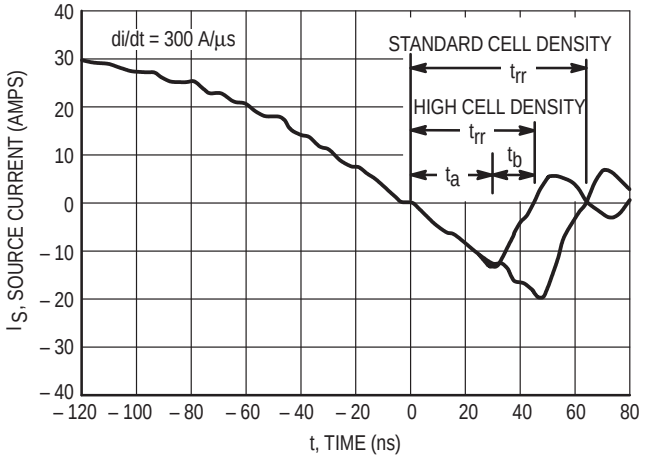


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r,t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

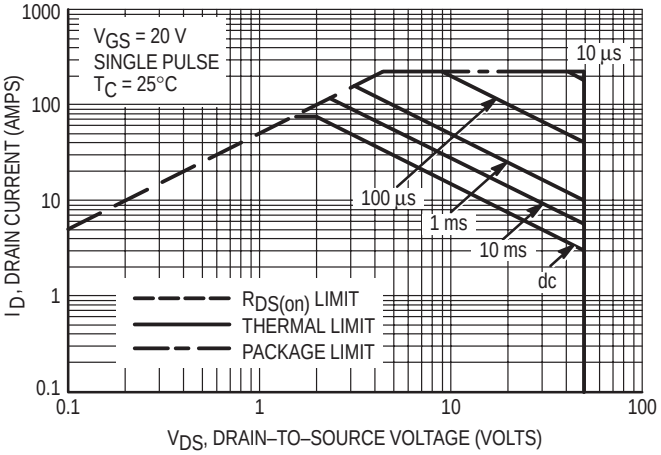


Figure 12. Maximum Rated Forward Biased Safe Operating Area

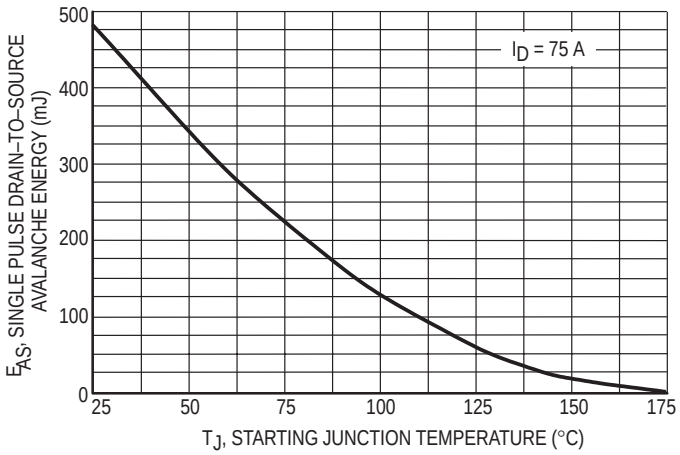


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

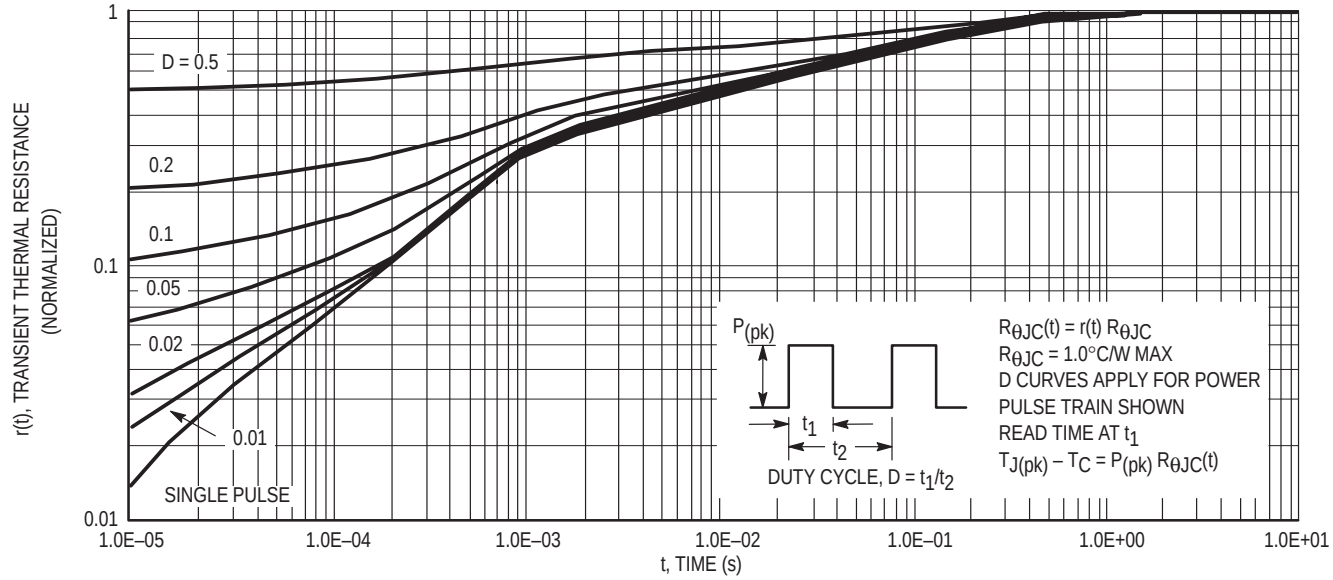


Figure 14. Thermal Response

Designer's™ Data Sheet

HDTMOS E-FET™
High Density Power FET
N–Channel Enhancement–Mode Silicon Gate

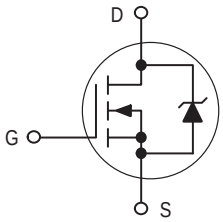
MTP75N06HD

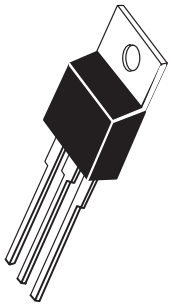
Motorola Preferred Device

TMOS POWER FET
75 AMPERES
$R_{DS(on)}$ = 10.0 mOHM
60 VOLTS

This advanced high–cell density HDTMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low–voltage, high–speed switching applications in power supplies, converters and PWM motor controls, and inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched, and to offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$, High–Cell Density, HDTMOS
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Avalanche Energy Specified





CASE 221A–06, Style 5
TO–220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Single Pulse	V_{GS}	± 20 ± 30	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	75 50 225	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 75 Apk, L = 0.177 mH, R_G = 25 Ω)	E_{AS}	500	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage ($C_{pk} \geq 2.0$) (3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 —	 68 60.4	 — —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	 — —	 — —	 10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 V)		I_{GSS}	—	5.0	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage ($C_{pk} \geq 5.0$) (3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	 2.0 —	 3.0 8.38	 4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance ($C_{pk} \geq 2.0$) (3) (V_{GS} = 10 Vdc, I_D = 37.5 Adc)		$R_{DS(on)}$	 —	 8.3	 10	mΩ
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 75 Adc) (I_D = 37.5 Adc, T_J = 125°C)		$V_{DS(on)}$	 — —	 0.7 0.53	 0.9 0.8	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 37.5 Adc)		g_{FS}	15	32	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	2800	3920	pF
Output Capacitance		C_{oss}	—	928	1300	
Reverse Transfer Capacitance		C_{rss}	—	180	252	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DS} = 30 Vdc, I_D = 75 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	18	26	ns
Rise Time		t_r	—	218	306	
Turn–Off Delay Time		$t_{d(off)}$	—	67	94	
Fall Time		t_f	—	125	175	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 75 Adc, V_{GS} = 10 Vdc)	Q_T	—	71	100	nC
		Q_1	—	16.3	—	
		Q_2	—	31	—	
		Q_3	—	29.4	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 75 Adc, V_{GS} = 0 Vdc) (I_S = 75 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	 — —	 0.97 0.88	 1.1 —	Vdc
Reverse Recovery Time	(I_S = 75 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	56	—	ns
		t_a	—	44	—	
		t_b	—	12	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.103	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	3.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

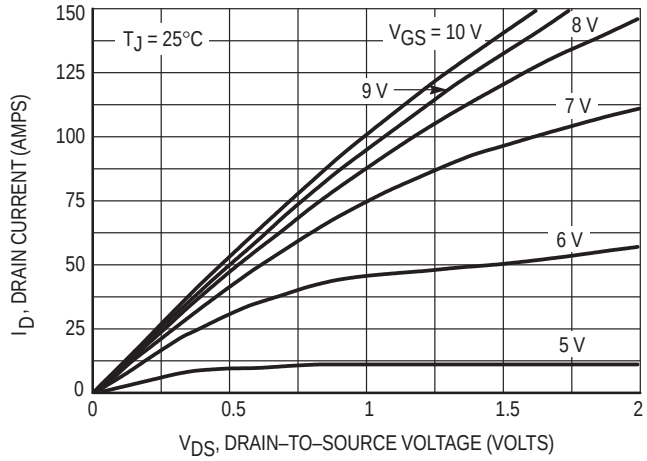


Figure 1. On–Region Characteristics

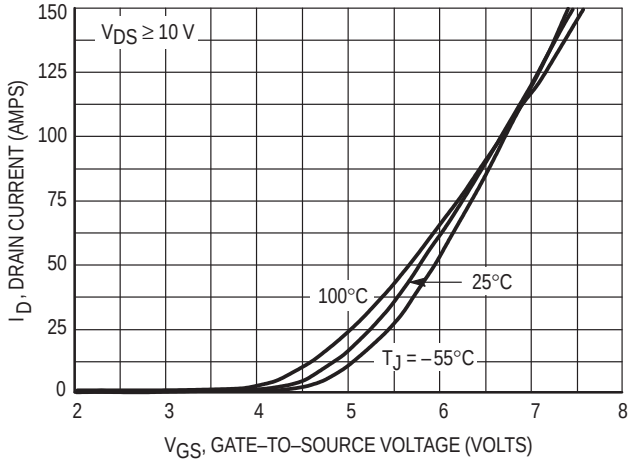


Figure 2. Transfer Characteristics

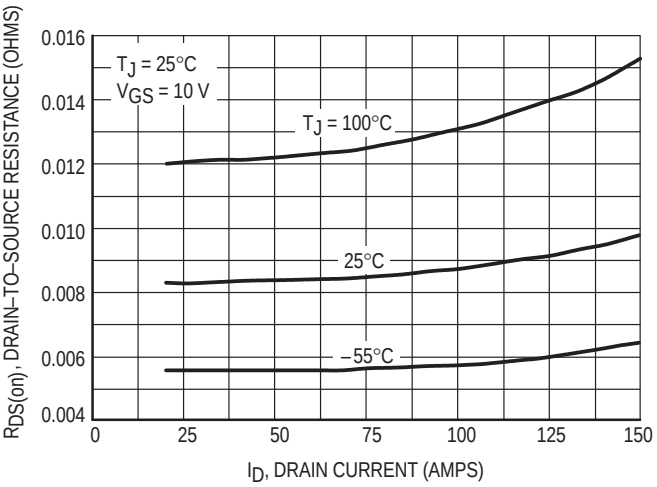


Figure 3. On–Resistance versus Drain Current and Temperature

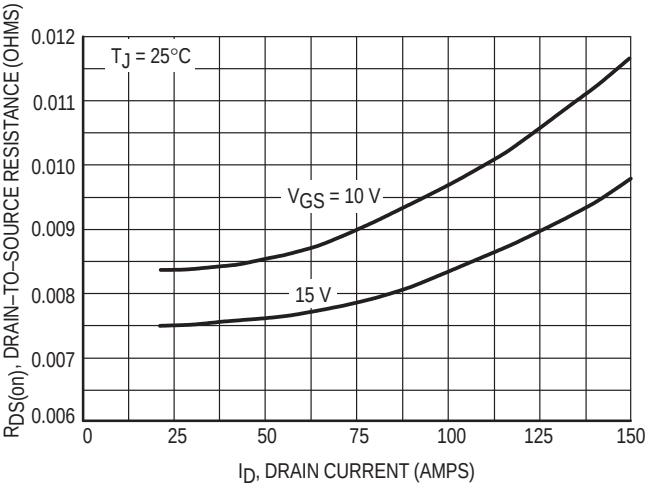


Figure 4. On–Resistance versus Drain Current and Gate Voltage

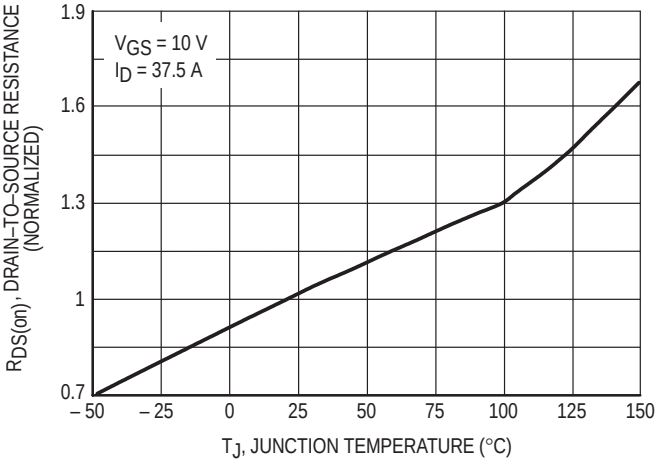


Figure 5. On–Resistance Variation with Temperature

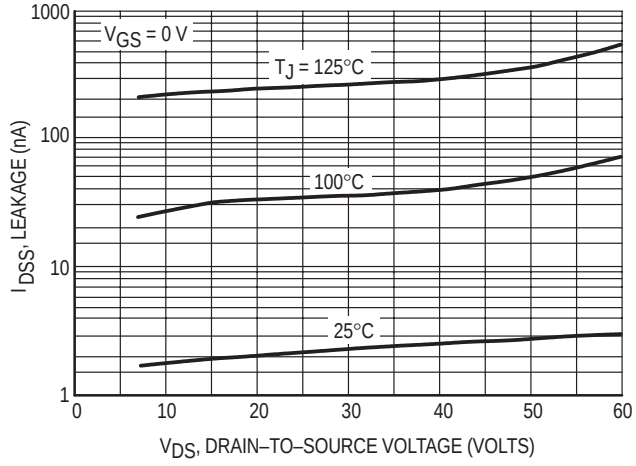


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

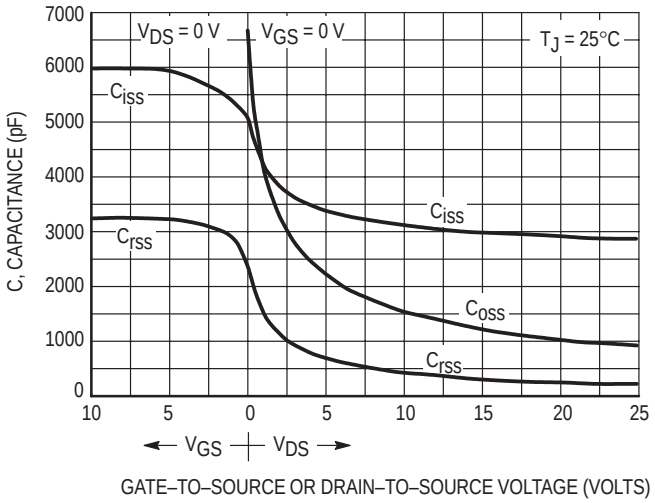


Figure 7. Capacitance Variation

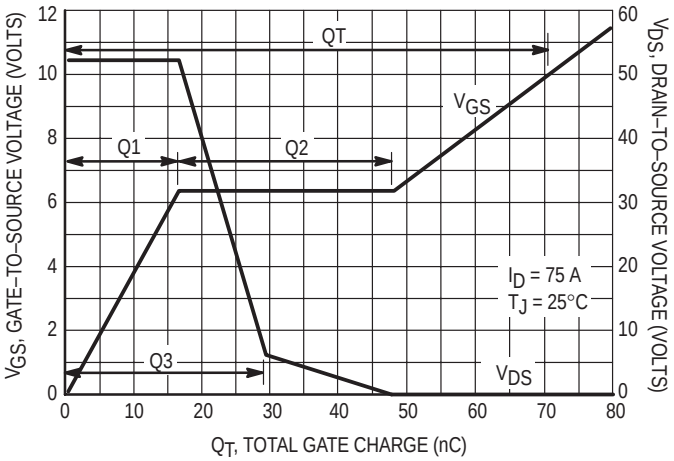


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

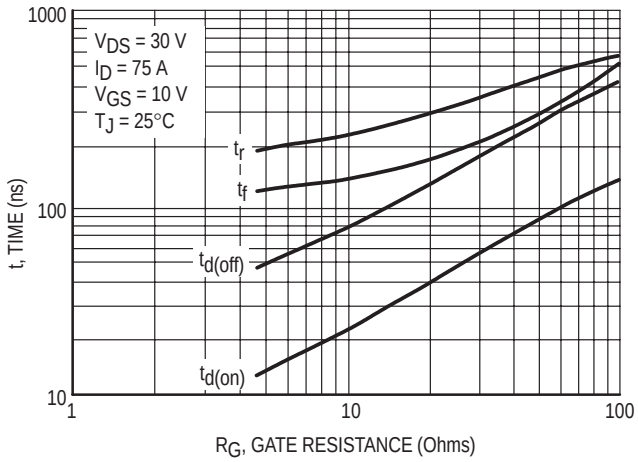


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

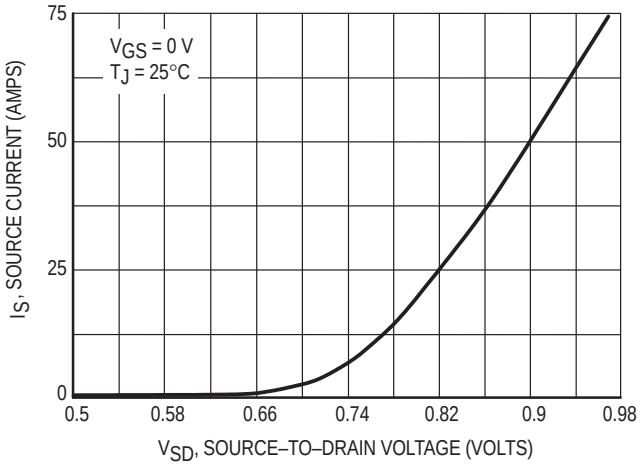


Figure 10. Diode Forward Voltage versus Current

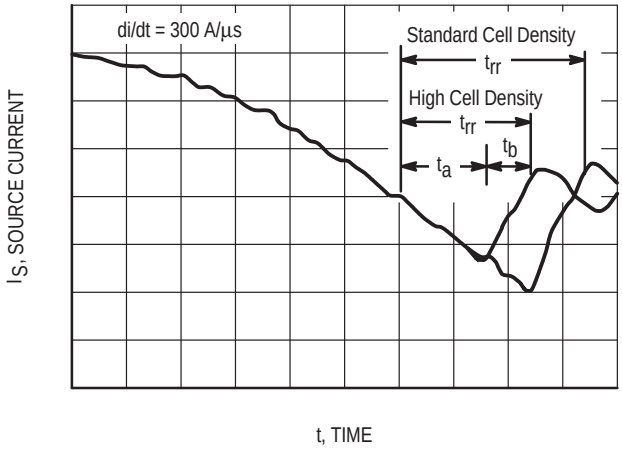


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

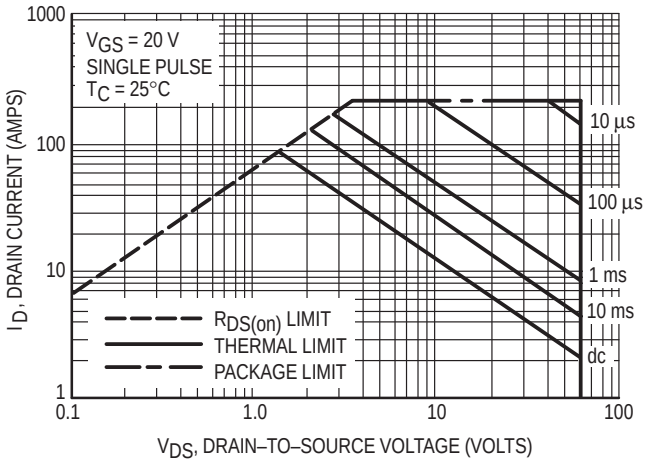


Figure 12. Maximum Rated Forward Biased Safe Operating Area

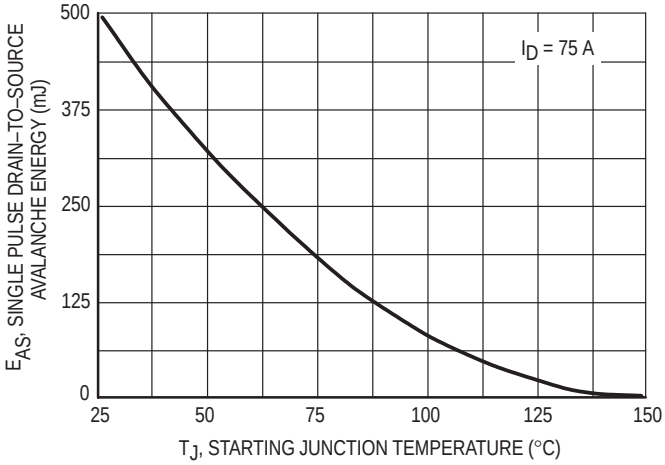


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

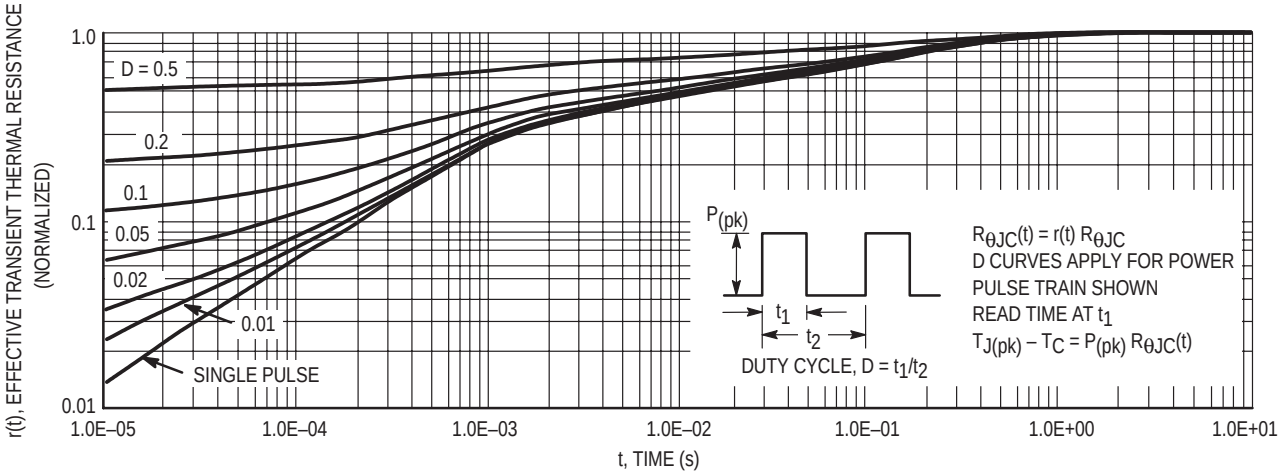


Figure 14. Thermal Response

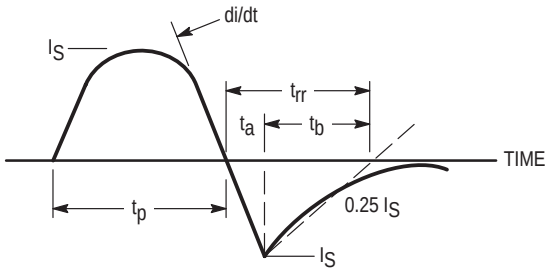


Figure 15. Diode Reverse Recovery Waveform

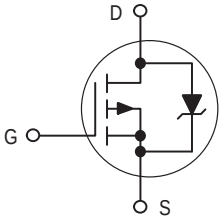
Product Preview

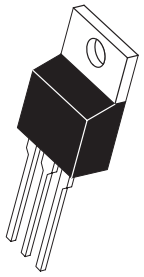
TMOS V™
Power Field Effect Transistor
P–Channel Enhancement–Mode Silicon Gate

MTP2955V

TMOS POWER FET
12 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.200 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 221A–06, Style 5
TO–220AB

New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 15 ± 25	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	12 8.0 42	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	60 0.40	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, Peak I_L = 12 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	216	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	2.5 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.8	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	—	0.185	0.200	Ohm
Drain–to–Source On–Voltage		$V_{DS(on)}$				Vdc
(V_{GS} = 10 Vdc, I_D = 12 Adc)			—	—	2.9	
(V_{GS} = 10 Vdc, I_D = 6.0 Adc, T_J = 150°C)			—	—	2.8	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 6.0 Adc)		g_{FS}	3.0	5.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	500	700	pF
Output Capacitance		C_{oss}	—	200	280	
Reverse Transfer Capacitance		C_{rss}	—	40	80	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 12 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	11	20	ns
Rise Time		t_r	—	38	80	
Turn–Off Delay Time		$t_{d(off)}$	—	18	40	
Fall Time		t_f	—	26	50	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 12 Adc, V_{GS} = 10 Vdc)	Q_T	—	15	20	nC
		Q_1	—	4.0	—	
		Q_2	—	7.0	—	
		Q_3	—	6.0	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 12 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.8	3.0	Vdc
	(I_S = 12 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	TBD	—	
Reverse Recovery Time	(I_S = 12 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	114	—	ns
		t_a	—	86	—	
		t_b	—	28	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.553	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

Designer's™ Data Sheet

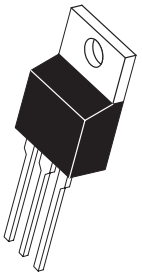
TMOS V™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

MTP3055V

Motorola Preferred Device

TMOS POWER FET
12 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.15 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.



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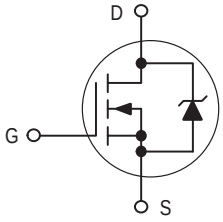

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 25	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	12 7.3 37	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C	P_D	48 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 12 Apk, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	72	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.13 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)			—	65	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)			—	—	10	
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage		$V_{GS(th)}$				
(V_{DS} = V_{GS}, I_D = 250 μAdc)			2.0	2.7	4.0	Vdc
Temperature Coefficient (Negative)			—	5.4	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	—	0.10	0.15	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 12 Adc)			—	1.3	2.2	
(I_D = 6.0 Adc, T_J = 150°C)			—	—	1.9	
Forward Transconductance (V_{DS} = 7.0 Vdc, I_D = 6.0 Adc)		g_{FS}	4.0	5.0	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	410	500	pF
Output Capacitance		C_{oss}	—	130	180	
Reverse Transfer Capacitance		C_{rss}	—	25	50	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 12 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	7.0	10	ns
Rise Time		t_r	—	34	60	
Turn–Off Delay Time		$t_{d(off)}$	—	17	30	
Fall Time		t_f	—	18	50	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 12 Adc, V_{GS} = 10 Vdc)	Q_T	—	12.2	17	nC
		Q_1	—	3.2	—	
		Q_2	—	5.2	—	
		Q_3	—	5.5	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 12 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.6	Vdc
	(I_S = 12 Adc, V_{GS} = 0 Vdc, T_J = 150°C)		—	0.91	—	
Reverse Recovery Time (See Figure 15)	(I_S = 12 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	56	—	ns
		t_a	—	40	—	
		t_b	—	16	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.128	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance		L_D				nH
(Measured from contact screw on tab to center of die)			—	3.5	—	
(Measured from the drain lead 0.25″ from package to center of die)				4.5		
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

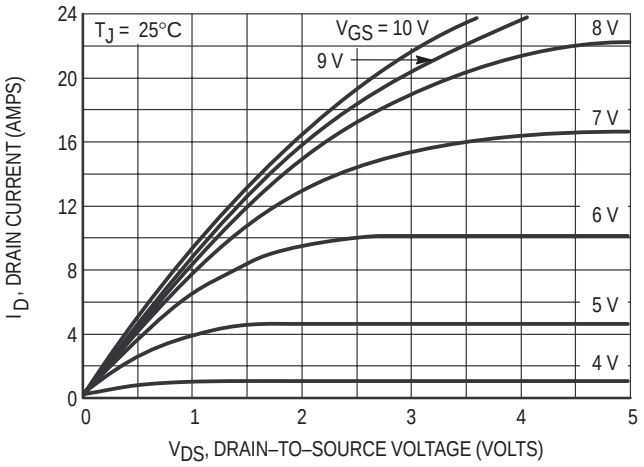

Figure 1. On–Region Characteristics

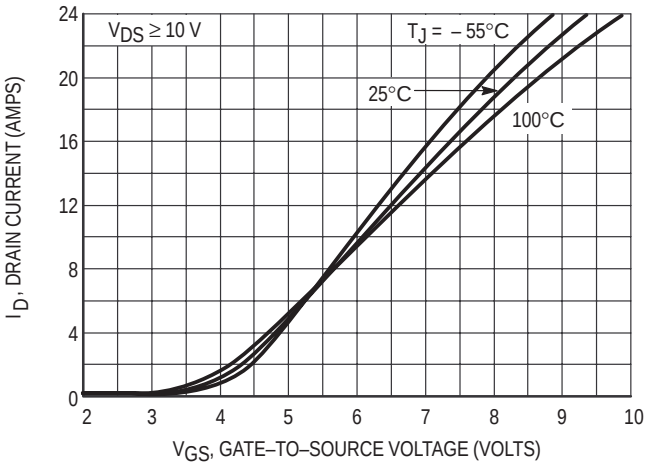

Figure 2. Transfer Characteristics

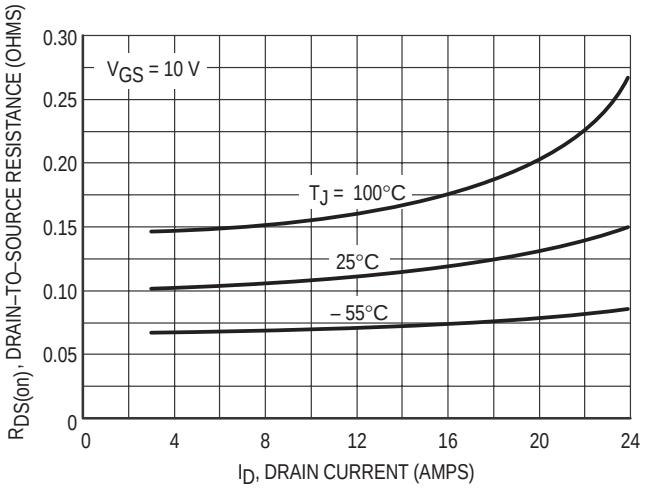

Figure 3. On–Resistance versus Drain Current and Temperature

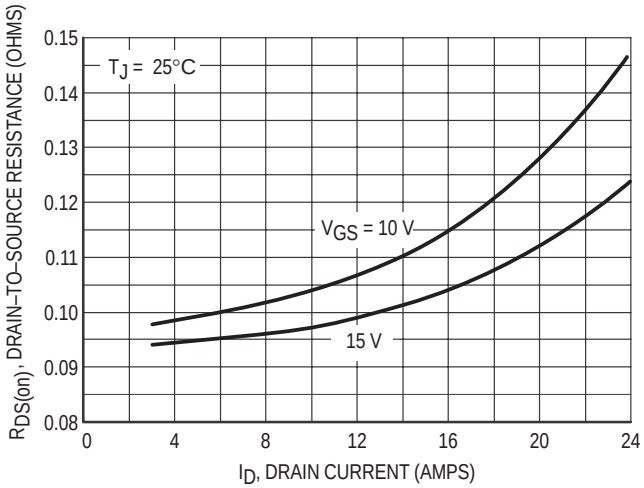

Figure 4. On–Resistance versus Drain Current and Gate Voltage

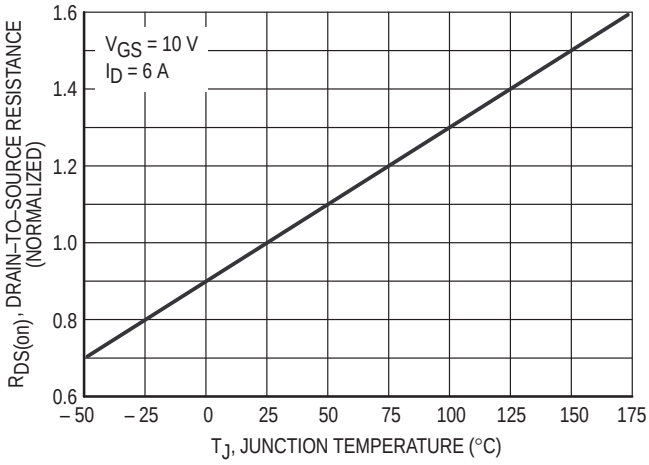

Figure 5. On–Resistance Variation with Temperature

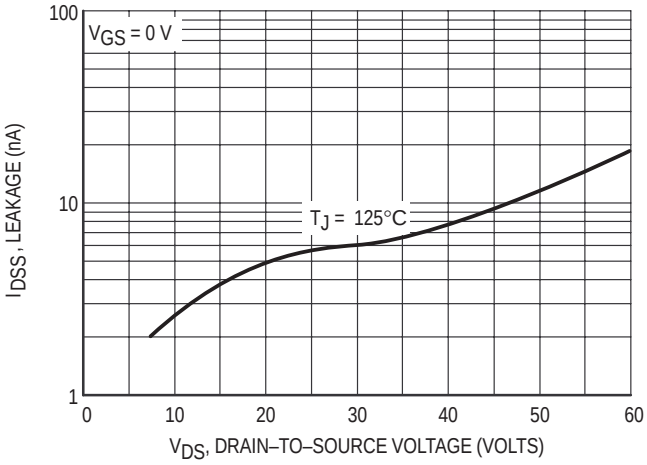

Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

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$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

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The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

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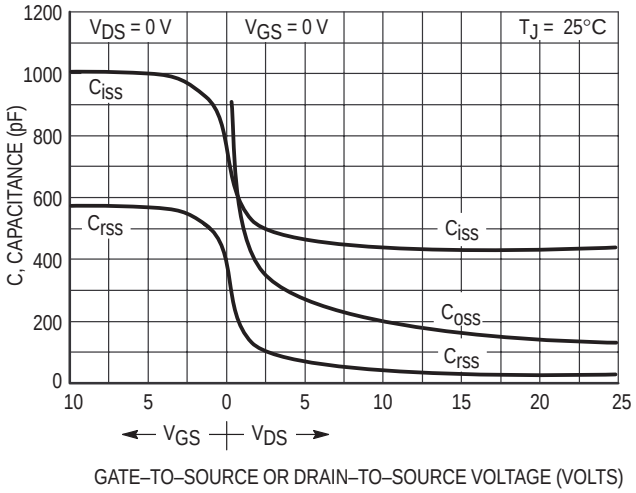


Figure 7. Capacitance Variation

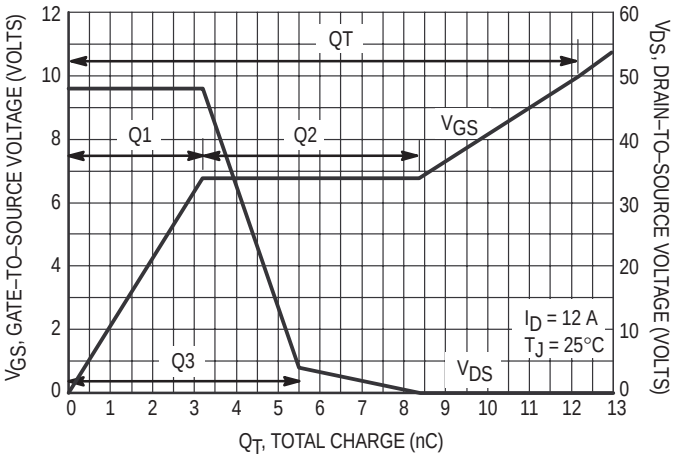


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

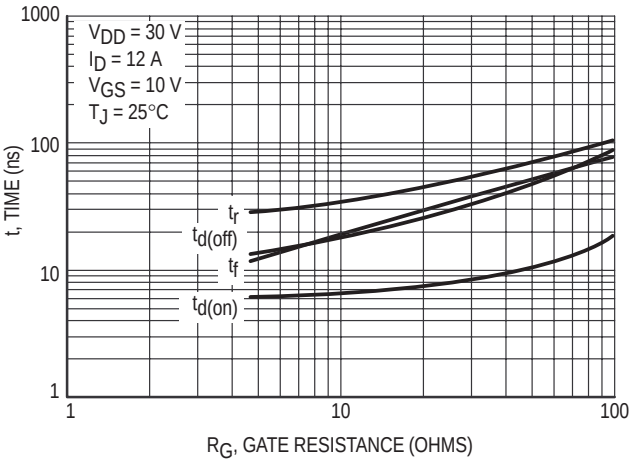


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

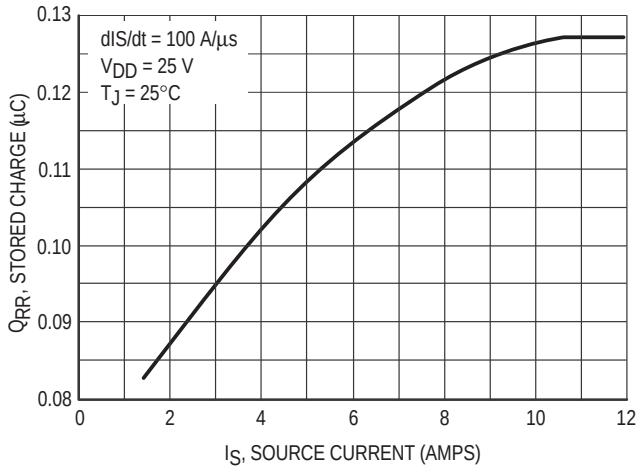


Figure 10. Stored Charge

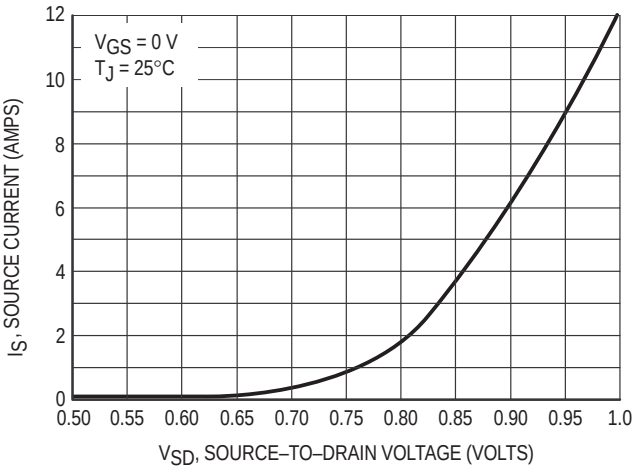


Figure 11. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

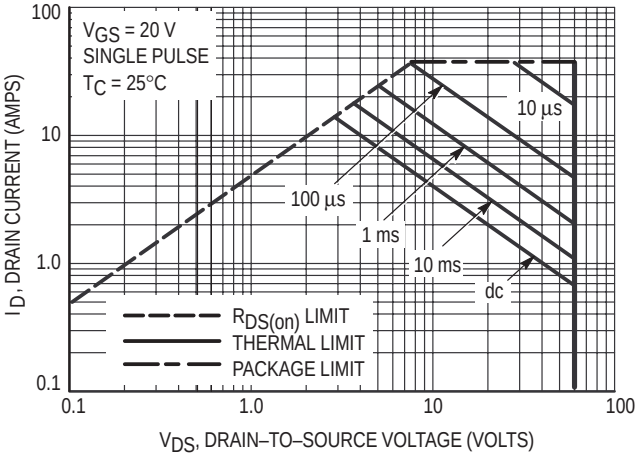


Figure 12. Maximum Rated Forward Biased Safe Operating Area

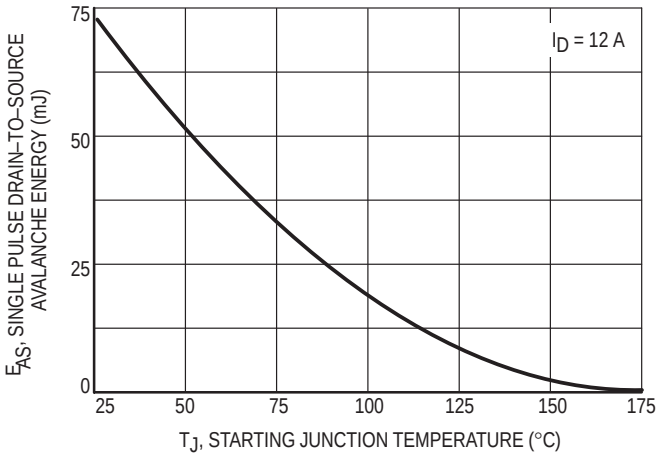


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

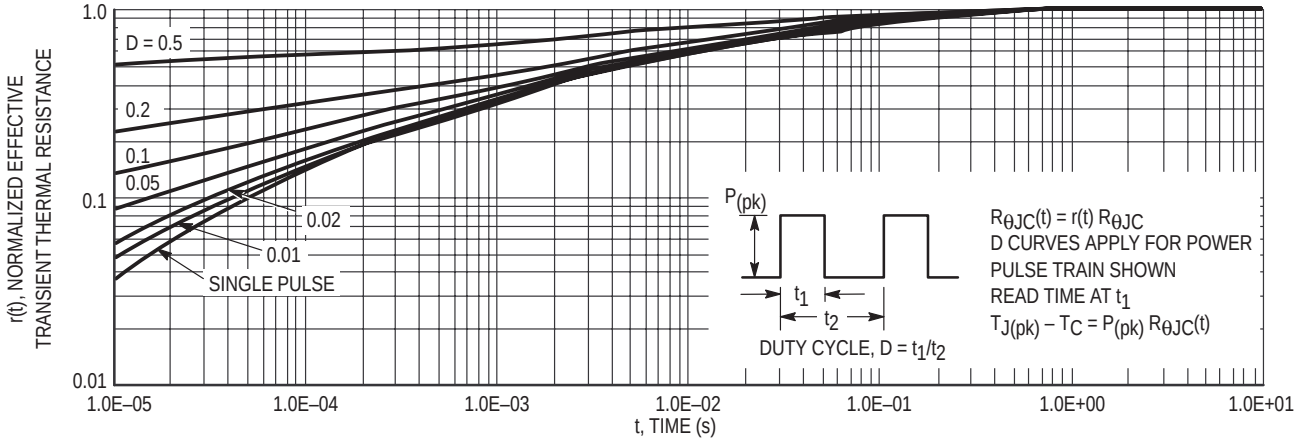


Figure 14. Thermal Response

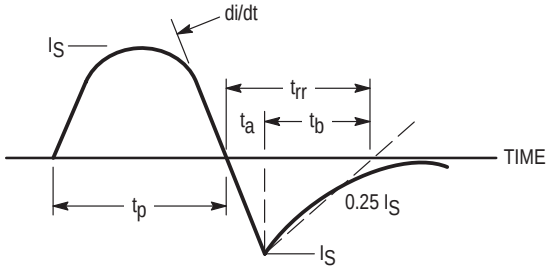


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

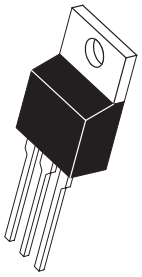
TMOS V™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

MTP3055VL

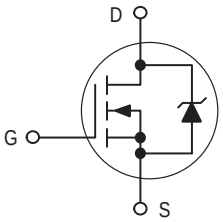
Motorola Preferred Device

TMOS POWER FET
12 AMPERES
60 VOLTS
$R_{DS(on)}$ = 0.18 OHM

TMOS V is a new technology designed to achieve an on–resistance area product about one–half that of standard MOSFETs. This new technology more than doubles the present cell density of our 50 and 60 volt TMOS devices. Just as with our TMOS E–FET designs, TMOS V is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.



CASE 221A–06, Style 5
TO–220AB



New Features of TMOS V
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors

Features Common to TMOS V and TMOS E–FETS
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	60	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate–Source Voltage — Continuous — Single Pulse ($t_p \le 50$ μs)	V_{GS} V_{GSM}	±15 ± 20	Vdc Vpk
Drain Current — Continuous @ 25°C — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	12 8.0 42	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C	P_D	48 0.32	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 175	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 12 Apk, L = 1.0 mH, R_G =25 Ω)	E_{AS}	72	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	3.13 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

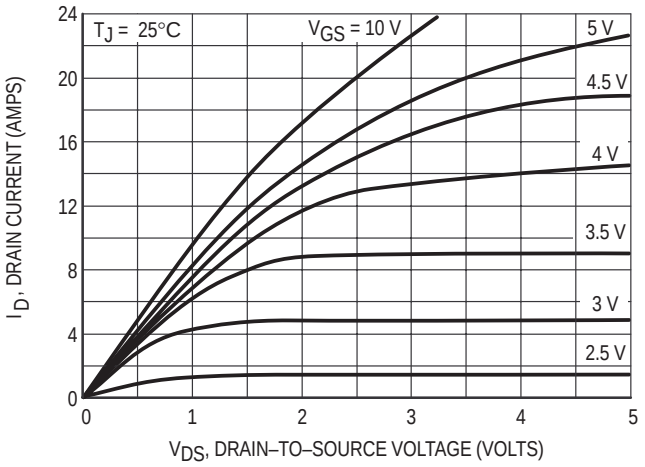
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	60 —	— 62	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	1.0 —	1.6 3.0	2.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 6.0 Adc)		$R_{DS(on)}$	—	0.12	0.18	Ohm
Drain–Source On–Voltage (V_{GS} = 5.0 Vdc) (I_D = 12 Adc) (I_D = 6.0 Adc, T_J = 150°C)		$V_{DS(on)}$	— —	1.6 —	2.6 2.5	Vdc
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 6.0 Adc)		g_{FS}	5.0	8.8	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	410	570	pF
Output Capacitance		C_{oss}	—	114	160	
Reverse Transfer Capacitance		C_{rss}	—	21	40	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 12 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	9.0	20	ns
Rise Time		t_r	—	85	190	
Turn–Off Delay Time		$t_{d(off)}$	—	14	30	
Fall Time		t_f	—	43	90	
Gate Charge (See Figure 8)	(V_{DS} = 48 Vdc, I_D = 12 Adc, V_{GS} = 5.0 Vdc)	Q_T	—	8.1	10	nC
		Q_1	—	1.8	—	
		Q_2	—	4.2	—	
		Q_3	—	3.8	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 12 Adc, V_{GS} = 0 Vdc) (I_S = 12 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	— —	0.97 0.86	1.3 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 12 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	55.7	—	ns
		t_a	—	37	—	
		t_b	—	18.7	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.116	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	3.5 4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS



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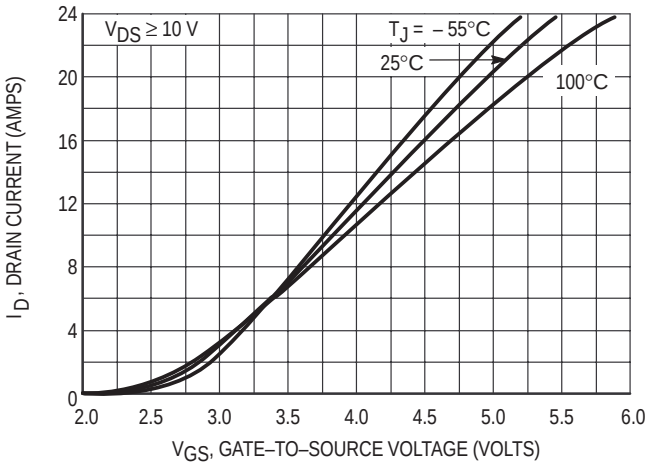

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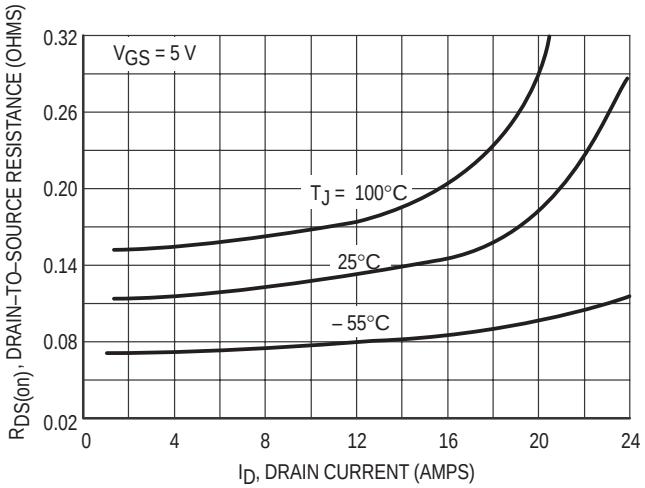

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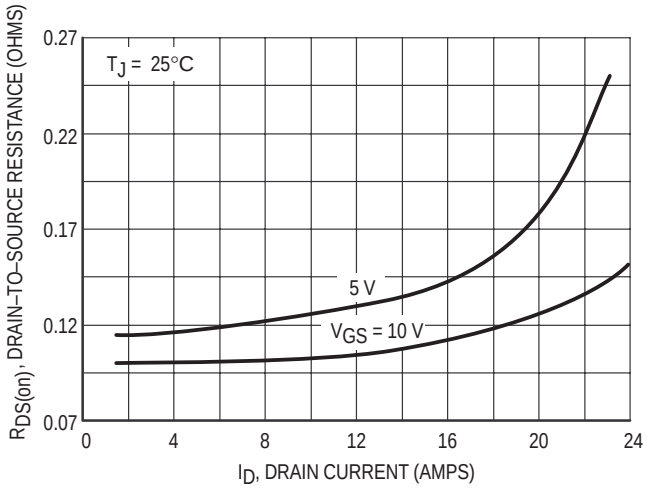

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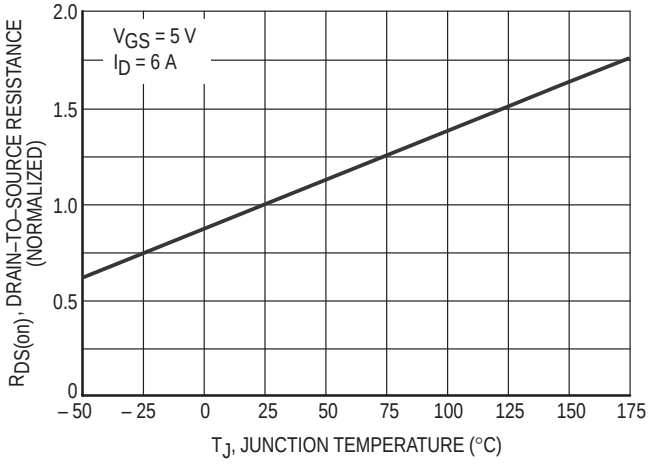

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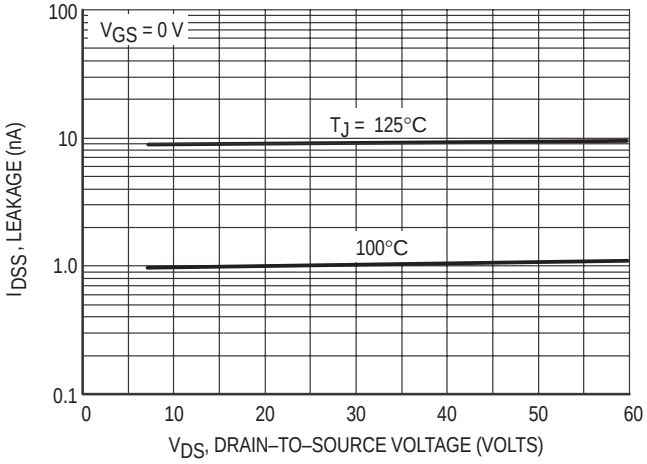

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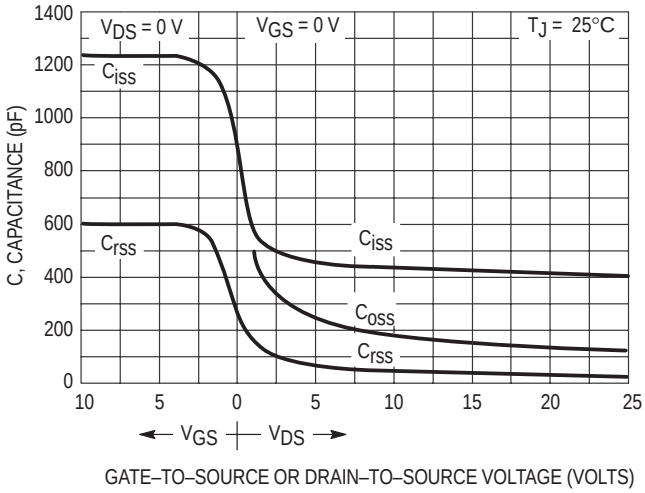

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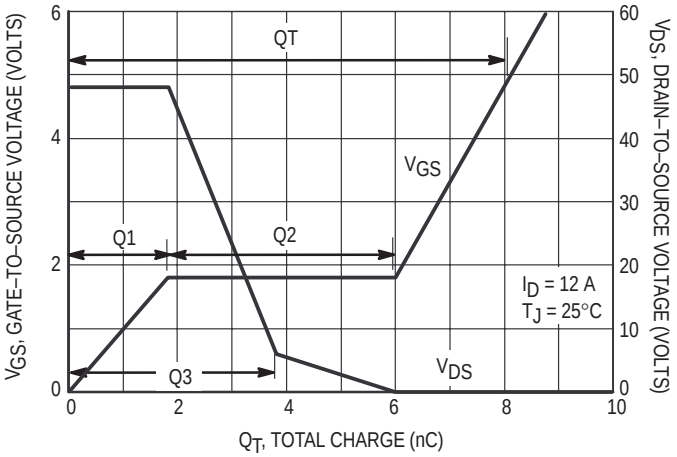


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

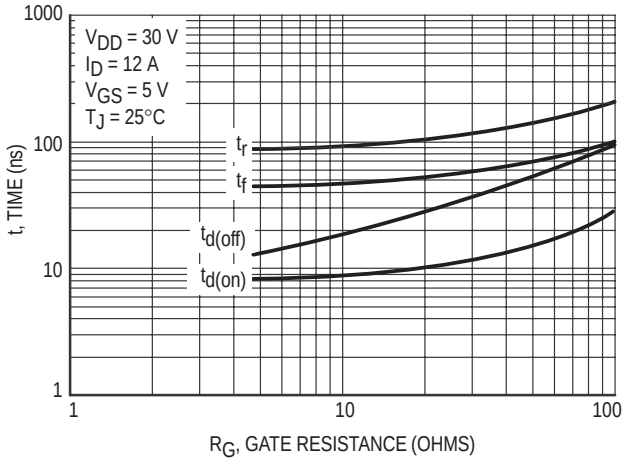


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

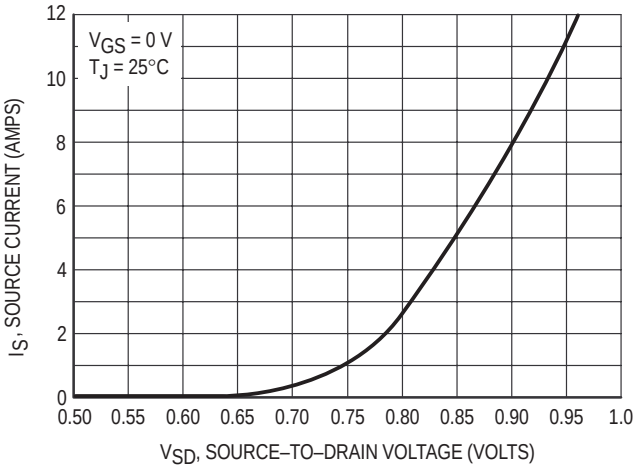


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

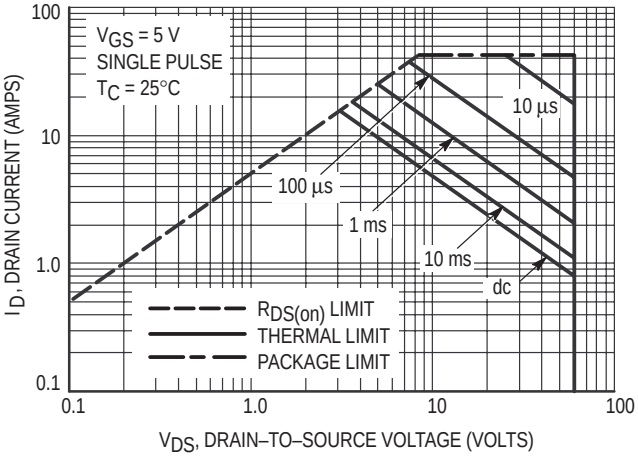


Figure 11. Maximum Rated Forward Biased Safe Operating Area

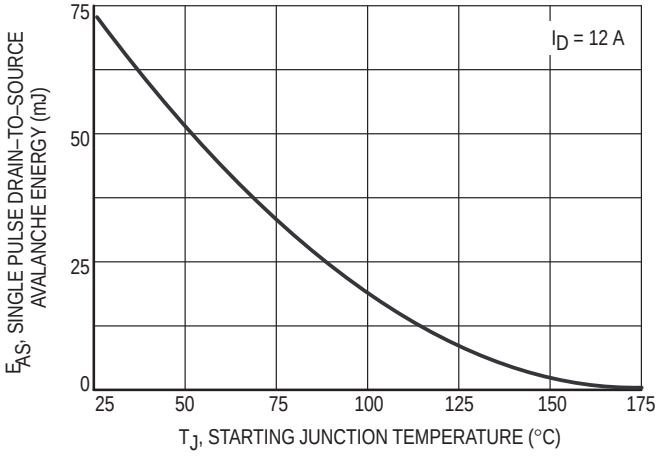


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

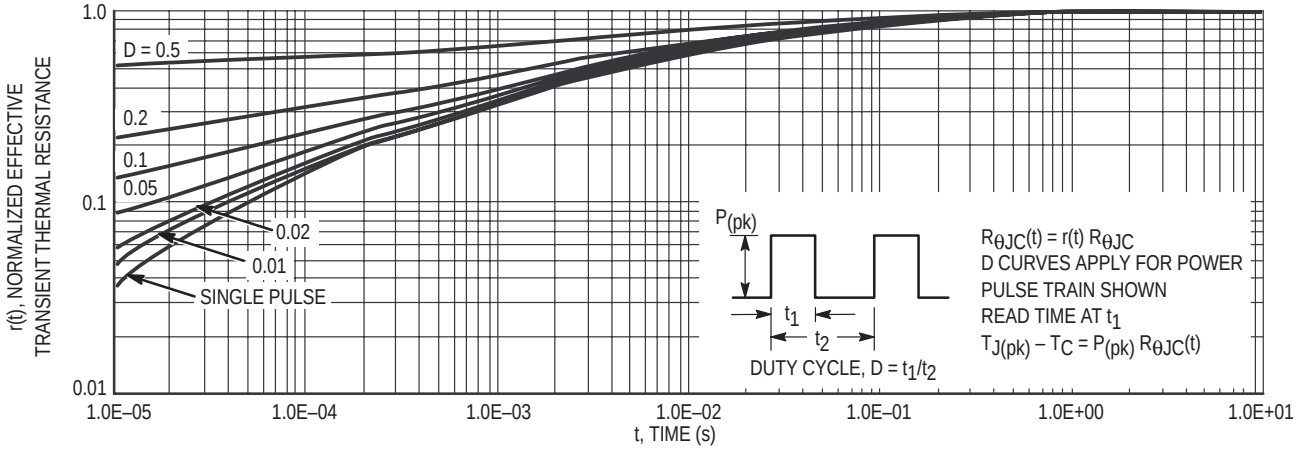


Figure 13. Thermal Response

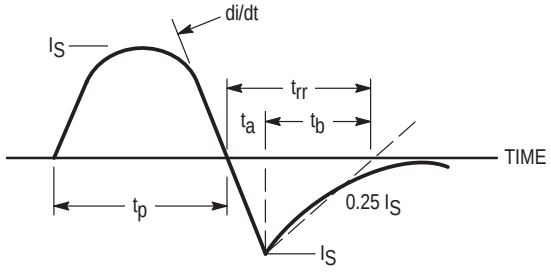


Figure 14. Diode Reverse Recovery Waveform

Advance Information

Medium Power Surface Mount Products

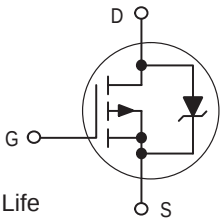
TMOS Single P-Channel Field Effect Transistor

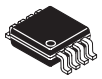
MTSF1P02HD

Motorola Preferred Device

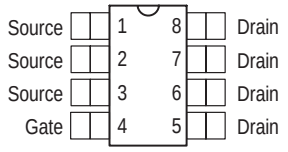
SINGLE TMOS POWER FET 1.8 AMPERES 20 VOLTS $R_{DS(on)}$ = 0.16 OHM

Micro8™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process to achieve lowest possible on–resistance per silicon area. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Micro8™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.





CASE 846A–02, Style 1
Micro8



- Miniature Micro8 Surface Mount Package — Saves Board Space
- Extremely Low Profile (<1.1mm) for thin applications such as PCMCIA cards
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for Micro8 Package Provided

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) *

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 8.0	Vdc
Drain Current — Continuous @ T_A = 25°C (2) — Continuous @ T_A = 70°C (2) — Pulsed Drain Current (3)	I_D I_D I_{DM}	1.8 1.6 14.4	Adc Apk
Total Power Dissipation @ T_A = 25°C (1) Linear Derating Factor (1)	P_D	1.8 14.3	Watts mW/°C
Total Power Dissipation @ T_A = 25°C (2) Linear Derating Factor (2)	P_D	0.78 6.25	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C

THERMAL RESISTANCE

Rating	Symbol	Typ.	Max.	Unit
Thermal Resistance — Junction to Ambient, PCB Mount (1) — Junction to Ambient, PCB Mount (2)	$R_{\theta JA}$ $R_{\theta JA}$	55 125	70 160	°C/W

* Negative signs for P–Channel device omitted for clarity.
(1) When mounted on 1 inch square FR–4 or G–10 board (V_{GS} = 4.5 V, @ Steady State)
(2) When mounted on minimum recommended FR–4 or G–10 board (V_{GS} = 4.5 V, @ Steady State)
(3) Repetitive rating; pulse width limited by maximum junction temperature.

DEVICE MARKING

AB

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MTSF1P02HDR2	13″	12 mm embossed tape	4000 units

This document contains information on a new product. Specifications and information are subject to change without notice.
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)(1)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (Cpk ≥ 2.0) (1) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			20	—	—	
Temperature Coefficient (Positive)			—	12.8	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc)			—	—	1.0	
(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	10	
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(2)						
Gate Threshold Voltage (Cpk ≥ 2.0) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			0.6	0.8	—	
Threshold Temperature Coefficient (Negative)			—	2.5	—	mV/°C
Static Drain–to–Source On–Resistance (3)		$R_{DS(on)}$				mΩ
(V_{GS} = 4.5 Vdc, I_D = 1.8 Adc)			—	120	160	
(V_{GS} = 2.7 Vdc, I_D = 0.9 Adc)			—	160	190	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 0.9 Adc) (1)		g_{FS}	2.0	4.0	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 10 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	440	—	pF
Output Capacitance		C_{oss}	—	300	—	
Transfer Capacitance		C_{rss}	—	150	—	
SWITCHING CHARACTERISTICS(3)						
Turn–On Delay Time	(V_{DS} = 10 Vdc, I_D = 1.8 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω) (1)	$t_{d(on)}$	—	15	—	ns
Rise Time		t_r	—	35	—	
Turn–Off Delay Time		$t_{d(off)}$	—	55	—	
Fall Time		t_f	—	75	—	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 0.9 Adc, V_{GS} = 2.7 Vdc, R_G = 6.0 Ω) (1)	$t_{d(on)}$	—	20	—	
Rise Time		t_r	—	93	—	
Turn–Off Delay Time		$t_{d(off)}$	—	50	—	
Fall Time		t_f	—	75	—	
Gate Charge	(V_{DS} = 10 Vdc, I_D = 1.8 Adc, V_{GS} = 4.5 Vdc)	Q_T	—	11	22	nC
		Q_1	—	0.7	—	
		Q_2	—	5.5	—	
		Q_3	—	3.8	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 1.8 Adc, V_{GS} = 0 Vdc) (1)	V_{SD}				Vdc
	(I_S = 1.8 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.24	2.0	
			—	0.9	—	
Reverse Recovery Time	(I_S = 1.8 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (1)	t_{rr}	—	120	—	ns
		t_a	—	33	—	
		t_b	—	87	—	
Reverse Recovery Stored Charge		Q_{RR}	—	0.223	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

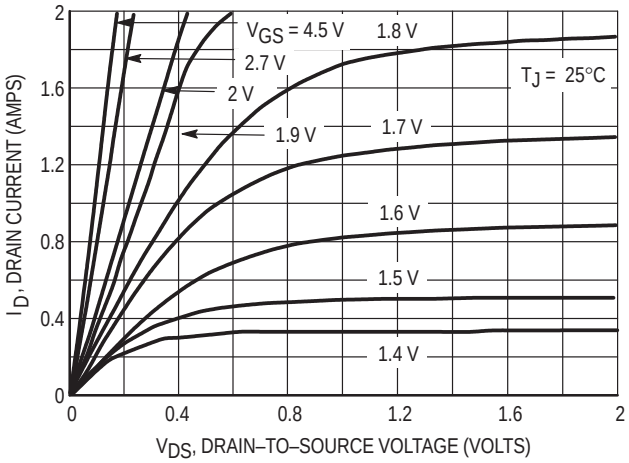


Figure 1. On–Region Characteristics

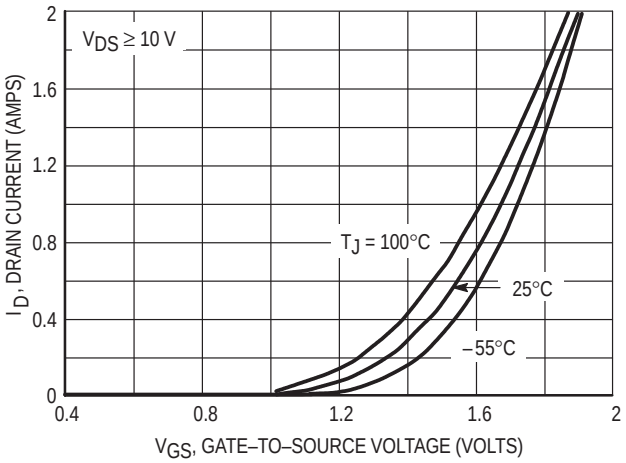


Figure 2. Transfer Characteristics

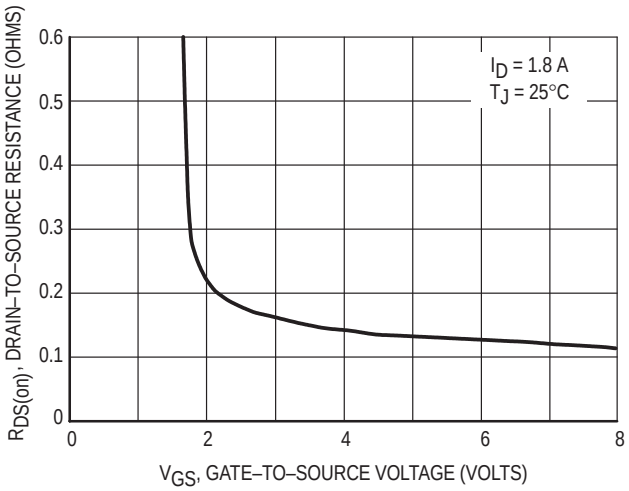


Figure 3. On–Resistance versus Gate–To–Source Voltage

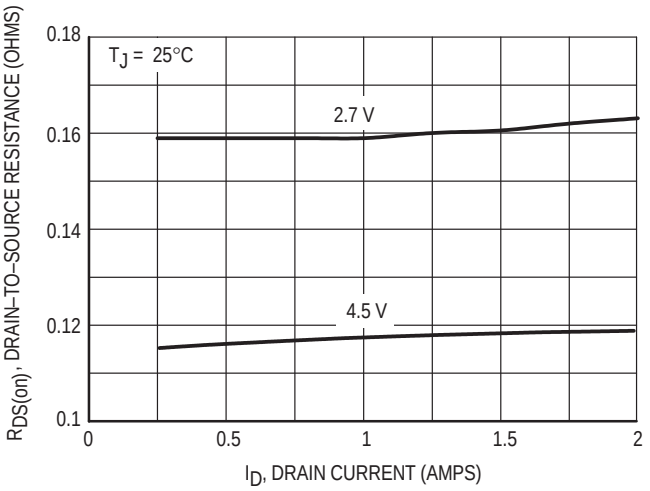


Figure 4. On–Resistance versus Drain Current and Gate Voltage

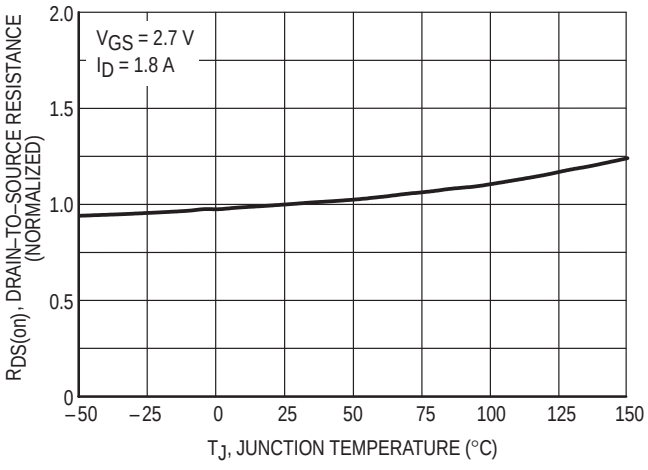


Figure 5. On–Resistance Variation with Temperature

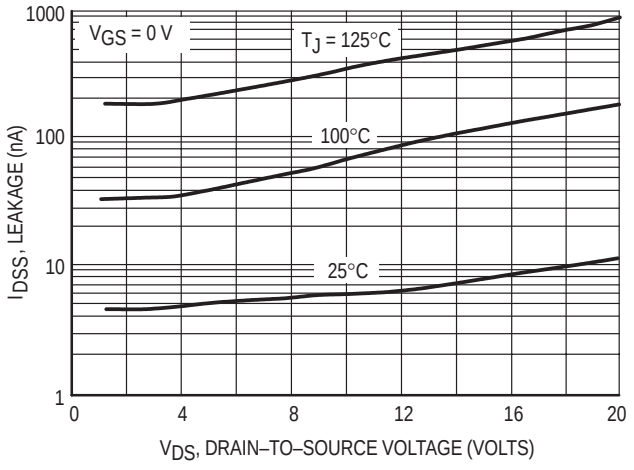


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

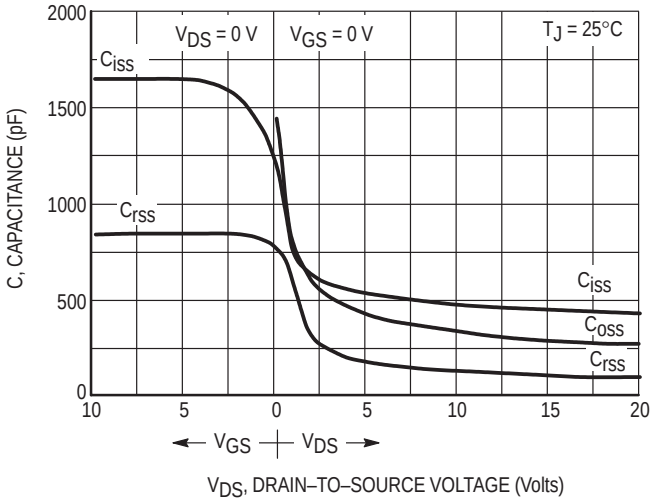


Figure 7. Capacitance Variation

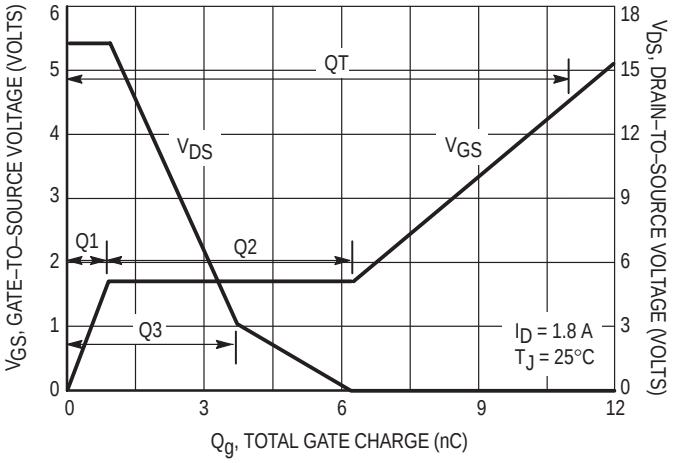


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

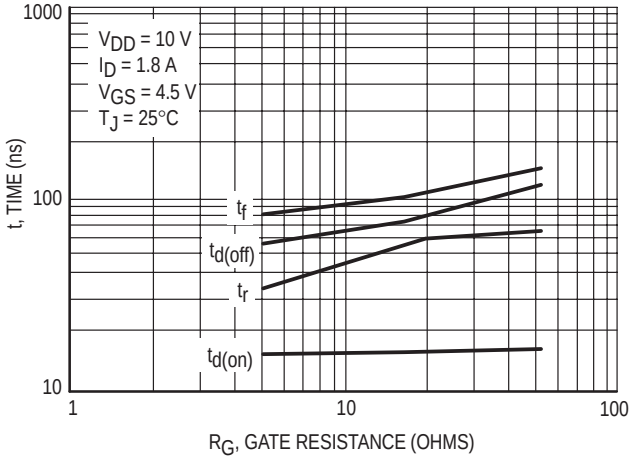


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

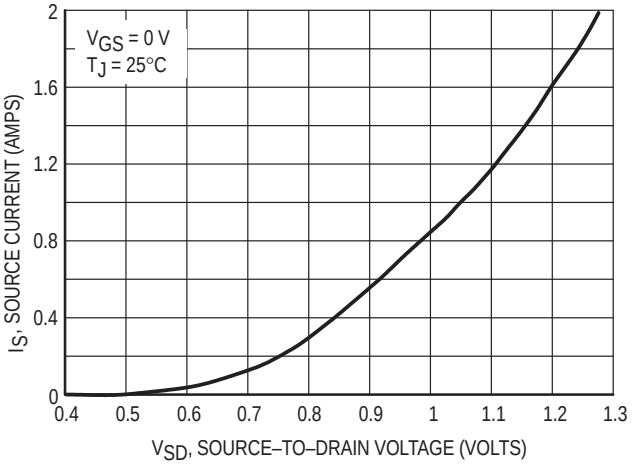


Figure 10. Diode Forward Voltage versus Current

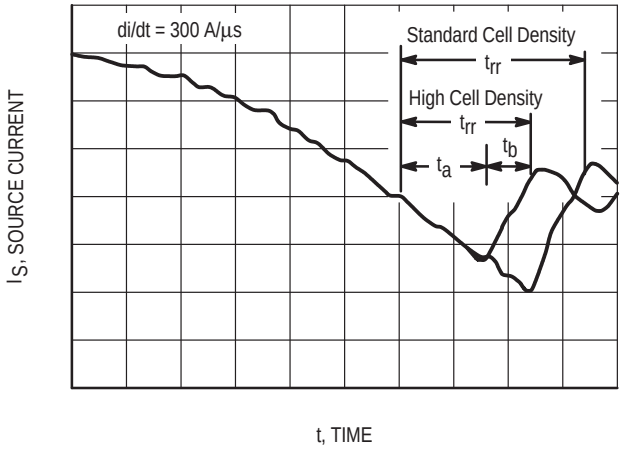


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curve (Figure 12) defines the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

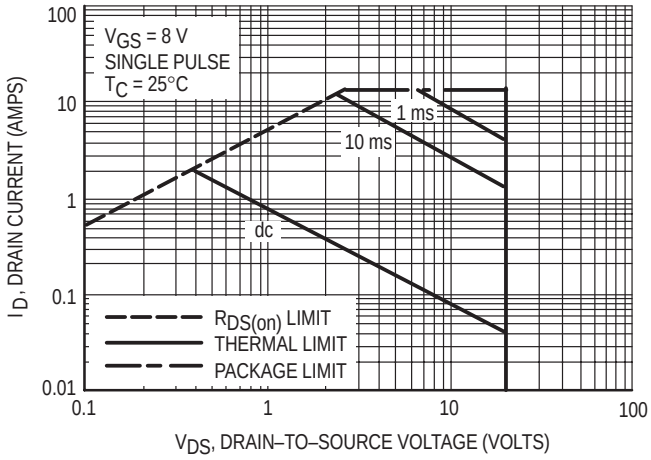


Figure 12. Maximum Rated Forward Biased Safe Operating Area

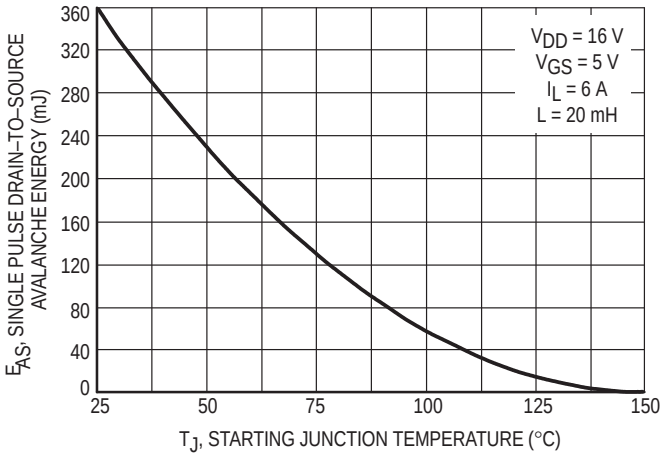


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

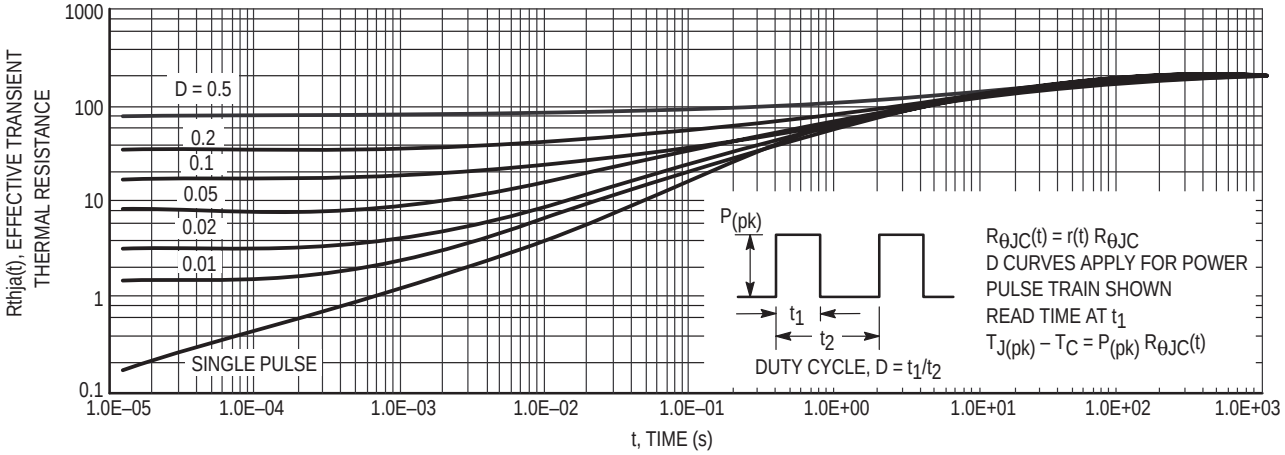


Figure 14. Thermal Response

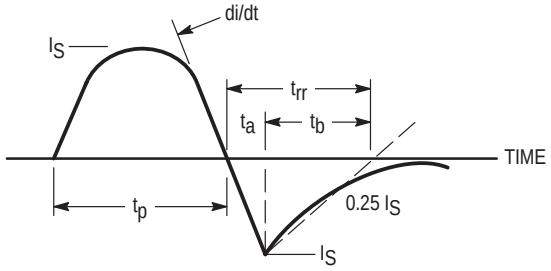
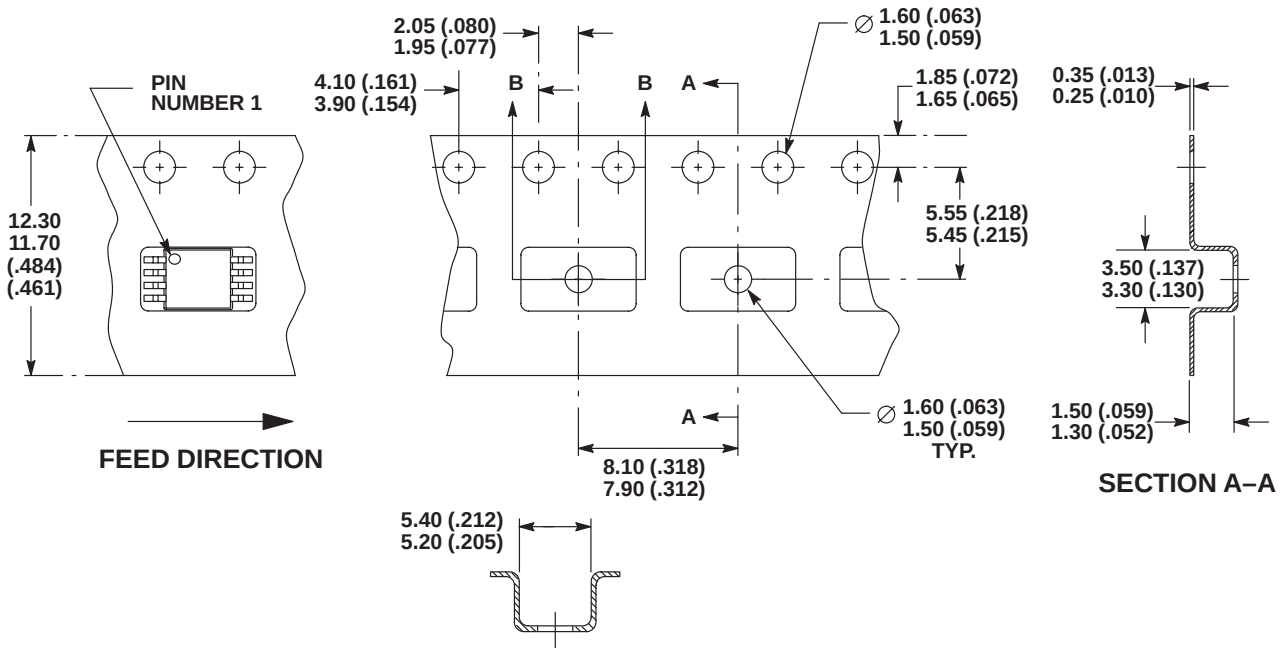


Figure 15. Diode Reverse Recovery Waveform

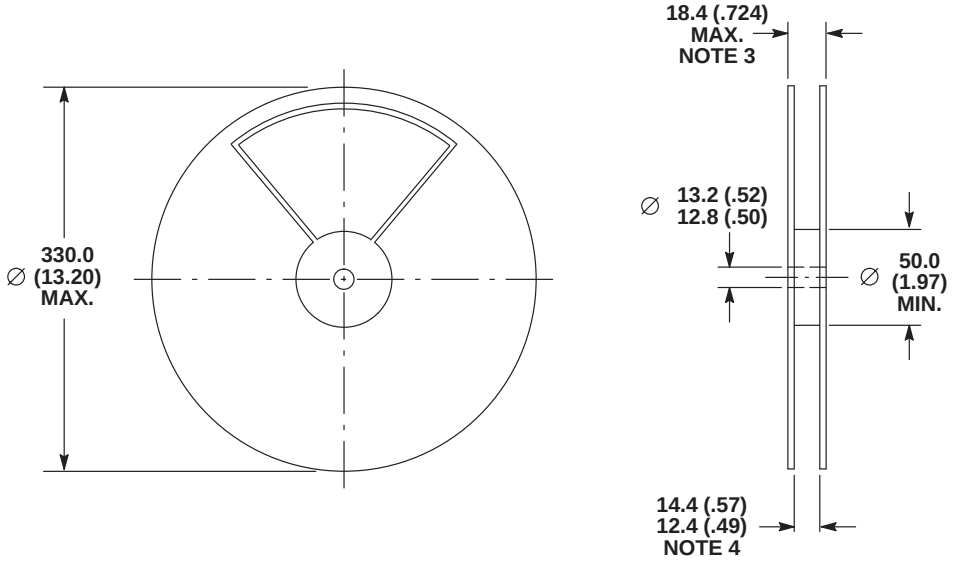
TAPE & REEL INFORMATION

Micro8
Dimensions are shown in millimeters (inches)



SECTION B–B

NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.



NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.
3. INCLUDES FLANGE DISTORTION AT OUTER EDGE.
4. DIMENSION MEASURED AT INNER HUB.

Product Preview

Medium Power Surface Mount Products

TMOS Single P-Channel Field Effect Transistor

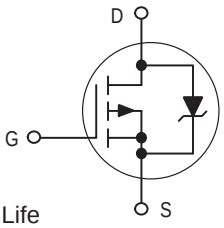
MTSF2P02HD

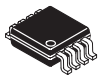
Motorola Preferred Device

SINGLE TMOS POWER FET 2.4 AMPERES 20 VOLTS $R_{DS(on)}$ = 0.090 OHM

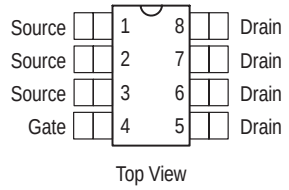
Micro8™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process to achieve lowest possible on–resistance per silicon area. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Micro8™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Miniature Micro8 Surface Mount Package — Saves Board Space
- Extremely Low Profile (<1.1mm) for thin applications such as PCMCIA cards
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for Micro8 Package Provided





CASE 846A–02, Style 1
Micro8



MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) *

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 8.0	Vdc
Drain Current — Continuous @ T_A = 25°C (1) — Continuous @ T_A = 70°C (1) — Pulsed Drain Current (3)	I_D I_D I_{DM}	2.4 2.2 19	Adc Apk
Total Power Dissipation @ T_A = 25°C (1) Linear Derating Factor (1)	P_D	1.8 14.3	Watts mW/°C
Total Power Dissipation @ T_A = 25°C (2) Linear Derating Factor (2)	P_D	0.78 6.25	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C

THERMAL RESISTANCE

Rating	Symbol	Typ.	Max.	Unit
Thermal Resistance — Junction to Ambient, PCB Mount (1) — Junction to Ambient, PCB Mount (2)	$R_{\theta JA}$ $R_{\theta JA}$	55 125	70 160	°C/W

* Negative signs for P–Channel device omitted for clarity.
(1) When mounted on 1 inch square FR–4 or G–10 board (V_{GS} = 4.5 V, @ Steady State)
(2) When mounted on minimum recommended FR–4 or G–10 board (V_{GS} = 4.5 V, @ Steady State)
(3) Repetitive rating; pulse width limited by maximum junction temperature.

DEVICE MARKING **ORDERING INFORMATION**

	Device	Reel Size	Tape Width	Quantity
AD	MTSF2P02HDR2	13″	12 mm embossed tape	4000 units

This document contains information on a new product. Specifications and information are subject to change without notice.
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)(1)

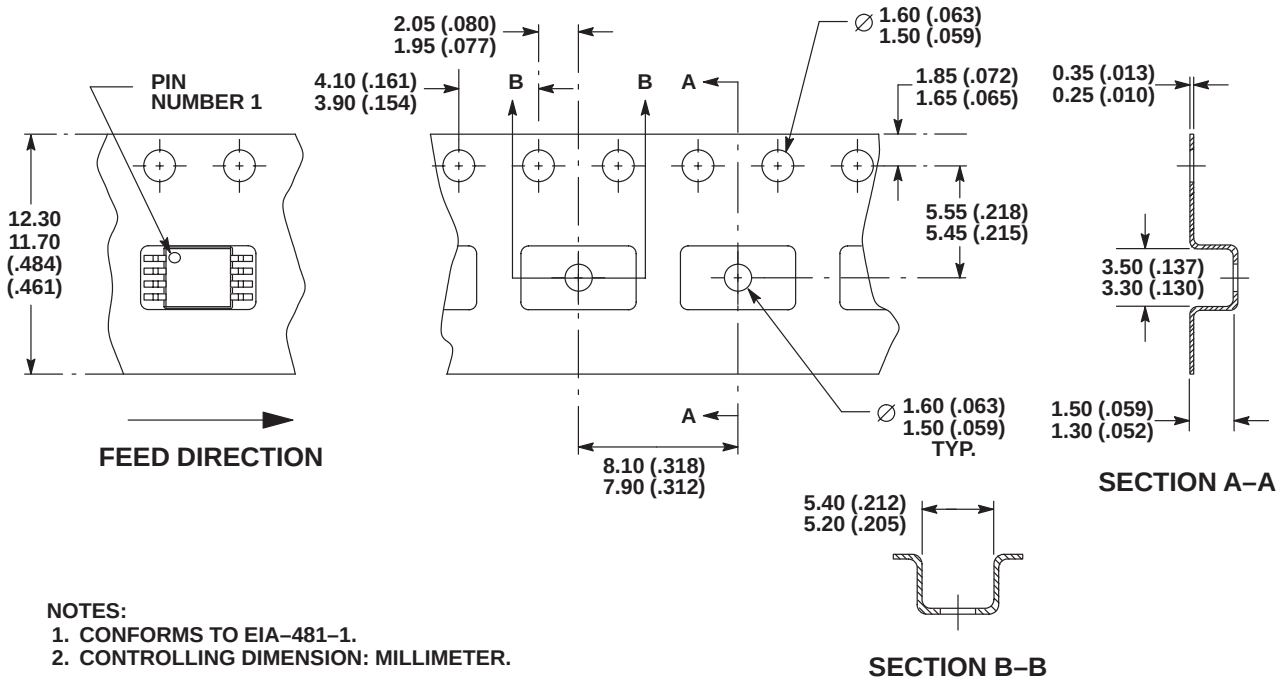
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (Cpk ≥ 2.0) (1) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			20	—	—	
Temperature Coefficient (Positive)			—	TBD	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc)			—	TBD	2.0	
(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	TBD	25	
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0)		I_{GSS}	—	TBD	100	nAdc
ON CHARACTERISTICS(2)						
Gate Threshold Voltage (Cpk ≥ 2.0) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			0.7	TBD	—	
Threshold Temperature Coefficient (Negative)			—	TBD	—	mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (3)		$R_{DS(on)}$				mΩ
(V_{GS} = 4.5 Vdc, I_D = 2.4 Adc)			—	TBD	90	
(V_{GS} = 2.7 Vdc, I_D = 1.2 Adc)			—	TBD	130	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1.2 Adc) (1)		g_{FS}	2.6	TBD	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 15 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	TBD	—	pF
Output Capacitance		C_{oss}	—	TBD	—	
Transfer Capacitance		C_{rss}	—	TBD	—	
SWITCHING CHARACTERISTICS(3)						
Turn–On Delay Time	(V_{DS} = 10 Vdc, I_D = 2.4 Adc, V_{GS} = 4.5 Vdc, R_G = 6.0 Ω) (1)	$t_{d(on)}$	—	TBD	—	ns
Rise Time		t_r	—	TBD	—	
Turn–Off Delay Time		$t_{d(off)}$	—	TBD	—	
Fall Time		t_f	—	TBD	—	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 1.2 Adc, V_{GS} = 2.7 Vdc, R_G = 6.0 Ω) (1)	$t_{d(on)}$	—	TBD	—	
Rise Time		t_r	—	TBD	—	
Turn–Off Delay Time		$t_{d(off)}$	—	TBD	—	
Fall Time		t_f	—	TBD	—	
Gate Charge	(V_{DS} = 16 Vdc, I_D = 2.4 Adc, V_{GS} = 4.5 Vdc)	Q_T	—	TBD	TBD	nC
		Q_1	—	TBD	—	
		Q_2	—	TBD	—	
		Q_3	—	TBD	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 2.4 Adc, V_{GS} = 0 Vdc) (1)	V_{SD}				Vdc
	(I_S = 2.4 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	TBD	1.0	
			—	TBD	—	
Reverse Recovery Time	(I_S = 2.4 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (1)	t_{rr}	—	TBD	—	ns
		t_a	—	TBD	—	
		t_b	—	TBD	—	
Reverse Recovery Stored Charge		Q_{RR}	—	TBD	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

TAPE & REEL INFORMATION

Micro8

Dimensions are shown in millimeters (inches)



NOTES:
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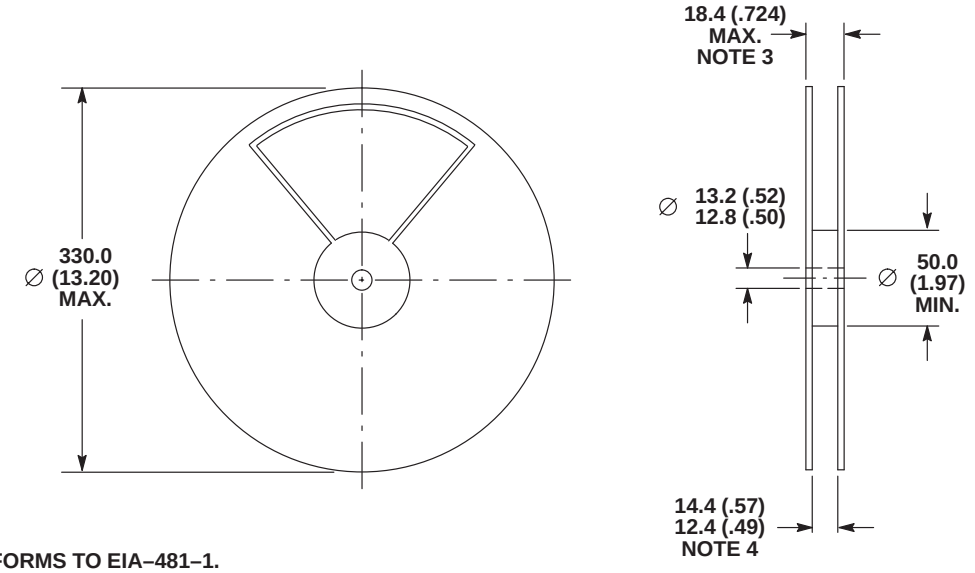

NOTES:
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4. DIMENSION MEASURED AT INNER HUB.

Advance Information

Medium Power Surface Mount Products

TMOS Single N-Channel Field Effect Transistor

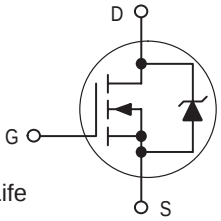
MTSF3N02HD

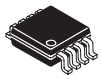
Motorola Preferred Device

SINGLE TMOS POWER MOSFET 3.8 AMPERES 20 VOLTS $R_{DS(on)}$ = 0.040 OHM

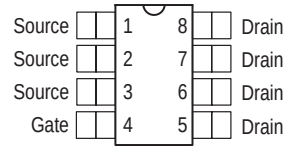
Micro8™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process to achieve lowest possible on–resistance per silicon area. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Micro8™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Miniature Micro8 Surface Mount Package — Saves Board Space
- Extremely Low Profile (<1.1mm) for thin applications such as PCMCIA cards
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for Micro8 Package Provided





CASE 846A–02, Style 1
Micro8



Top View

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	20	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	20	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 8.0	Vdc
Drain Current — Continuous @ T_A = 25°C (2) — Continuous @ T_A = 70°C (2) — Pulsed Drain Current (3)	I_D I_D I_{DM}	3.8 3.5 30	Adc Apk
Total Power Dissipation @ T_A = 25°C (1) Linear Derating Factor (1)	P_D	1.8 14.3	Watts mW/°C
Total Power Dissipation @ T_A = 25°C (2) Linear Derating Factor (2)	P_D	0.78 6.25	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C

THERMAL RESISTANCE

Rating	Symbol	Typ.	Max.	Unit
Thermal Resistance — Junction to Ambient, PCB Mount (1) — Junction to Ambient, PCB Mount (2)	$R_{\theta JA}$ $R_{\theta JA}$	55 125	70 160	°C/W

(1) When mounted on 1 inch square FR–4 or G–10 board (V_{GS} = 4.5 V, @ Steady State)
(2) When mounted on minimum recommended FR–4 or G–10 board (V_{GS} = 4.5 V, @ Steady State)
(3) Repetitive rating; pulse width limited by maximum junction temperature.

DEVICE MARKING

AC

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MTSF3N02HDR2	13″	12 mm embossed tape	4000 units

This document contains information on a new product. Specifications and information are subject to change without notice.
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (1) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			20	—	—	
Temperature Coefficient (Positive)			—	16	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc)			—	—	1.0	
(V_{DS} = 16 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	25	
Gate–Body Leakage Current (V_{GS} = ± 8.0 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			0.7	0.78	—	
Threshold Temperature Coefficient (Negative)			—	2.65	—	mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (3)		$R_{DS(on)}$				mΩ
(V_{GS} = 4.5 Vdc, I_D = 3.8 Adc)			—	30	40	
(V_{GS} = 2.7 Vdc, I_D = 1.9 Adc)			—	40	50	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1.9 Adc) (1)		g_{FS}	4.0	7.5	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 15 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	475	—	pF
Output Capacitance		C_{oss}	—	255	—	
Transfer Capacitance		C_{rss}	—	110	—	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DS} = 10 Vdc, I_D = 3.8 Adc, V_{GS} = 4.5 Vdc, R_G = 6 Ω) (1)	$t_{d(on)}$	—	9.5	—	ns
Rise Time		t_r	—	45	—	
Turn–Off Delay Time		$t_{d(off)}$	—	50	—	
Fall Time		t_f	—	62	—	
Turn–On Delay Time	(V_{DD} = 10 Vdc, I_D = 1.9 Adc, V_{GS} = 2.7 Vdc, R_G = 6 Ω) (1)	$t_{d(on)}$	—	19	—	ns
Rise Time		t_r	—	130	—	
Turn–Off Delay Time		$t_{d(off)}$	—	38	—	
Fall Time		t_f	—	47	—	
Gate Charge	(V_{DS} = 16 Vdc, I_D = 3.8 Adc, V_{GS} = 4.5 Vdc)	Q_T	—	12	17	nC
		Q_1	—	1.0	—	
		Q_2	—	5.0	—	
		Q_3	—	3.5	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 3.8 Adc, V_{GS} = 0 Vdc) (1)	V_{SD}				Vdc
	(I_S = 3.8 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.83	1.0	
			—	0.68	—	
Reverse Recovery Time	(I_S = 3.8 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (1)	t_{rr}	—	46	—	ns
		t_a	—	23	—	
		t_b	—	23	—	
Reverse Recovery Storage Charge		Q_{RR}	—	0.05	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

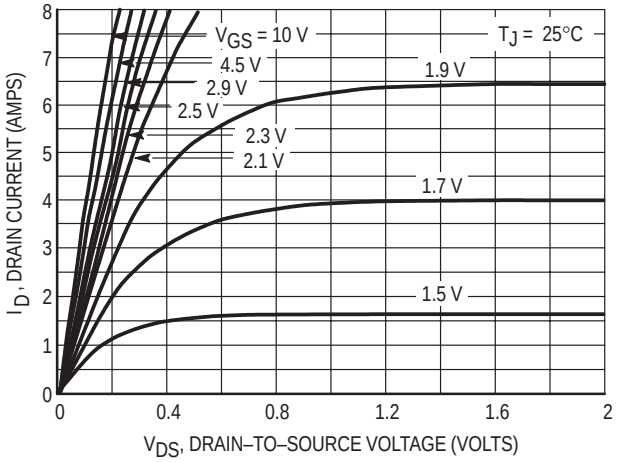


Figure 1. On–Region Characteristics

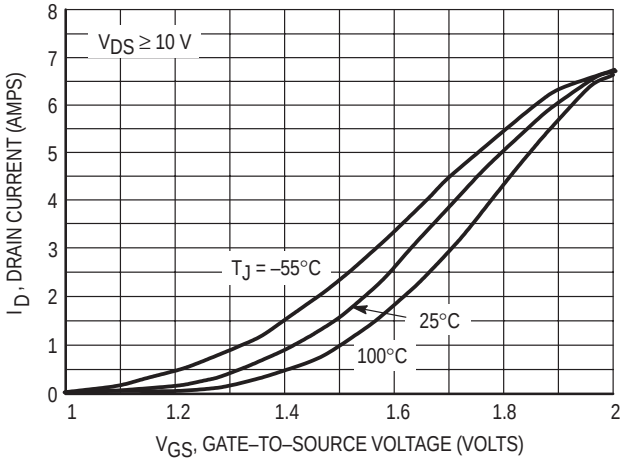


Figure 2. Transfer Characteristics

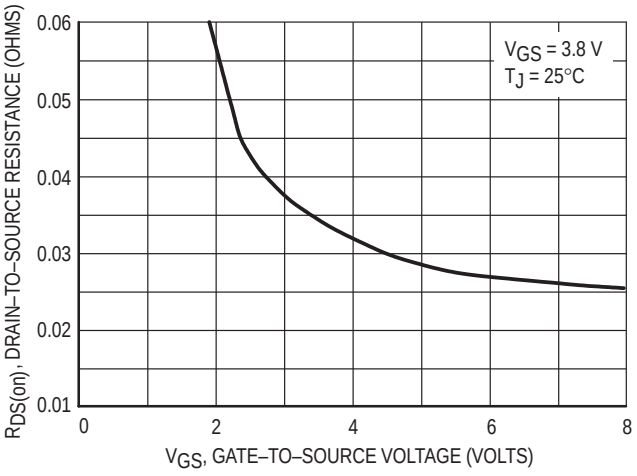


Figure 3. On–Resistance versus Gate–to–Source Voltage

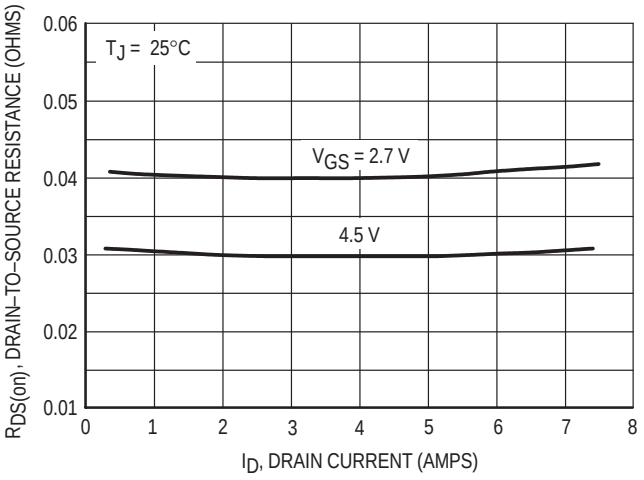


Figure 4. On–Resistance versus Drain Current and Gate Voltage

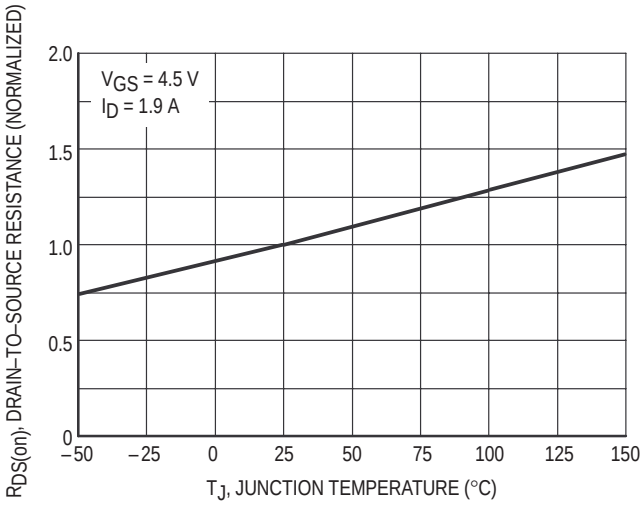


Figure 5. On–Resistance Variation with Temperature

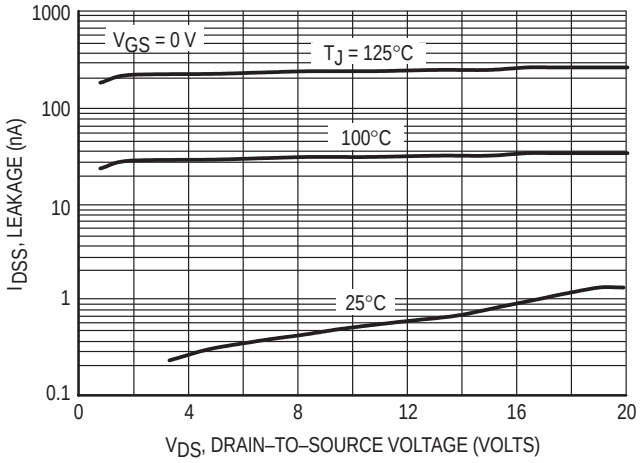


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

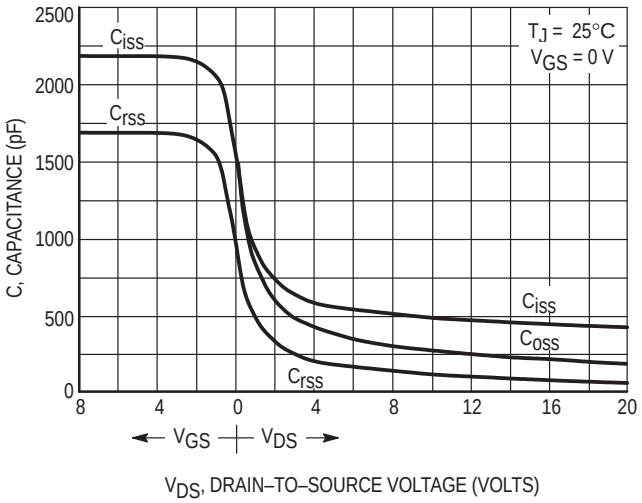


Figure 7. Capacitance Variation

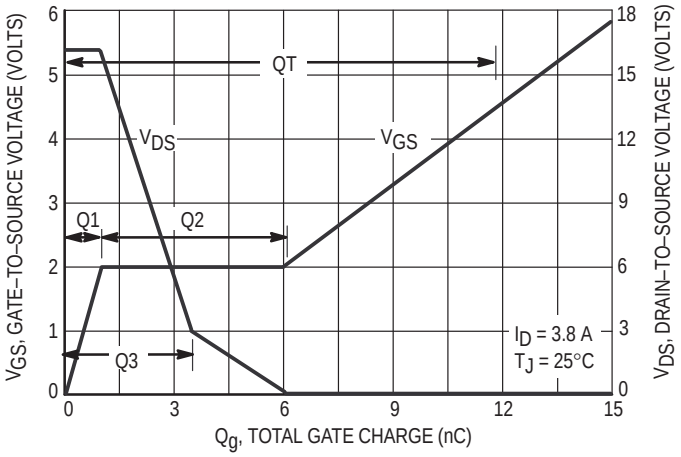


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

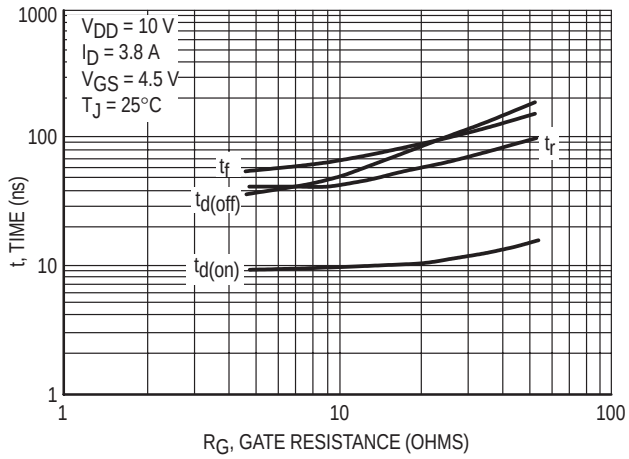


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

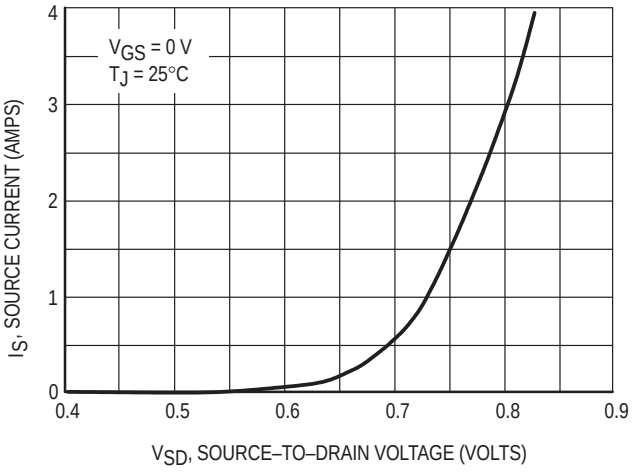


Figure 10. Diode Forward Voltage versus Current

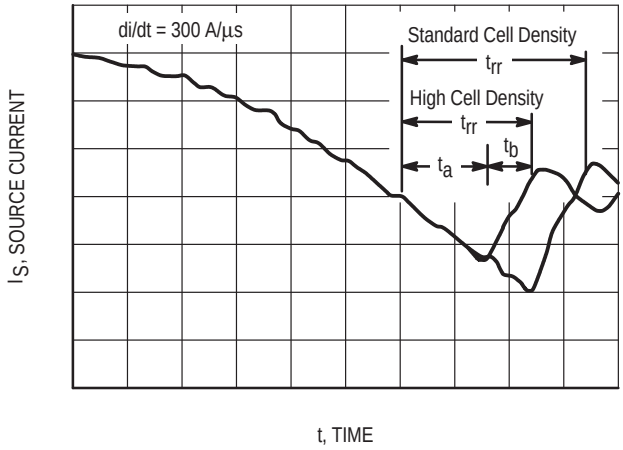


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

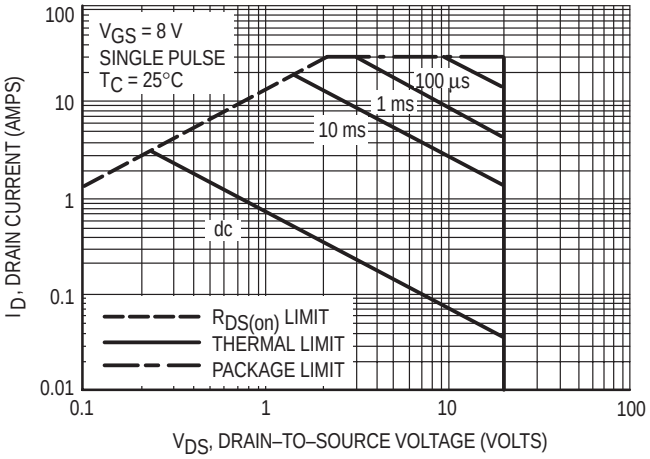


Figure 12. Maximum Rated Forward Biased Safe Operating Area

TYPICAL ELECTRICAL CHARACTERISTICS

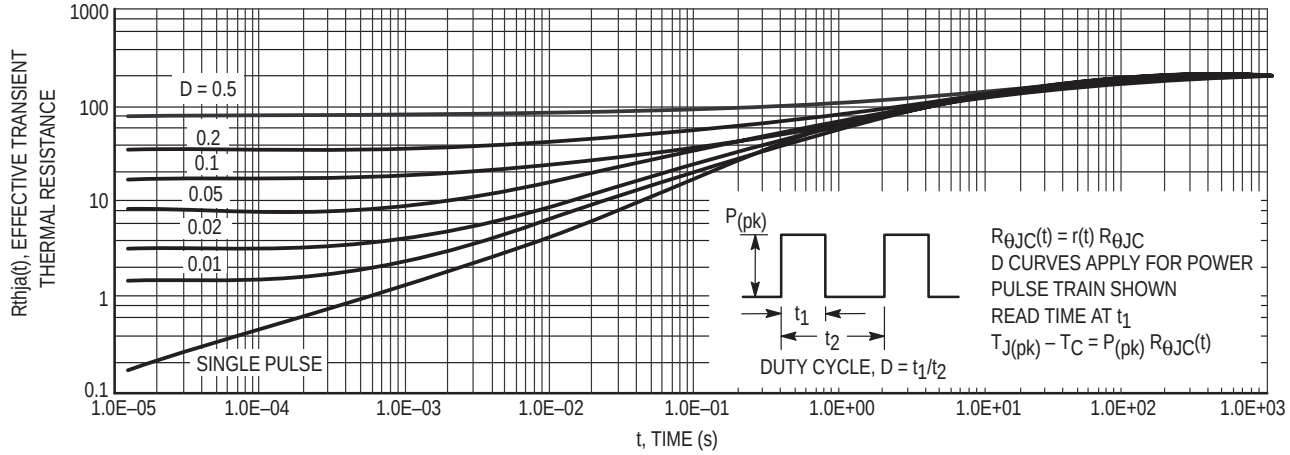


Figure 13. Thermal Response

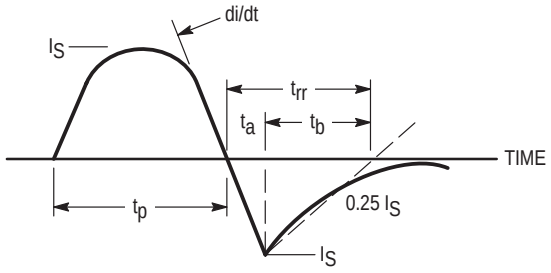
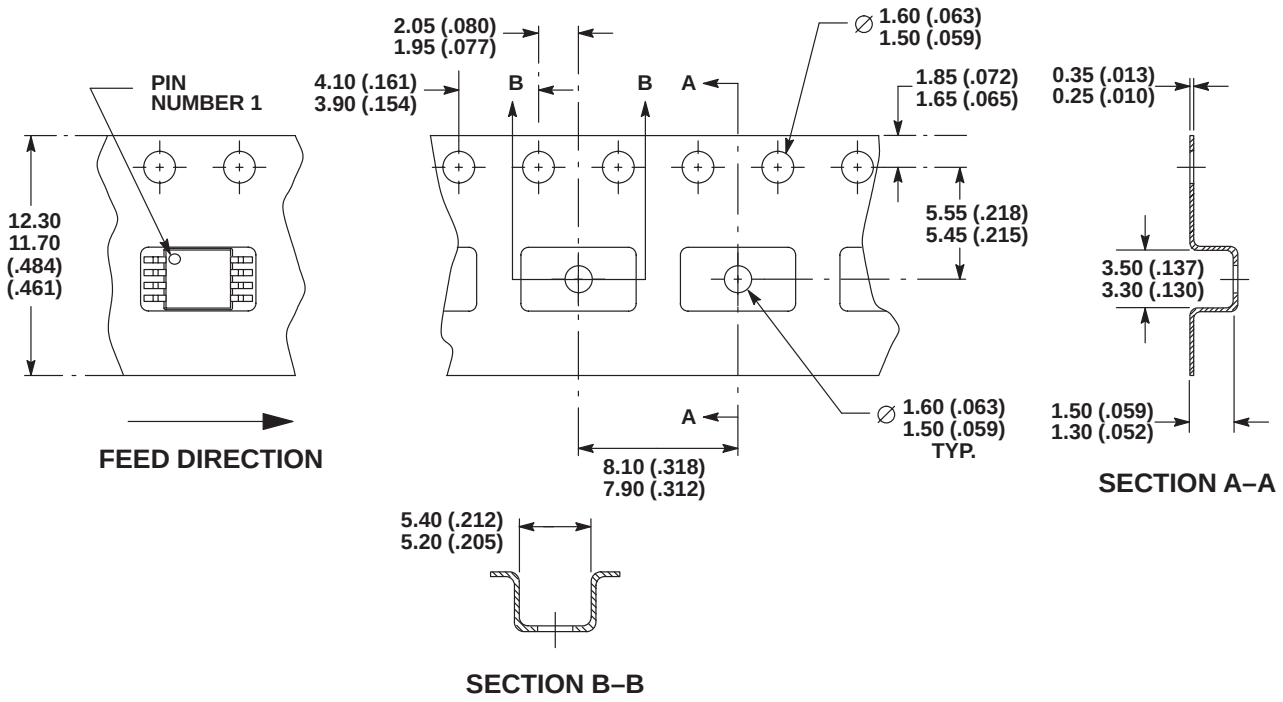


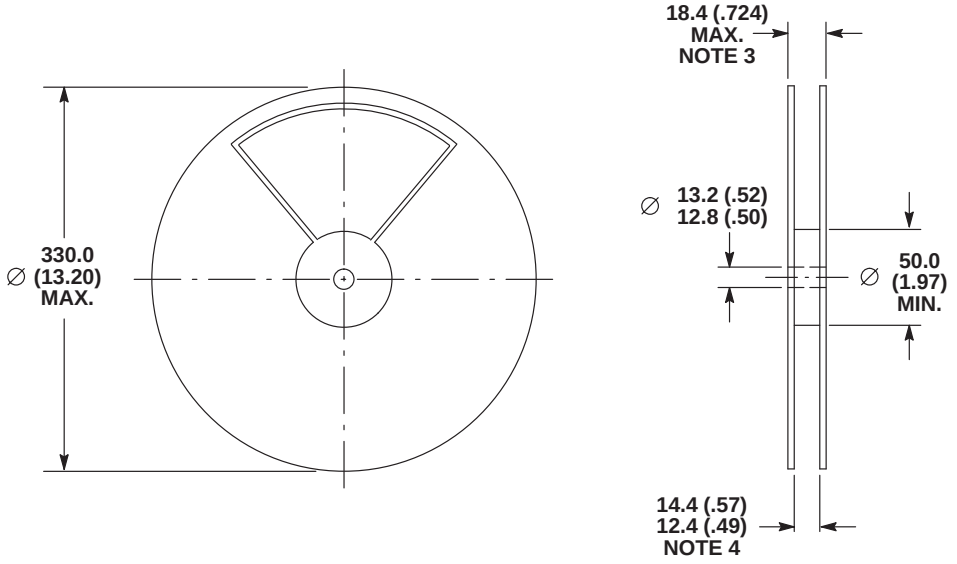
Figure 14. Diode Reverse Recovery Waveform

TAPE & REEL INFORMATION

Micro8
Dimensions are shown in millimeters (inches)



NOTES:
1. **CONFORMS TO EIA–481–1.**
2. **CONTROLLING DIMENSION: MILLIMETER.**



NOTES:
1. **CONFORMS TO EIA–481–1.**
2. **CONTROLLING DIMENSION: MILLIMETER.**
3. **INCLUDES FLANGE DISTORTION AT OUTER EDGE.**
4. **DIMENSION MEASURED AT INNER HUB.**

Advance Information

Medium Power Surface Mount Products

TMOS Single N-Channel Field Effect Transistor

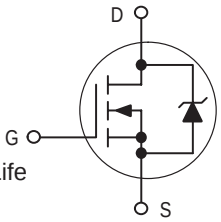
MTSF3N03HD

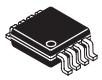
Motorola Preferred Device

SINGLE TMOS POWER MOSFET 3.7 AMPERES 30 VOLTS $R_{DS(on)}$ = 0.040 OHM

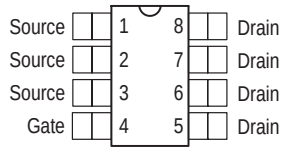
Micro8™ devices are an advanced series of power MOSFETs which utilize Motorola's High Cell Density HDTMOS process to achieve lowest possible on–resistance per silicon area. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Micro8™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Miniature Micro8 Surface Mount Package — Saves Board Space
- Extremely Low Profile (<1.1mm) for thin applications such as PCMCIA cards
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive — Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for Micro8 Package Provided





CASE 846A–02, Style 1
Micro8



Top View

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	30	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	30	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous @ T_A = 25°C (2) — Continuous @ T_A = 70°C (2) — Pulsed Drain Current (3)	I_D I_D I_{DM}	3.7 3.2 30	Adc Apk
Total Power Dissipation @ T_A = 25°C (1) Linear Derating Factor (1)	P_D	1.8 14.3	Watts mW/°C
Total Power Dissipation @ T_A = 25°C (2) Linear Derating Factor (2)	P_D	0.78 6.25	Watts mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	– 55 to 150	°C

THERMAL RESISTANCE

Rating	Symbol	Typ.	Max.	Unit
Thermal Resistance — Junction to Ambient, PCB Mount (1) — Junction to Ambient, PCB Mount (2)	$R_{\theta JA}$ $R_{\theta JA}$	55 125	70 160	°C/W

(1) When mounted on 1 inch square FR–4 or G–10 board (V_{GS} = 10 V, @ Steady State)
(2) When mounted on minimum recommended FR–4 or G–10 board (V_{GS} = 10 V, @ Steady State)
(3) Repetitive rating; pulse width limited by maximum junction temperature.

DEVICE MARKING

AA

ORDERING INFORMATION

Device	Reel Size	Tape Width	Quantity
MTSF3N03HDR2	13″	12 mm embossed tape	4000 units

This document contains information on a new product. Specifications and information are subject to change without notice.
Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (1) (3)		$V_{(BR)DSS}$				Vdc
(V_{GS} = 0 Vdc, I_D = 250 μAdc)			30	—	—	
Temperature Coefficient (Positive)			—	27	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc)			—	—	1.0	
(V_{DS} = 24 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	25	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)						
Gate Threshold Voltage (Cpk ≥ 2.0) (3)		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 250 μAdc)			1.0	1.5	—	
Threshold Temperature Coefficient (Negative)			—	4.5	—	mV/°C
Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (3)		$R_{DS(on)}$				mΩ
(V_{GS} = 10 Vdc, I_D = 3.7 Adc)			—	35	40	
(V_{GS} = 4.5 Vdc, I_D = 1.9 Adc)			—	45	60	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 1.9 Adc)		g_{FS}	2.0	—	—	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	420	—	pF
Output Capacitance		C_{oss}	—	190	—	
Transfer Capacitance		C_{rss}	—	65	—	
SWITCHING CHARACTERISTICS(2)						
Turn–On Delay Time	(V_{DS} = 15 Vdc, I_D = 3.7 Adc, V_{GS} = 10 Vdc, R_G = 6 Ω) (1)	$t_{d(on)}$	—	7.0	—	ns
Rise Time		t_r	—	19	—	
Turn–Off Delay Time		$t_{d(off)}$	—	32	—	
Fall Time		t_f	—	36	—	
Turn–On Delay Time	(V_{DD} = 15 Vdc, I_D = 1.9 Adc, V_{GS} = 4.5 Vdc, R_G = 6 Ω) (1)	$t_{d(on)}$	—	7.0	—	ns
Rise Time		t_r	—	11	—	
Turn–Off Delay Time		$t_{d(off)}$	—	29	—	
Fall Time		t_f	—	23	—	
Gate Charge	(V_{DS} = 24 Vdc, I_D = 3.7 Adc, V_{GS} = 10 Vdc)	Q_T	—	18.5	26	nC
		Q_1	—	1.4	—	
		Q_2	—	5.5	—	
		Q_3	—	7.1	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 3.7 Adc, V_{GS} = 0 Vdc) (1)	V_{SD}				Vdc
	(I_S = 3.7 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.82	1.0	
			—	0.7	—	
Reverse Recovery Time	(I_S = 3.7 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (1)	t_{rr}	—	28	—	ns
		t_a	—	14	—	
		t_b	—	14	—	
Reverse Recovery Storage Charge		Q_{RR}	—	0.028	—	μC

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{3 \times \text{SIGMA}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

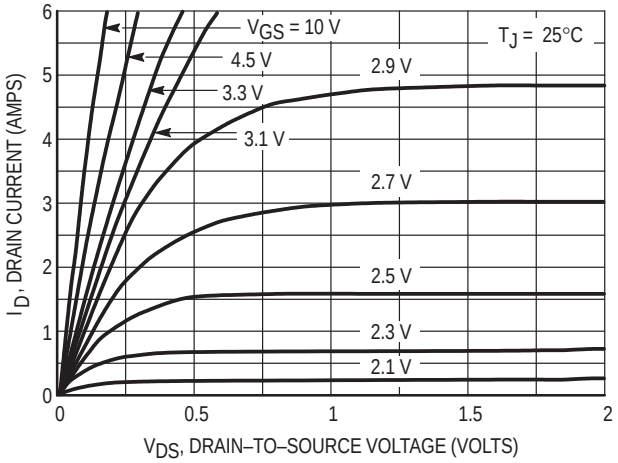


Figure 1. On–Region Characteristics

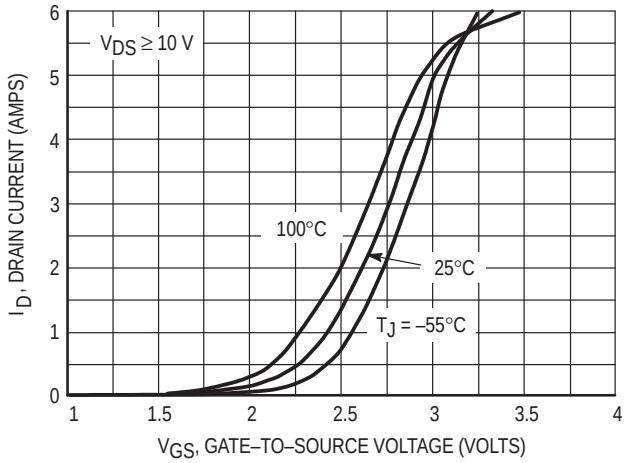


Figure 2. Transfer Characteristics

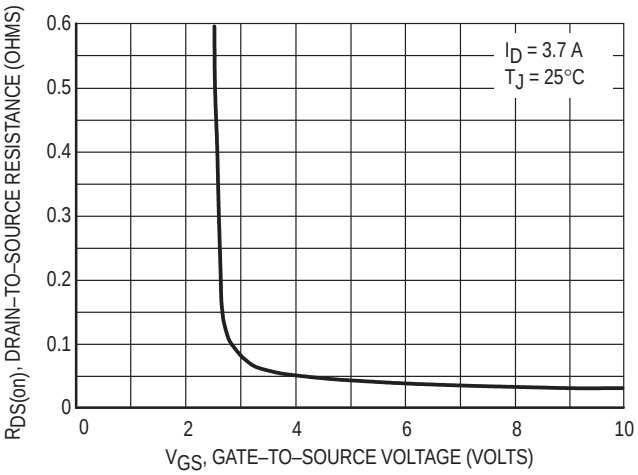


Figure 3. On–Resistance versus Gate–to–Source Voltage

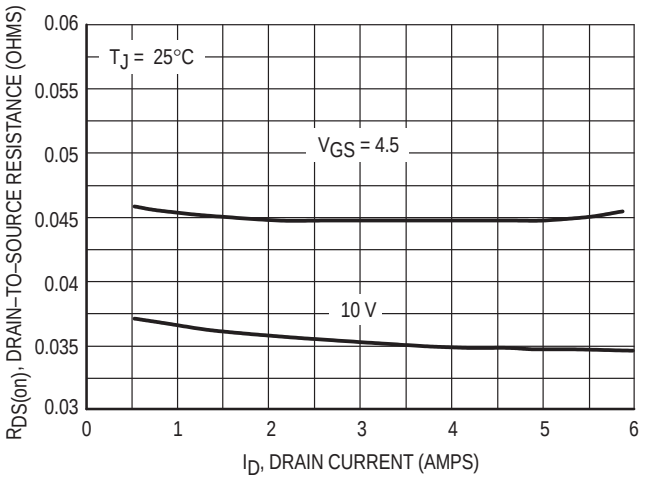


Figure 4. On–Resistance versus Drain Current and Gate Voltage

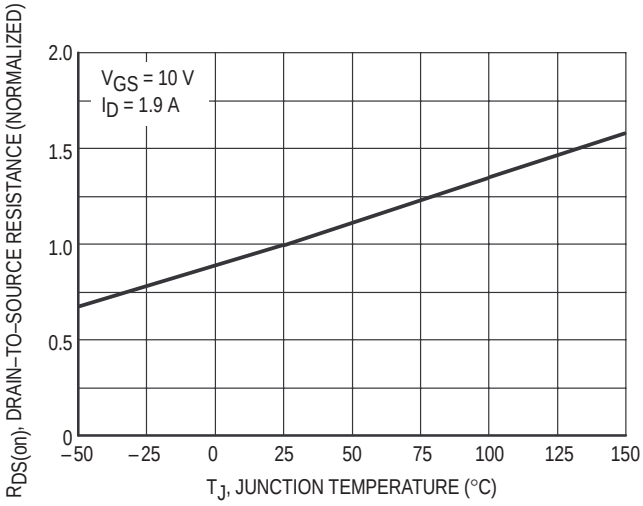


Figure 5. On–Resistance Variation with Temperature

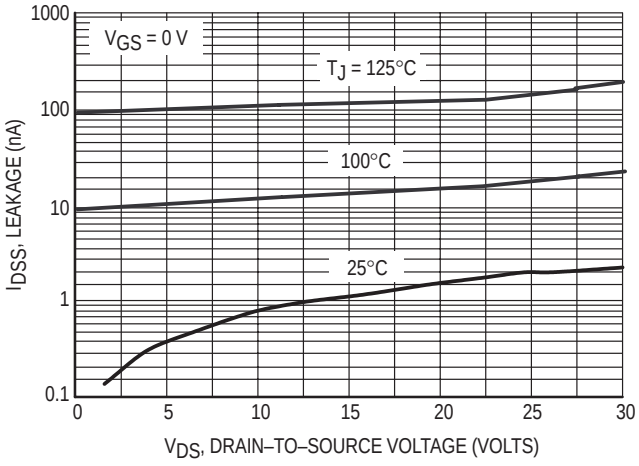


Figure 6. Drain–to–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

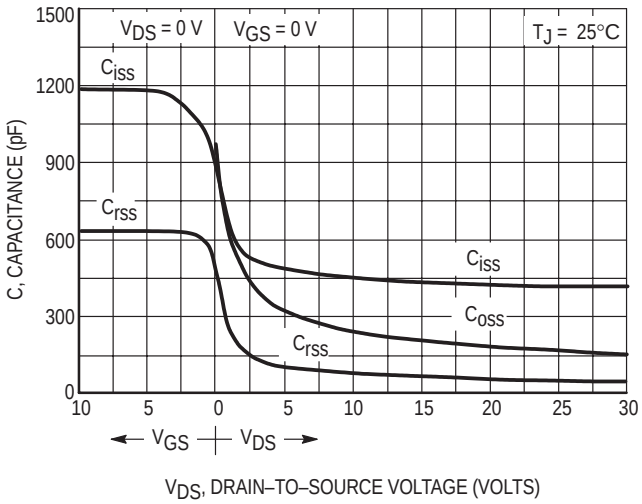


Figure 7. Capacitance Variation

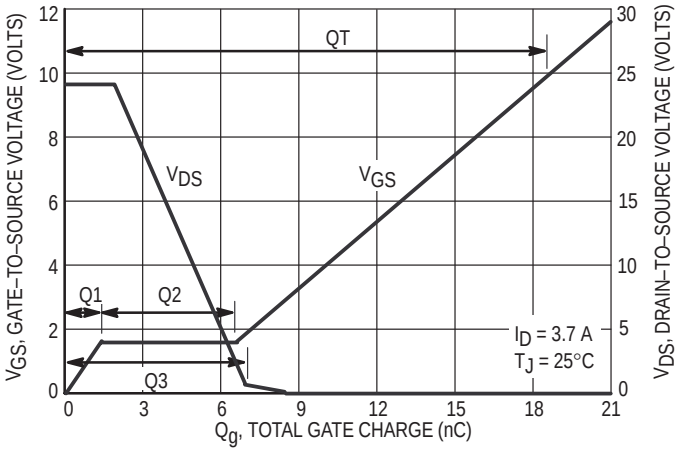


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

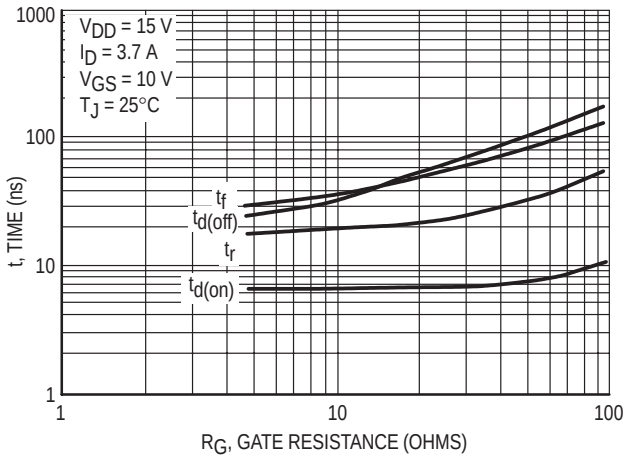


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

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System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, t_{rr}, due to the storage of minority carrier charge, Q_{RR}, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short t_{rr} and low Q_{RR} specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during t_a is directly controlled by the device clearing the stored charge. However, the positive di/dt during t_b is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of t_b/t_a serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to Motorola standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter t_{rr}), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

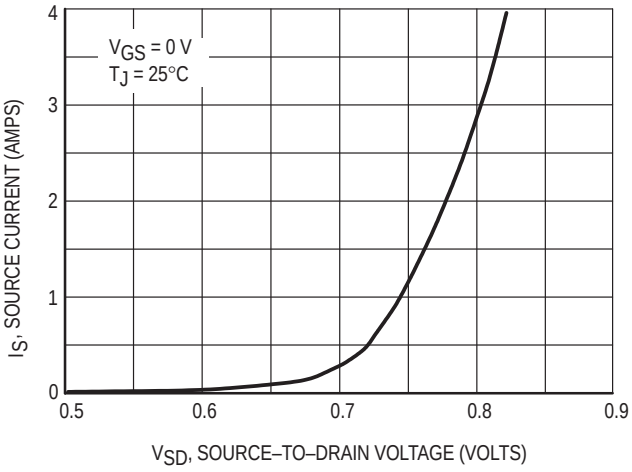


Figure 10. Diode Forward Voltage versus Current

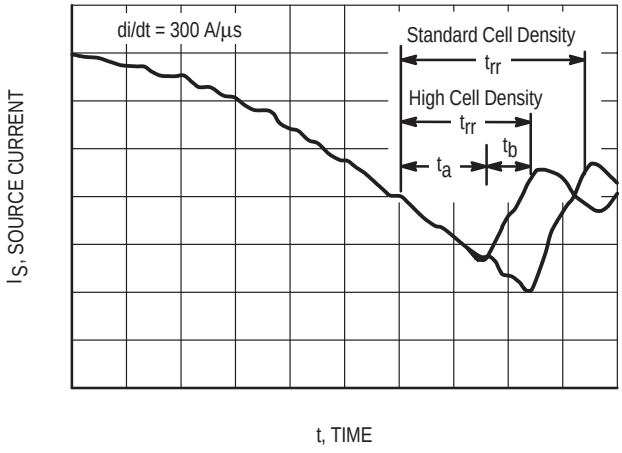


Figure 11. Reverse Recovery Time (t_{rr})

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curve (Figure 12) defines the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded, and that the transition time (t_r, t_f) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

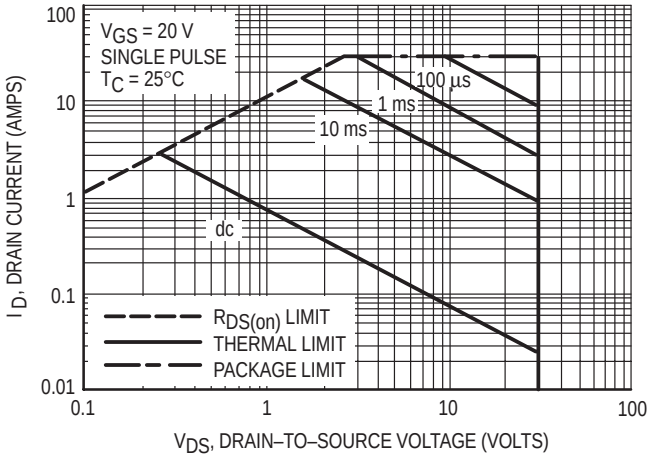


Figure 12. Maximum Rated Forward Biased Safe Operating Area

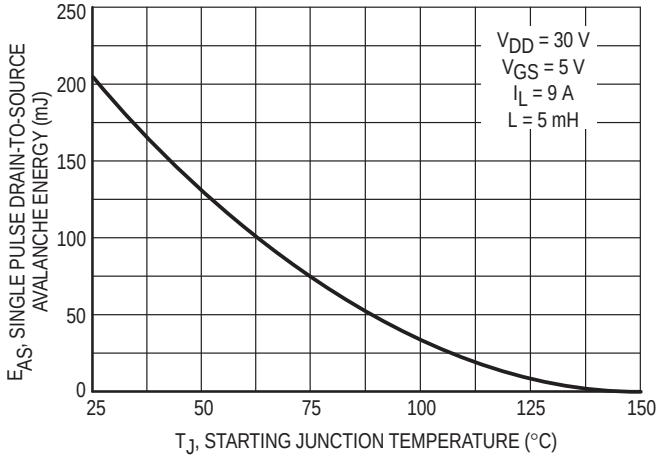


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

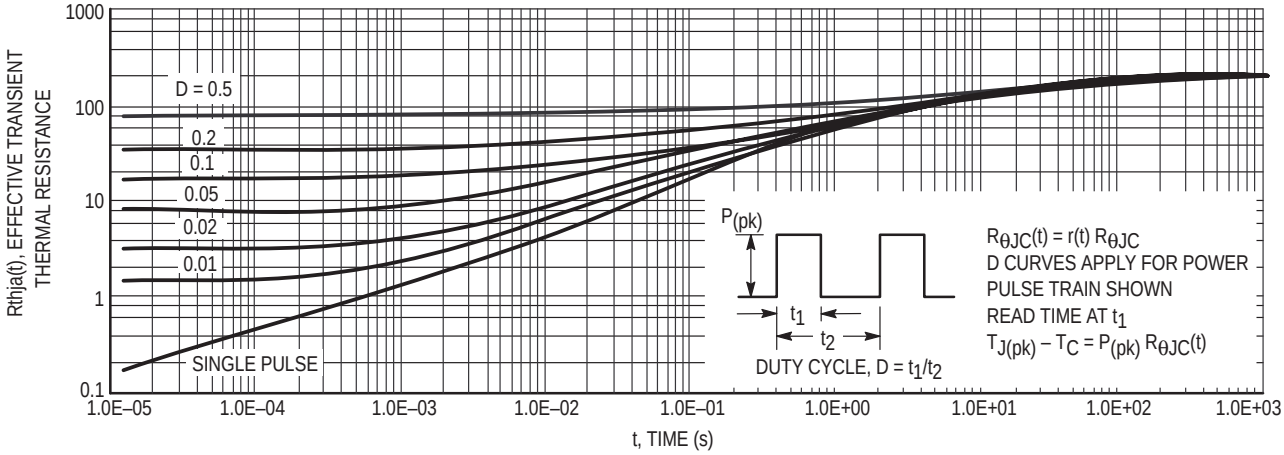


Figure 14. Thermal Response

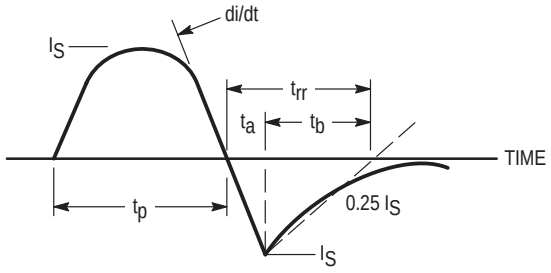
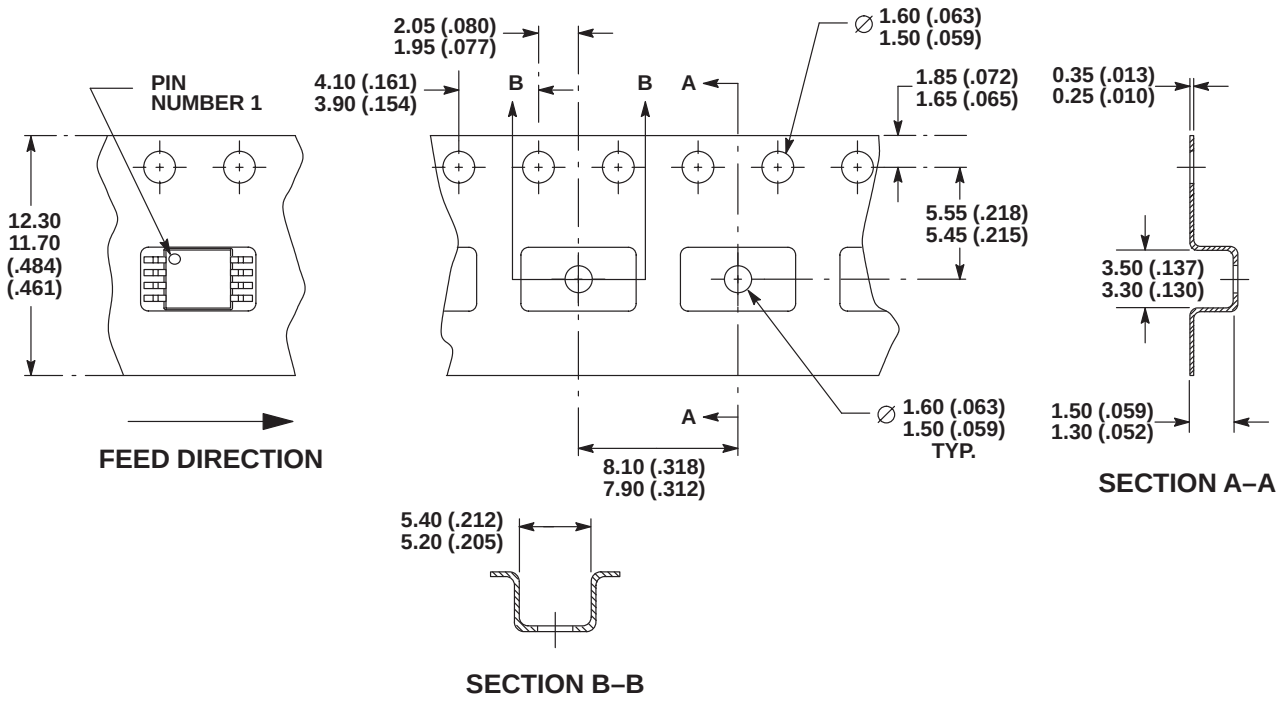


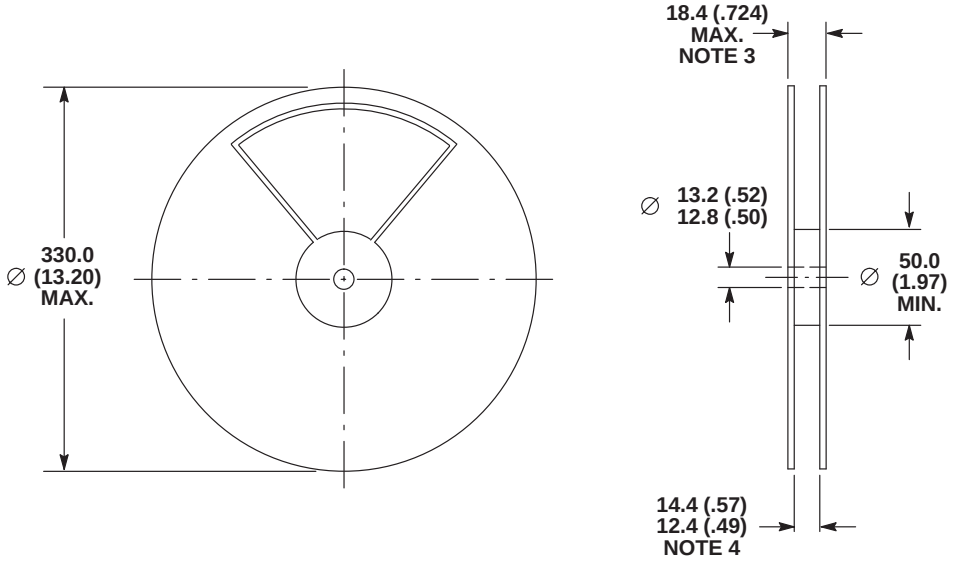
Figure 15. Diode Reverse Recovery Waveform

TAPE & REEL INFORMATION

Micro8
Dimensions are shown in millimeters (inches)



NOTES:
1. **CONFORMS TO EIA–481–1.**
2. **CONTROLLING DIMENSION: MILLIMETER.**



NOTES:
1. **CONFORMS TO EIA–481–1.**
2. **CONTROLLING DIMENSION: MILLIMETER.**
3. **INCLUDES FLANGE DISTORTION AT OUTER EDGE.**
4. **DIMENSION MEASURED AT INNER HUB.**

Designer's™ Data Sheet

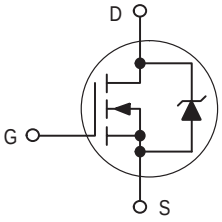
TMOS E-FET ™
Power Field Effect Transistor
D3PAK for Surface Mount

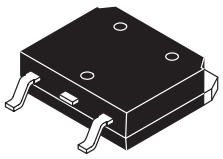
N–Channel Enhancement–Mode Silicon Gate

MTV6N100E

TMOS POWER FET
6.0 AMPERES
1000 VOLTS
$R_{DS(on)}$ = 1.5 OHM

The D3PAK package has the capability of housing the largest chip size of any standard, plastic, surface mount power semiconductor. This allows it to be used in applications that require surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in surface mount PWM motor controls and both ac–dc and dc–dc power supplies. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 433–01, Style 2
D3PAK Surface Mount

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specifically Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm, 13–inch/500 Unit Tape & Reel, Add –RL Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	1000	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	1000	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	6.0 4.2 18	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_C = 25°C (1)	P_D	178 1.43 2.0	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 6.0 Apk, L = 27.77 mH, R_G = 25 Ω)	E_{AS}	 720	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	0.70 62.5 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	1000	—	—	Vdc
Temperature Coefficient (Positive)			—	1270	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	—	1.28	1.5	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 6.0 Adc)		$V_{DS(on)}$	—	7.9	14.4	Vdc
(V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J = 125°C)			—	—	9.5	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3.0 Adc)		g_{FS}	4.0	7.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3000	4210	pF
Output Capacitance		C_{oss}	—	219	440	
Transfer Capacitance		C_{rss}	—	43	90	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 500 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	27	45	ns
Rise Time		t_r	—	29	65	
Turn–Off Delay Time		$t_{d(off)}$	—	93	170	
Fall Time		t_f	—	43	95	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	66	100	nC
		Q_1	—	12.5	—	
		Q_2	—	25.9	—	
		Q_3	—	26	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 6.0 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.81	1.0	Vdc
	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.64	—	
Reverse Recovery Time	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	735	—	ns
		t_a	—	188	—	
		t_b	—	547	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4.7	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

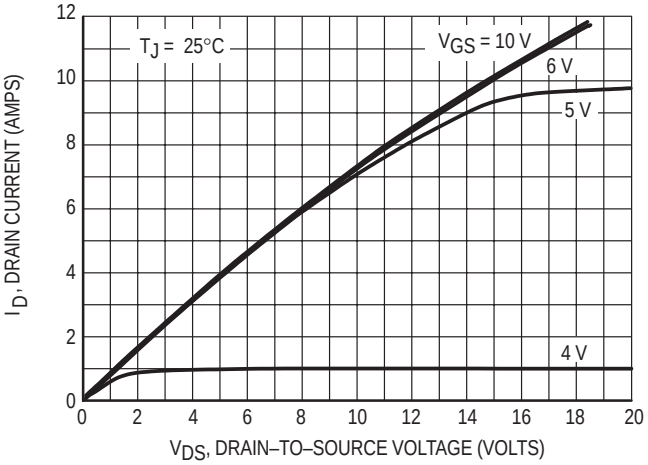


Figure 1. On–Region Characteristics

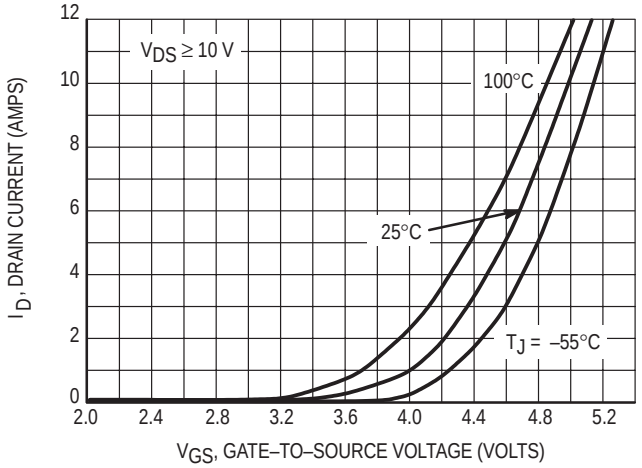


Figure 2. Transfer Characteristics

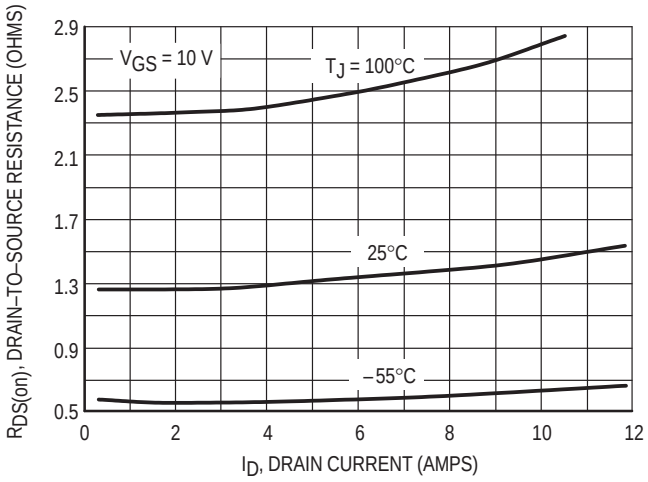


Figure 3. On–Resistance versus Drain Current and Temperature

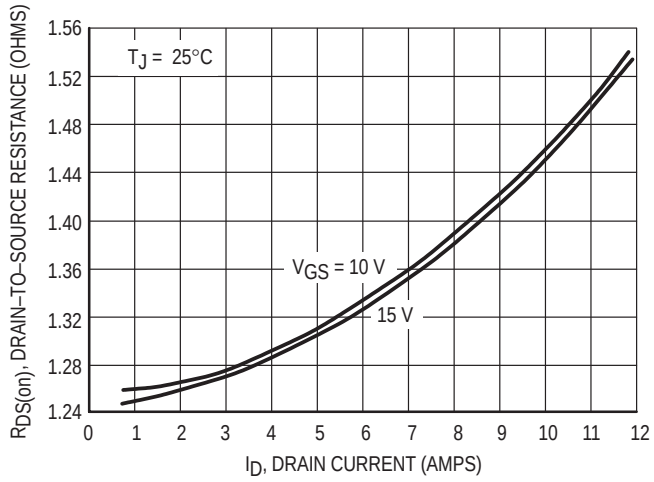


Figure 4. On–Resistance versus Drain Current and Gate Voltage

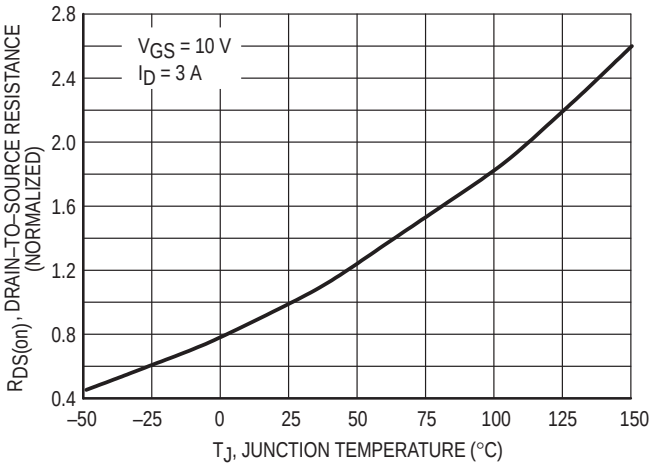


Figure 5. On–Resistance Variation with Temperature

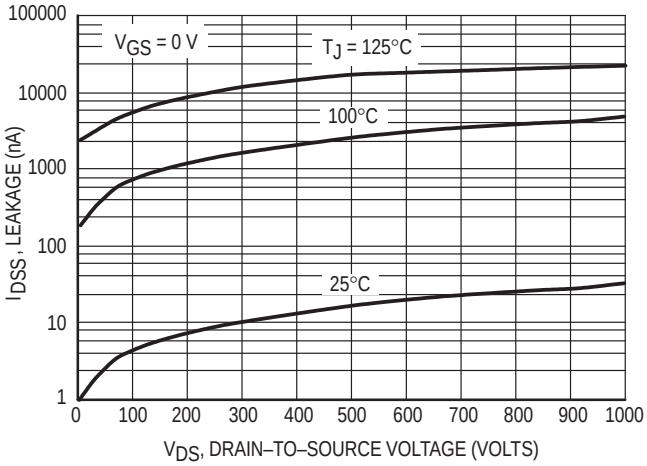


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

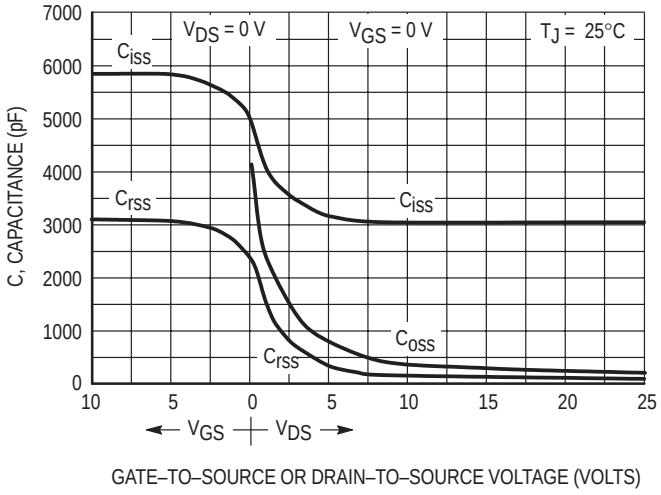


Figure 7a. Capacitance Variation

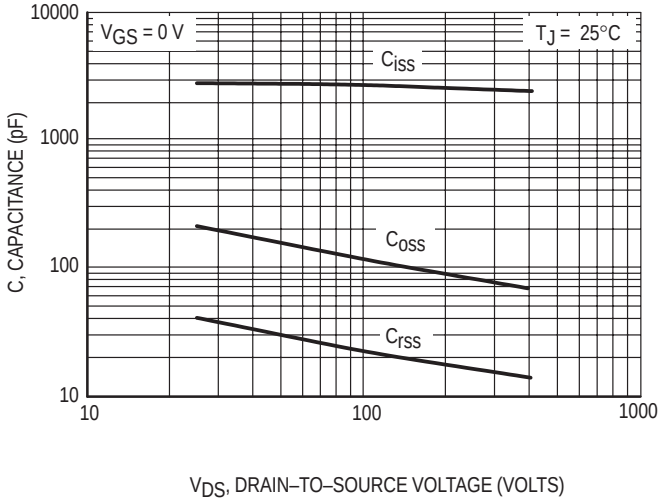


Figure 7b. High Voltage Capacitance Variation

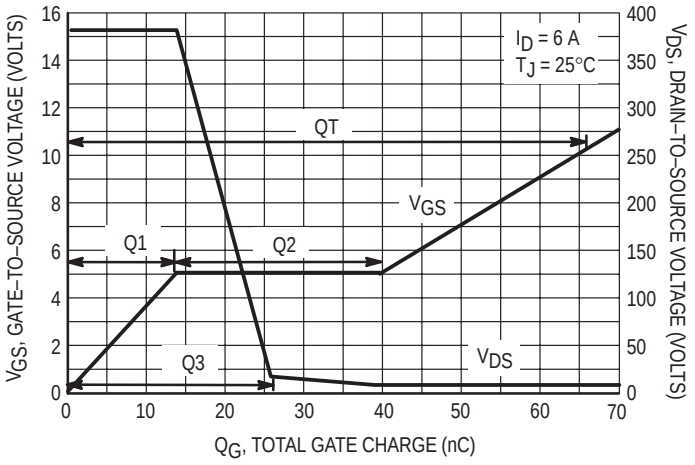


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

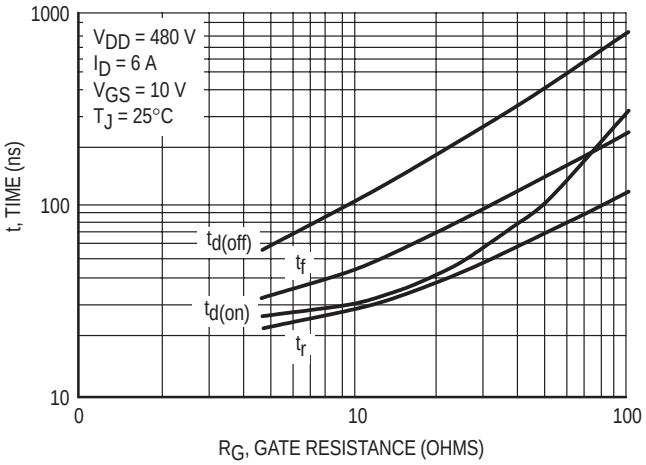


Figure 9. Resistive Switching Time Variation versus Gate Resistance

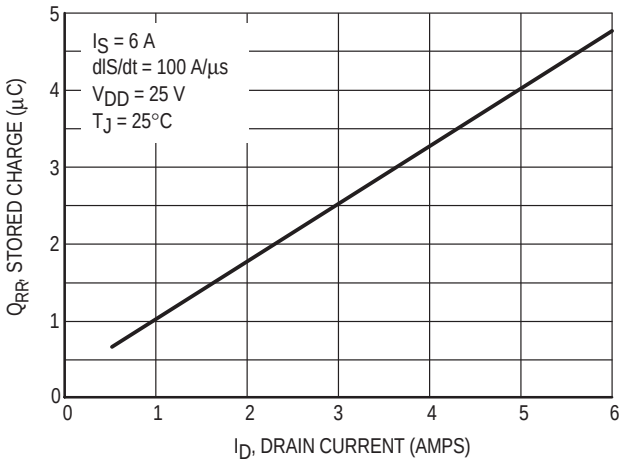


Figure 10. Stored Charge

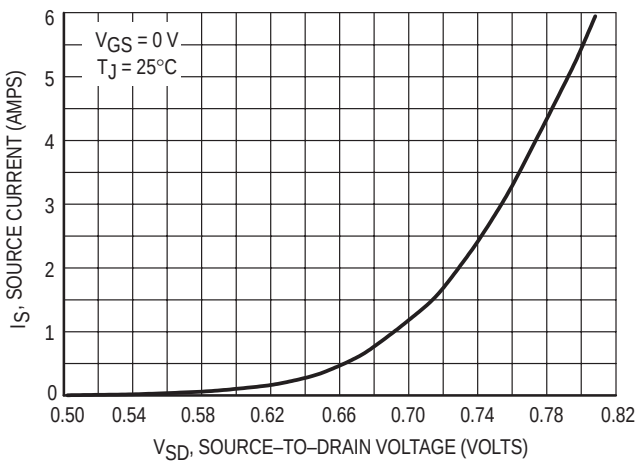


Figure 11. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

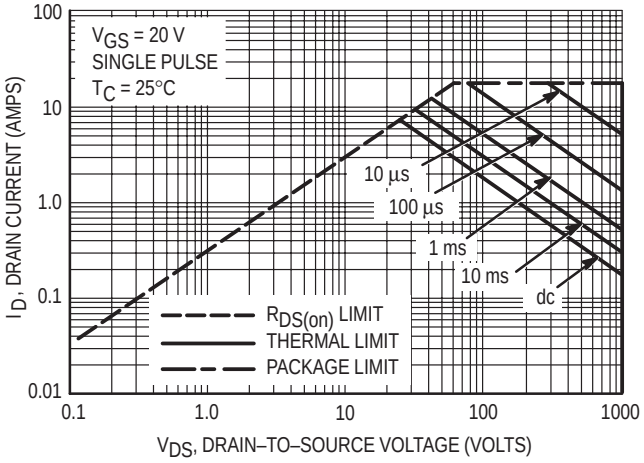


Figure 12. Maximum Rated Forward Biased Safe Operating Area

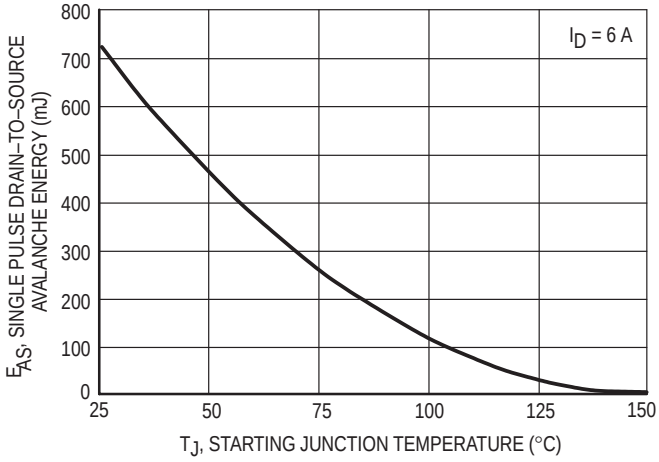


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

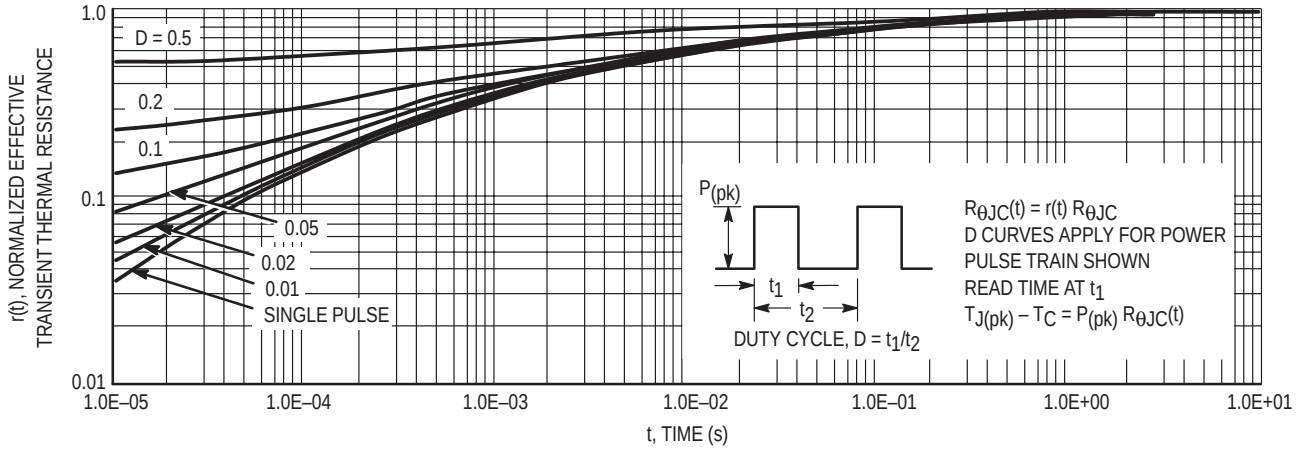


Figure 14. Thermal Response

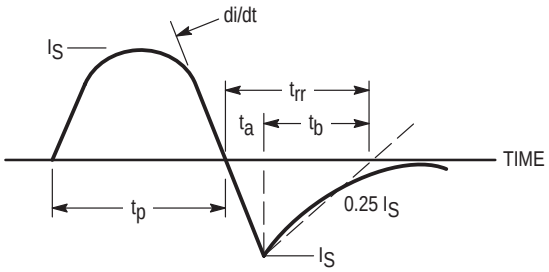


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

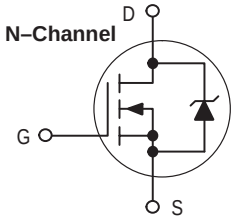
TMOS E-FET ™
Power Field Effect Transistor
D3PAK for Surface Mount

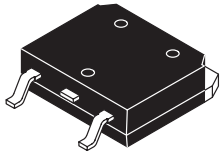
N–Channel Enhancement–Mode Silicon Gate

MTV10N100E

TMOS POWER FET
10 AMPERES
1000 VOLTS
$R_{DS(on)}$ = 1.3 OHM

The D3PAK package has the capability of housing the largest chip size of any standard, plastic, surface mount power semiconductor. This allows it to be used in applications that require surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in surface mount PWM motor controls and both ac–dc and dc–dc power supplies. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 433–01, Style 2
D3PAK Surface Mount

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specifically Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm, 13–inch/500 Unit Tape & Reel, Add –RL Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	1000	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	1000	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	10 6.2 30	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_C = 25°C (1)	P_D	250 2.0 3.57	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 10 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	 500	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	0.5 62.5 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	1000	—	—	Vdc
Temperature Coefficient (Positive)			—	1254	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc)		$R_{DS(on)}$	—	1.07	1.3	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 10 Adc)		$V_{DS(on)}$	—	11	15	Vdc
(V_{GS} = 10 Vdc, I_D = 5.0 Adc, T_J = 125°C)			—	—	15.3	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 5.0 Adc)		g_{FS}	8.0	10	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3500	5600	pF
Output Capacitance		C_{oss}	—	264	530	
Transfer Capacitance		C_{rss}	—	52	90	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 500 Vdc, I_D = 10 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	29	60	ns
Rise Time		t_r	—	57	120	
Turn–Off Delay Time		$t_{d(off)}$	—	118	240	
Fall Time		t_f	—	70	140	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 10 Adc, V_{GS} = 10 Vdc)	Q_T	—	100	120	nC
		Q_1	—	18.4	—	
		Q_2	—	33	—	
		Q_3	—	36.7	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 10 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.885	1.1	Vdc
	(I_S = 10 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.8	—	
Reverse Recovery Time	(I_S = 10 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	885	—	ns
		t_a	—	220	—	
		t_b	—	667	—	
Reverse Recovery Stored Charge		Q_{RR}	—	8.0	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

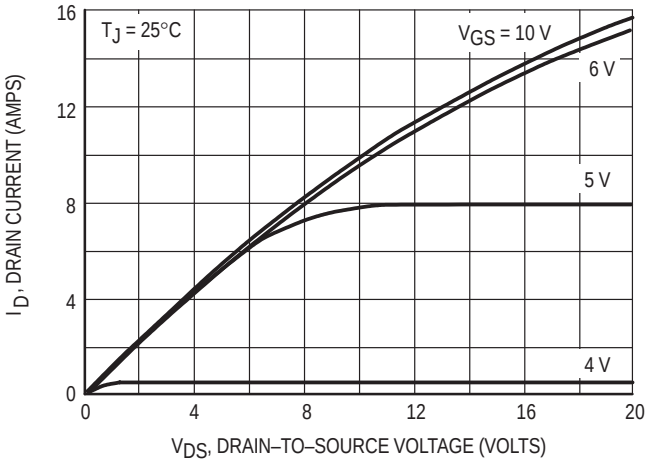


Figure 1. On–Region Characteristics

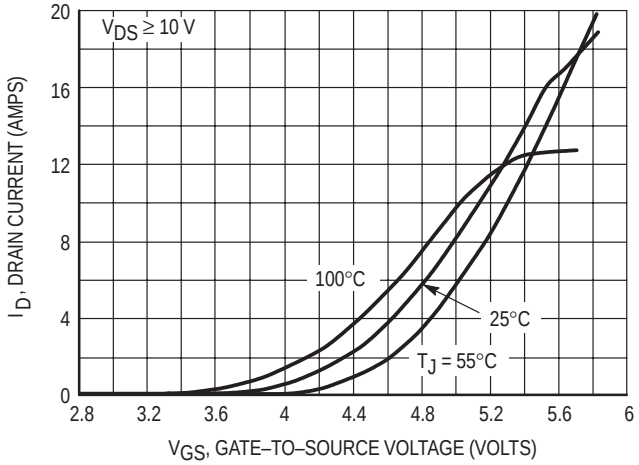


Figure 2. Transfer Characteristics

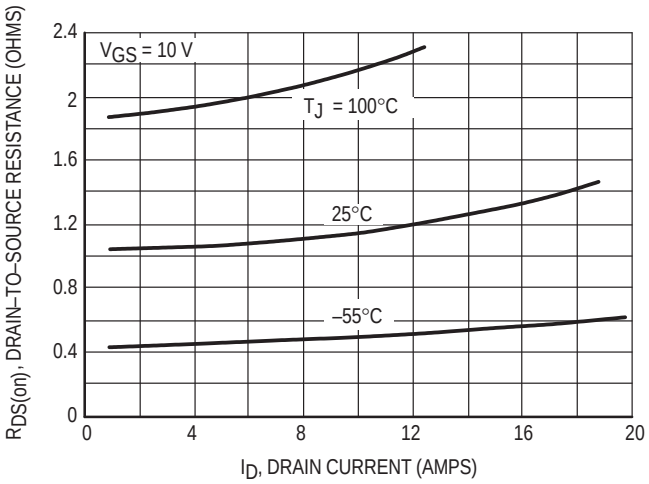


Figure 3. On–Resistance versus Drain Current and Temperature

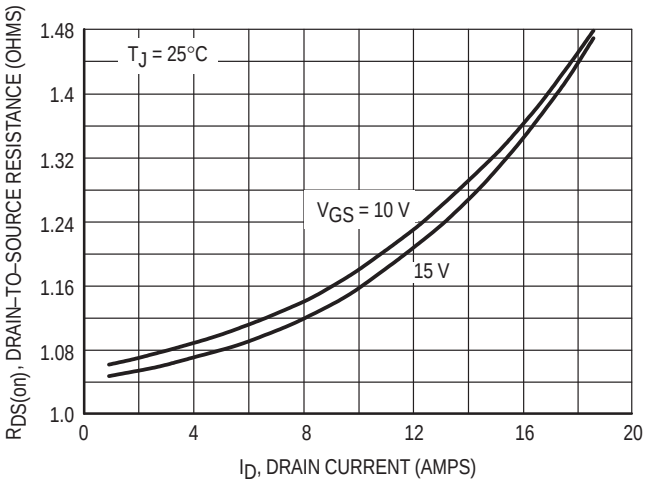


Figure 4. On–Resistance versus Drain Current and Gate Voltage

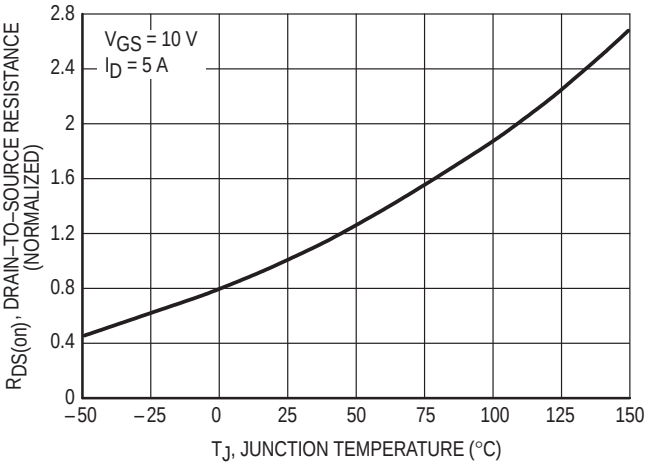


Figure 5. On–Resistance Variation with Temperature

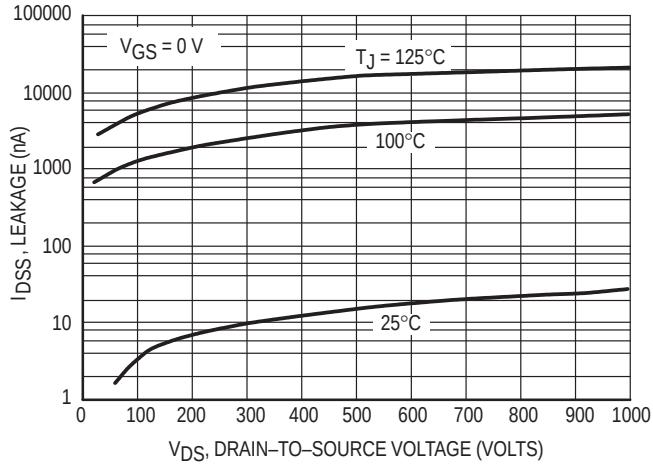


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

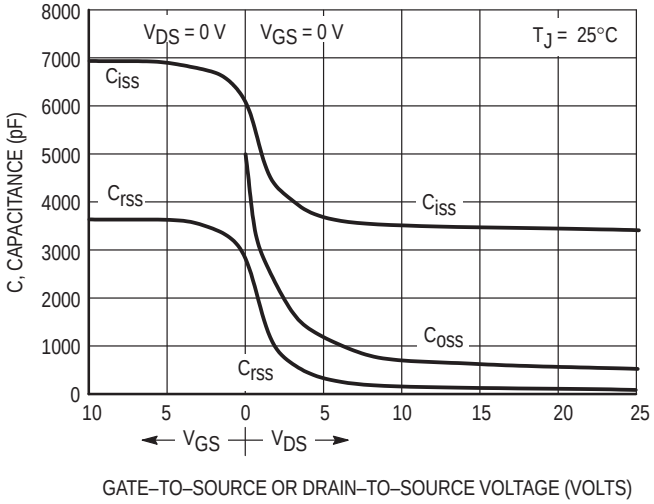


Figure 8a. Capacitance Variation

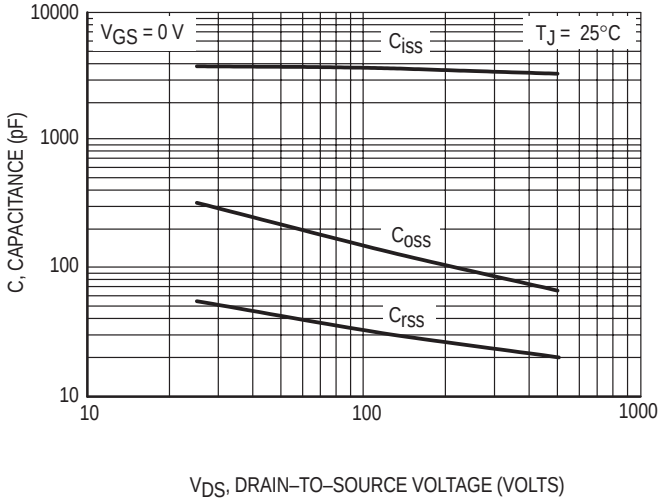


Figure 8b. High Voltage Capacitance Variation

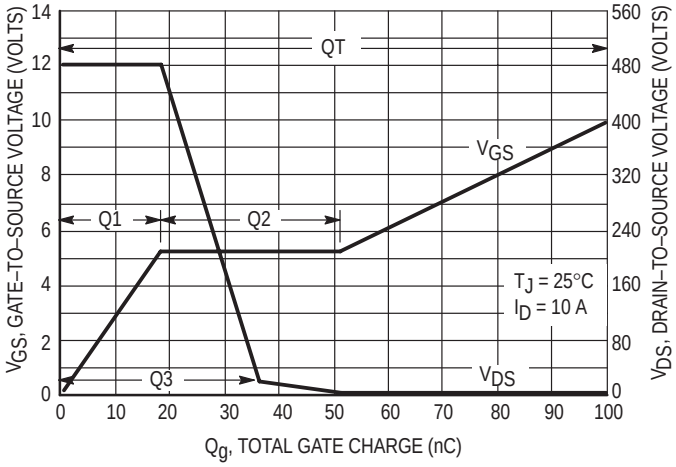


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

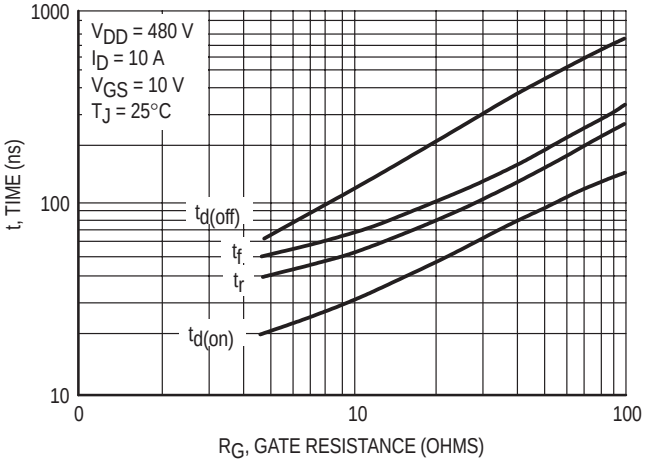


Figure 9. Resistive Switching Time Variation versus Gate Resistance

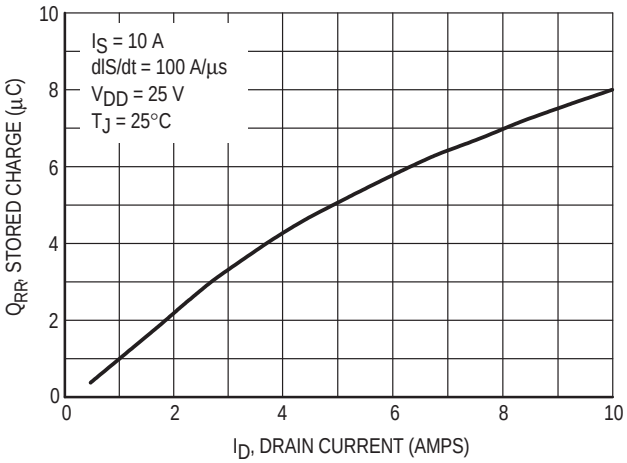


Figure 10. Stored Charge

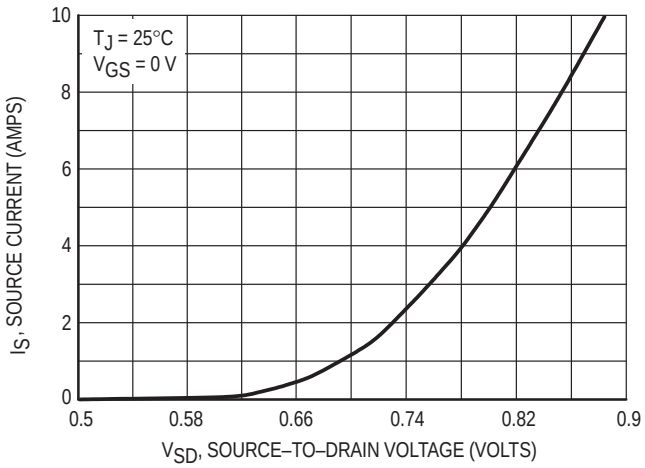


Figure 11. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

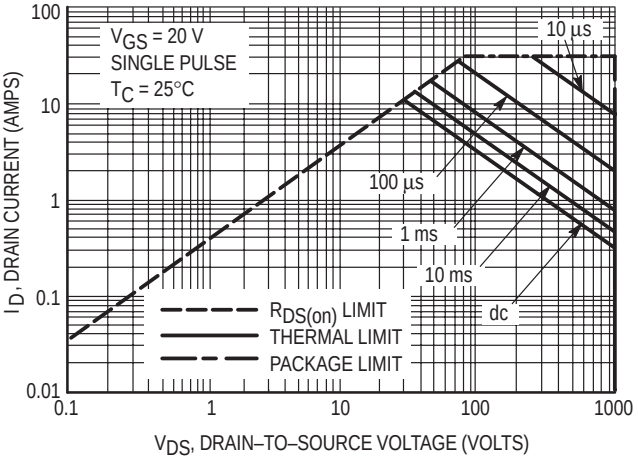


Figure 12. Maximum Rated Forward Biased Safe Operating Area

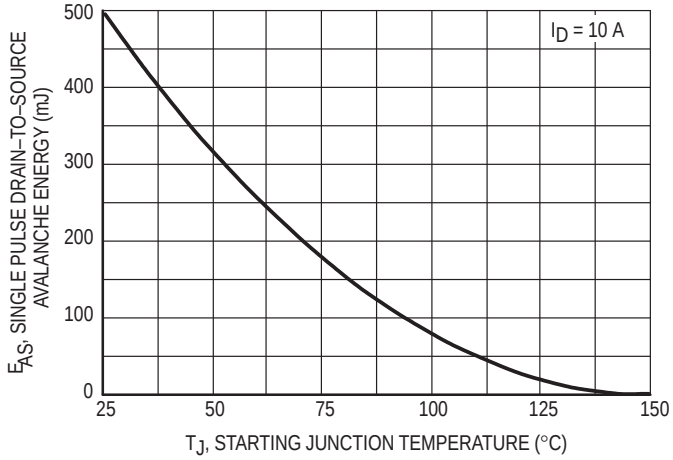


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

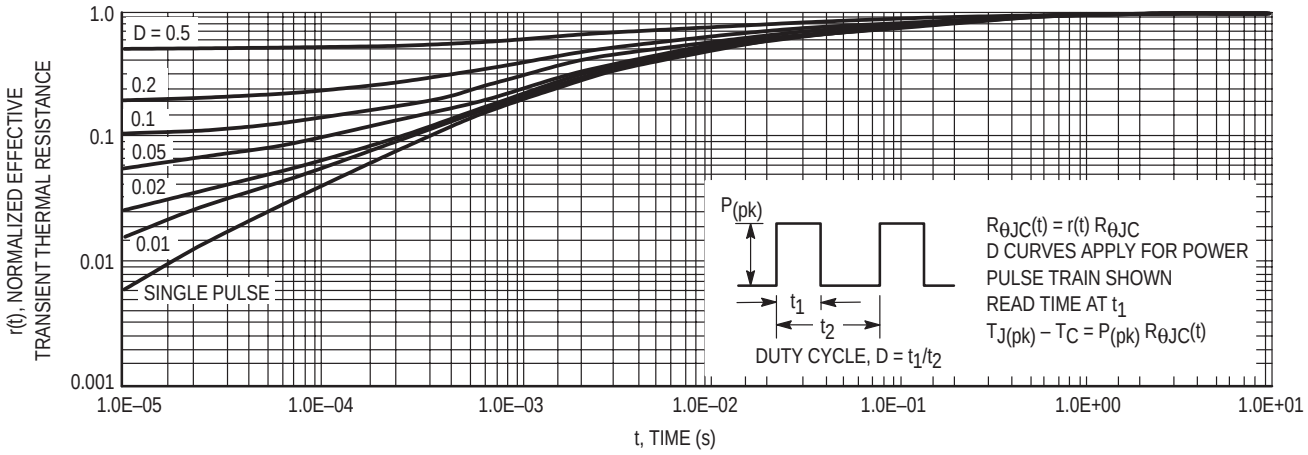


Figure 14. Thermal Response

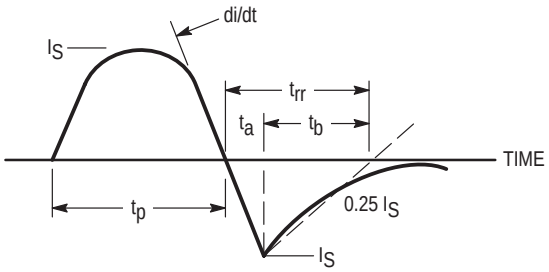


Figure 15. Diode Reverse Recovery Waveform

Advance Information

TMOS E-FET™
Power Field Effect Transistor
D³PAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

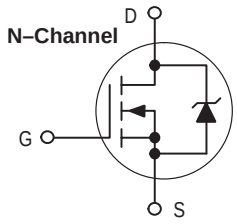
MTV16N50E

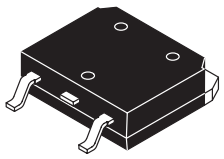
TMOS POWER FET
16 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.40 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high speed switching applications in power supplies, converters, PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature

TMOS®





CASE 433–01, Style 2
D³PAK Surface Mount

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	500	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	16 9.0 60	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	180 1.4 2.0	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, Peak I_L = 16 Apk, L = 6.7 mH, R_G = 25 Ω)	E_{AS}	 860	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	0.7 62.5 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	500	—	—	Vdc
Temperature Coefficient (Positive)			—	520	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	250	μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	1000	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.2	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 8.0 Adc)		$R_{DS(on)}$	—	0.32	0.40	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 16 Adc)		$V_{DS(on)}$	—	—	6.7	Vdc
(V_{GS} = 10 Vdc, I_D = 8.0 Adc, T_J = 125°C)			—	—	5.6	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 8.0 Adc)		g_{FS}	5.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3200	4480	pF
Output Capacitance		C_{oss}	—	400	560	
Transfer Capacitance		C_{rss}	—	320	448	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 16 Adc, V_{GS} = 10 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	28	60	ns
Rise Time		t_r	—	80	160	
Turn–Off Delay Time		$t_{d(off)}$	—	80	160	
Fall Time		t_f	—	60	120	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 16 Adc, V_{GS} = 10 Vdc)	Q_T	—	65	—	nC
		Q_1	—	17	—	
		Q_2	—	47	—	
		Q_3	—	34	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 16 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.6	Vdc
	(I_S = 16 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.9	—	
Reverse Recovery Time	(I_S = 16 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	390	—	ns
		t_a	—	245	—	
		t_b	—	145	—	
Reverse Recovery Stored Charge		Q_{RR}	—	5.35	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	5.0	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

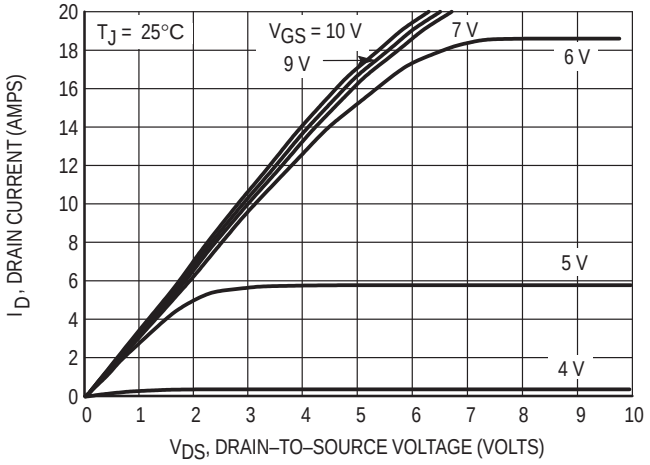


Figure 1. On–Region Characteristics

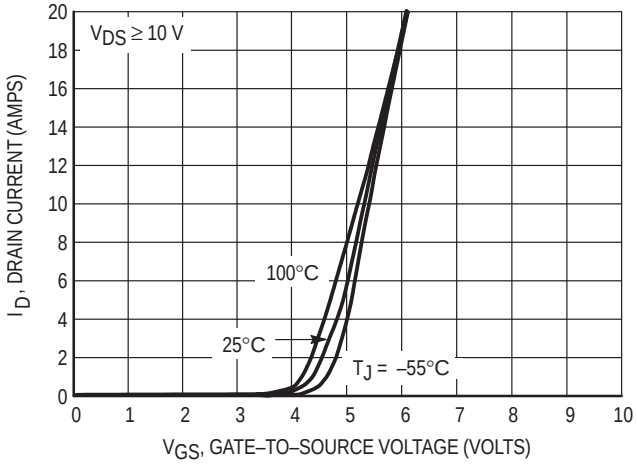


Figure 2. Transfer Characteristics

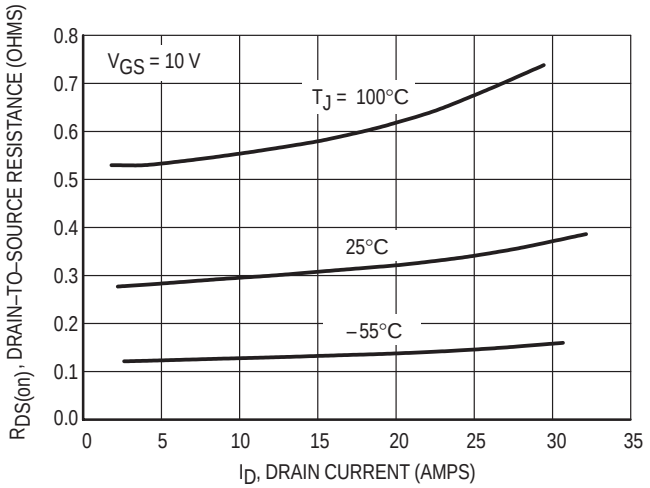


Figure 3. On–Resistance versus Drain Current and Temperature

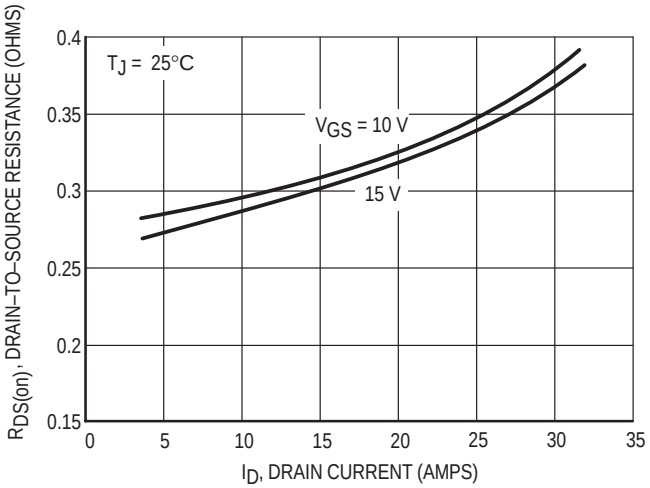


Figure 4. On–Resistance versus Drain Current and Gate Voltage

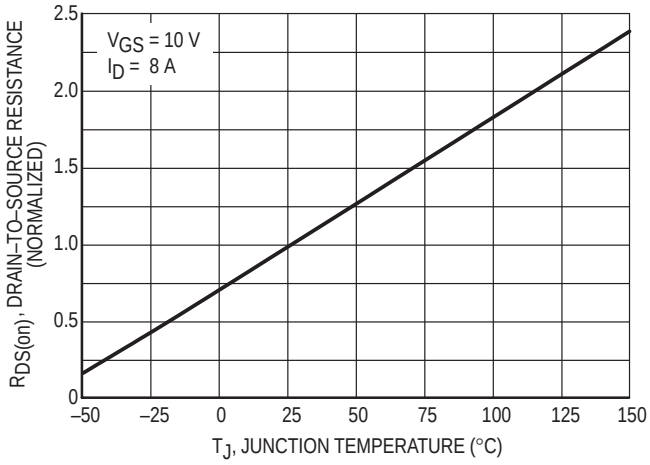


Figure 5. On–Resistance Variation with Temperature

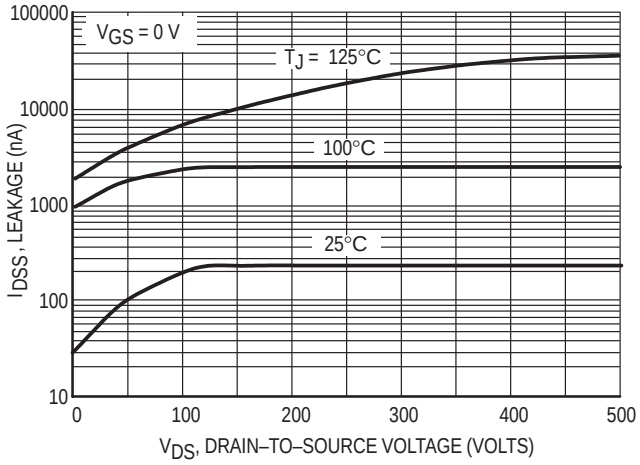


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

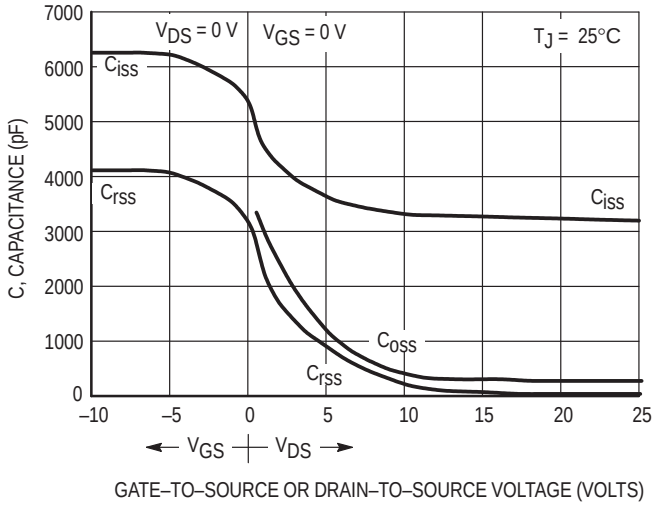


Figure 9a. Low Voltage Capacitance Variation

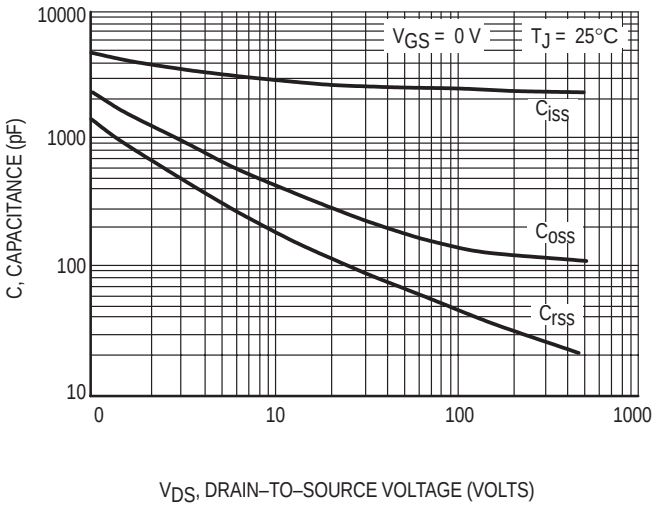


Figure 9b. High Voltage Capacitance Variation

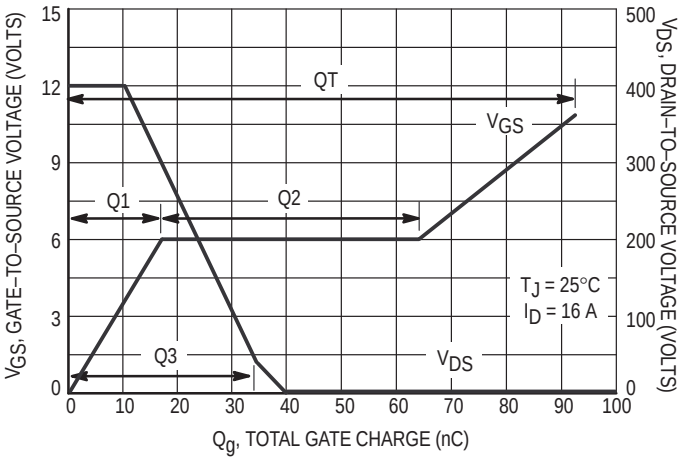


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

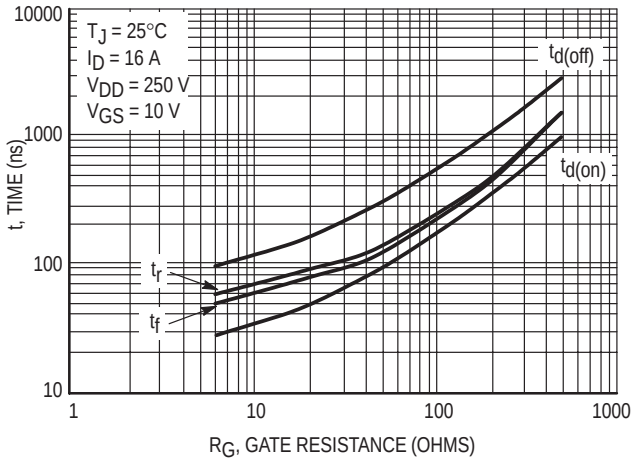


Figure 9. Resistive Switching Time Variation versus Gate Resistance

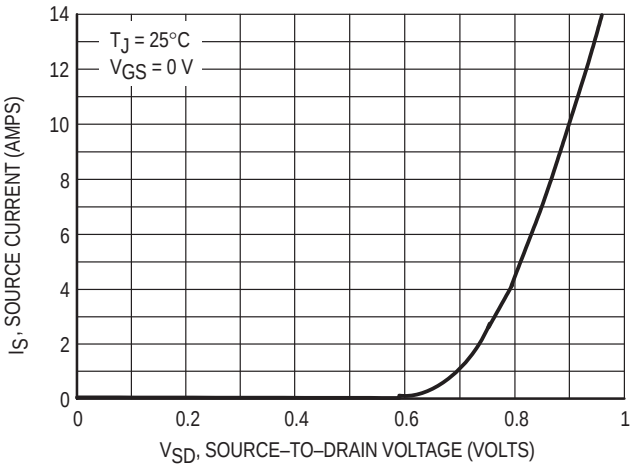


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

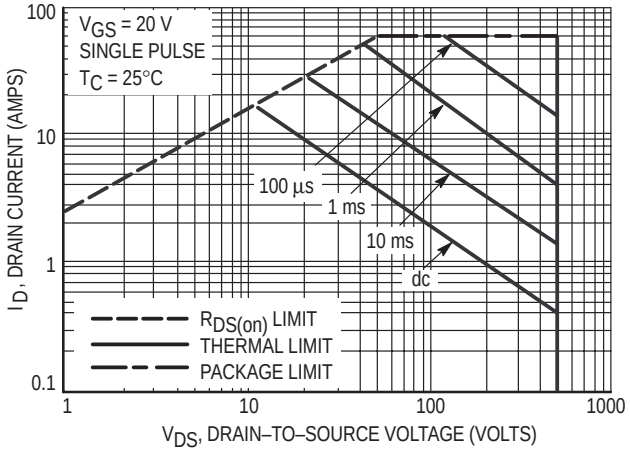


Figure 11. Maximum Rated Forward Biased Safe Operating Area

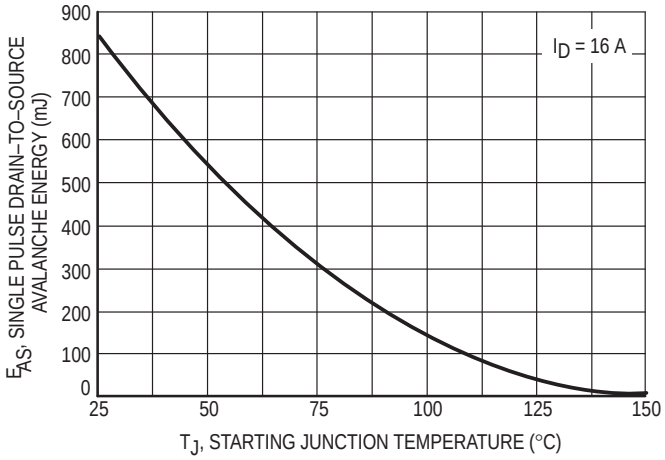


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

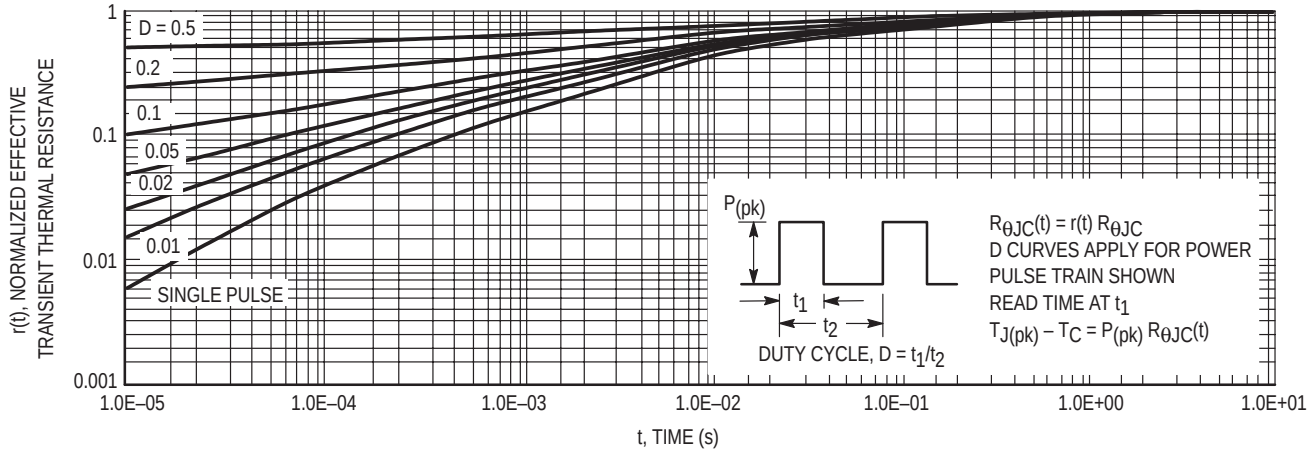


Figure 13. Thermal Response

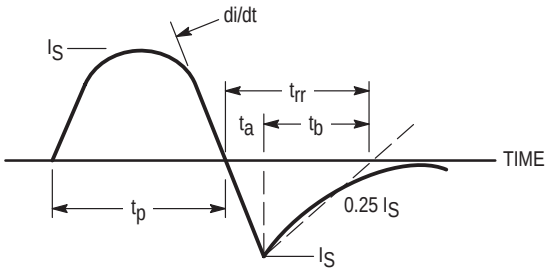


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

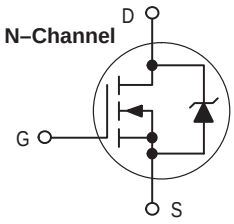
TMOS E-FET ™
Power Field Effect Transistor
D³PAK for Surface Mount

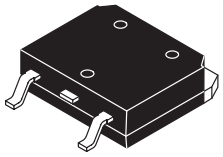
N–Channel Enhancement–Mode Silicon Gate

MTV20N50E

TMOS POWER FET
20 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.240 OHM

The D³PAK package has the capability of housing the largest chip size of any standard, plastic, surface mount power semiconductor. This allows it to be used in applications that require surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in surface mount PWM motor controls and both ac–dc and dc–dc power supplies. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 433–01, Style 2
D³PAK Surface Mount

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specifically Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm, 13–inch/500 Unit Tape & Reel, Add –RL Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	500	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS}	±20 ±40	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	20 14.1 60	Adc Apk
Total Power Dissipation Derate above 25°C Total Power Dissipation @ T_C = 25°C (1)	P_D	250 2.0 3.57	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 20 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	 2000	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	0.5 62.5 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	500	—	—	Vdc
Temperature Coefficient (Positive)			—	583	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$R_{DS(on)}$	—	0.23	0.24	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 20 Adc)		$V_{DS(on)}$	—	4.75	6.0	Vdc
(V_{GS} = 10 Vdc, I_D = 10 Adc, T_J = 125°C)			—	—	6.0	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 10 Adc)		g_{FS}	11	16.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3880	6950	pF
Output Capacitance		C_{oss}	—	452	920	
Transfer Capacitance		C_{rss}	—	96	140	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	29	55	ns
Rise Time		t_r	—	90	165	
Turn–Off Delay Time		$t_{d(off)}$	—	97	190	
Fall Time		t_f	—	84	170	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc)	Q_T	—	100	132	nC
		Q_1	—	20	—	
		Q_2	—	44	—	
		Q_3	—	36	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 20 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.916	1.1	Vdc
	(I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.81	—	
Reverse Recovery Time	(I_S = 20 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	431	—	ns
		t_a	—	272	—	
		t_b	—	159	—	
Reverse Recovery Stored Charge		Q_{RR}	—	6.67	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

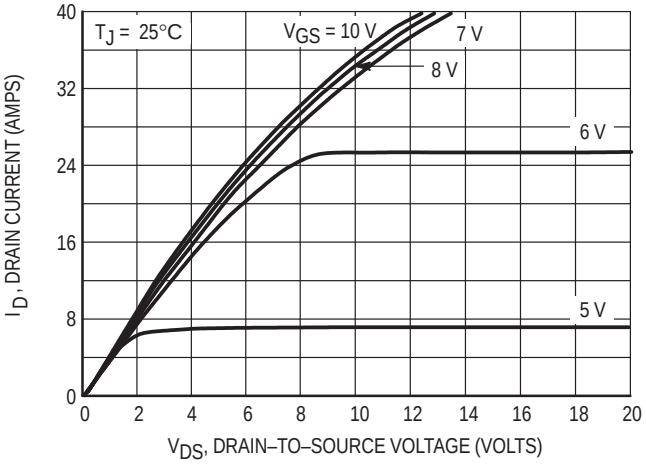


Figure 1. On–Region Characteristics

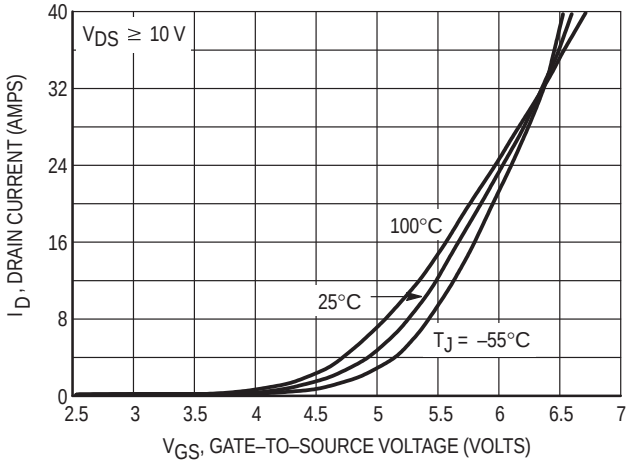


Figure 2. Transfer Characteristics

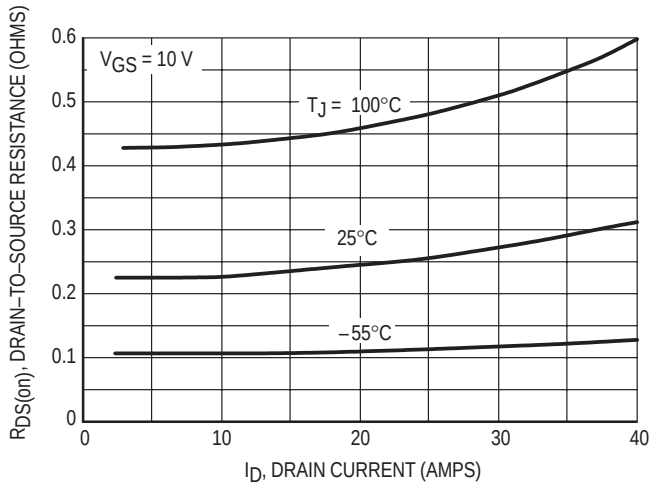


Figure 3. On–Resistance versus Drain Current and Temperature

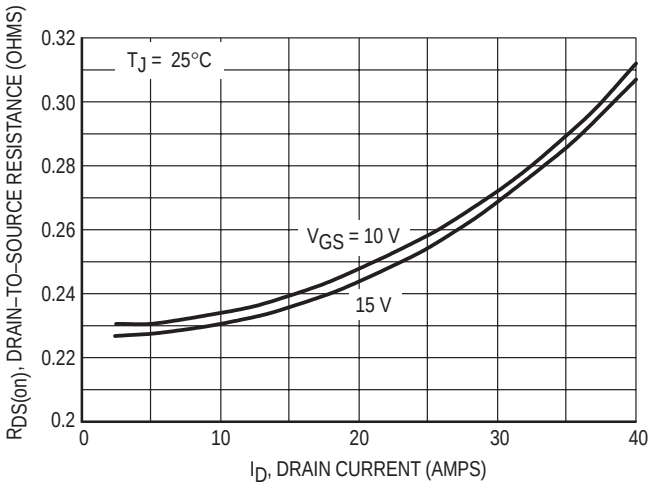


Figure 4. On–Resistance versus Drain Current and Gate Voltage

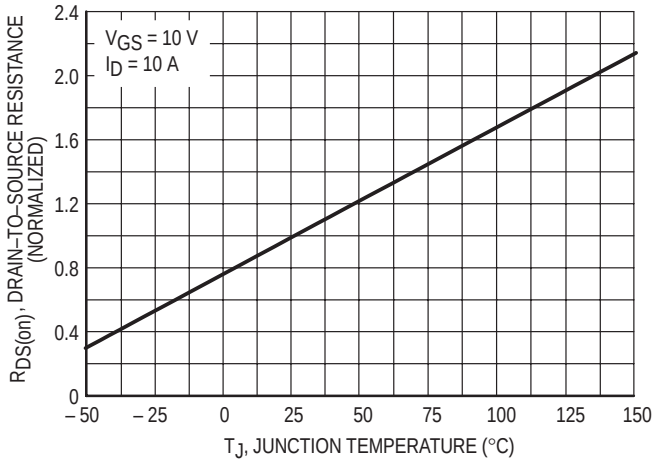


Figure 5. On–Resistance Variation with Temperature

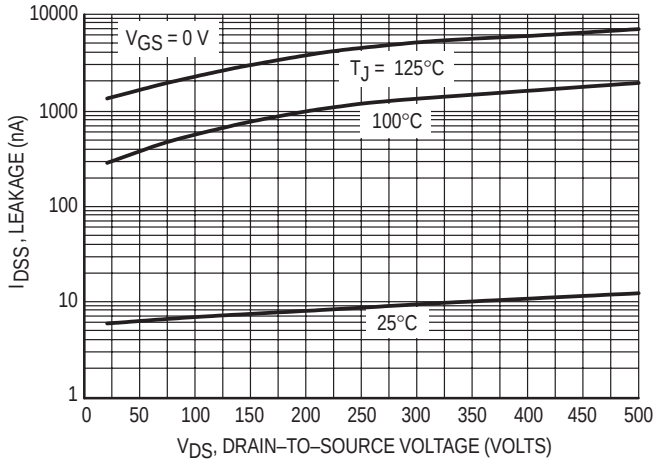


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

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$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

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$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

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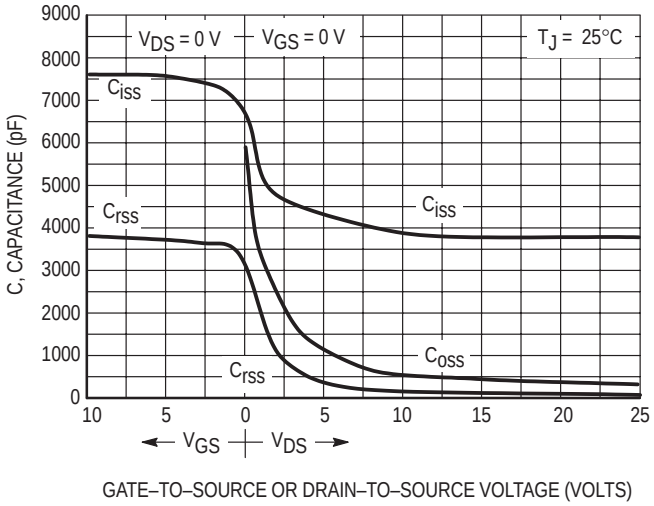

Figure 10a. Capacitance Variation

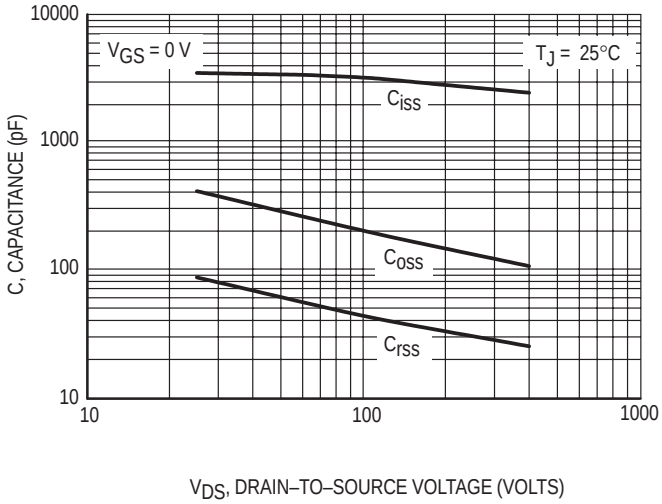

Figure 10b. High Voltage Capacitance Variation

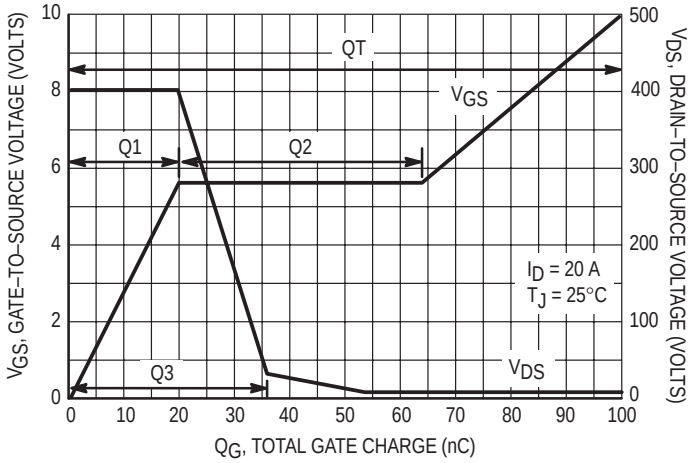

Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

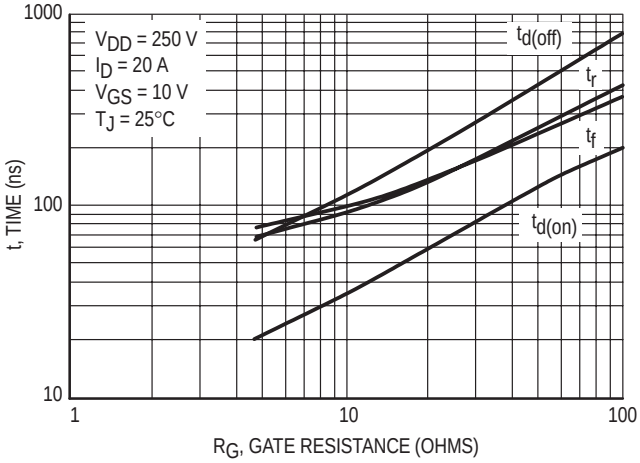

Figure 9. Resistive Switching Time Variation versus Gate Resistance

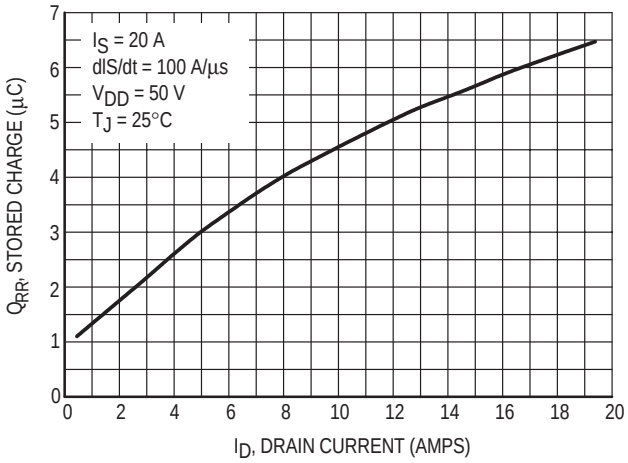

Figure 10. Stored Charge

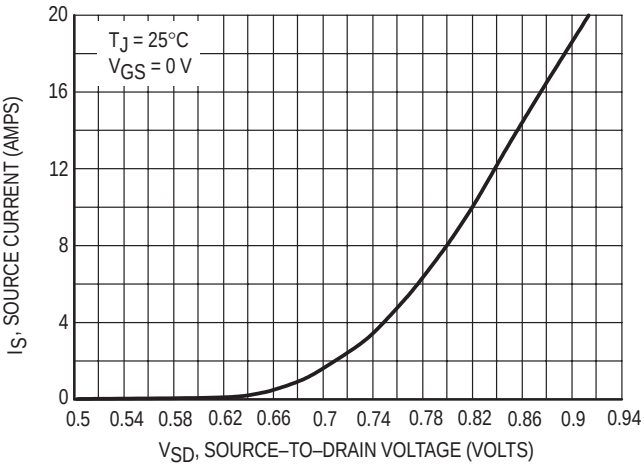

Figure 11. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

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A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

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SAFE OPERATING AREA

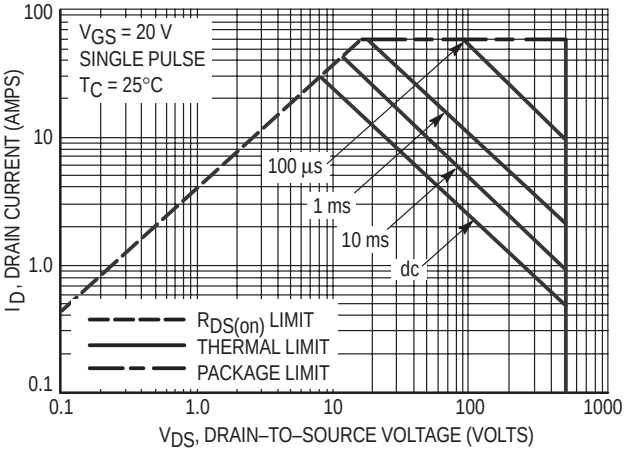


Figure 12. Maximum Rated Forward Biased Safe Operating Area

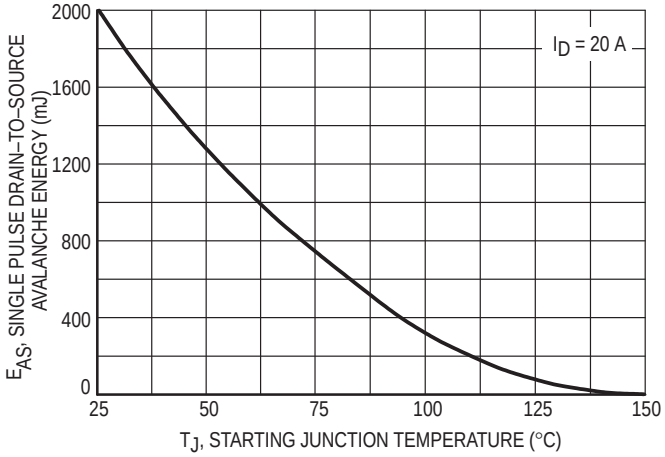


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

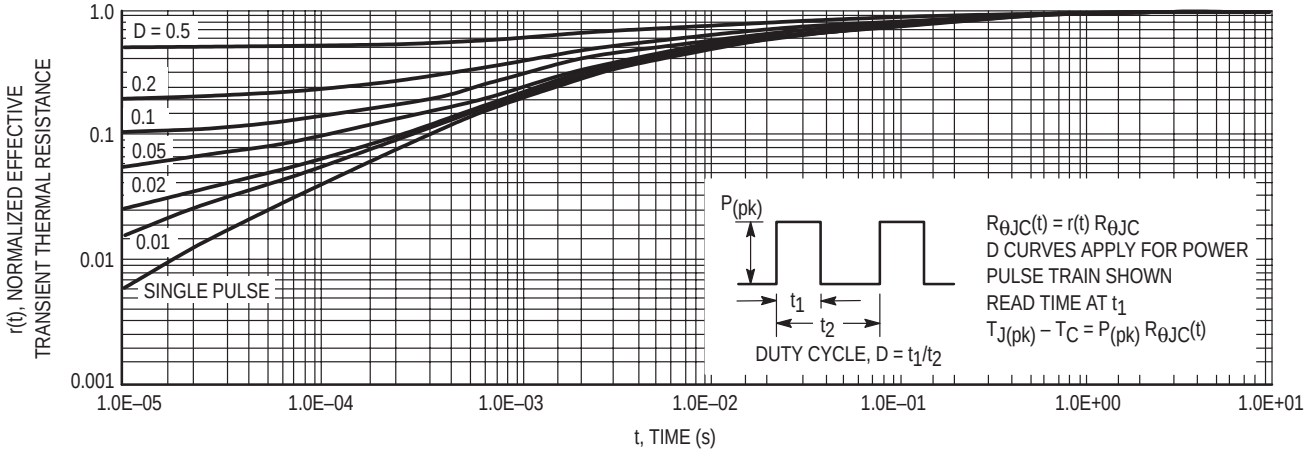


Figure 14. Thermal Response

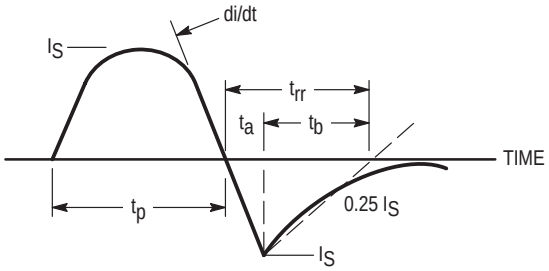


Figure 15. Diode Reverse Recovery Waveform

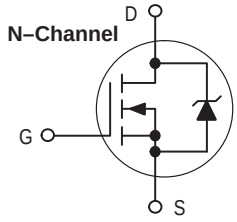
Advance Information

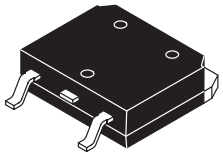
TMOS E-FET™
Power Field Effect Transistor
D³PAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

MTV25N50E

TMOS POWER FET
25 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.200 OHM

The D³PAK package has the capability of housing the largest chip size of any standard, plastic, surface mount power semiconductor. This allows it to be used in applications that require surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in surface mount PWM motor controls and both ac–dc and dc–dc power supplies. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 433–01, Style 2
D³PAK Surface Mount

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specifically Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm, 13–inch/500 Unit Tape & Reel, Add –RL Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	500	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	25 15.8 88	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	250 2.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 25 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	 938	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	0.5 62.5 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	500	—	—	Vdc
Temperature Coefficient (Positive)			—	0.51	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	2.9	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 12.5 Adc)		$R_{DS(on)}$	—	0.19	0.2	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 25 Adc)		$V_{DS(on)}$	—	5.4	6.0	Vdc
(V_{GS} = 10 Vdc, I_D = 12.5 Adc, T_J = 125°C)			—	—	5.3	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 12.5 Adc)		g_{FS}	11	17	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	4700	6580	pF
Output Capacitance		C_{oss}	—	520	728	
Transfer Capacitance		C_{rss}	—	200	280	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 25 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	37	70	ns
Rise Time		t_r	—	137	280	
Turn–Off Delay Time		$t_{d(off)}$	—	118	240	
Fall Time		t_f	—	112	230	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 25 Adc, V_{GS} = 10 Vdc)	Q_T	—	132	180	nC
		Q_1	—	29	—	
		Q_2	—	63	—	
		Q_3	—	61	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 25 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.9	1.1	Vdc
	(I_S = 25 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.79	—	
Reverse Recovery Time	(I_S = 25 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	501	—	ns
		t_a	—	332	—	
		t_b	—	170	—	
Reverse Recovery Stored Charge		Q_{RR}	—	9.42	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	5.0	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

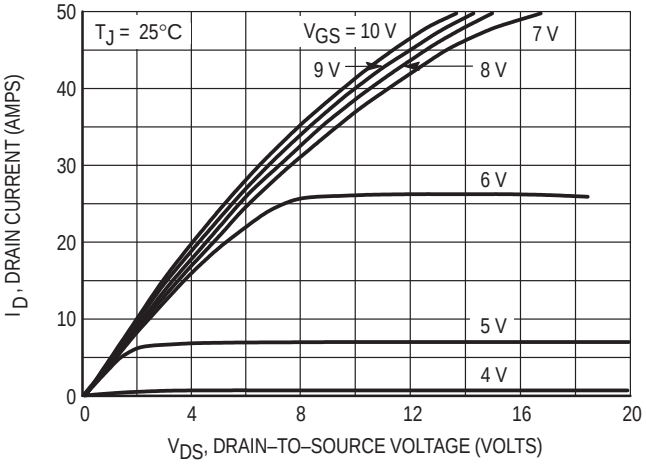


Figure 1. On–Region Characteristics

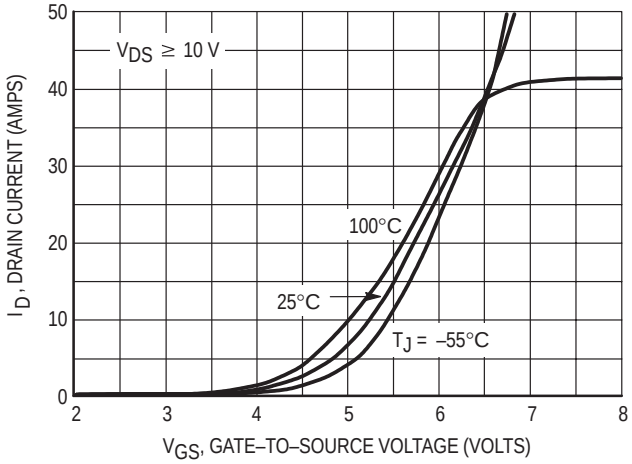


Figure 2. Transfer Characteristics

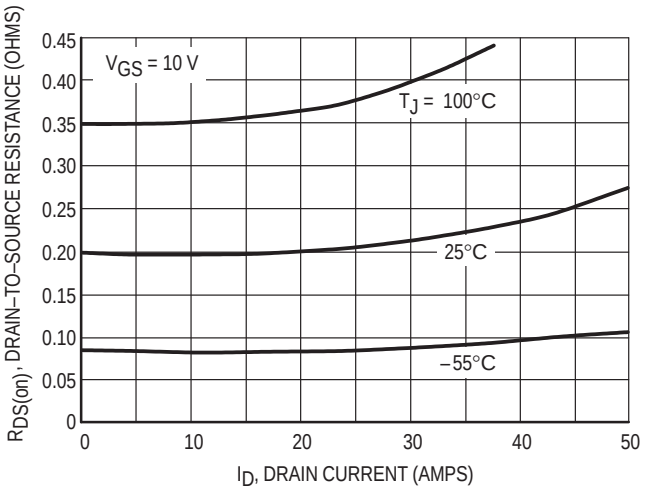


Figure 3. On–Resistance versus Drain Current and Temperature

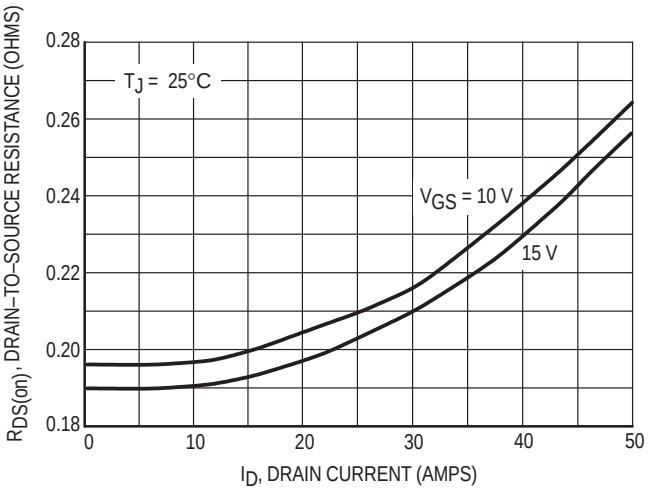


Figure 4. On–Resistance versus Drain Current and Gate Voltage

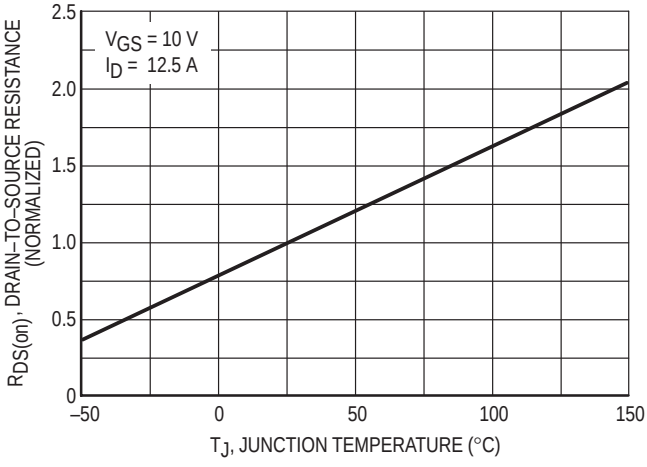
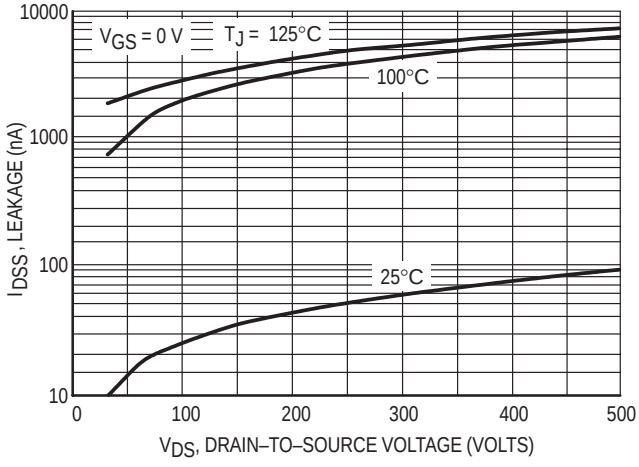


Figure 5. On–Resistance Variation with Temperature



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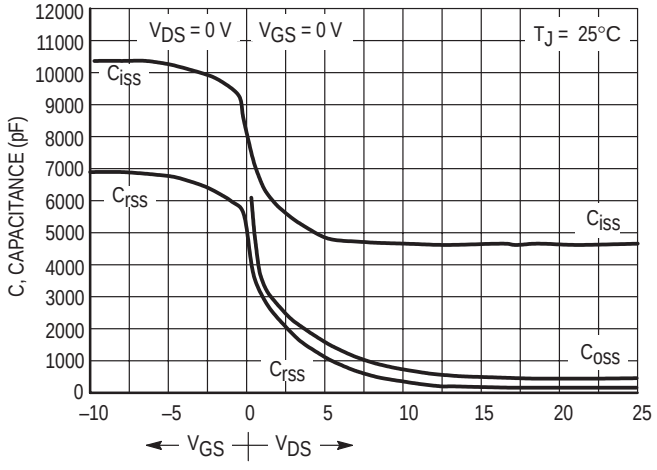

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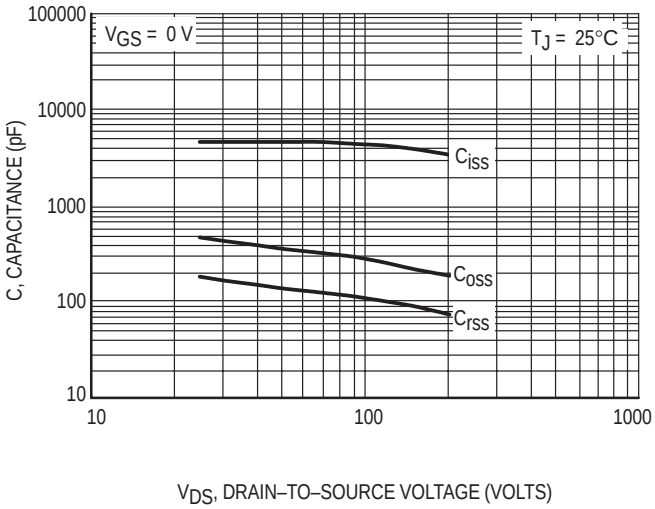

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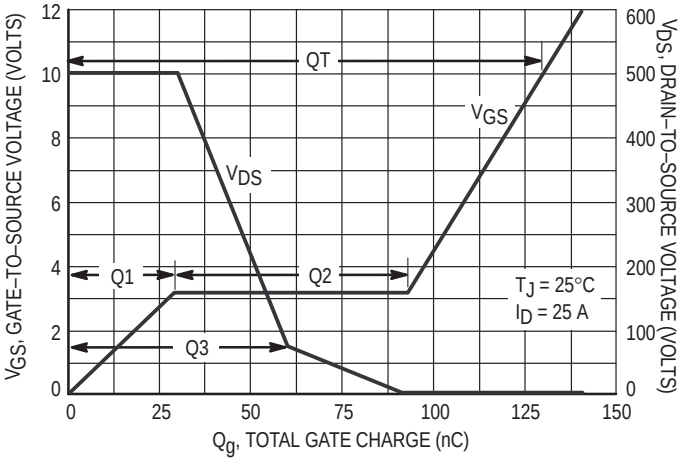

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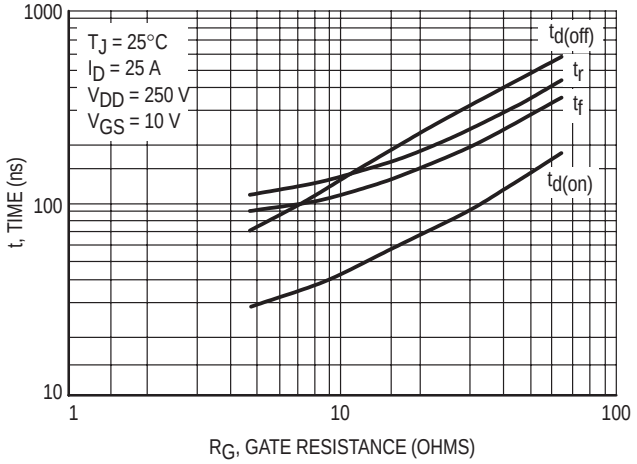

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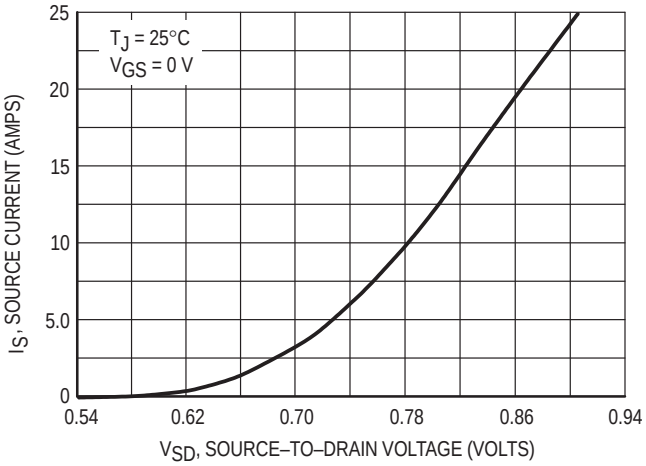

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Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

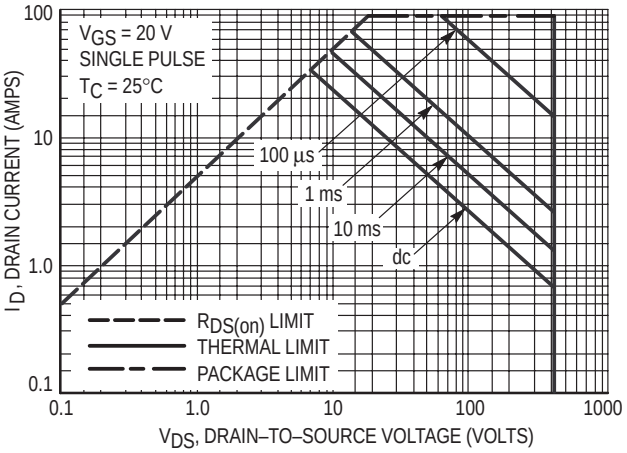


Figure 11. Maximum Rated Forward Biased Safe Operating Area

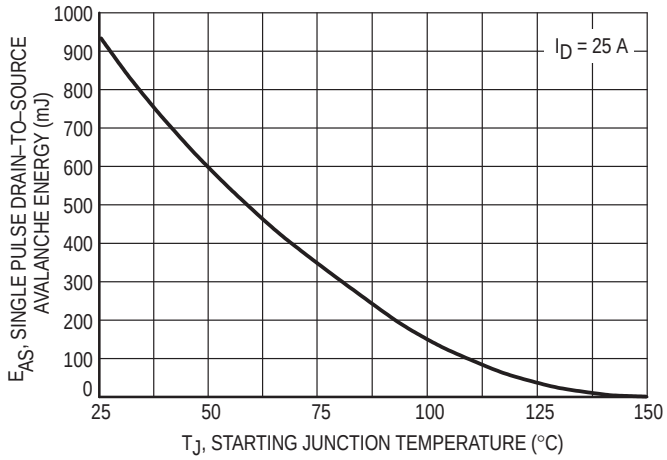


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

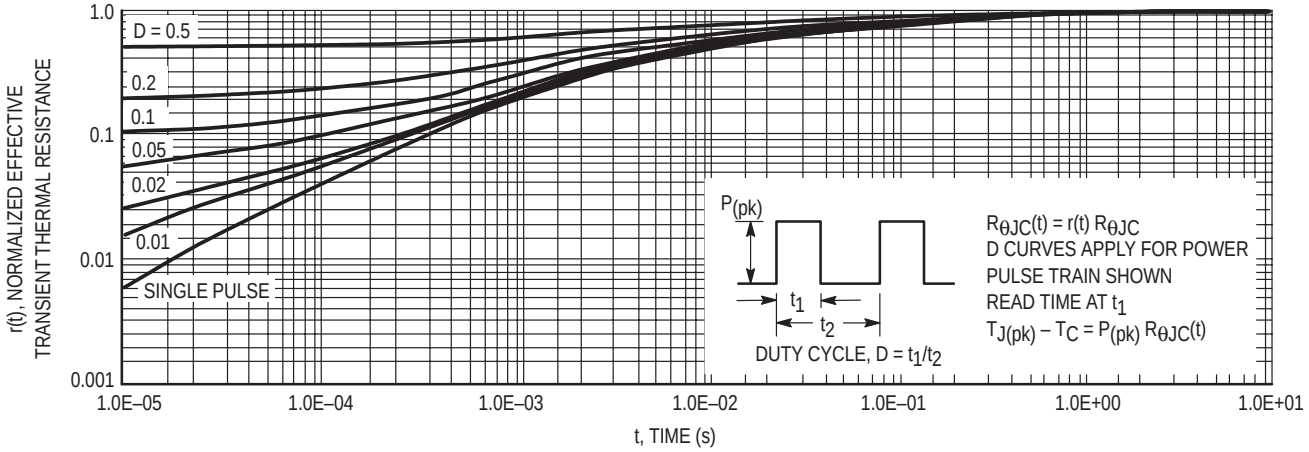


Figure 13. Thermal Response

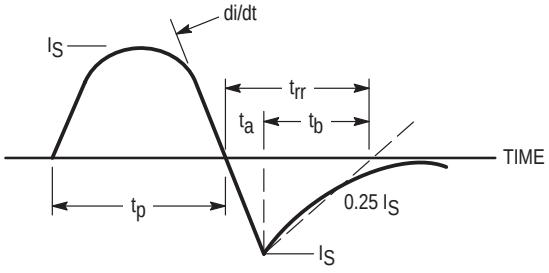


Figure 14. Diode Reverse Recovery Waveform

Advance Information

TMOS E-FET™
Power Field Effect Transistor
D³PAK for Surface Mount

N–Channel Enhancement–Mode Silicon Gate

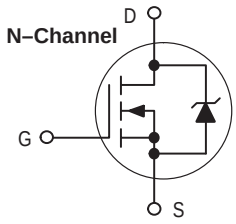
MTV32N20E

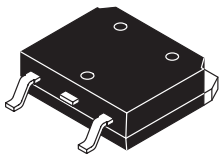
TMOS POWER FET
32 AMPERES
200 VOLTS
$R_{DS(on)}$ = 0.075 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high speed switching applications in power supplies, converters, PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature

TMOS®





CASE 433–01, Style 2
D³PAK Surface Mount

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	200	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	Vdc
Gate–to–Source Voltage — Continuous	V_{GS}	±20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	32 19 128	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	180 1.44 2.0	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, Peak I_L = 32 Apk, L = 1.58 mH, R_G = 25 Ω)	E_{AS}	 810	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	0.7 62.5 35	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	200	—	—	Vdc
Temperature Coefficient (Positive)			—	247	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	250	μAdc
(V_{DS} = 200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	1000	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	8.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc)		$R_{DS(on)}$	—	0.064	0.075	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 32 Adc)		$V_{DS(on)}$	—	2.1	3.0	Vdc
(V_{GS} = 10 Vdc, I_D = 16 Adc, T_J = 125°C)			—	—	2.7	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 16 Adc)		g_{FS}	12	20	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3600	5000	pF
Output Capacitance		C_{oss}	—	130	250	
Transfer Capacitance		C_{rss}	—	690	1000	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 100 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc, R_G = 6.2 Ω)	$t_{d(on)}$	—	25	50	ns
Rise Time		t_r	—	120	240	
Turn–Off Delay Time		$t_{d(off)}$	—	75	150	
Fall Time		t_f	—	91	182	
Gate Charge (See Figure 8)	(V_{DS} = 160 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc)	Q_T	—	85	120	nC
		Q_1	—	12	—	
		Q_2	—	40	—	
		Q_3	—	30	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 32 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.1	2.0	Vdc
	(I_S = 32 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.9	—	
Reverse Recovery Time	(I_S = 32 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	280	—	ns
		t_a	—	195	—	
		t_b	—	85	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.94	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	5.0	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

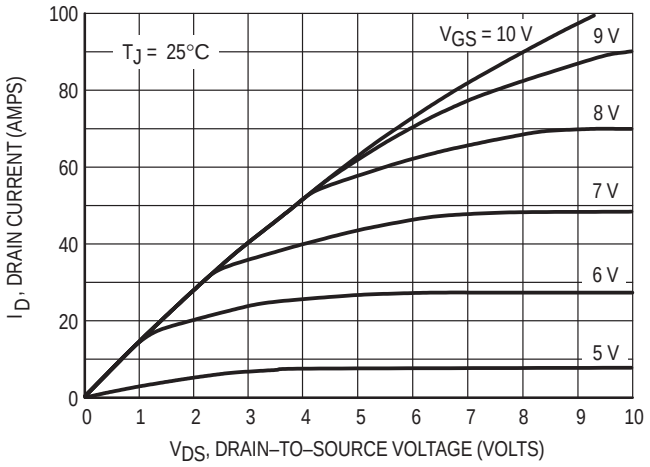


Figure 1. On–Region Characteristics

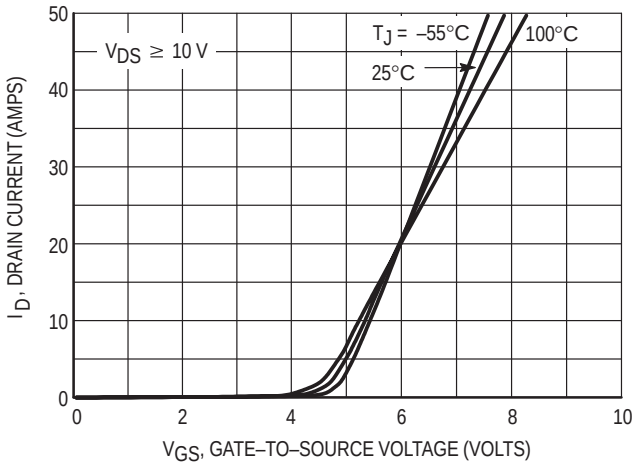


Figure 2. Transfer Characteristics

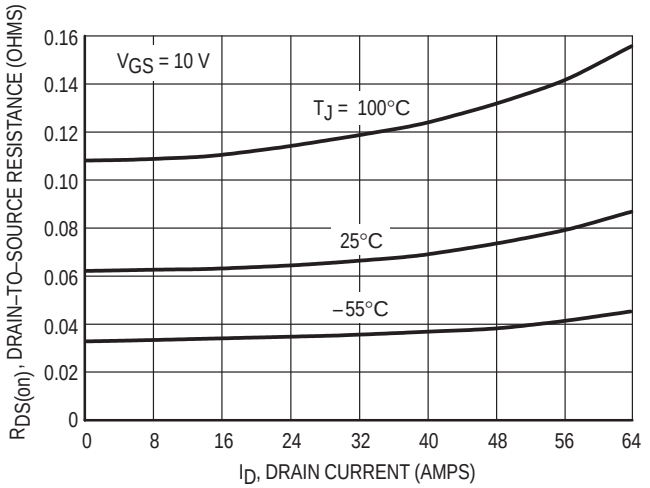


Figure 3. On–Resistance versus Drain Current and Temperature

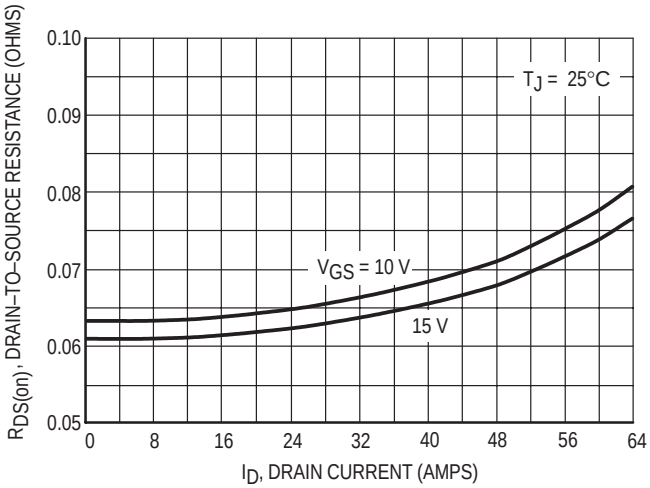


Figure 4. On–Resistance versus Drain Current and Gate Voltage

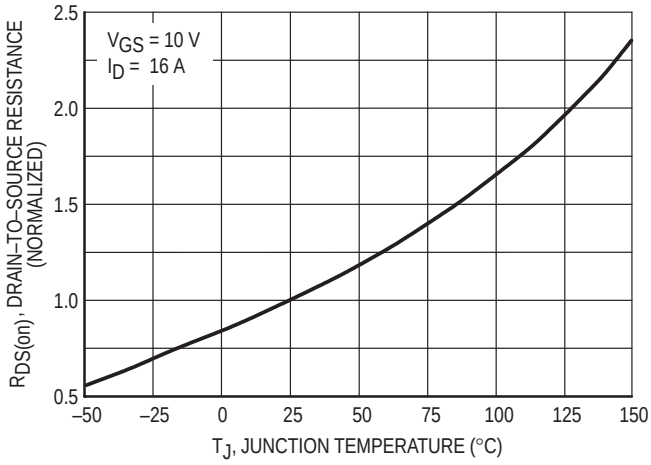


Figure 5. On–Resistance Variation with Temperature

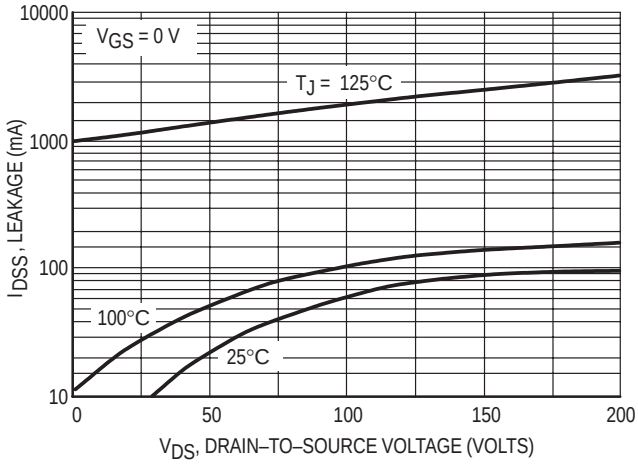


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

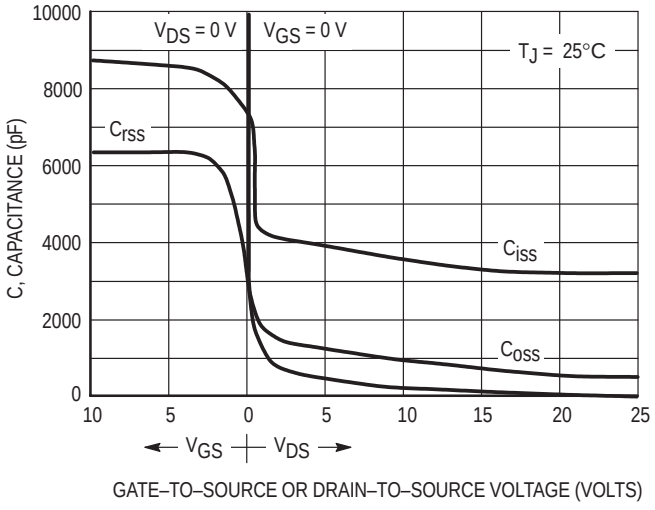


Figure 7. Capacitance Variation

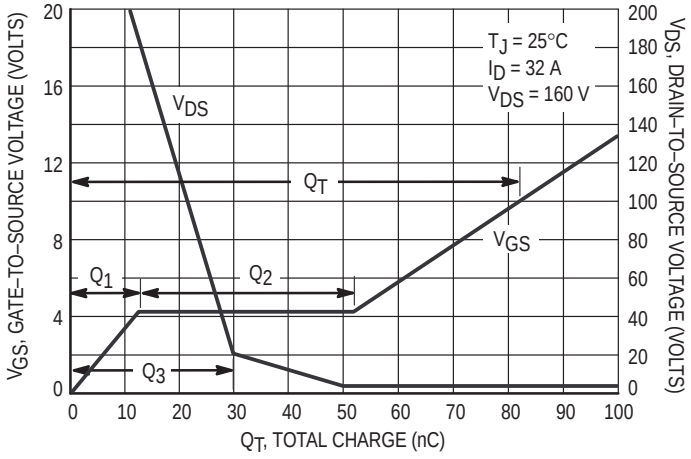


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

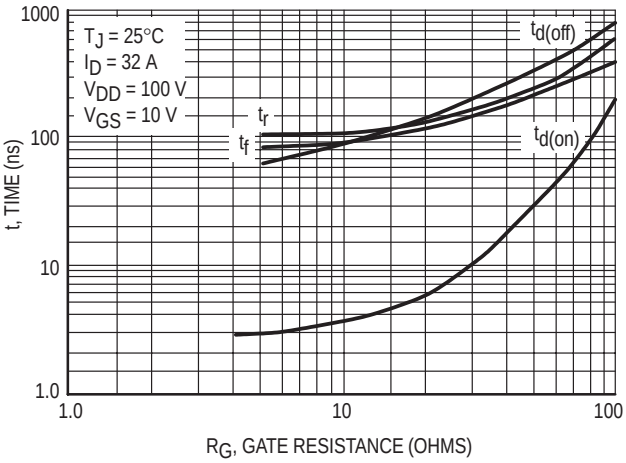


Figure 9. Resistive Switching Time Variation versus Gate Resistance

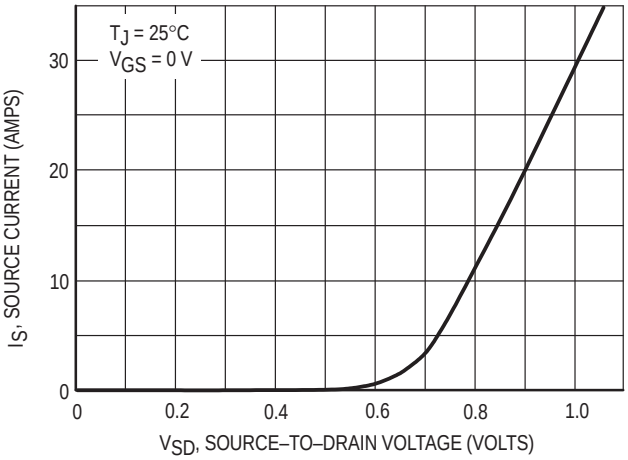


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

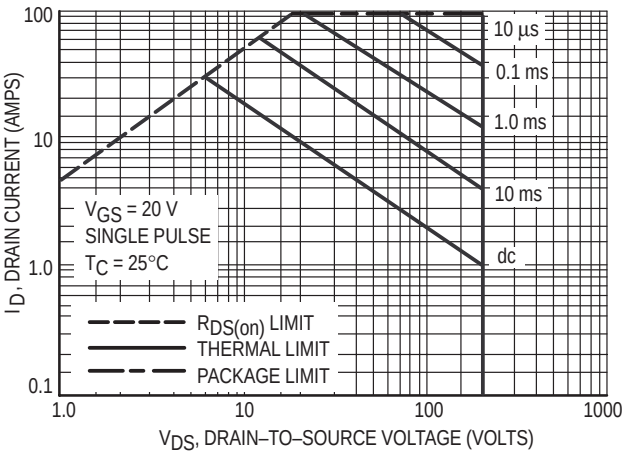


Figure 11. Maximum Rated Forward Biased Safe Operating Area

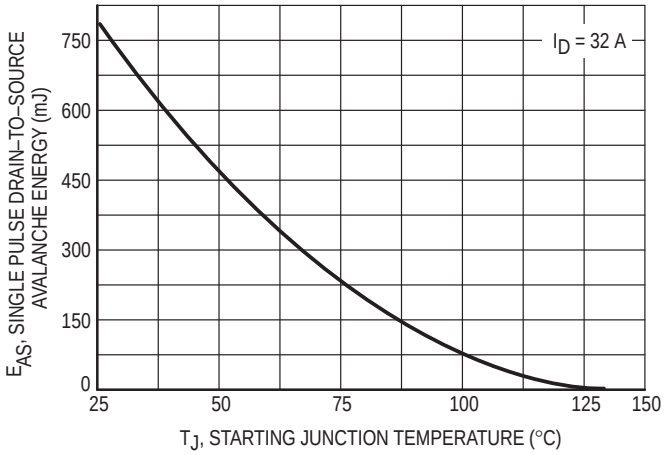


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

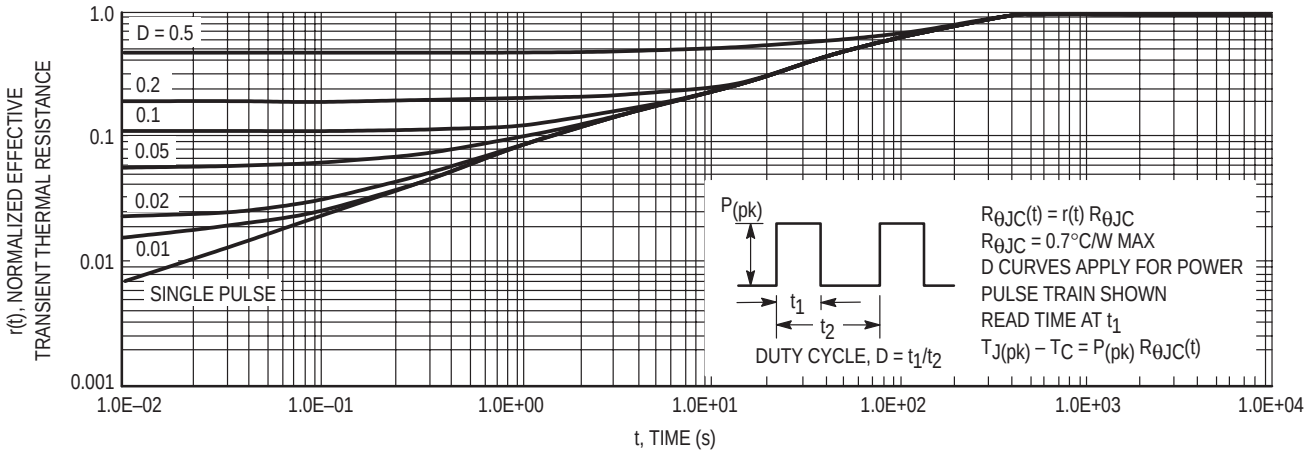


Figure 13. Thermal Response

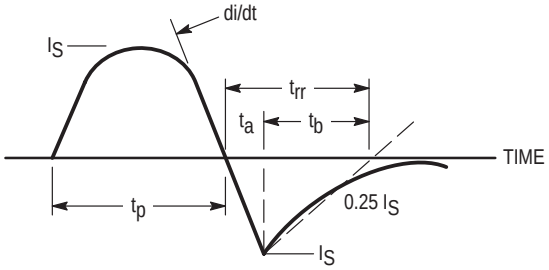


Figure 14. Diode Reverse Recovery Waveform

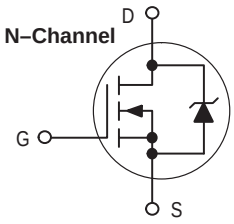
Designer's™ Data Sheet

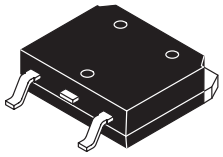
TMOS E-FET ™
Power Field Effect Transistor
D³PAK for Surface Mount
N–Channel Enhancement–Mode Silicon Gate

MTV32N25E

TMOS POWER FET
32 AMPERES
250 VOLTS
$R_{DS(on)}$ = 0.08 OHM

The D³PAK package has the capability of housing the largest chip size of any standard, plastic, surface mount power semiconductor. This allows it to be used in applications that require surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in surface mount PWM motor controls and both ac–dc and dc–dc power supplies. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.





CASE 433–01, Style 2
D³PAK Surface Mount

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specifically Designed Leadframe for Maximum Power Dissipation
- Available in 24 mm, 13–inch/500 Unit Tape & Reel, Add –RL Suffix to Part Number

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	250	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	250	Vdc
Gate–Source Voltage — Continuous	V_{GS}	±20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	32 25 96	Adc Apk
Total Power Dissipation @ 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (1)	P_D	250 2.0 3.57	Watts W/°C Watts
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, Peak I_L = 32 Apk, L = 8.8 mH, R_G = 25 Ω)	E_{AS}	600	mJ
Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	0.5 62.5 35	°C/W
Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

(1) When surface mounted to an FR4 board using the minimum recommended pad size.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	250	—	—	Vdc
Temperature Coefficient (Positive)			—	380	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 250 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 250 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	—	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc)		$R_{DS(on)}$	—	0.69	0.08	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 32 Adc)		$V_{DS(on)}$	—	2.25	2.6	Vdc
(V_{GS} = 10 Vdc, I_D = 16 Adc, T_J = 125°C)			—	—	2.5	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 16 Adc)		g_{FS}	11	20	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3800	5320	pF
Output Capacitance		C_{oss}	—	750	1020	
Transfer Capacitance		C_{rss}	—	240	370	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 125 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	31	60	ns
Rise Time		t_r	—	133	266	
Turn–Off Delay Time		$t_{d(off)}$	—	93	186	
Fall Time		t_f	—	108	216	
Gate Charge (See Figure 8)	(V_{DS} = 200 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc)	Q_T	—	97	136	nC
		Q_1	—	22	—	
		Q_2	—	43	—	
		Q_3	—	41	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 32 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.5	Vdc
	(I_S = 32 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.92	—	
Reverse Recovery Time	(I_S = 32 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	312	—	ns
		t_a	—	220	—	
		t_b	—	93	—	
Reverse Recovery Stored Charge		Q_{RR}	—	3.6	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

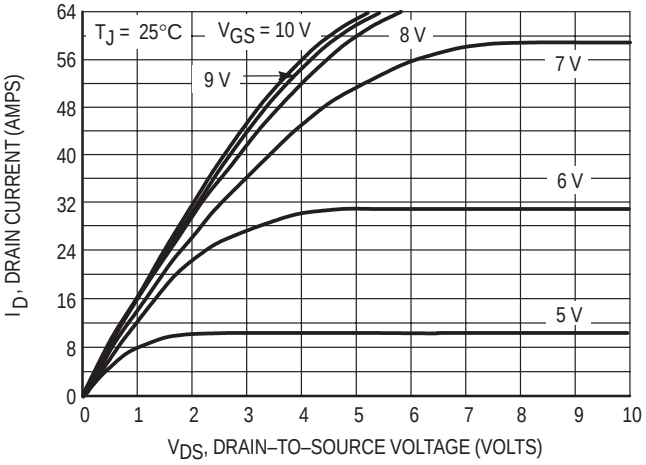


Figure 1. On–Region Characteristics

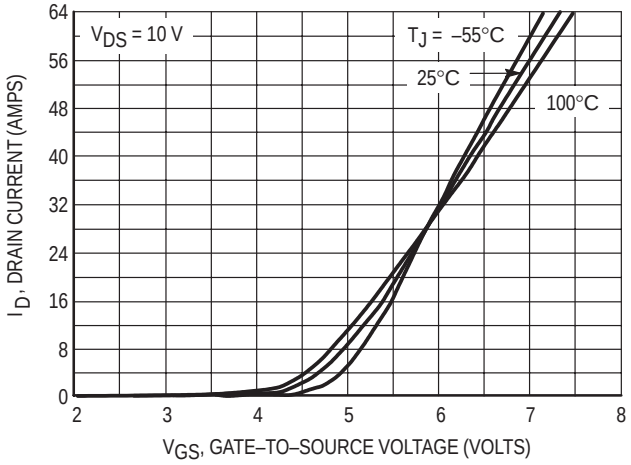


Figure 2. Transfer Characteristics

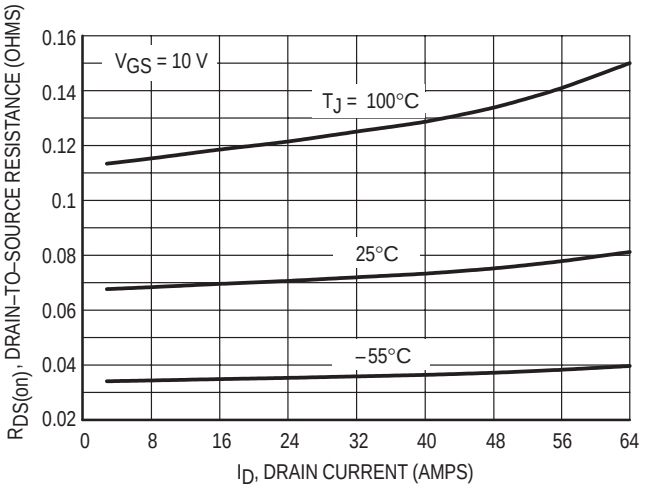


Figure 3. On–Resistance versus Drain Current and Temperature

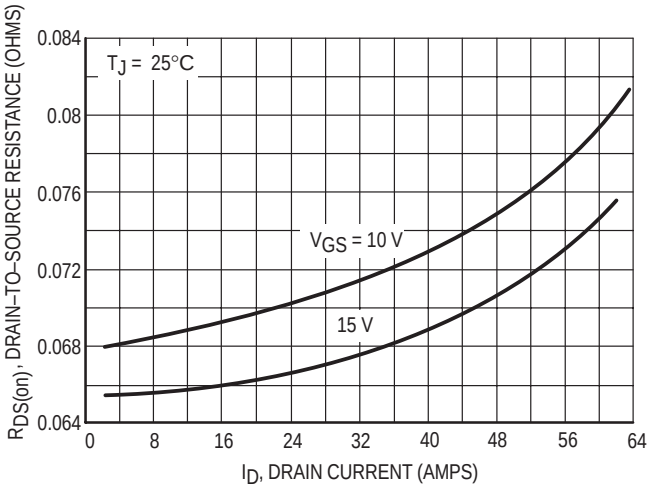


Figure 4. On–Resistance versus Drain Current and Gate Voltage

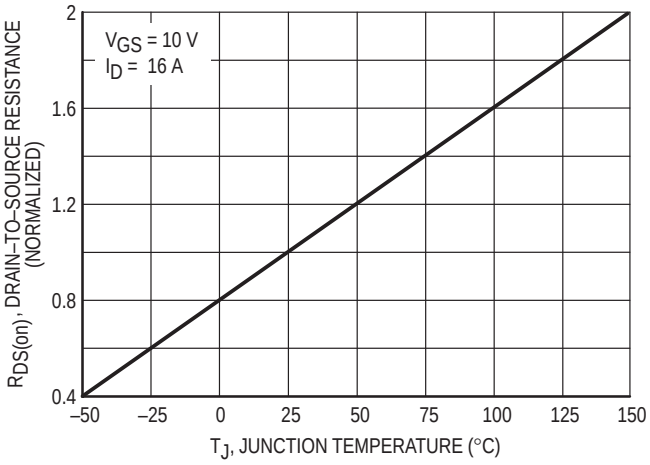


Figure 5. On–Resistance Variation with Temperature

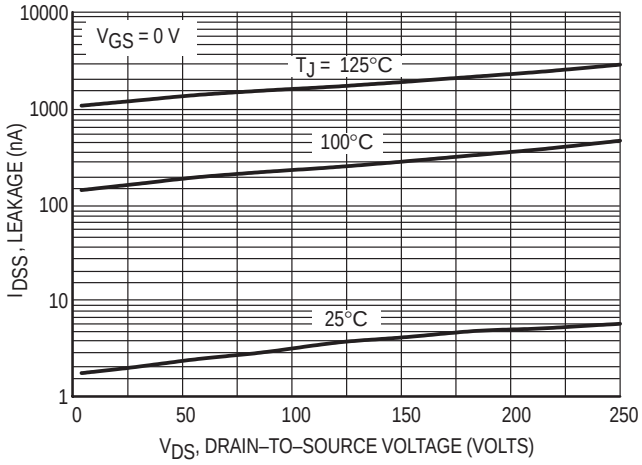


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

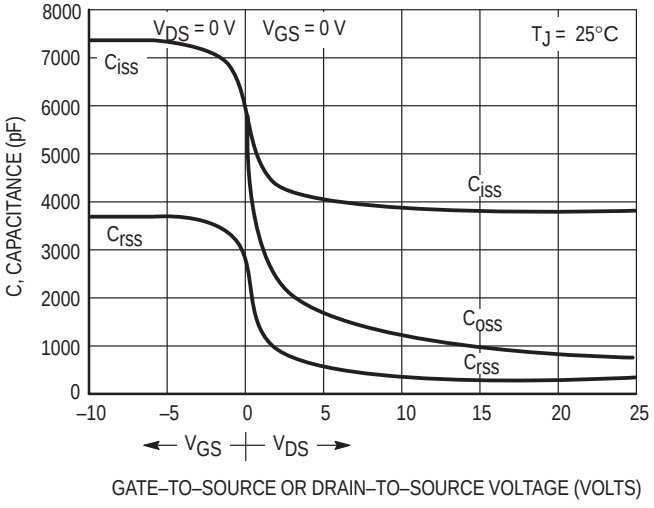


Figure 7. Capacitance Variation

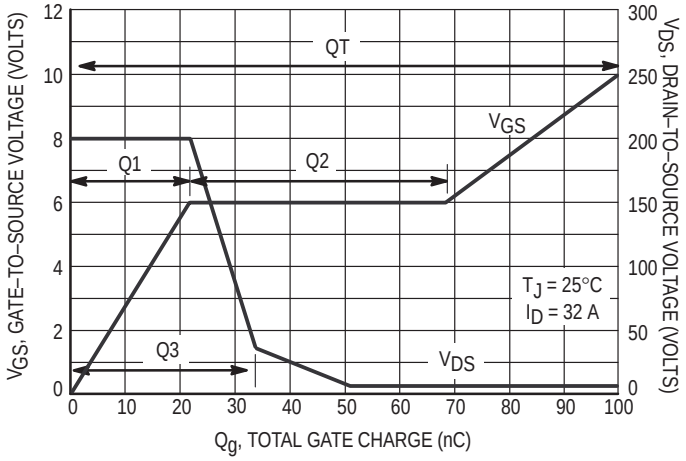


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

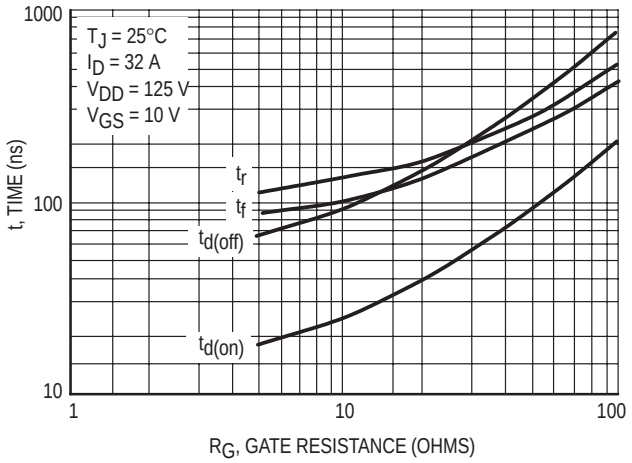


Figure 9. Resistive Switching Time Variation versus Gate Resistance

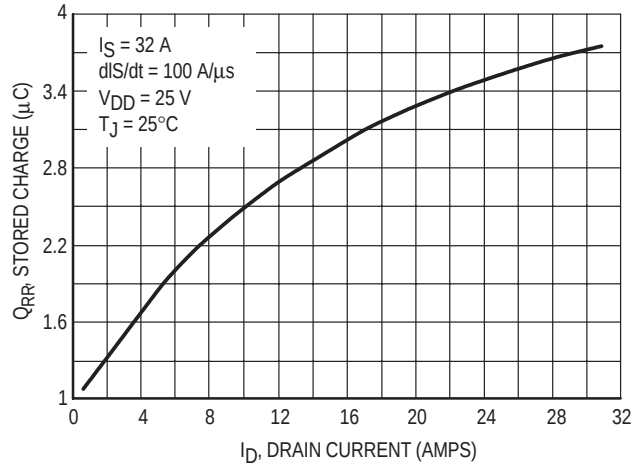


Figure 10. Stored Charge

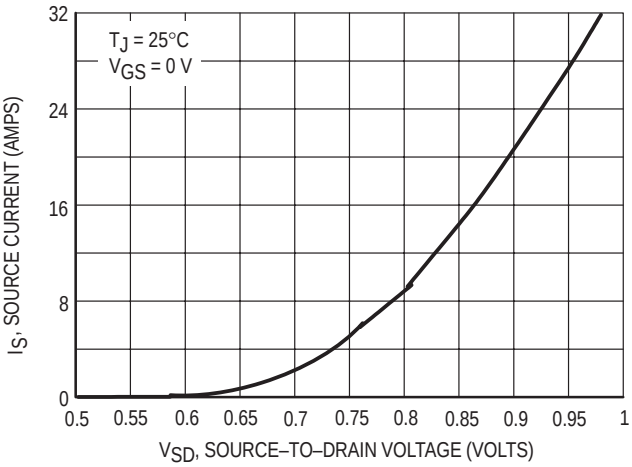


Figure 11. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

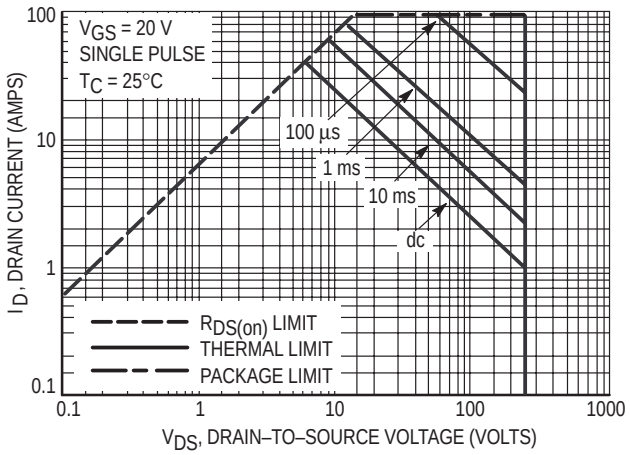


Figure 12. Maximum Rated Forward Biased Safe Operating Area

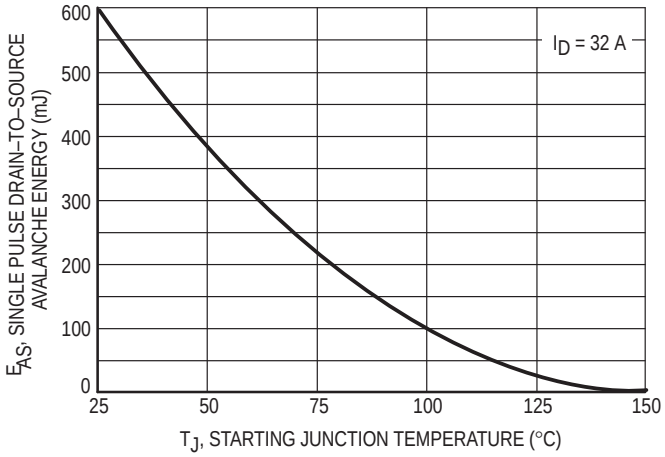


Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

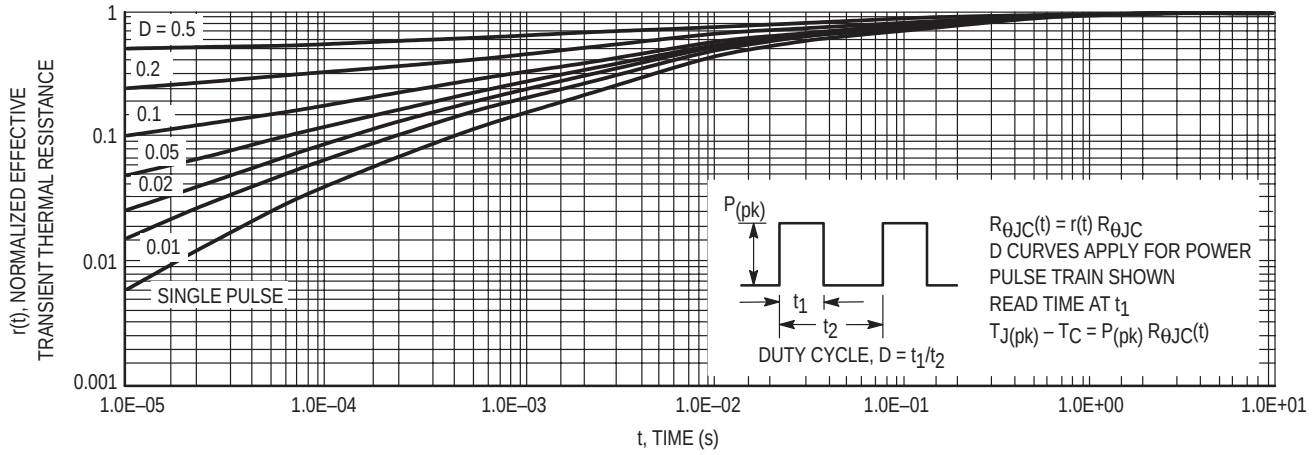


Figure 14. Thermal Response

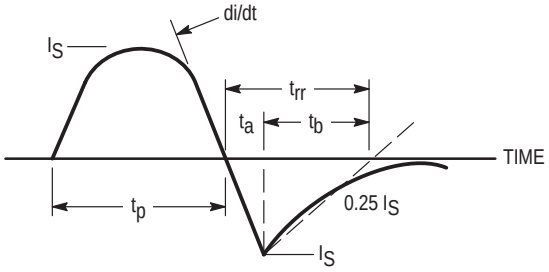


Figure 15. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
TO-247 With Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

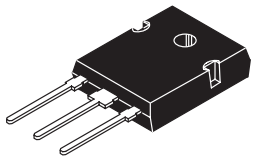
MTW6N100E

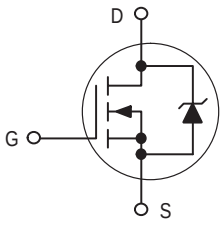
Motorola Preferred Device

TMOS POWER FET
6.0 AMPERES
1000 VOLTS
$R_{DS(on)}$ = 1.5 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	1000	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	1000	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	6.0 4.2 18	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	180 1.43	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, I_L = 6.0 Apk, L = 27.77 mH, R_G = 25 Ω)	E_{AS}	720	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.70 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	1000 —	— 1,270	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 7.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.0 Adc)		$R_{DS(on)}$	—	1.28	1.5	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 6.0 Adc) (I_D = 3.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	8.0 —	14.4 12.6	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 3.0 Adc)		g_{FS}	4.0	7.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3000	4210	pF
Output Capacitance		C_{oss}	—	219	440	
Reverse Transfer Capacitance		C_{rss}	—	43	90	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 500 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	27	45	ns
Rise Time		t_r	—	29	65	
Turn–Off Delay Time		$t_{d(off)}$	—	93	170	
Fall Time		t_f	—	43	95	
Gate Charge (See Figure 8)	(V_{DS} = 800 Vdc, I_D = 6.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	66	100	nC
		Q_1	—	12.5	—	
		Q_2	—	25.9	—	
		Q_3	—	26	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc) (I_S = 6.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.808 0.64	1.0 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 6.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	735	—	ns
		t_a	—	188	—	
		t_b	—	547	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4.7	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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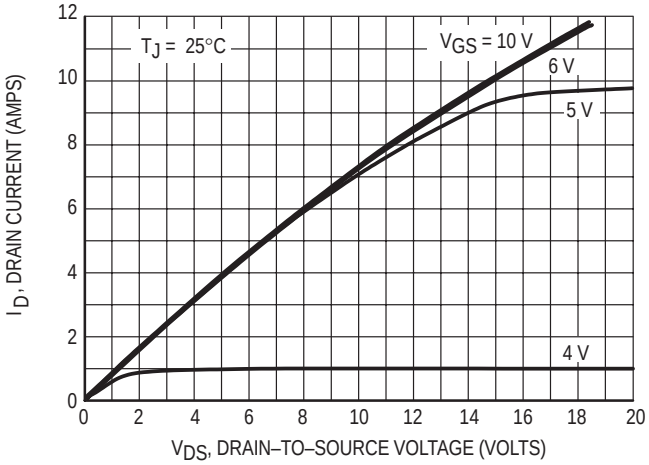
TYPICAL ELECTRICAL CHARACTERISTICS



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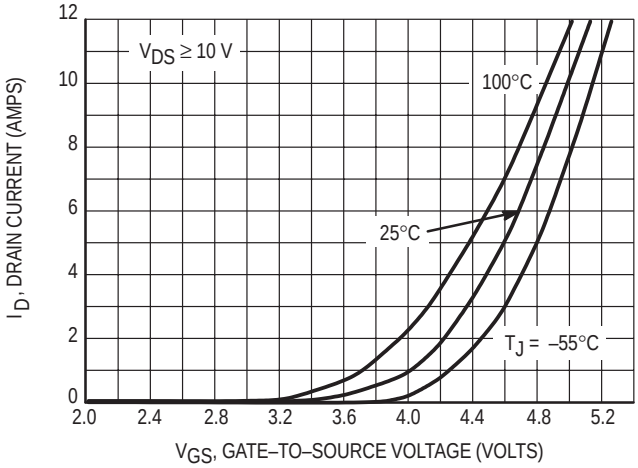

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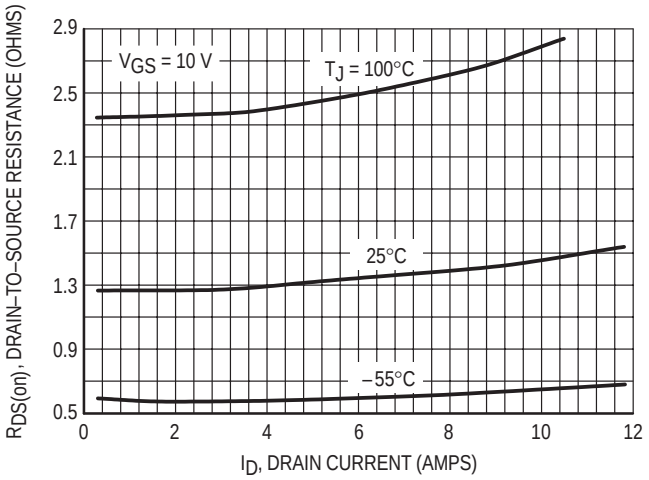

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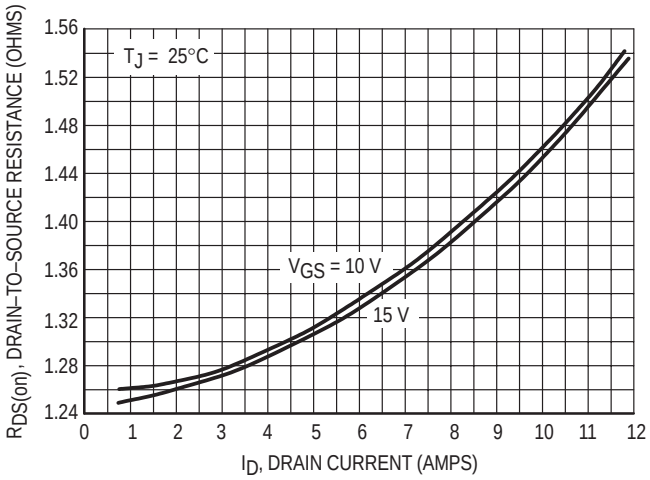


Figure 4. On–Resistance versus Drain Current and Gate Voltage

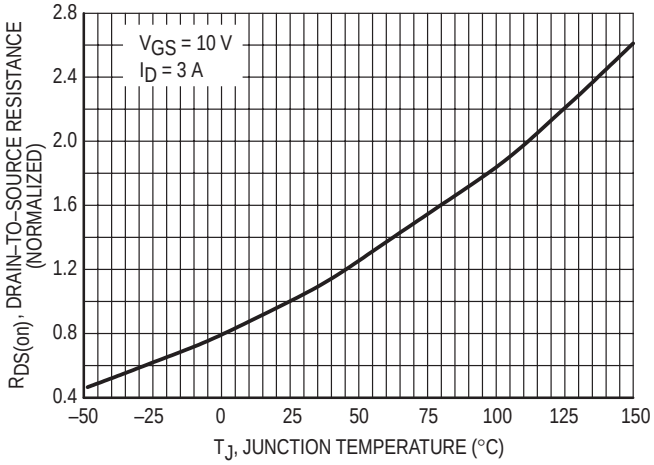
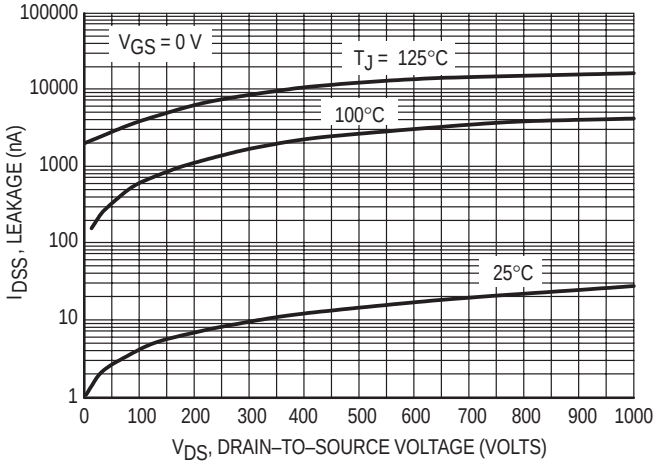


Figure 5. On–Resistance Variation with Temperature



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$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

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$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

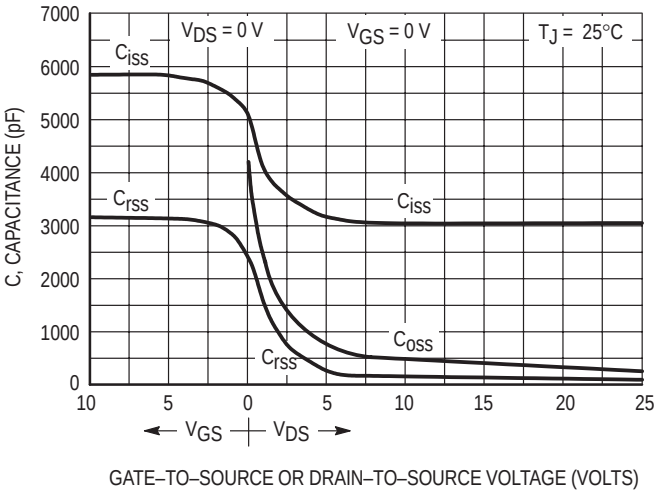


Figure 7a. Capacitance Variation

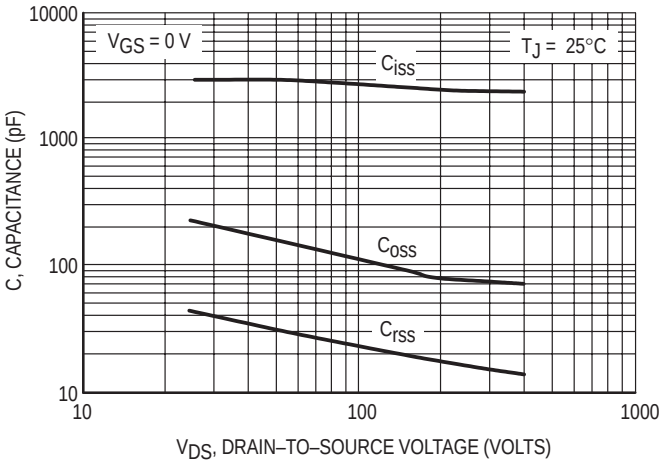


Figure 7b. High Voltage Capacitance Variation

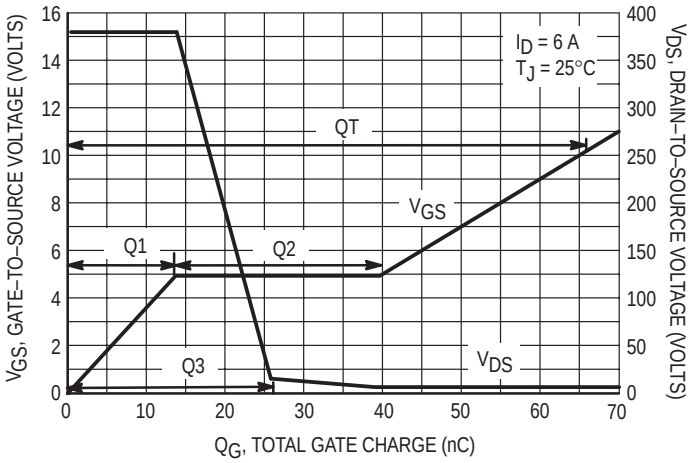


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

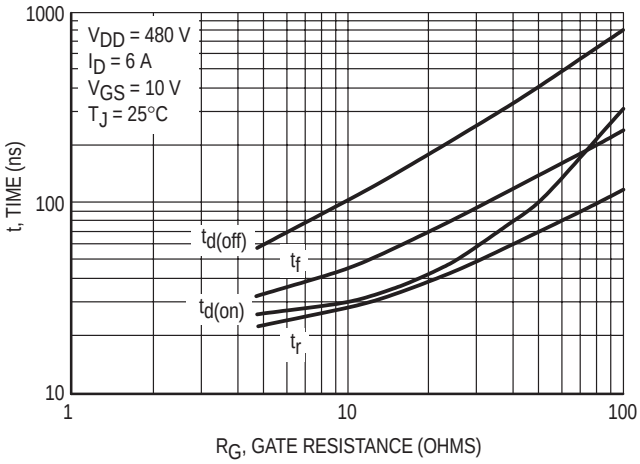


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

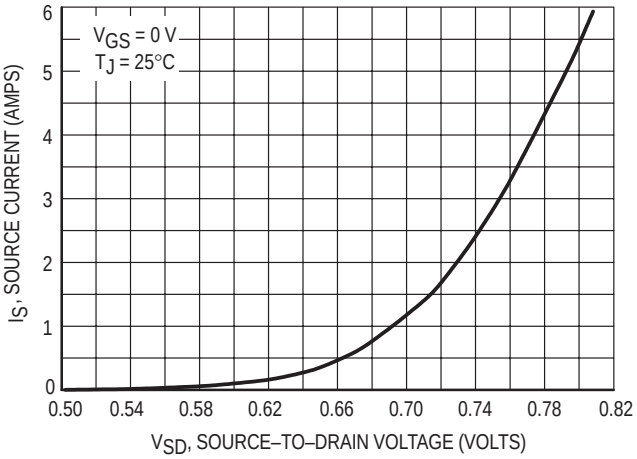


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

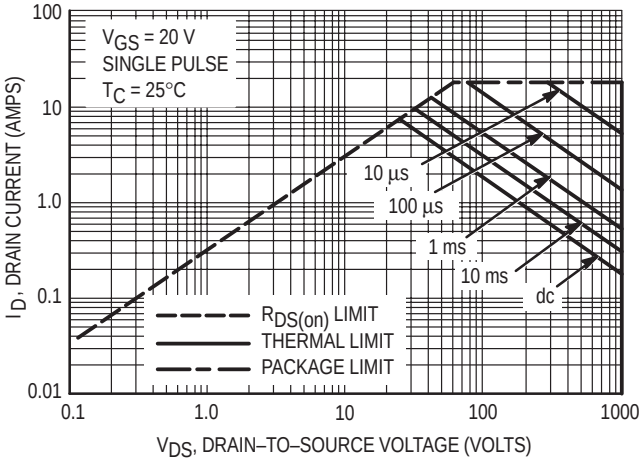


Figure 11. Maximum Rated Forward Biased Safe Operating Area

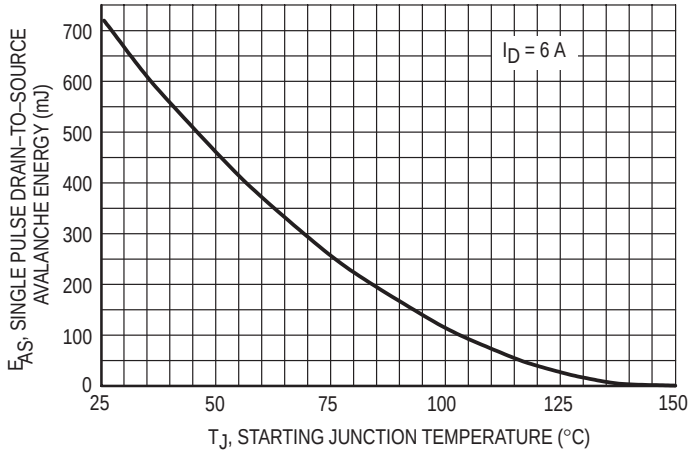


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

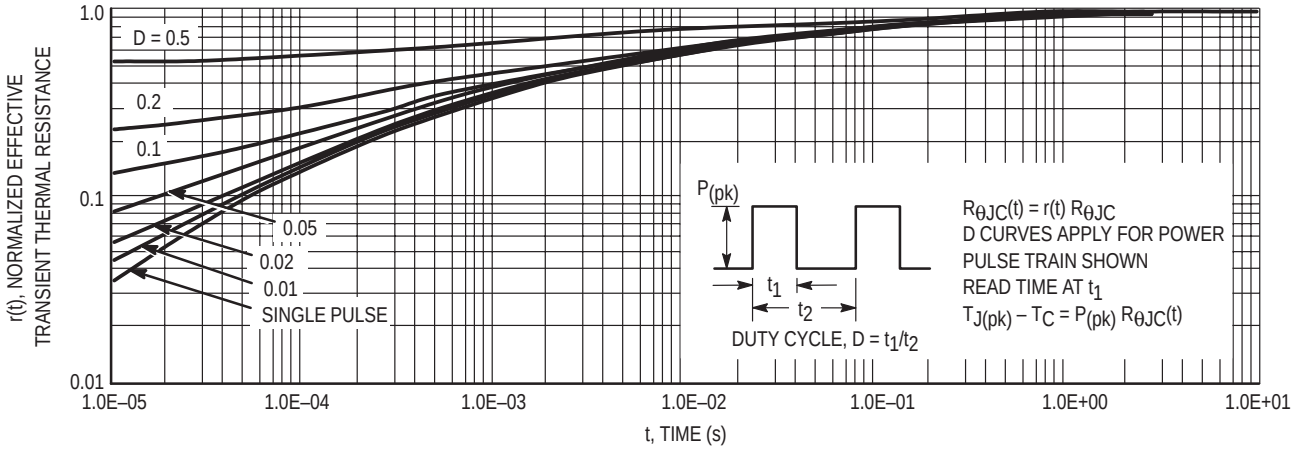


Figure 13. Thermal Response

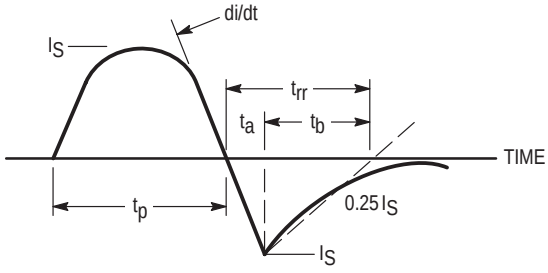


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
TO-247 With Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

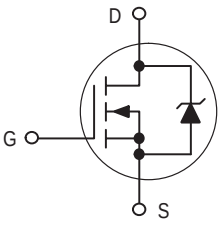
MTW7N80E

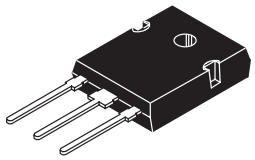
Motorola Preferred Device

TMOS POWER FET
7.0 AMPERES
800 VOLTS
$R_{DS(on)}$ = 1.0 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	800	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	800	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	7.0 5.1 21	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	180 1.43	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} =100 Vdc, V_{GS} = 10 Vdc, I_L = 21 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	661	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.70 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	800 —	— 1,030	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 800 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 800 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 7.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 3.5 Adc)		$R_{DS(on)}$	—	0.87	1.0	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 7.0 Adc) (I_D = 3.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	6.8 —	10 10.5	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 3.5 Adc)		g_{FS}	4.0	7.63	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3000	4160	pF
Output Capacitance		C_{oss}	—	244	490	
Reverse Transfer Capacitance		C_{rss}	—	46	90	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 400 Vdc, I_D = 7.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	20	40	ns
Rise Time		t_r	—	37	85	
Turn–Off Delay Time		$t_{d(off)}$	—	84	165	
Fall Time		t_f	—	49	105	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 7.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	70	105	nC
		Q_1	—	13	—	
		Q_2	—	28	—	
		Q_3	—	23	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 7.0 Adc, V_{GS} = 0 Vdc) (I_S = 7.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.817 0.7	1.14 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 7.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	651	—	ns
		t_a	—	164	—	
		t_b	—	487	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4.78	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

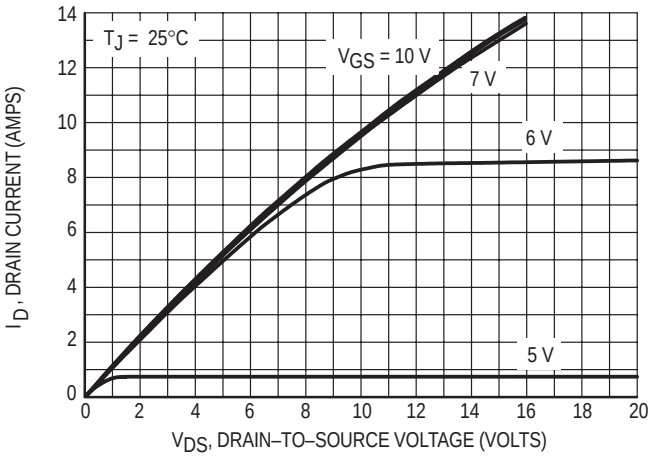


Figure 1. On–Region Characteristics

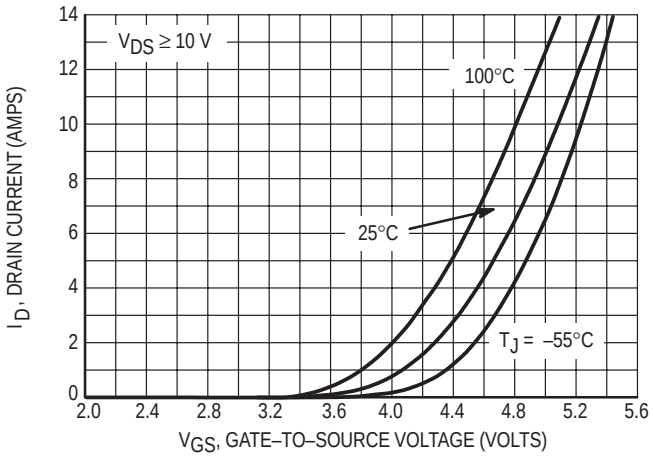


Figure 2. Transfer Characteristics

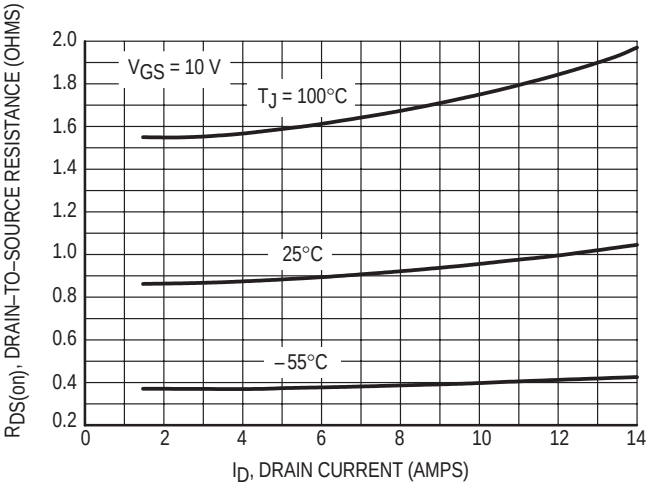


Figure 3. On–Resistance versus Drain Current and Temperature

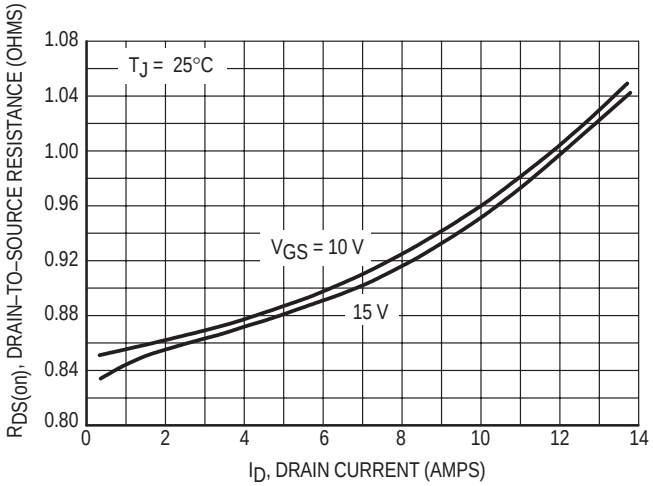


Figure 4. On–Resistance versus Drain Current and Gate Voltage

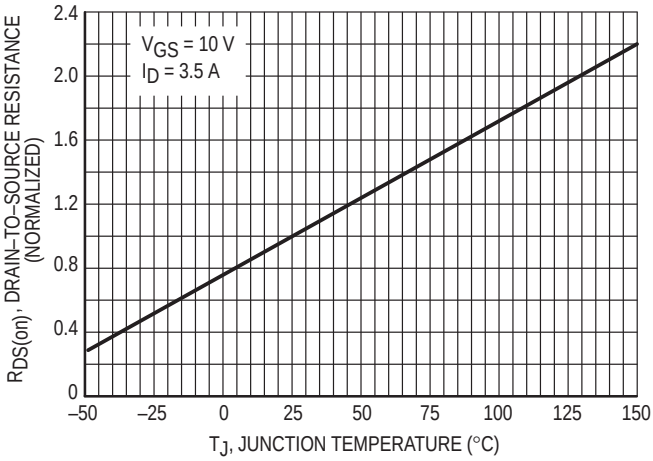


Figure 5. On–Resistance Variation with Temperature

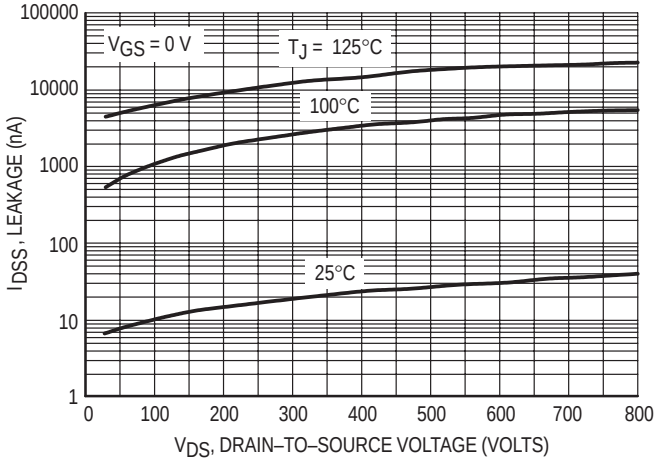


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

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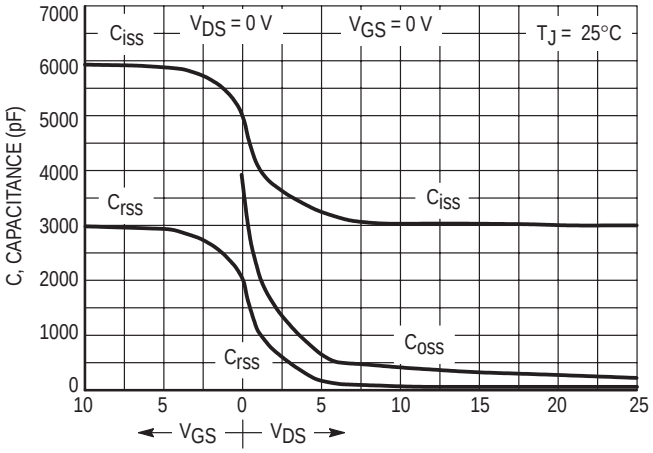

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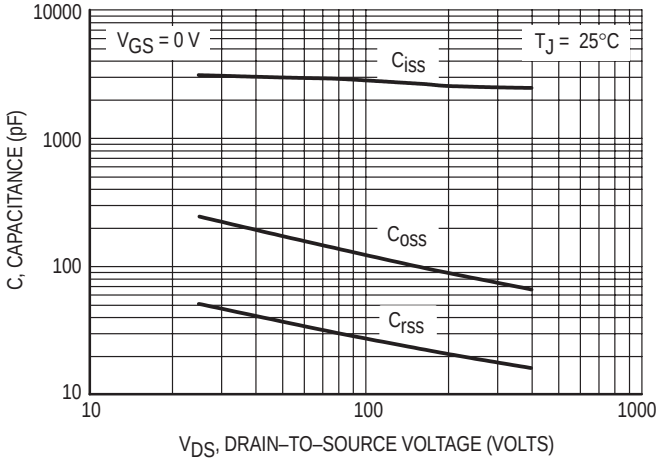
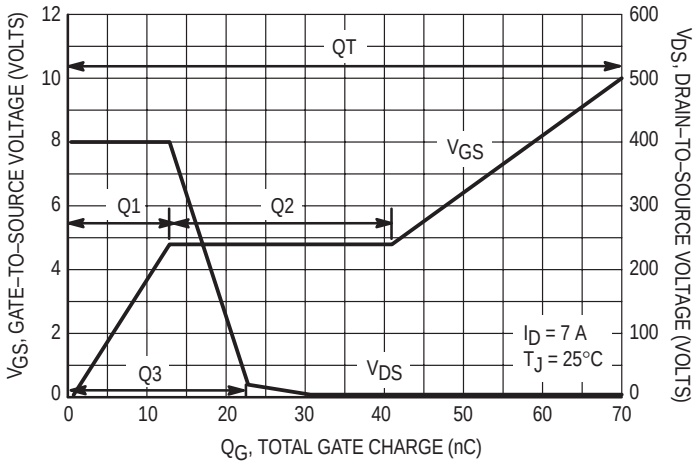


Figure 7b. High Voltage Capacitance Variation



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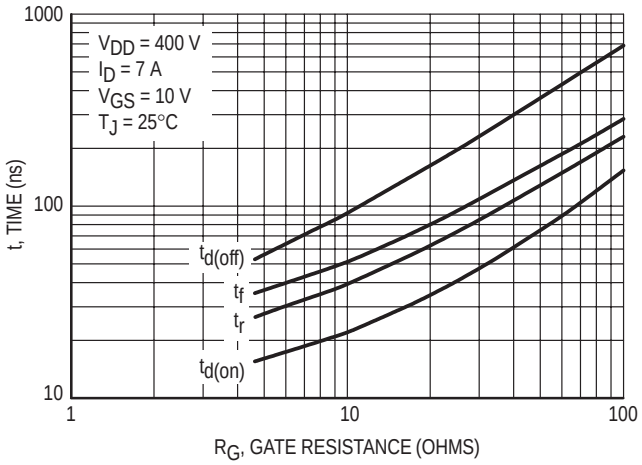

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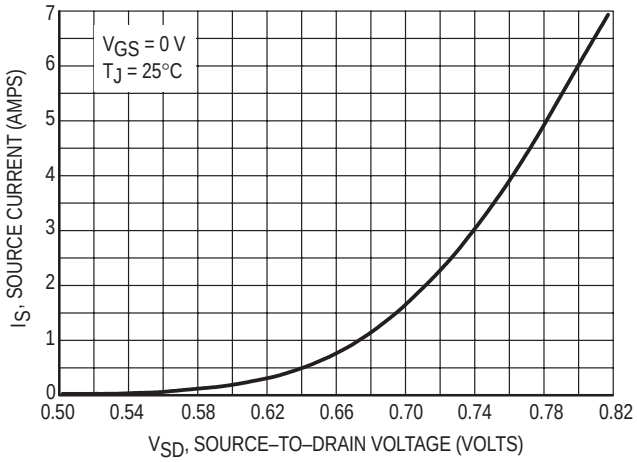
DRAIN–TO–SOURCE DIODE CHARACTERISTICS



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SAFE OPERATING AREA

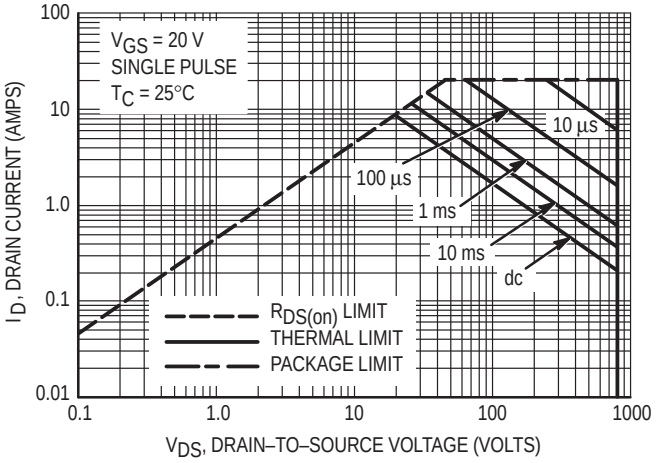
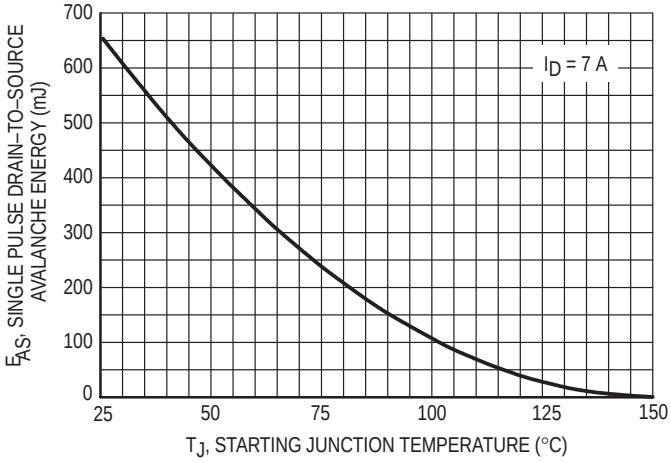


Figure 11. Maximum Rated Forward Biased Safe Operating Area



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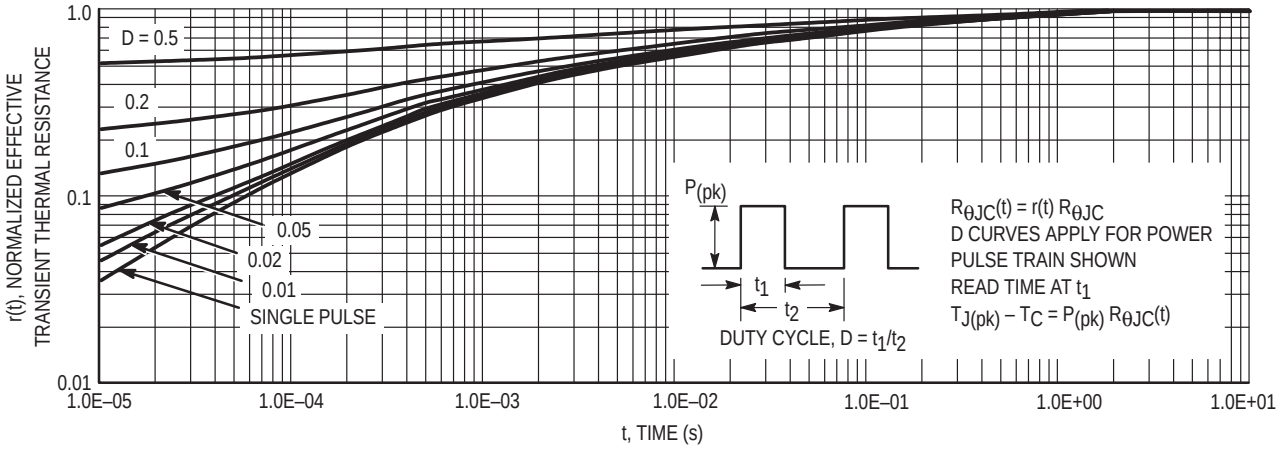


Figure 13. Thermal Response

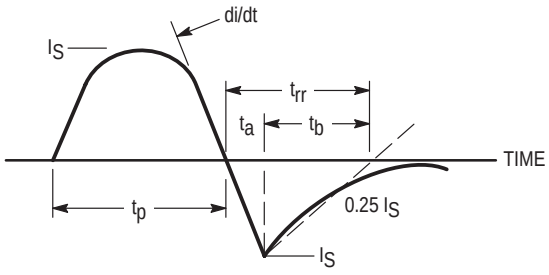


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

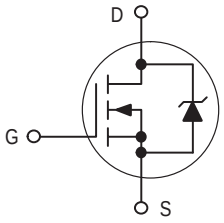
MTW8N60E

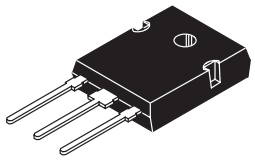
Motorola Preferred Device

TMOS POWER FET
8.0 AMPERES
600 VOLTS
$R_{DS(on)}$ = 0.55 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	600	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	8.0 6.4 24	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	180 1.43	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 24 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	864	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.70 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	600 —	— 695	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 7.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 4.0 Adc)		$R_{DS(on)}$	—	0.46	0.55	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 8.0 Adc) (I_D = 4.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	3.2 —	4.8 4.6	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 4.0 Adc)		g_{FS}	4.0	8.5	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	2480	3470	pF
Output Capacitance		C_{oss}	—	247	346	
Reverse Transfer Capacitance		C_{rss}	—	56	120	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 300 Vdc, I_D = 8.0 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	23.6	50	ns
Rise Time		t_r	—	37.6	70	
Turn–Off Delay Time		$t_{d(off)}$	—	80	170	
Fall Time		t_f	—	48	95	
Gate Charge (See Figure 8)	(V_{DS} = 300 Vdc, I_D = 8.0 Adc, V_{GS} = 10 Vdc)	Q_T	—	67	100	nC
		Q_1	—	17	—	
		Q_2	—	26	—	
		Q_3	—	27	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 8.0 Adc, V_{GS} = 0 Vdc) (I_S = 8.0 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.829 0.71	1.1 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 8.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	381	—	ns
		t_a	—	225	—	
		t_b	—	156	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4.61	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

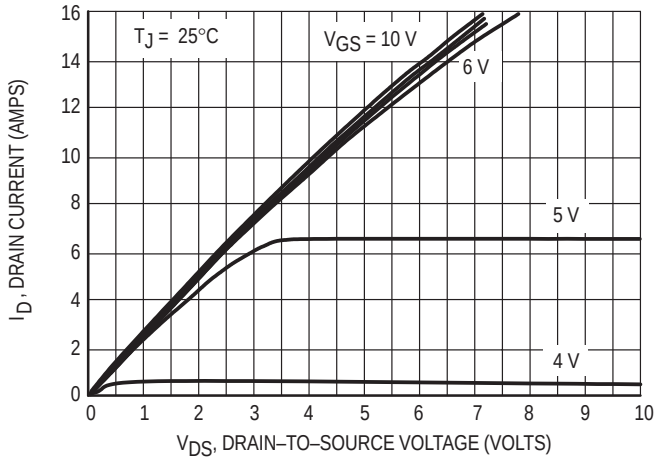


Figure 1. On–Region Characteristics

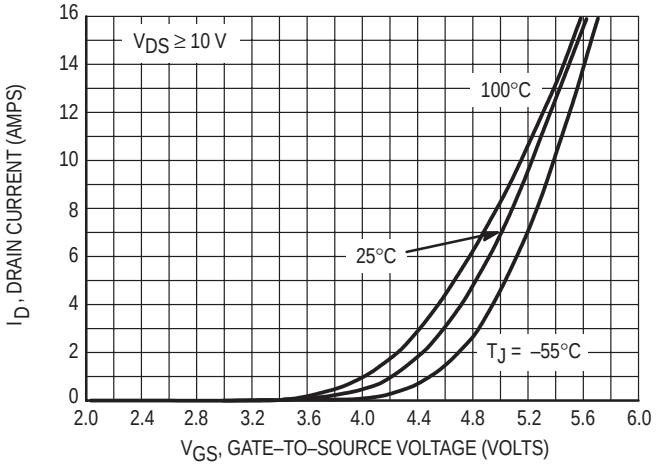


Figure 2. Transfer Characteristics

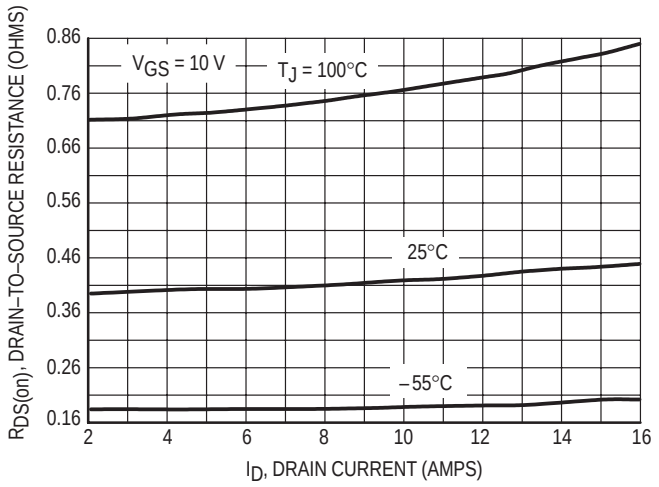


Figure 3. On–Resistance versus Drain Current and Temperature

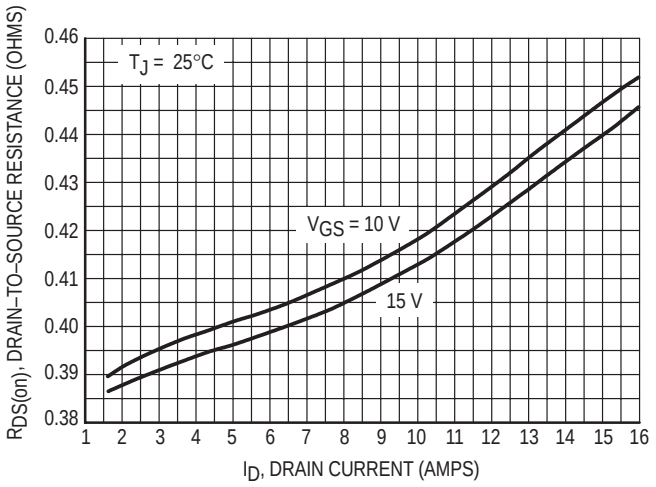


Figure 4. On–Resistance versus Drain Current and Gate Voltage

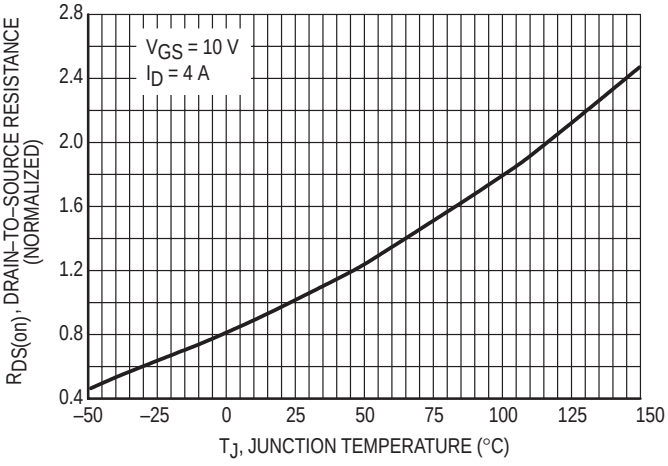


Figure 5. On–Resistance Variation with Temperature

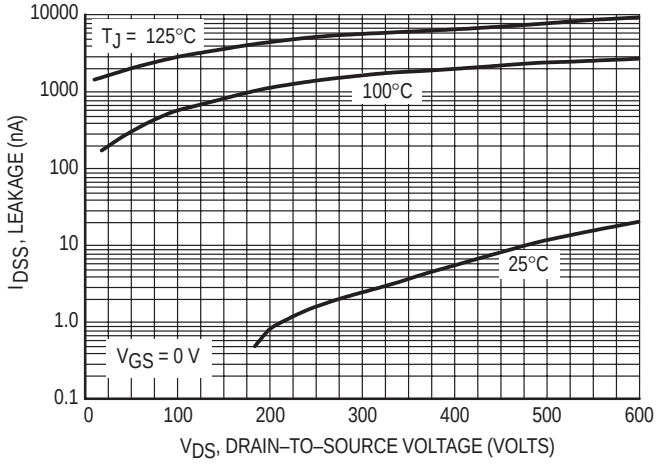


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

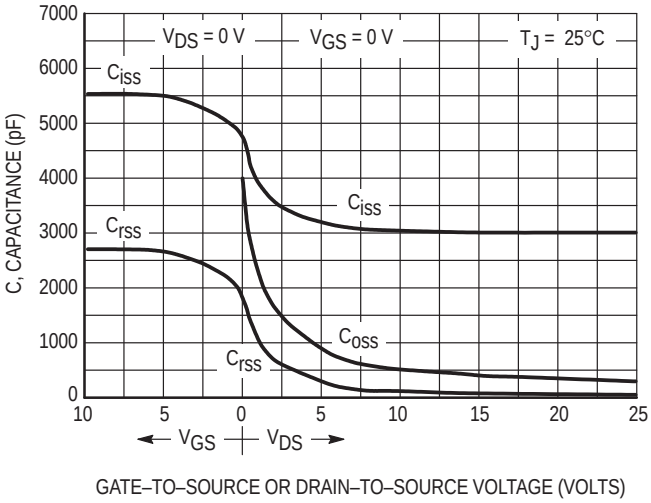


Figure 7a. Capacitance Variation

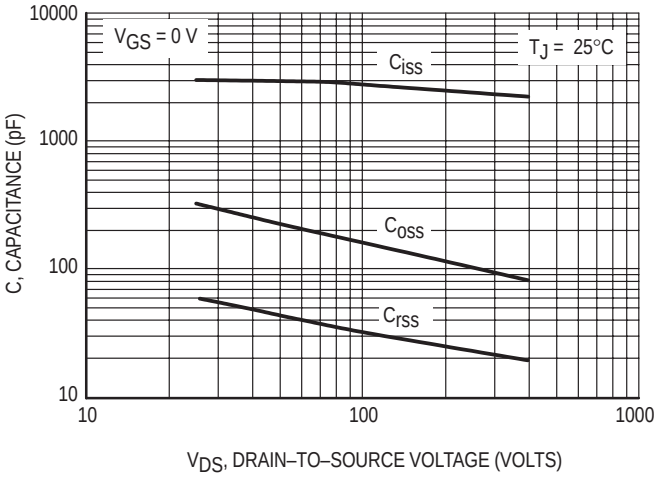


Figure 7b. High Voltage Capacitance Variation

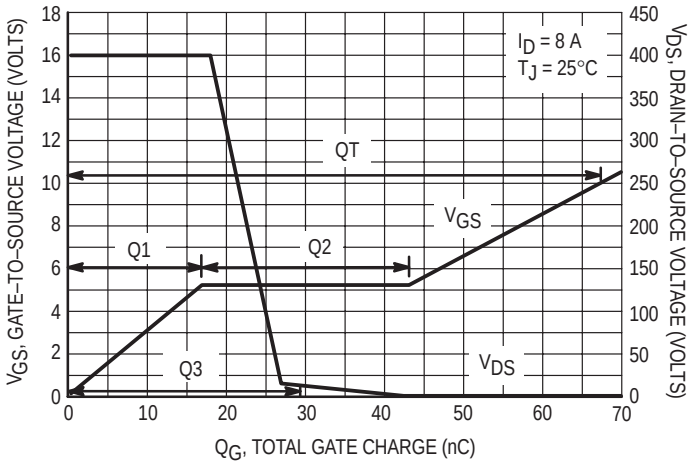


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

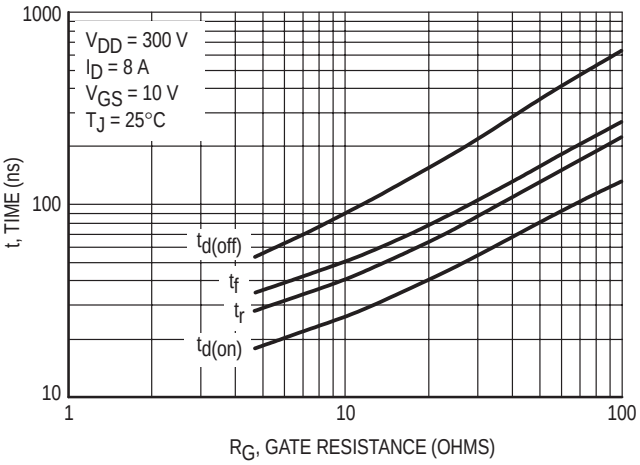


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

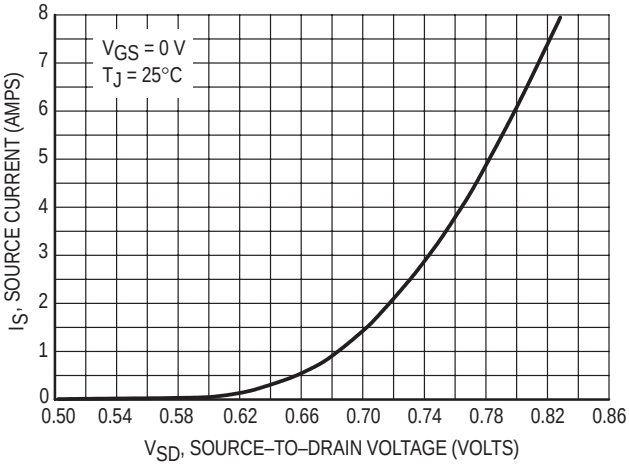


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

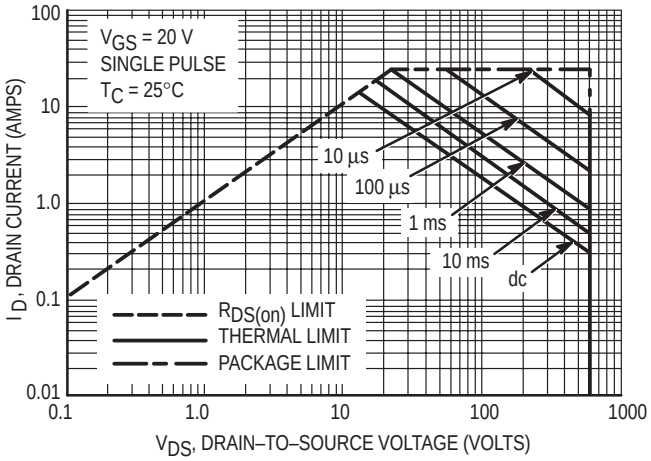


Figure 11. Maximum Rated Forward Biased Safe Operating Area

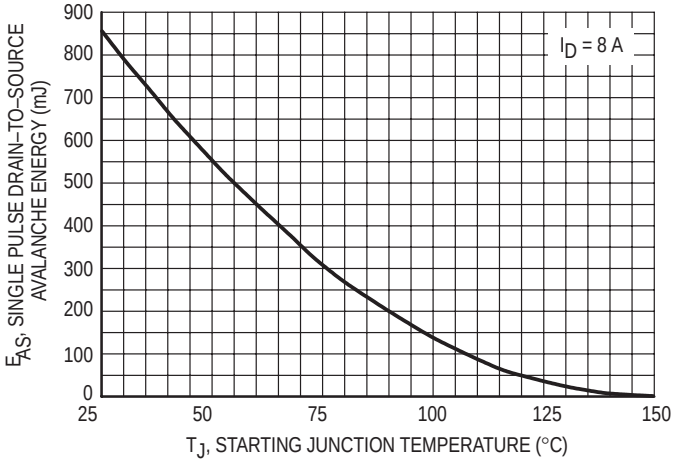


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

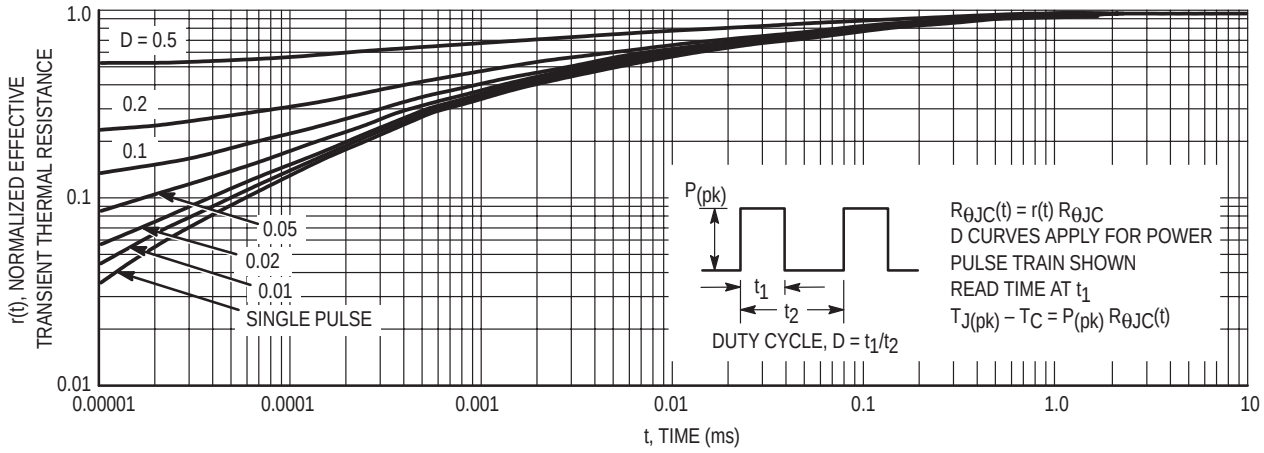


Figure 13. Thermal Response

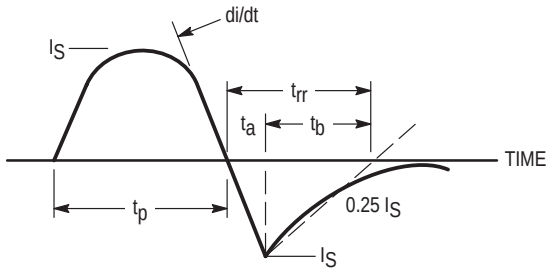


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

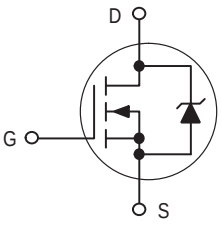
MTW10N100E

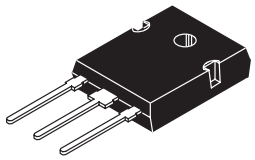
Motorola Preferred Device

TMOS POWER FET
10 AMPERES
1000 VOLTS
$R_{DS(on)}$ = 1.3 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transient.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	1000	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	1000	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	10 6.2 30	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	250 2.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 10 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	500	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.50 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	1000 —	— 1,254	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.0 7.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 5.0 Adc)		$R_{DS(on)}$	—	1.10	1.3	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 10 Adc) (I_D = 5.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	11 —	15 15.3	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 5.0 Adc)		g_{FS}	8.0	10	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3500	5600	pF
Output Capacitance		C_{oss}	—	264	530	
Reverse Transfer Capacitance		C_{rss}	—	52	90	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 500 Vdc, I_D = 10 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	29	60	ns
Rise Time		t_r	—	57	120	
Turn–Off Delay Time		$t_{d(off)}$	—	118	240	
Fall Time		t_f	—	70	140	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 10 Adc, V_{GS} = 10 Vdc)	Q_T	—	100	120	nC
		Q_1	—	18.4	—	
		Q_2	—	33	—	
		Q_3	—	36.7	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 10 Adc, V_{GS} = 0 Vdc) (I_S = 10 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.885 0.8	1.1 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 10 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	885	—	ns
		t_a	—	220	—	
		t_b	—	667	—	
Reverse Recovery Stored Charge		Q_{RR}	—	8.0	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

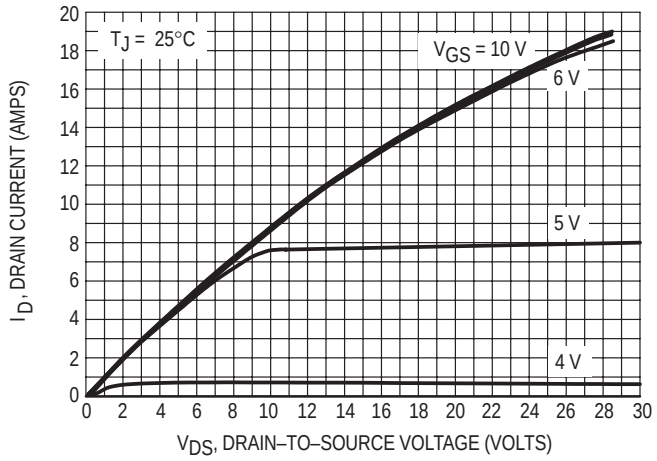


Figure 1. On–Region Characteristics

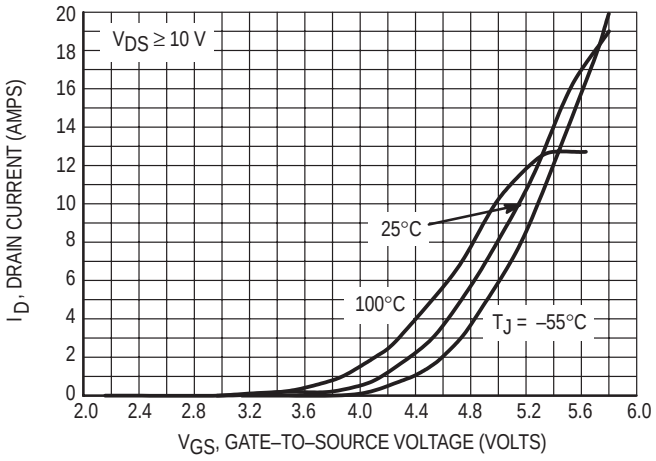


Figure 2. Transfer Characteristics

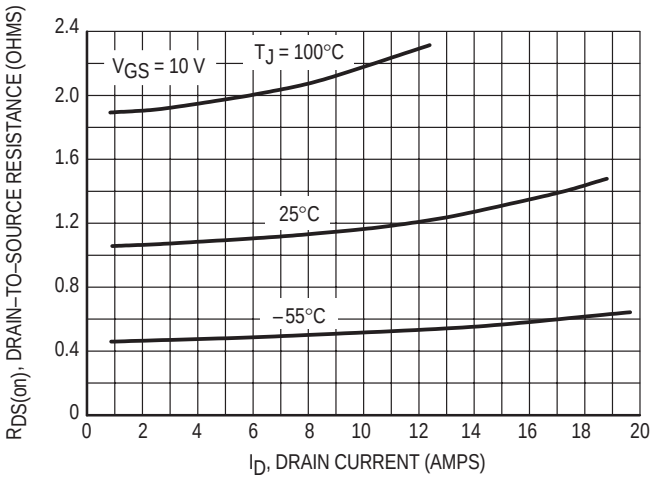


Figure 3. On–Resistance versus Drain Current and Temperature

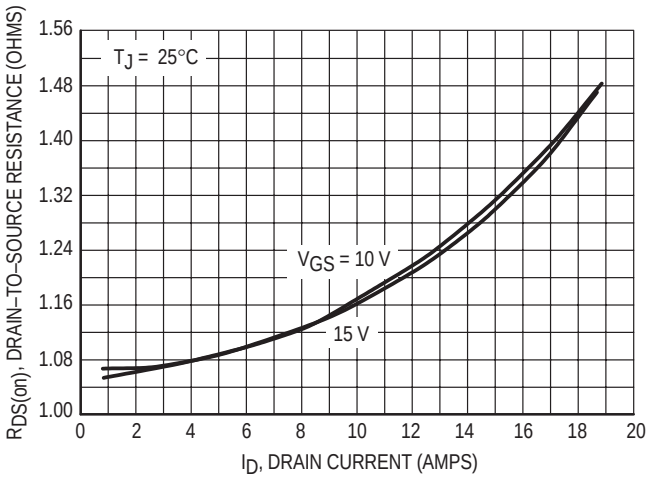


Figure 4. On–Resistance versus Drain Current and Gate Voltage

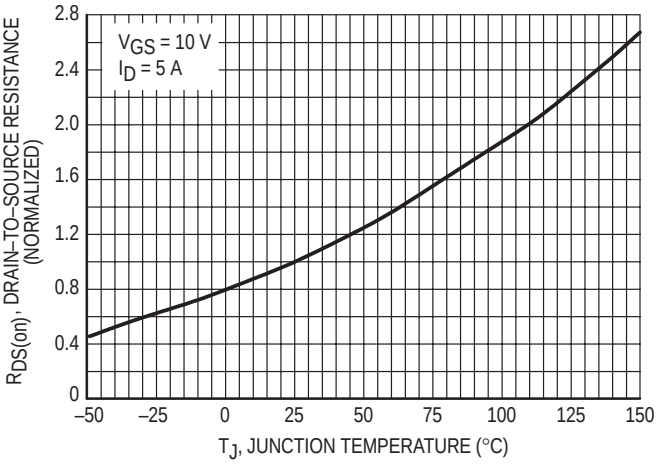


Figure 5. On–Resistance Variation with Temperature

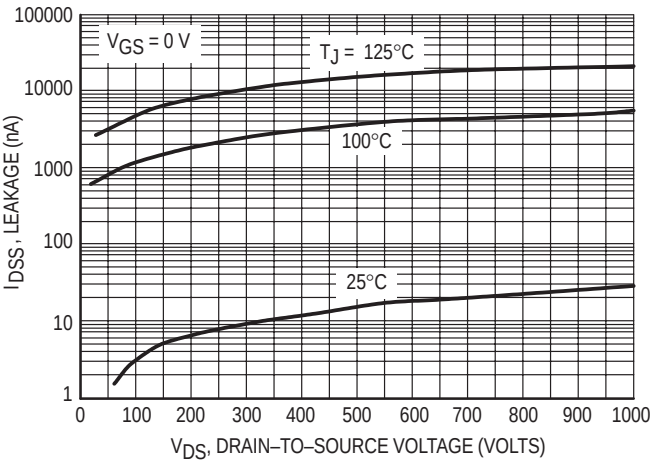


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

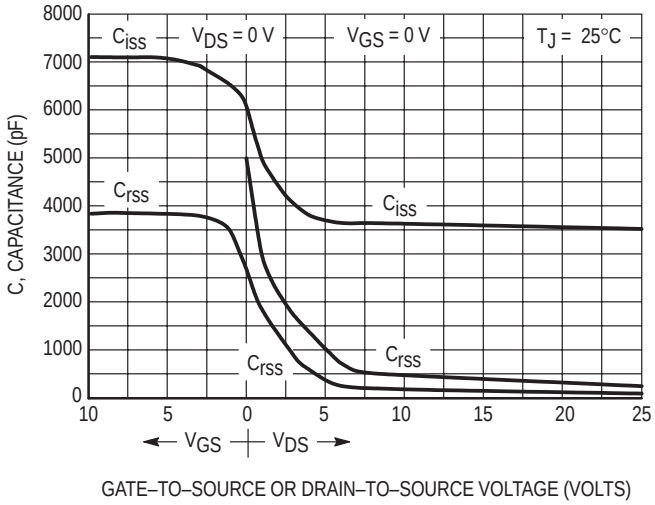


Figure 7a. Capacitance Variation

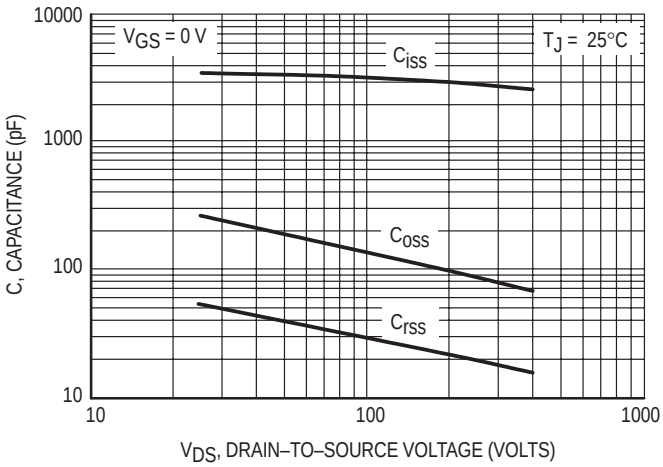


Figure 7b. High Voltage Capacitance Variation

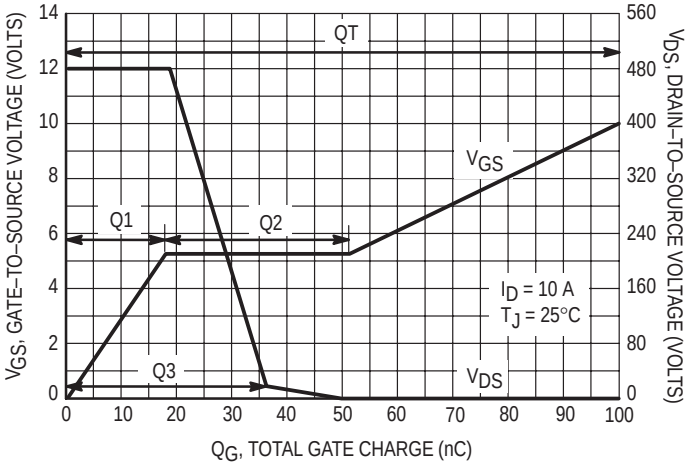


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

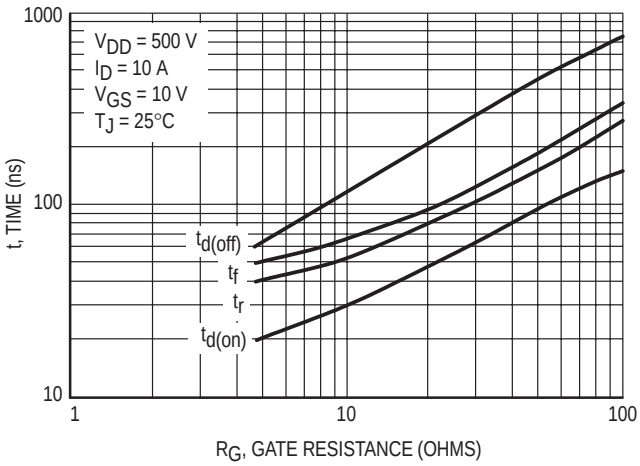


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

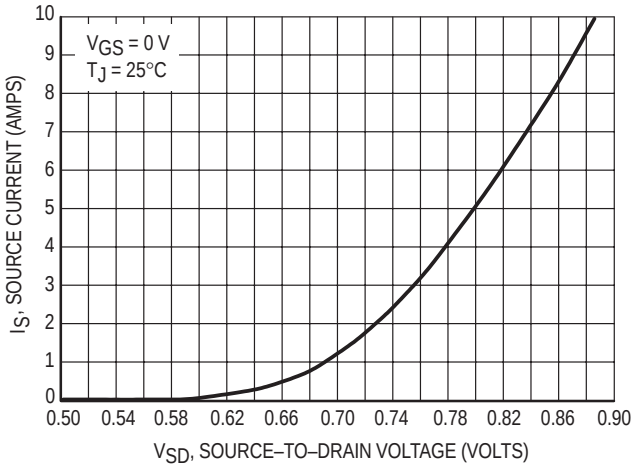


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

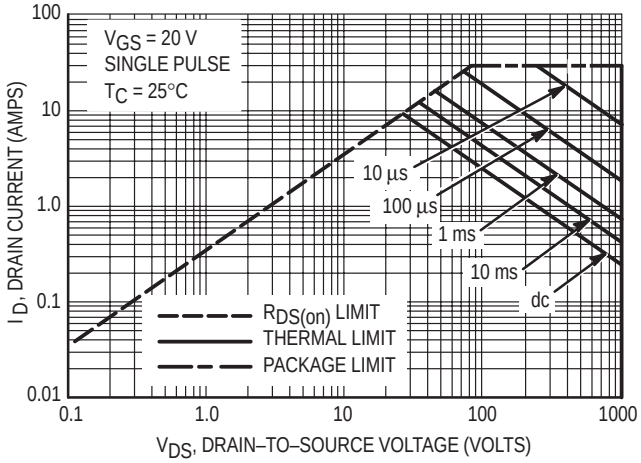


Figure 11. Maximum Rated Forward Biased Safe Operating Area

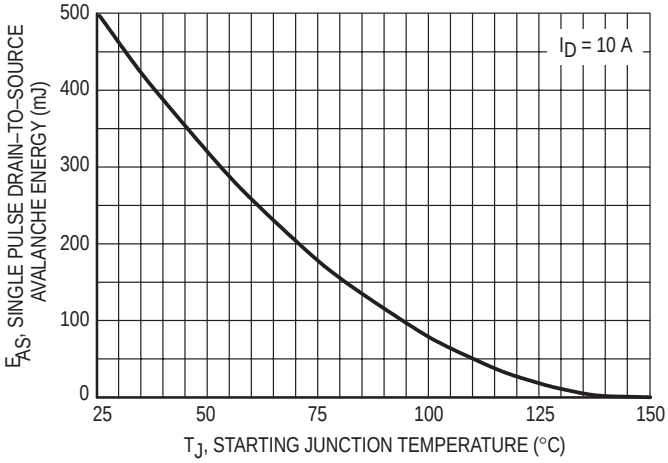


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

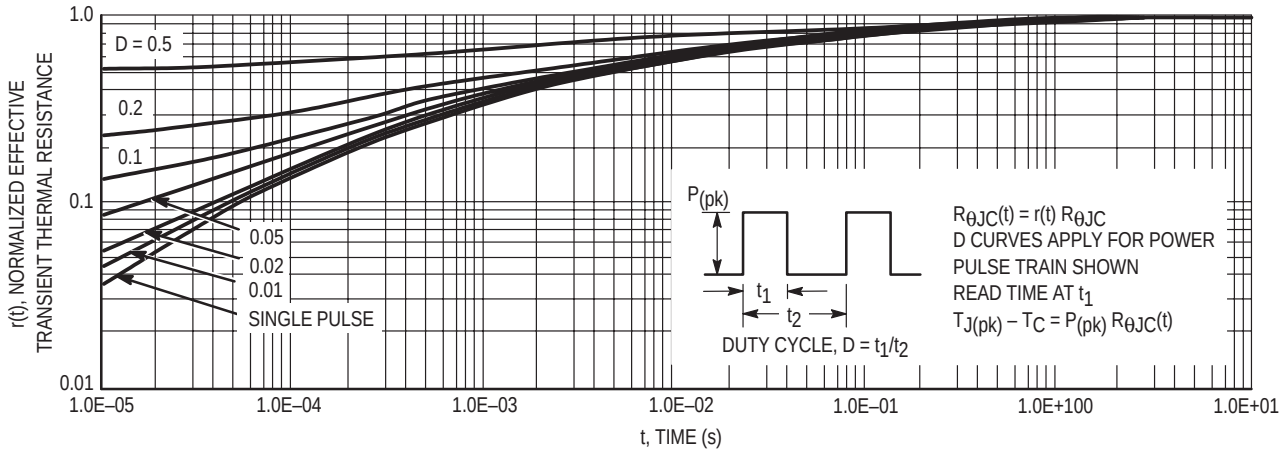


Figure 13. Thermal Response

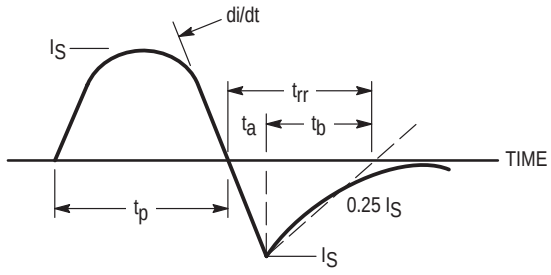


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

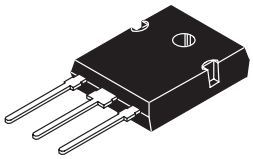
MTW14N50E

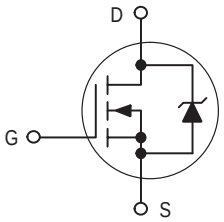
Motorola Preferred Device

TMOS POWER FET
14 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.40 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous	V_{GS}	±20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	14 9.0 60	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	180 1.44	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vpk, I_L = 14 Apk, L = 8.8 mH, R_G = 25 Ω)	E_{AS}	860	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.7 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 V, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	500 —	— 520	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0) (V_{DS} = 500 Vdc, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	— —	250 1000	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	3.2 7.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 7.0 Adc)		$R_{DS(on)}$	—	0.32	0.40	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 14 Adc) (I_D = 7.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	6.7 5.6	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 7.0 Adc)		g_{FS}	5.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	2510	3510	pF
Output Capacitance		C_{oss}	—	280	392	
Reverse Transfer Capacitance		C_{rss}	—	67	94	
SWITCHING CHARACTERISTICS*†						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 14 Adc, V_{GS} = 10 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	28	60	ns
Rise Time		t_r	—	80	160	
Turn–Off Delay Time		$t_{d(off)}$	—	80	160	
Fall Time		t_f	—	60	120	
Gate Charge	(V_{DS} = 400 Vdc, I_D = 14 Adc, V_{GS} = 10 Vdc)	Q_T	—	65	85	nC
		Q_1	—	17	—	
		Q_2	—	47	—	
		Q_3	—	34	—	
SOURCE–DRAIN DIODE CHARACTERISTICS*						
Forward On–Voltage	(I_S = 14 Adc, V_{GS} = 0) (I_S = 14 Adc, V_{GS} = 0, T_J = 125°C)	V_{SD}	— —	1.0 0.9	1.6 —	Vdc
Reverse Recovery Time	(I_S = 14 Adc, V_{GS} = 0, dI_S/dt = 100 A/μs, V_{GS} = 0)	t_{rr}	—	390	—	ns
		t_a	—	245	—	
		t_b	—	145	—	
Reverse Recovery Stored Charge		Q_{RR}	—	5.35	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	5.0	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

†Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

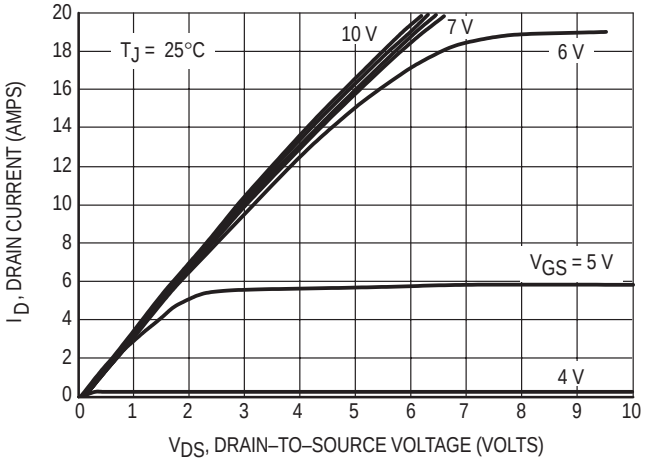
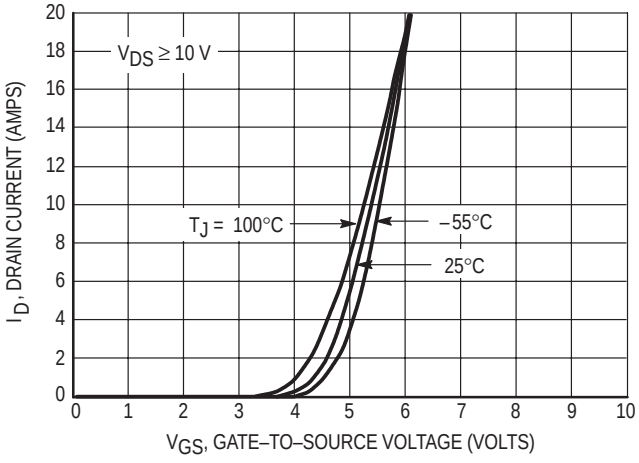


Figure 1. On–Region Characteristics



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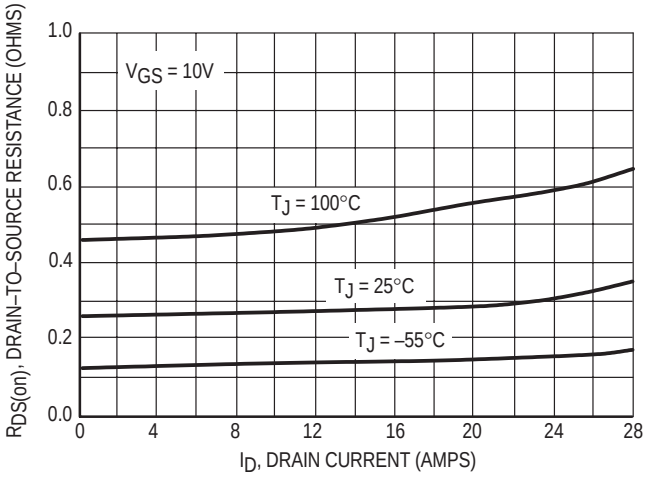

Figure 3.On–Resistance versus Drain Current

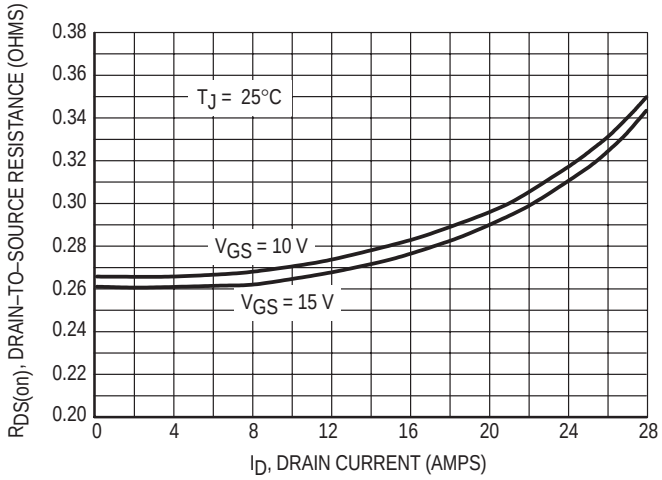

Figure 4.On–Resistance versus Drain Current

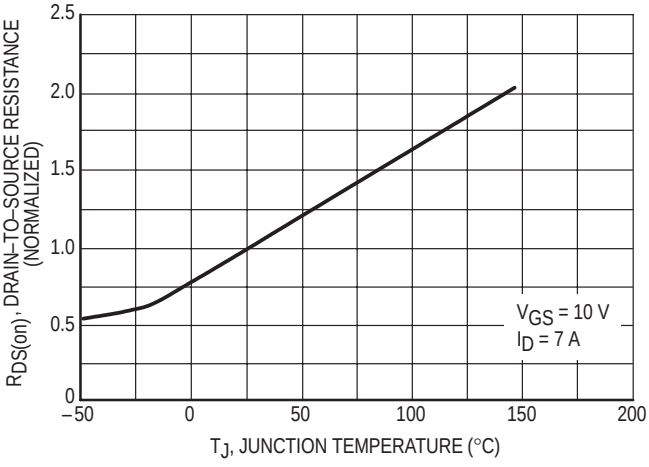

Figure 5.On–Resistance Variation With Temperature

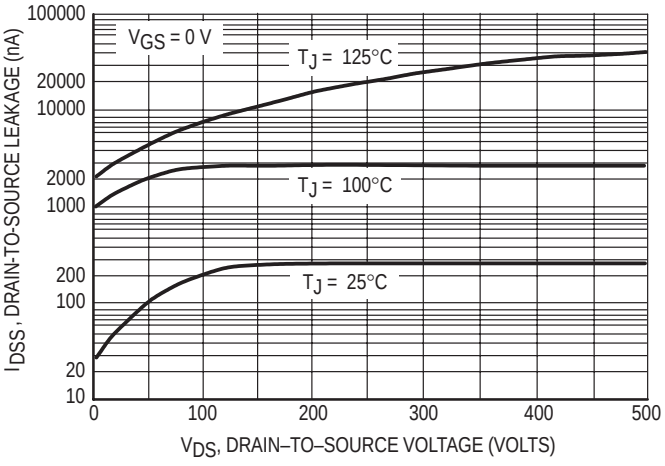

Figure 6.Drain–To–Source Leakage Current versus Voltage

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$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 10) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

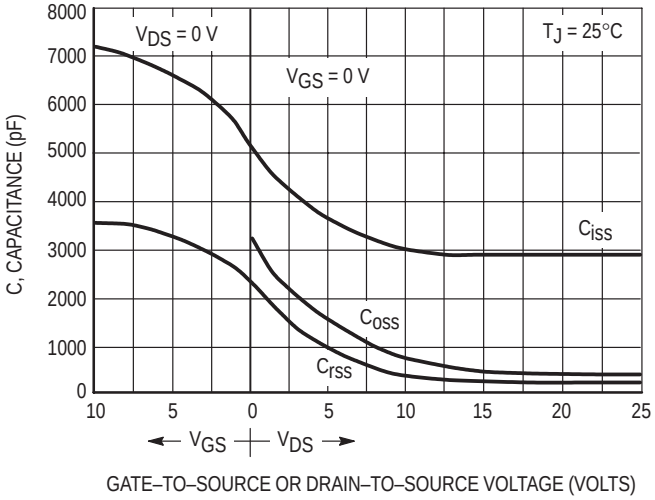


Figure 7a. Low Voltage Capacitance Variation

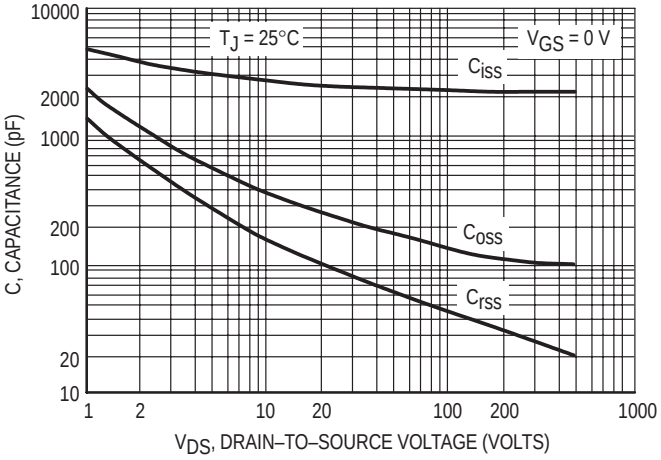


Figure 7b. High Voltage Capacitance Variation

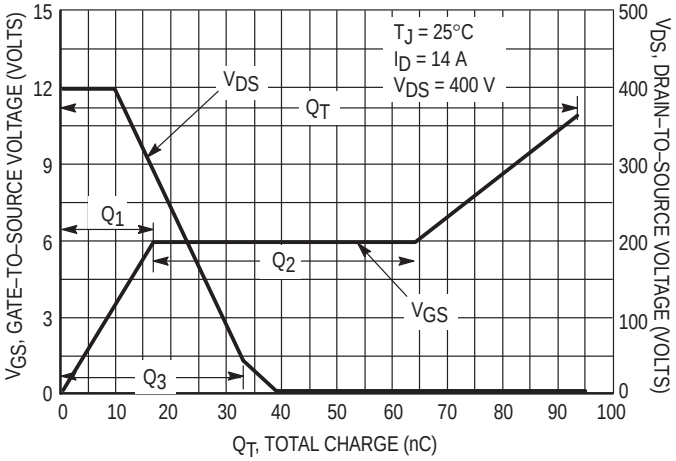


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

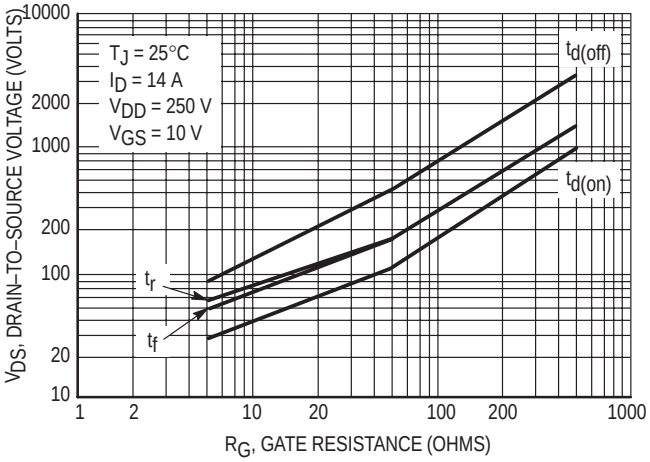


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

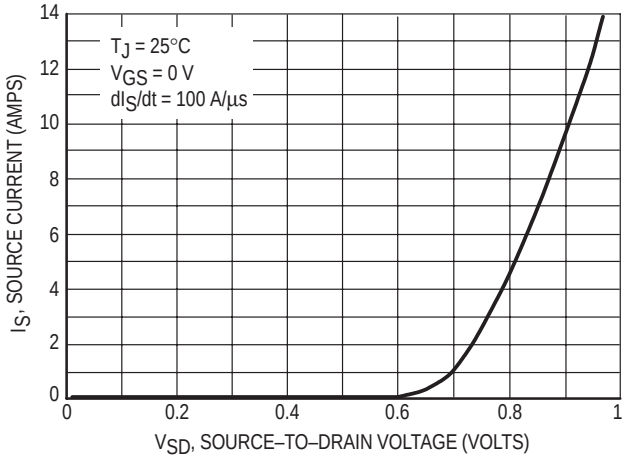


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

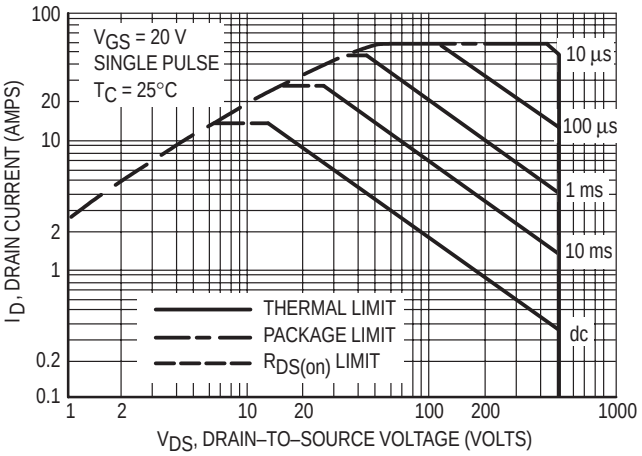


Figure 11. Maximum Rated Forward Biased Safe Operating Area

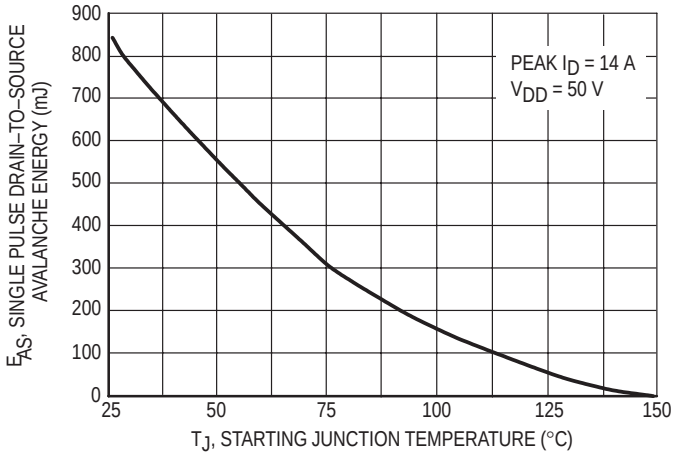


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

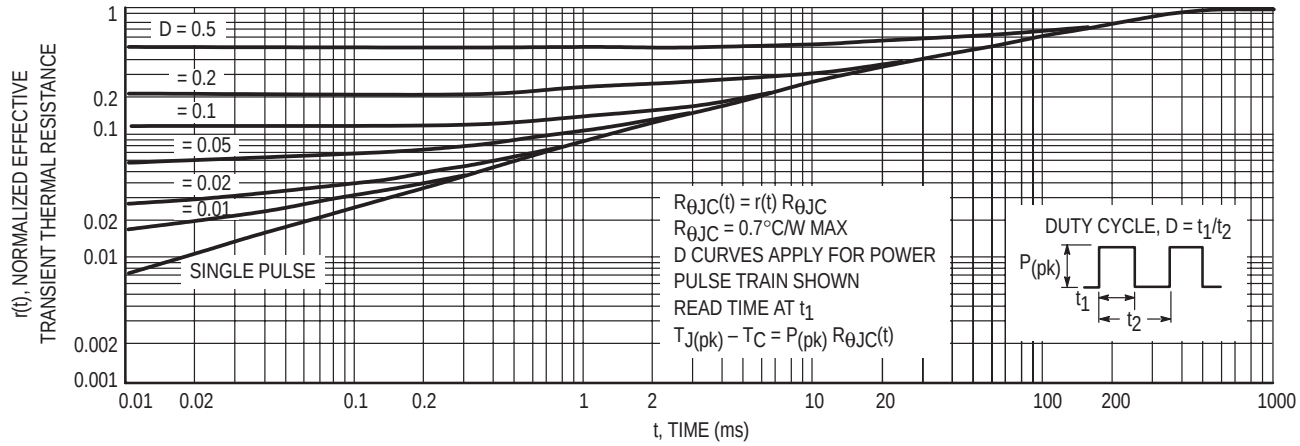


Figure 13. Thermal Response

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

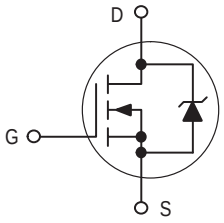
MTW16N40E

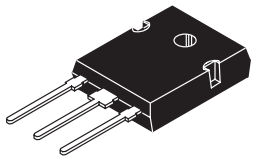
Motorola Preferred Device

TMOS POWER FET
16 AMPERES
400 VOLTS
$R_{DS(on)}$ = 0.24 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	400	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	16 9.0 56	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	180 1.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 16 Apk, L = 6.8 mH, R_G = 25 Ω)	E_{AS}	870	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.70 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	400	—	—	Vdc
Temperature Coefficient (Positive)			—	420	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				mAdc
(V_{DS} = 400 Vdc, V_{GS} = 0 Vdc)			—	—	0.25	
(V_{DS} = 320 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	1.0	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage		$V_{GS(th)}$				Vdc
(V_{DS} = V_{GS}, I_D = 0.25 mAdc)			2.0	3.0	4.0	
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 8.0 Adc)		$R_{DS(on)}$	—	0.225	0.24	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 16 Adc)			—	—	4.8	
(I_D = 8.0 Adc, T_J = 125°C)			—	—	4.3	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 8.0 Adc)		g_{FS}	8.0	10	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	2570	3600	pF
Output Capacitance		C_{oss}	—	330	460	
Reverse Transfer Capacitance		C_{rss}	—	82	164	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 200 Vdc, I_D = 16 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	29	50	ns
Rise Time		t_r	—	62	70	
Turn–Off Delay Time		$t_{d(off)}$	—	76	170	
Fall Time		t_f	—	57	95	
Gate Charge (See Figure 8)	(V_{DS} = 320 Vdc, I_D = 16 Adc, V_{GS} = 10 Vdc)	Q_T	—	66	93	nC
		Q_1	—	17	—	
		Q_2	—	31	—	
		Q_3	—	30	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 16 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.6	Vdc
	(I_S = 16 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.9	—	
Reverse Recovery Time (See Figure 9)	(I_S = 16 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	340	—	ns
		t_a	—	228	—	
		t_b	—	112	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4.3	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	5.0	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

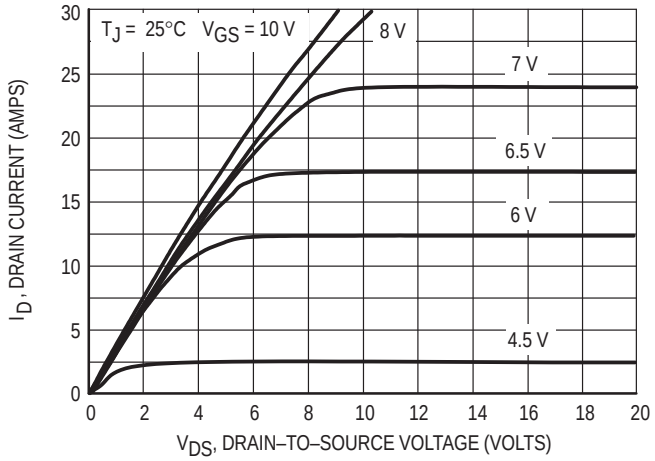


Figure 1. On–Region Characteristics

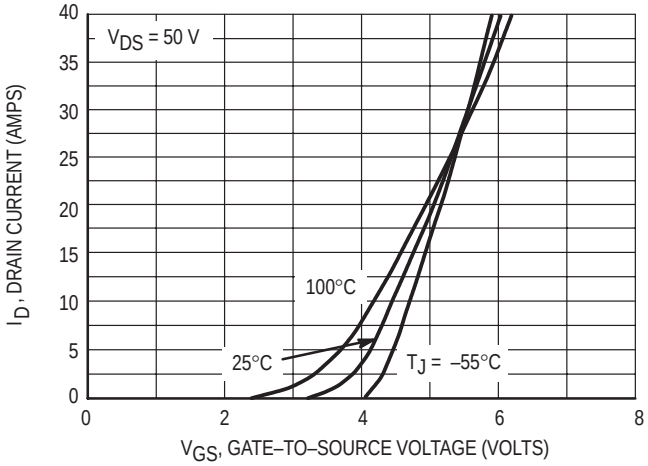


Figure 2. Transfer Characteristics

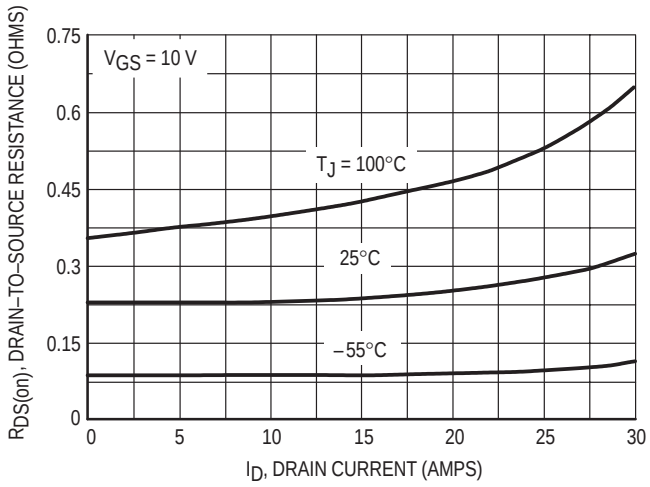


Figure 3. On–Resistance versus Drain Current and Temperature

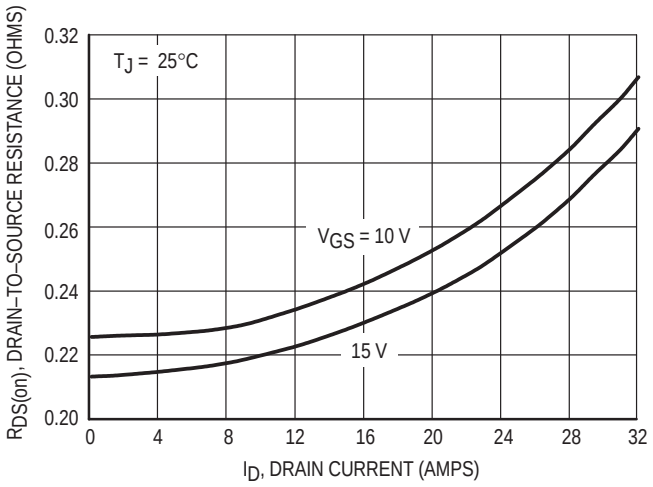


Figure 4. On–Resistance versus Drain Current and Gate Voltage

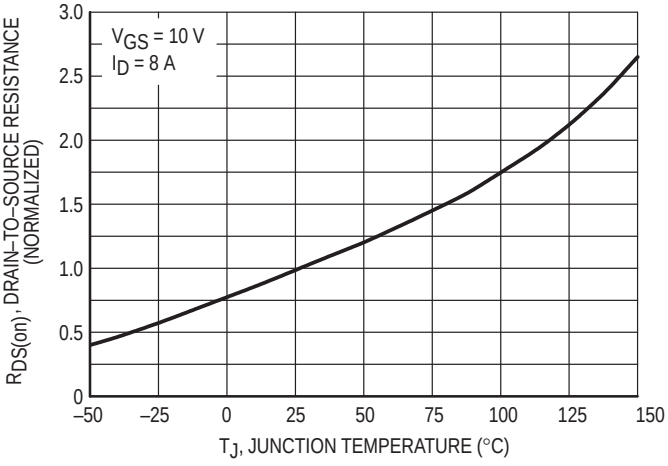


Figure 5. On–Resistance Variation with Temperature

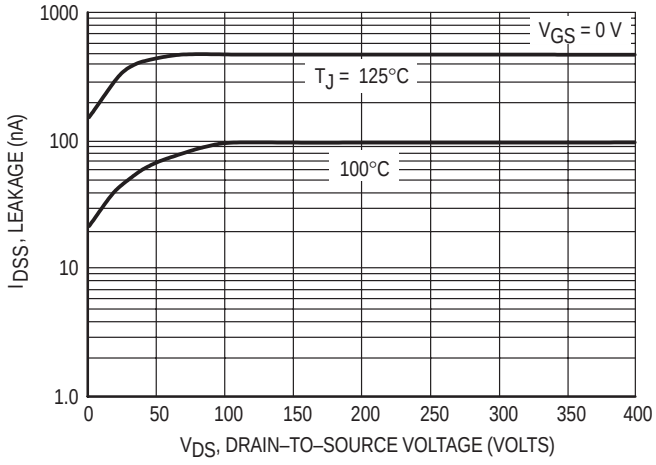


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

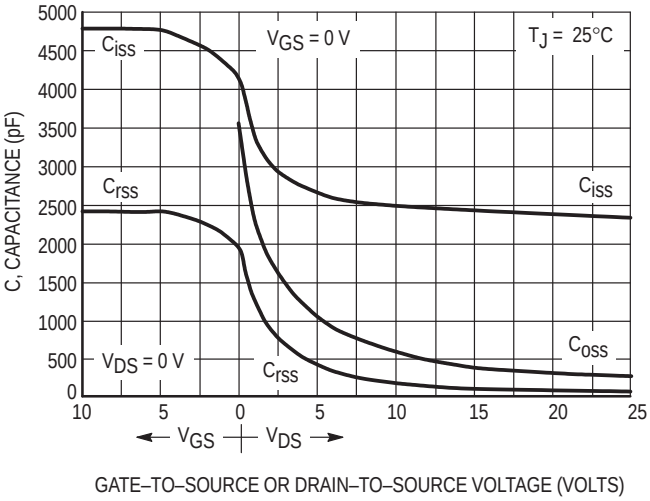


Figure 7a. Capacitance Variation

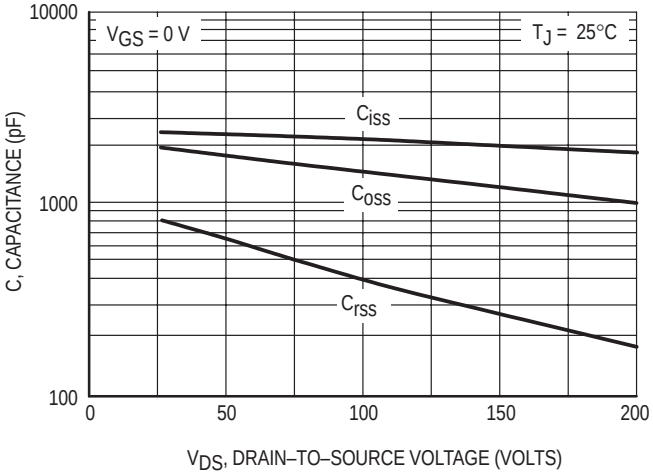


Figure 7b. High Voltage Capacitance Variation

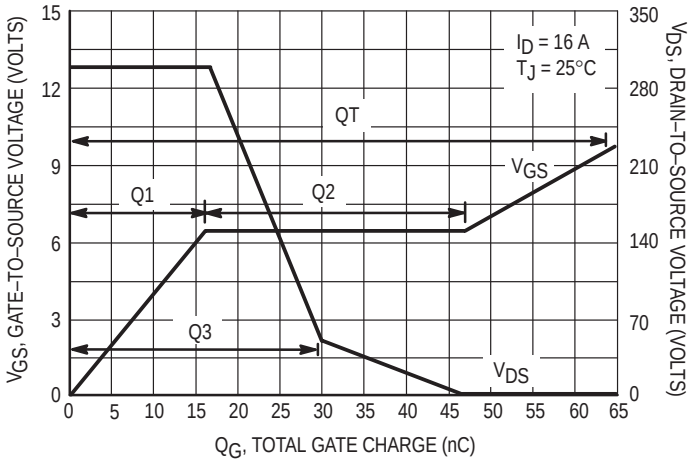


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

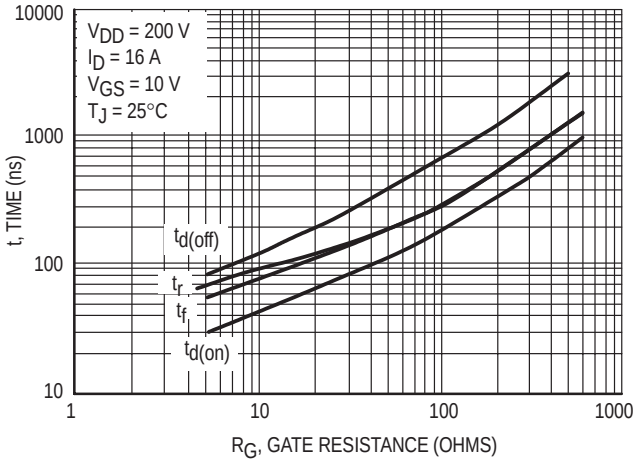


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

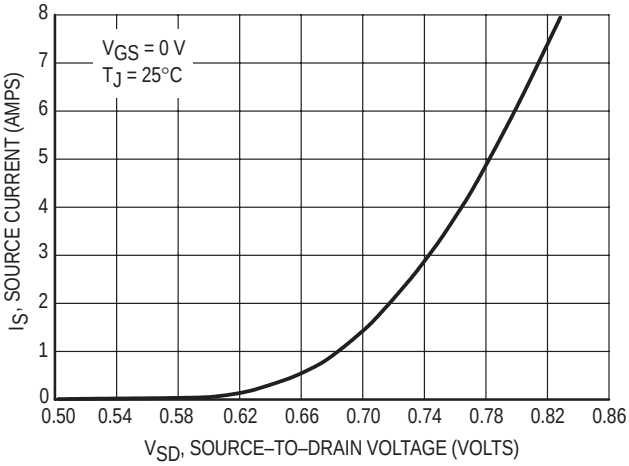


Figure 10. Diode Forward Voltage versus Current

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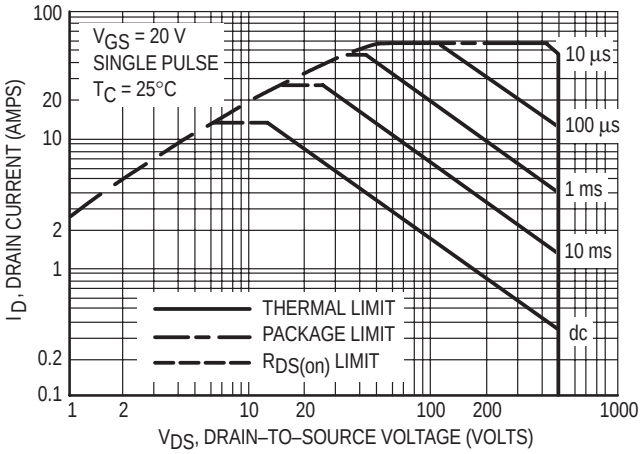

Figure 11. Maximum Rated Forward Biased Safe Operating Area

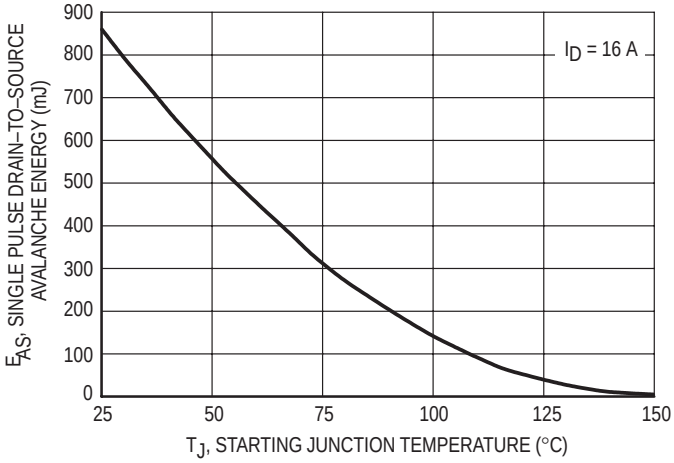

Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

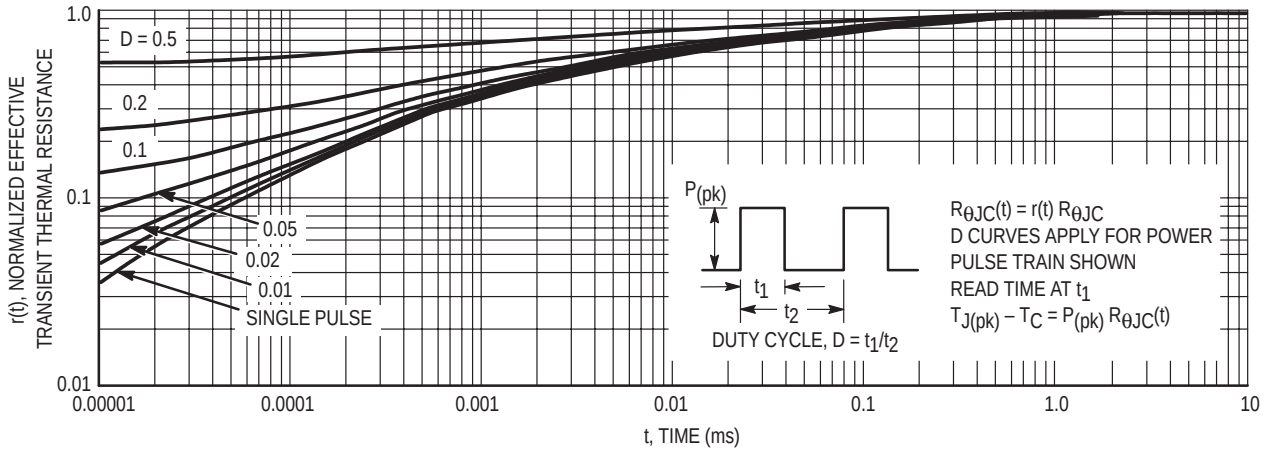

Figure 13. Thermal Response

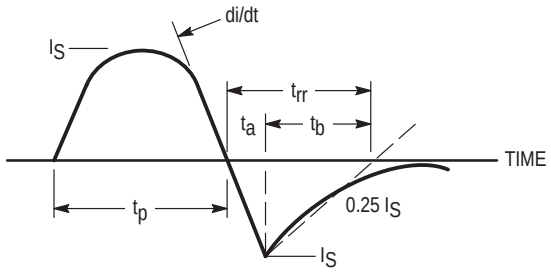

Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

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Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

MTW20N50E

Motorola Preferred Device

TMOS POWER FET
20 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.24 OHM

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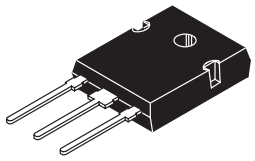
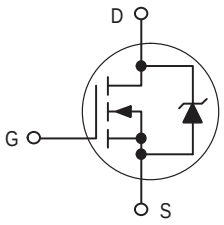
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	20 14.1 60	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	250 2.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 20 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	2000	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.50 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	500	—	—	Vdc
Temperature Coefficient (Positive)			—	583	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$R_{DS(on)}$	—	0.20	0.24	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 20 Adc)		$V_{DS(on)}$	—	5.75	6.0	Vdc
(I_D = 10 Adc, T_J = 125°C)			—	—	6.0	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 10 Adc)		g_{FS}	11	16.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3880	6950	pF
Output Capacitance		C_{oss}	—	452	920	
Reverse Transfer Capacitance		C_{rss}	—	96	140	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	29	55	ns
Rise Time		t_r	—	90	165	
Turn–Off Delay Time		$t_{d(off)}$	—	97	190	
Fall Time		t_f	—	84	170	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc)	Q_T	—	100	132	nC
		Q_1	—	20	—	
		Q_2	—	44	—	
		Q_3	—	36	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 20 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.916	1.1	Vdc
	(I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.81	—	
Reverse Recovery Time (See Figure 14)	(I_S = 20 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	431	—	ns
		t_a	—	272	—	
		t_b	—	159	—	
Reverse Recovery Stored Charge		Q_{RR}	—	6.67	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	5.0	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

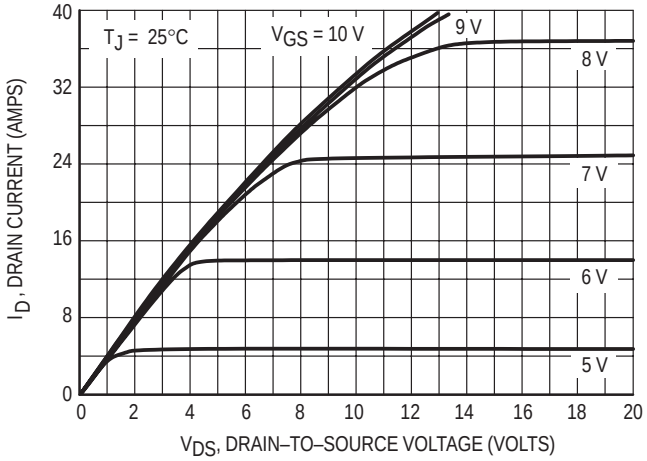


Figure 1. On–Region Characteristics

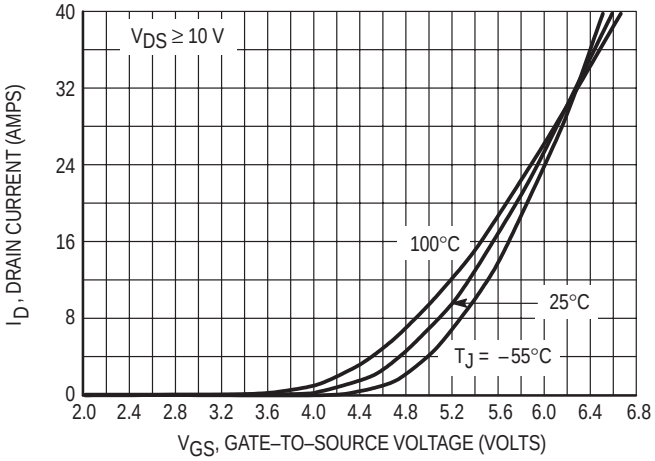


Figure 2. Transfer Characteristics

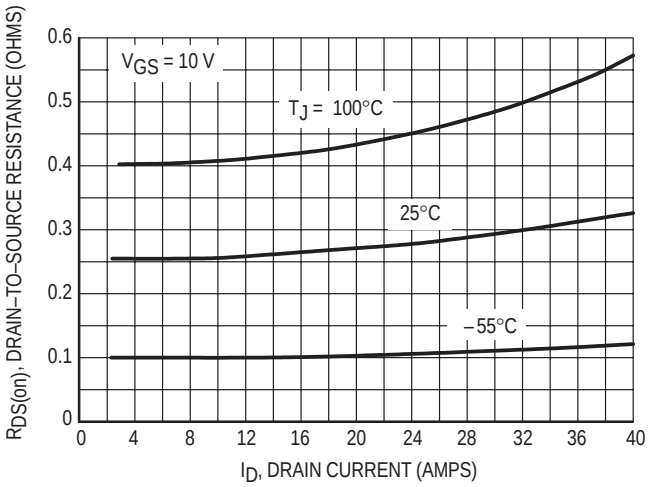


Figure 3. On–Resistance versus Drain Current and Temperature

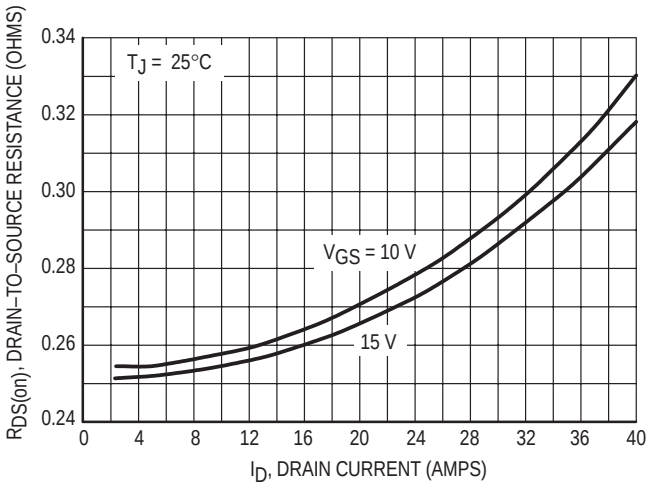


Figure 4. On–Resistance versus Drain Current and Gate Voltage

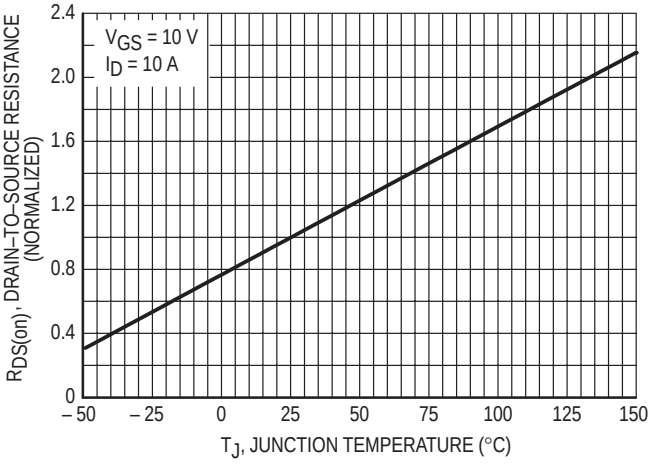


Figure 5. On–Resistance Variation with Temperature

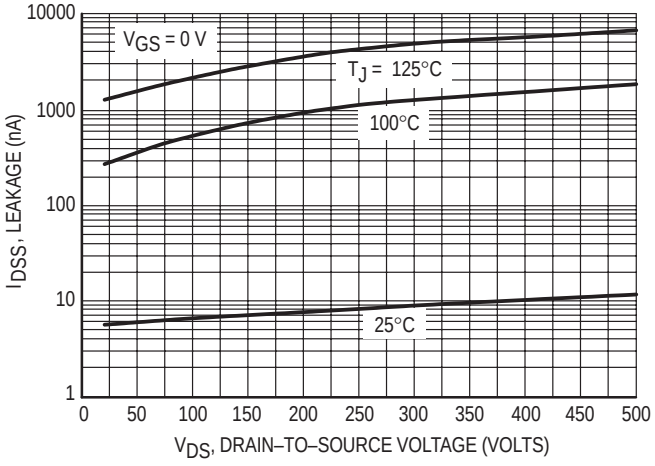


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

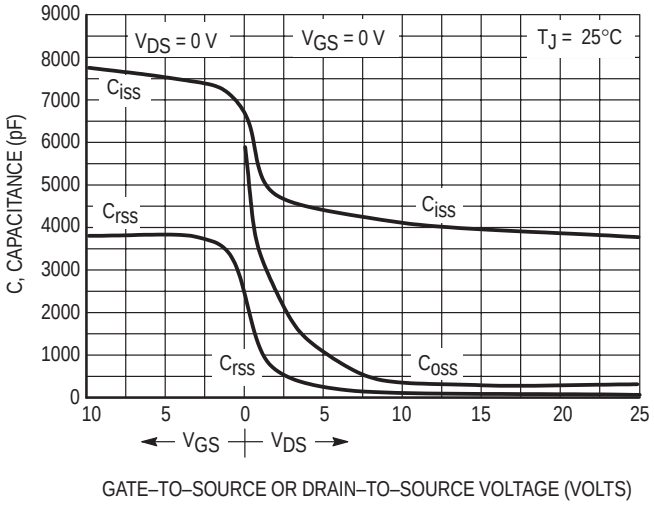


Figure 7a. Capacitance Variation

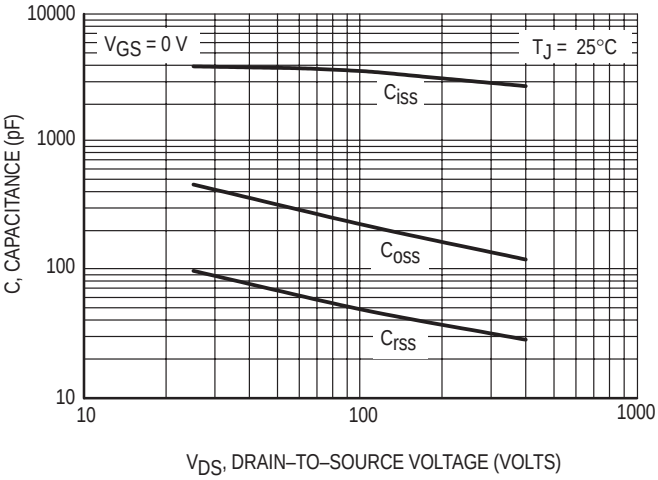


Figure 7b. High Voltage Capacitance Variation

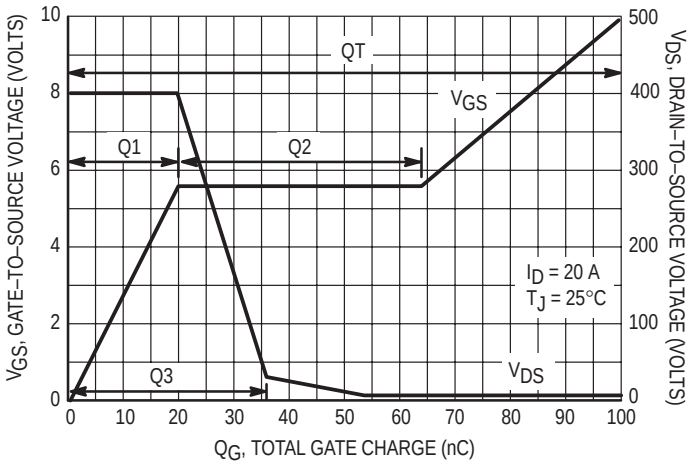


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

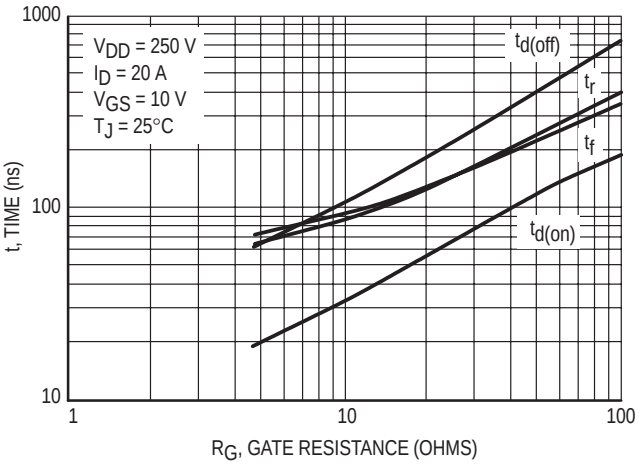


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

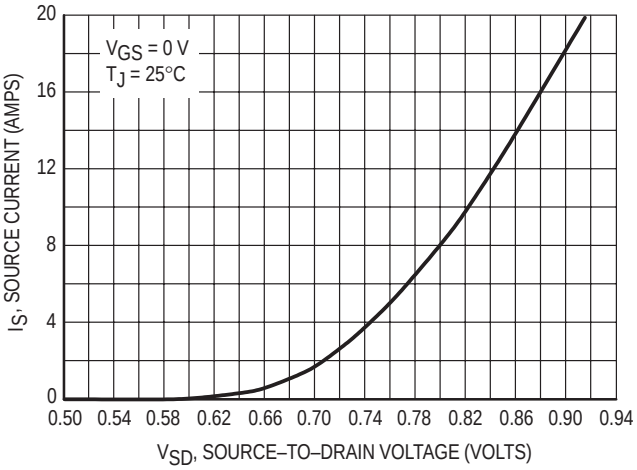


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

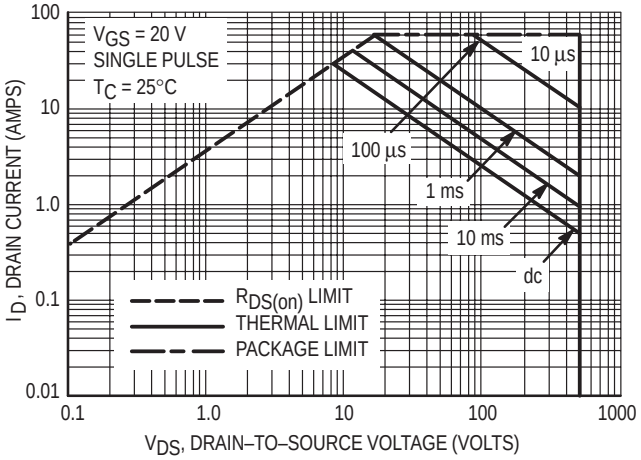


Figure 11. Maximum Rated Forward Biased Safe Operating Area

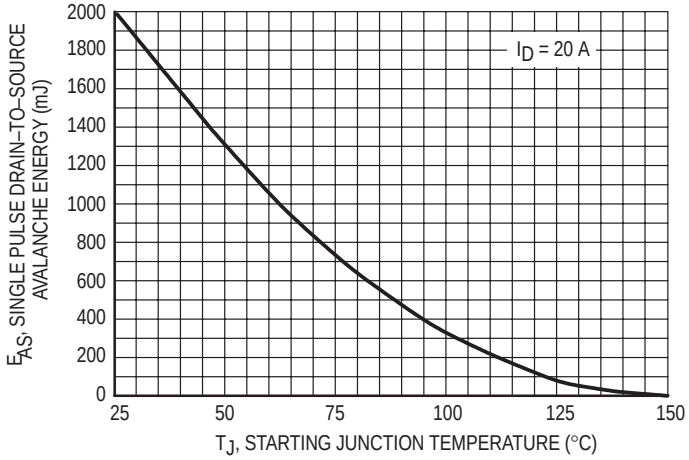


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

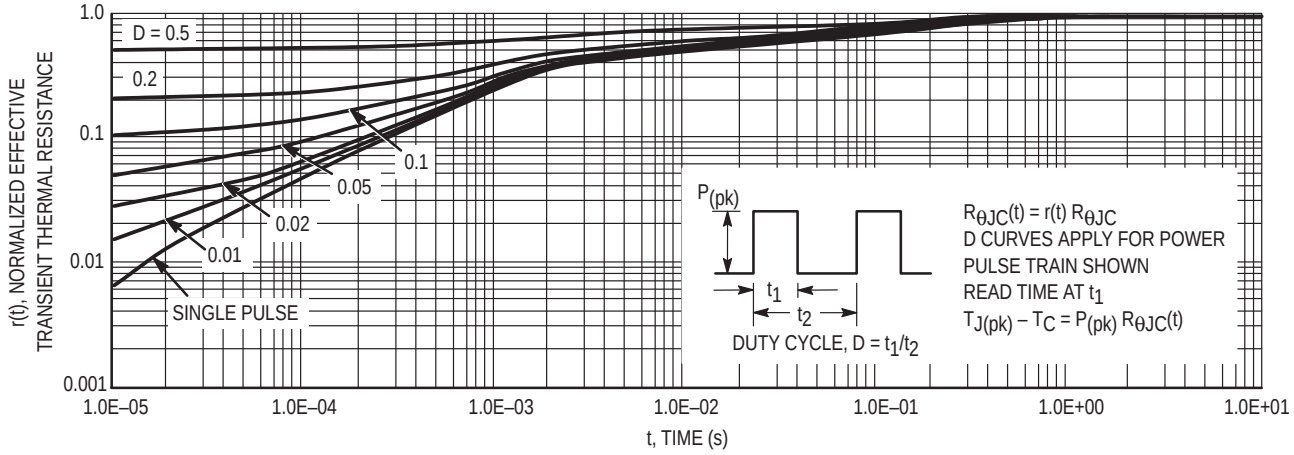


Figure 13. Thermal Response

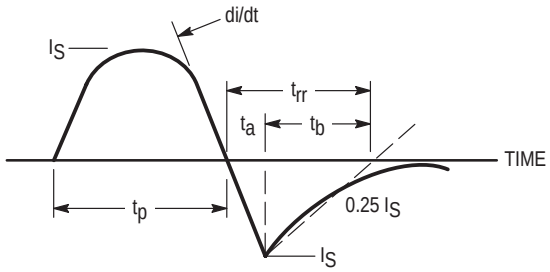


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

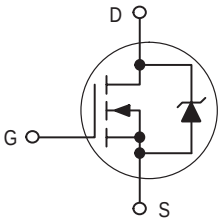
MTW24N40E

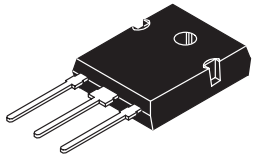
Motorola Preferred Device

TMOS POWER FET
24 AMPERES
400 VOLTS
$R_{DS(on)}$ = 0.16 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	400	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	24 17.7 72	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	250 2.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 20 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	600	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.50 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 3

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	400 —	— 360	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 400 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 400 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 100	μAdc
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	— 7.0	4.0 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 12 Adc)		$R_{DS(on)}$	—	0.13	0.16	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 24 Adc) (I_D = 12 Adc, T_J =125°C)		$V_{DS(on)}$	— —	— —	4.5 4.3	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 12 Adc)		g_{FS}	11	17	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	4000	5600	pF
Output Capacitance		C_{oss}	—	530	740	
Reverse Transfer Capacitance		C_{rss}	—	112	220	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} 200= Vdc, I_D = 24 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	32	60	ns
Rise Time		t_r	—	96	204	
Turn–Off Delay Time		$t_{d(off)}$	—	99	194	
Fall Time		t_f	—	92	186	
Gate Charge (See Figure 8)	(V_{DS} = 320 Vdc, I_D = 24 Adc, V_{GS} = 10 Vdc)	Q_T	—	98	160	nC
		Q_1	—	24	—	
		Q_2	—	38	—	
		Q_3	—	40	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 24 Adc, V_{GS} = 0 Vdc) (I_S = 24 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.94 0.9	1.5 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 24 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	372	—	ns
		t_a	—	244	—	
		t_b	—	128	—	
Reverse Recovery Stored Charge		Q_{RR}	—	5.3	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

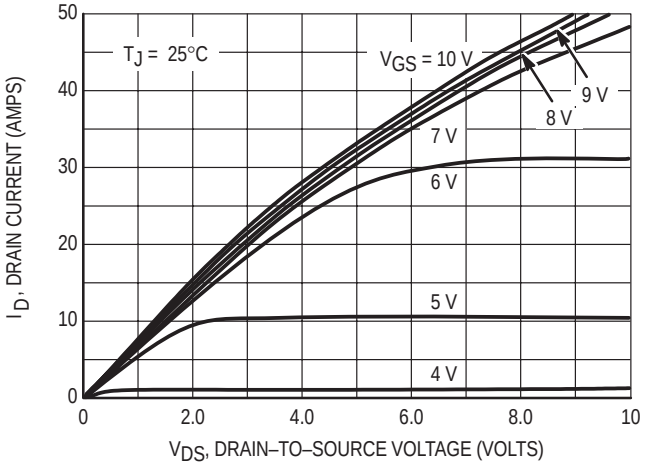


Figure 1. On–Region Characteristics

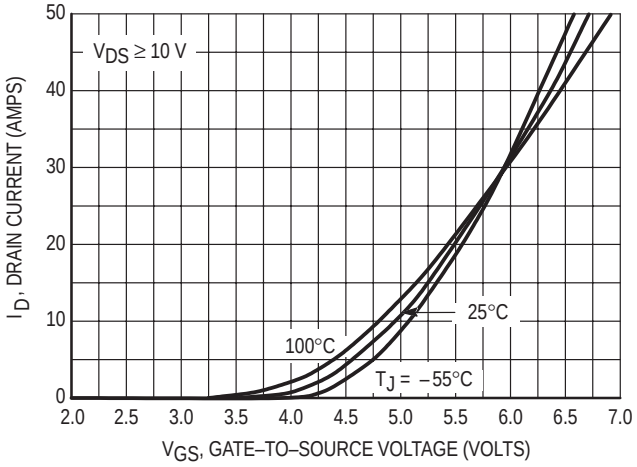


Figure 2. Transfer Characteristics

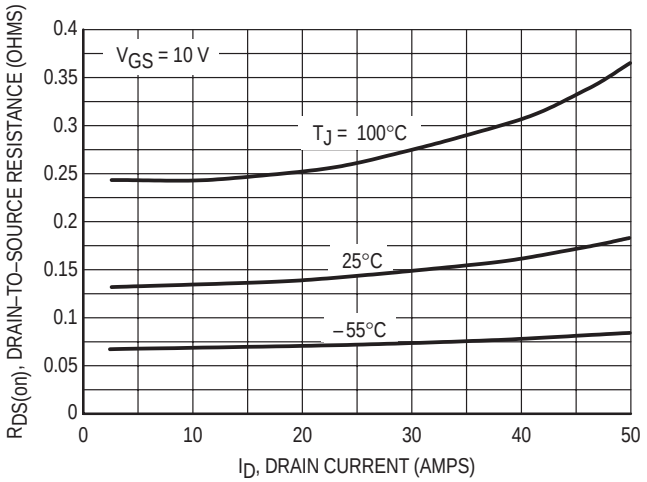


Figure 3. On–Resistance versus Drain Current and Temperature

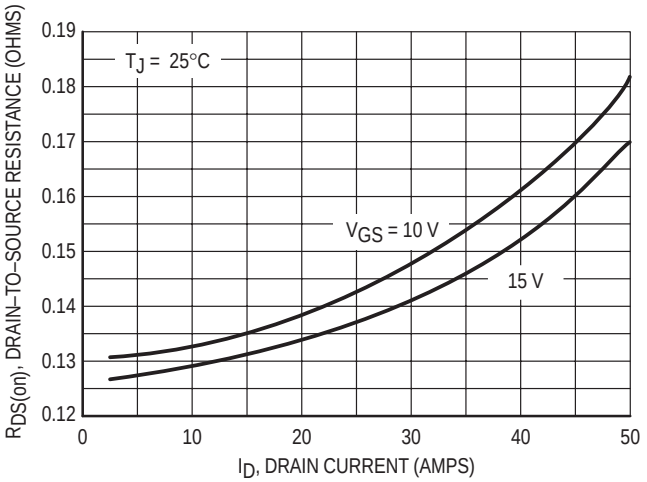


Figure 4. On–Resistance versus Drain Current and Gate Voltage

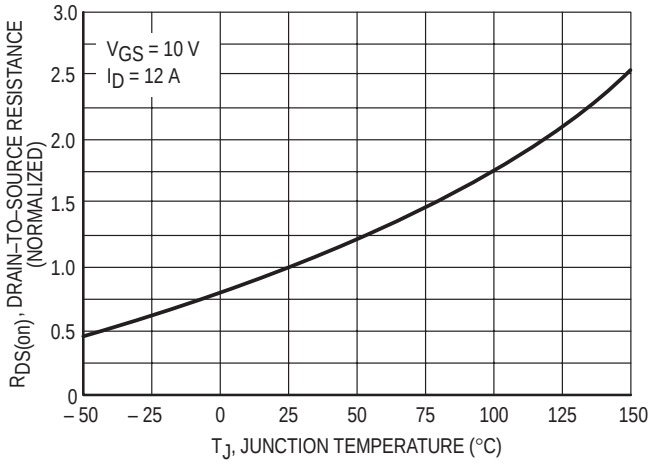


Figure 5. On–Resistance Variation with Temperature

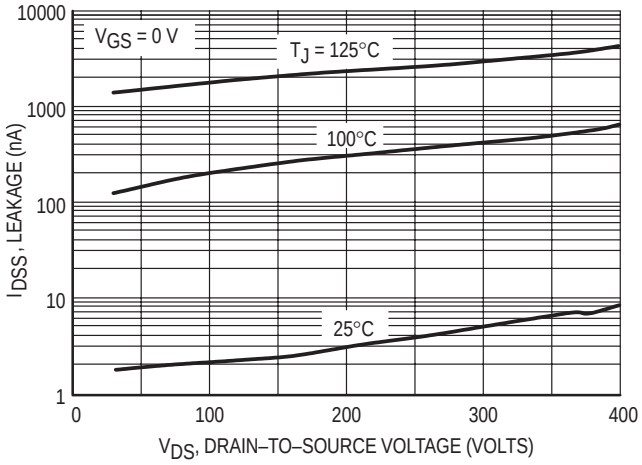


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

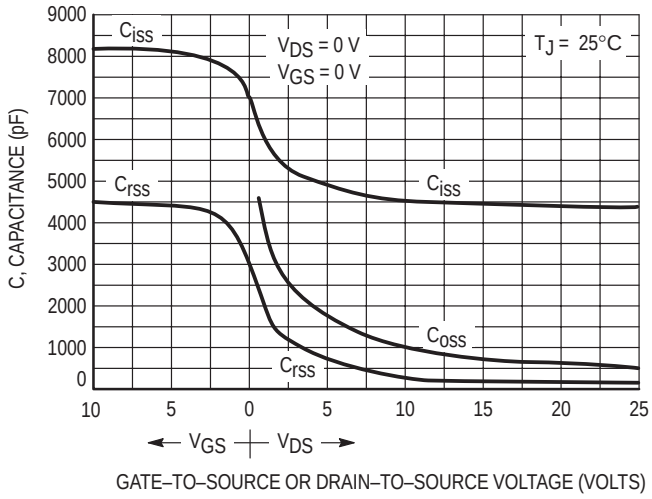


Figure 7a. Capacitance Variation

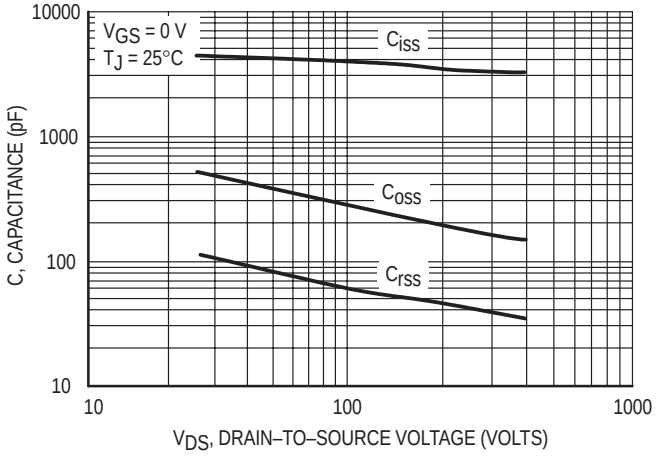


Figure 7b. High Voltage Capacitance Variation

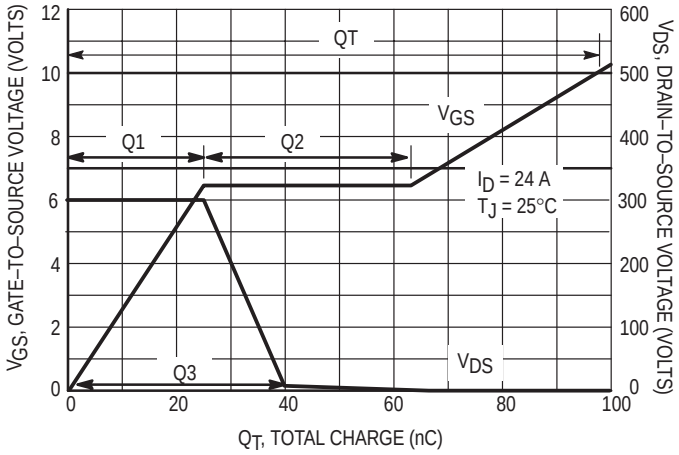


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

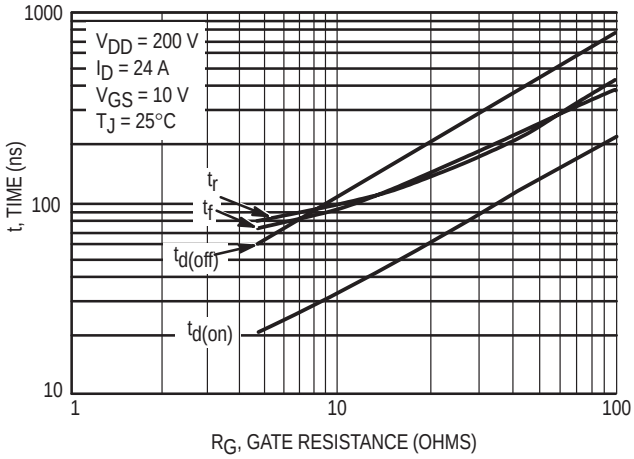


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

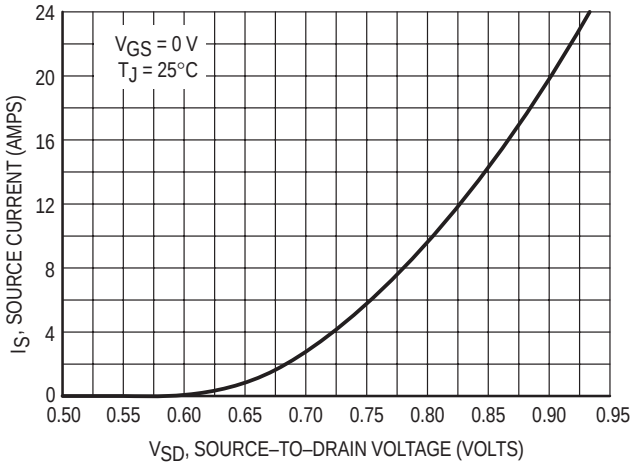


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

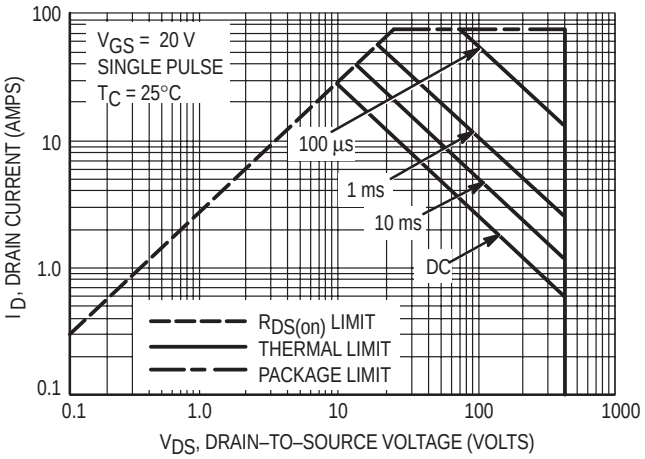


Figure 11. Maximum Rated Forward Biased Safe Operating Area

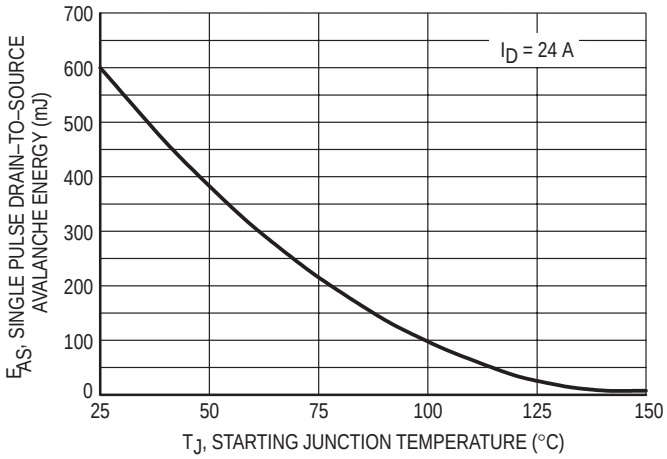


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

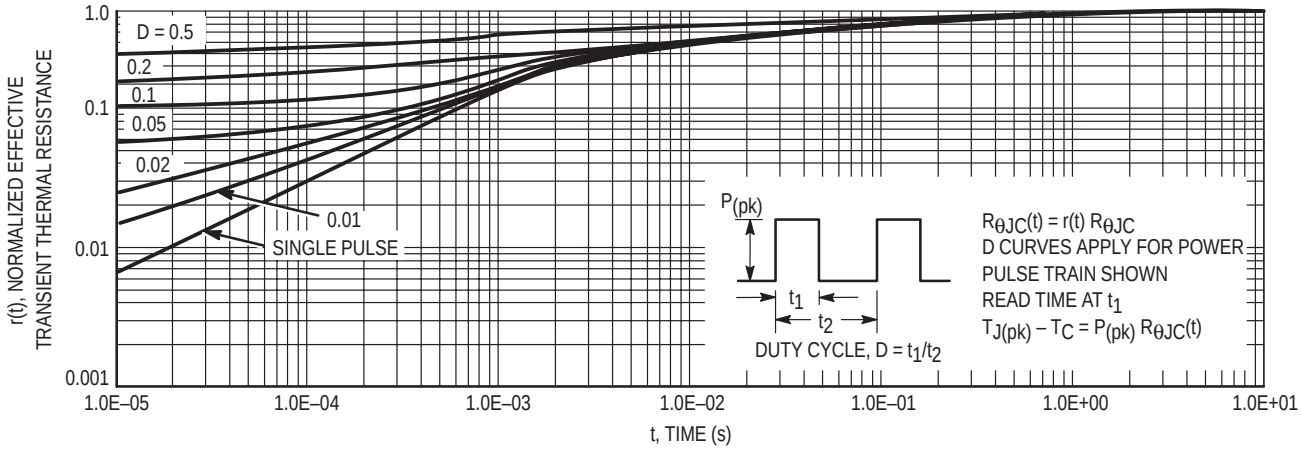


Figure 13. Thermal Response

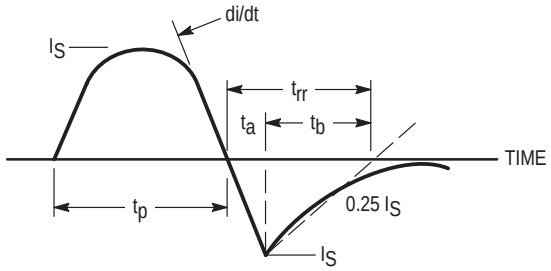


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

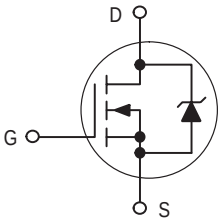
MTW32N20E

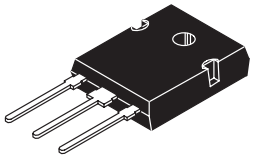
Motorola Preferred Device

TMOS POWER FET
32 AMPERES
200 VOLTS
$R_{DS(on)}$ = 0.075 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	200	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	200	Vdc
Gate–Source Voltage — Continuous	V_{GS}	± 20	Vdc
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	32 19 128	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	180 1.44	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vpk, I_L = 32 Apk, L = 1.58 mH, R_G = 25 Ω)	E_{AS}	810	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.7 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

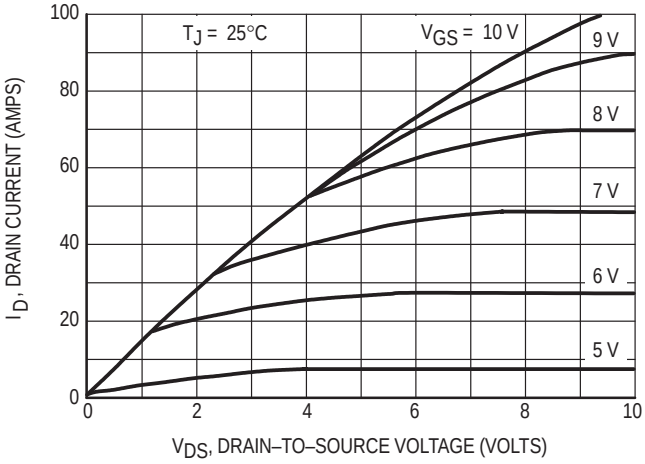
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 V, I_D = 250 μAdc)		$V_{(BR)DSS}$	200	—	—	Vdc
Temperature Coefficient (Positive)			—	247	—	mV/°C
Zero Gate Voltage Drain Current		I_{DSS}				μAdc
(V_{DS} = 200 Vdc, V_{GS} = 0)			—	—	250	
(V_{DS} = 200 Vdc, V_{GS} = 0, T_J = 125°C)			—	—	1000	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage		$V_{GS(th)}$				
(V_{DS} = V_{GS}, I_D = 250 μAdc)			2.0	—	4.0	Vdc
Temperature Coefficient (Negative)			—	8.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc)		$R_{DS(on)}$	—	0.064	0.075	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc)		$V_{DS(on)}$				Vdc
(I_D = 32 Adc)			—	—	3.0	
(I_D = 16 Adc, T_J = 125°C)			—	—	2.7	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 16 Adc)		g_{FS}	12	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	3600	5000	pF
Output Capacitance		C_{oss}	—	130	250	
Reverse Transfer Capacitance		C_{rss}	—	690	1000	
SWITCHING CHARACTERISTICS*†						
Turn–On Delay Time	(V_{DD} = 100 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc, R_G = 6.2 Ω)	$t_{d(on)}$	—	25	50	ns
Rise Time		t_r	—	120	240	
Turn–Off Delay Time		$t_{d(off)}$	—	75	150	
Fall Time		t_f	—	91	182	
Gate Charge	(V_{DS} = 160 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc)	Q_T	—	85	120	nC
		Q_1	—	12	—	
		Q_2	—	40	—	
		Q_3	—	30	—	
SOURCE–DRAIN DIODE CHARACTERISTICS*						
Forward On–Voltage	(I_S = 32 Adc, V_{GS} = 0)	V_{SD}				Vdc
	(I_S = 16 Adc, V_{GS} = 0, T_J = 125°C)		—	1.1	2.0	
			—	0.9	—	
Reverse Recovery Time	(I_S = 32 Adc, V_{GS} = 0, dI_S/dt = 100 A/μs)	t_{rr}	—	280	—	ns
		t_a	—	195	—	
		t_b	—	85	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.94	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	5.0	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

* Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

† Switching characteristics are independent of operating junction temperature.

YPICAL ELECTRICAL CHARACTERISTICS



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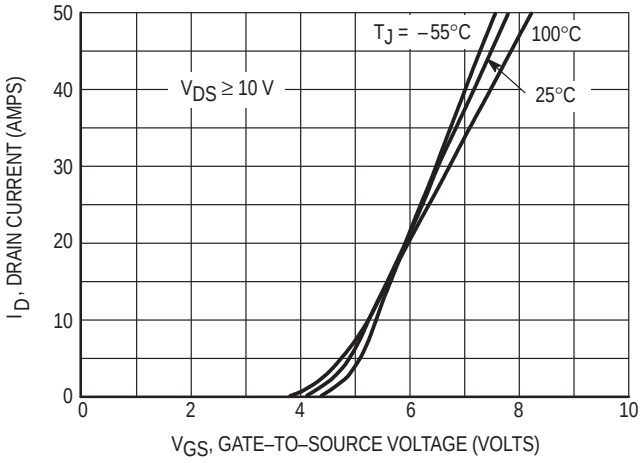

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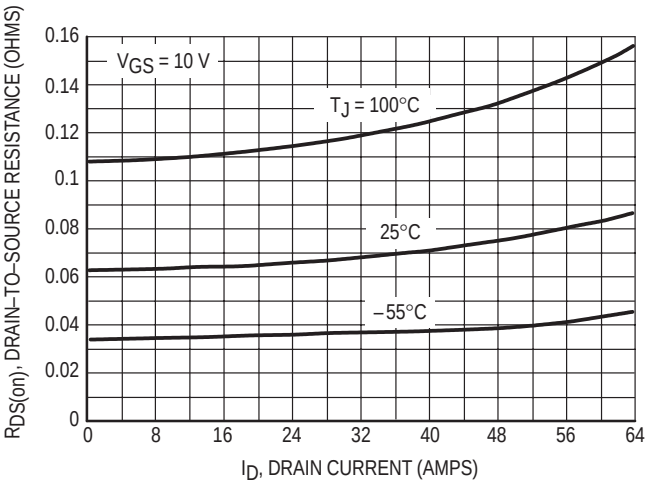

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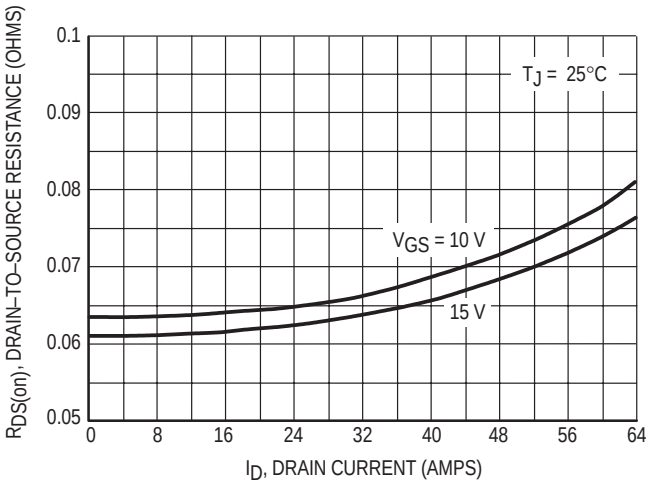

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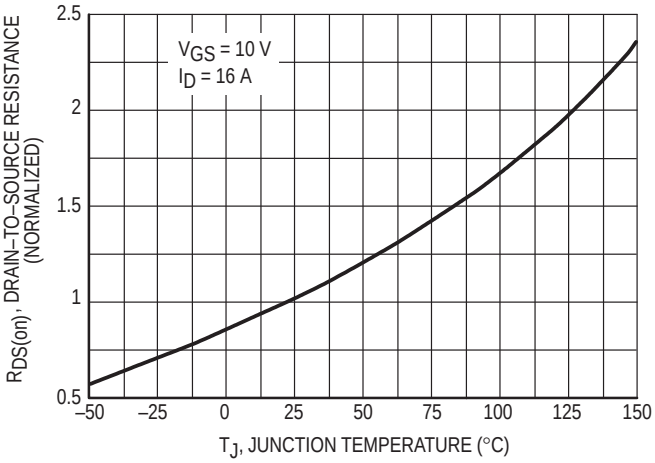
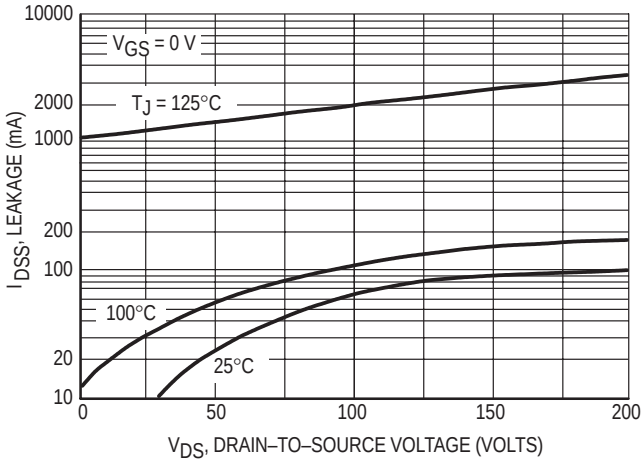


Figure 5. On–Resistance Variation with Temperature



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where

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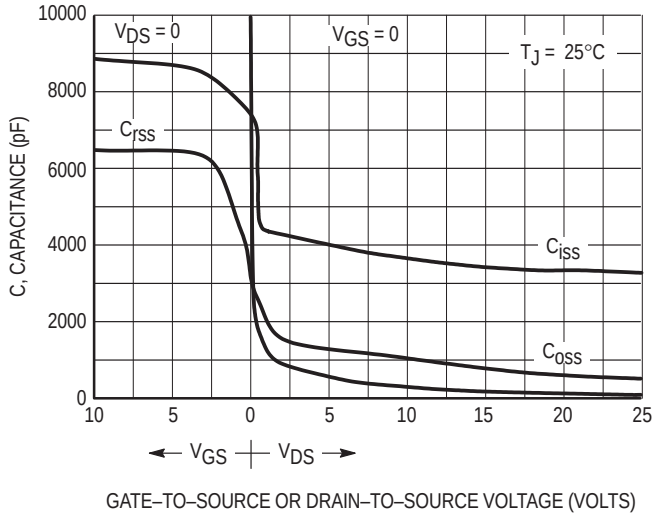


Figure 7. Capacitance Variation

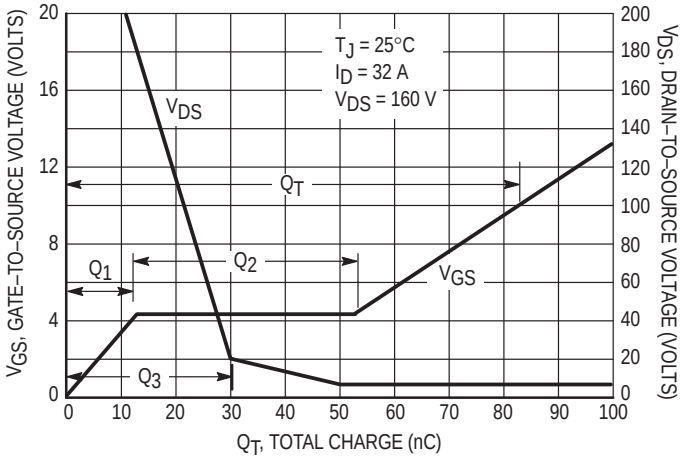


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

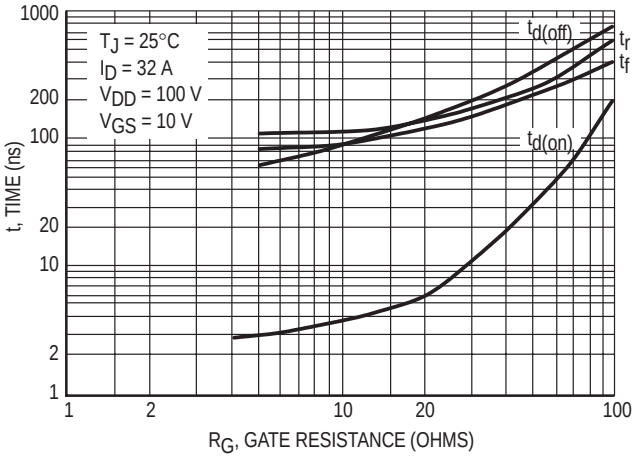


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

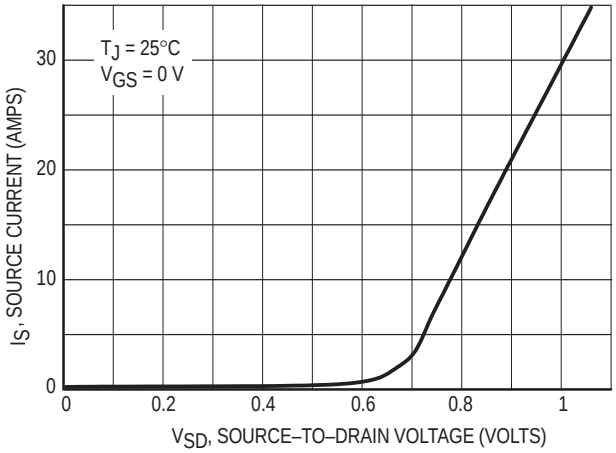


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} – T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

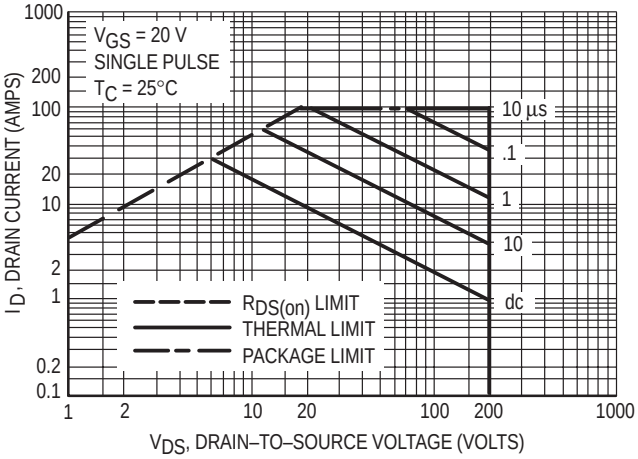


Figure 11. Maximum Rated Forward Biased Safe Operating Area

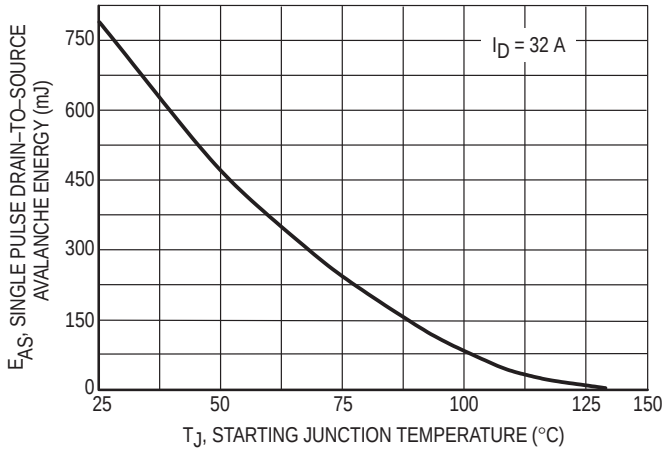


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

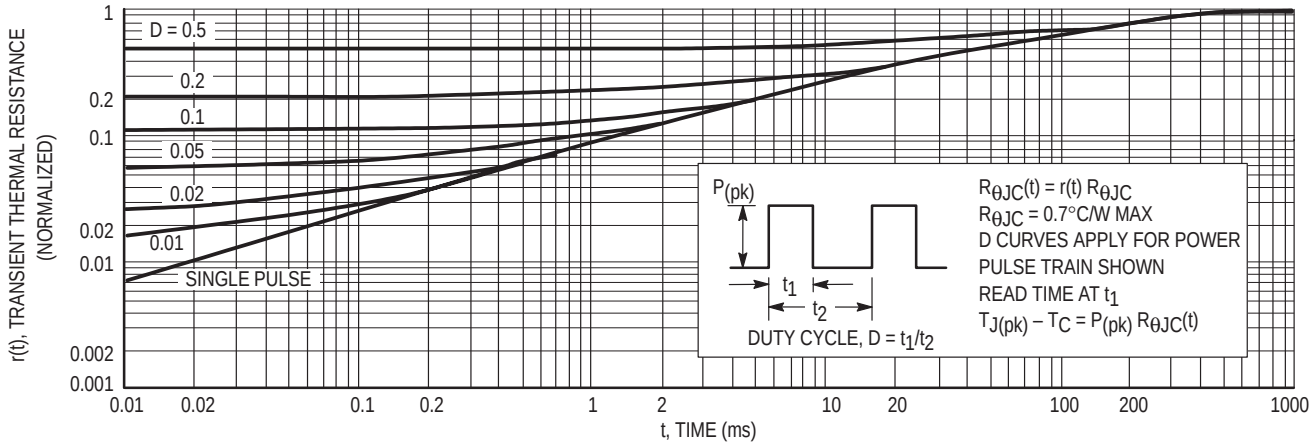


Figure 13. Thermal Response

Designer's™ Data Sheet

TMOS E-FET™
Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

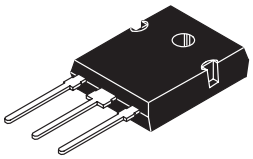
MTW32N25E

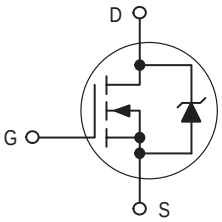
Motorola Preferred Device

TMOS POWER FET
32 AMPERES
250 VOLTS
$R_{DS(on)}$ = 0.08 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	250	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	250	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	32 25 96	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	250 2.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 20 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	600	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.50 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	250	300	—	Vdc
Temperature Coefficient (Positive)			—	380	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 250 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 250 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	—	4.0	Vdc
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 16 Adc)		$R_{DS(on)}$	—	0.07	0.08	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 32 Adc)		$V_{DS(on)}$	—	2.2	2.6	Vdc
(I_D = 16 Adc, T_J = 125°C)			—	—	2.5	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 16 Adc)		g_{FS}	11	20	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3800	5350	pF
Output Capacitance		C_{oss}	—	726	1020	
Reverse Transfer Capacitance		C_{rss}	—	183	370	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD}= 125 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	31	60	ns
Rise Time		t_r	—	133	266	
Turn–Off Delay Time		$t_{d(off)}$	—	93	186	
Fall Time		t_f	—	108	216	
Gate Charge (See Figure 8)	(V_{DS} = 200 Vdc, I_D = 32 Adc, V_{GS} = 10 Vdc)	Q_T	—	97	136	nC
		Q_1	—	22	—	
		Q_2	—	43	—	
		Q_3	—	41	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 32 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.0	1.5	Vdc
	(I_S = 32 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.92	—	
Reverse Recovery Time (See Figure 14)	(I_S = 32 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	312	—	ns
		t_a	—	220	—	
		t_b	—	93	—	
Reverse Recovery Stored Charge		Q_{RR}	—	3.6	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

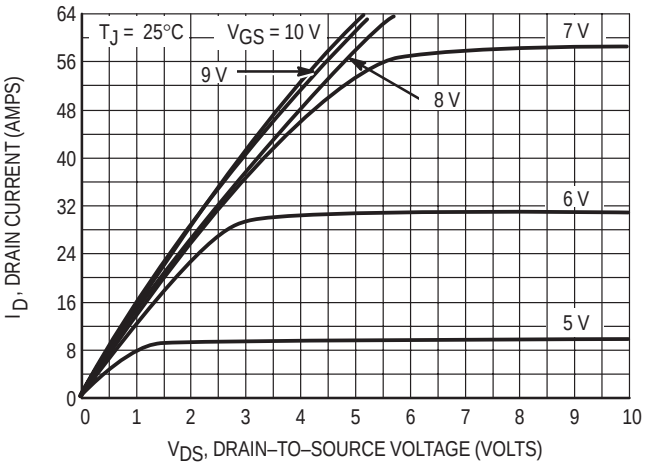


Figure 1. On–Region Characteristics

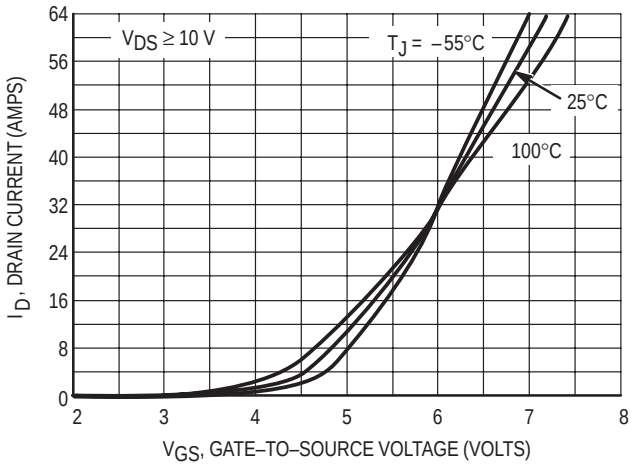


Figure 2. Transfer Characteristics

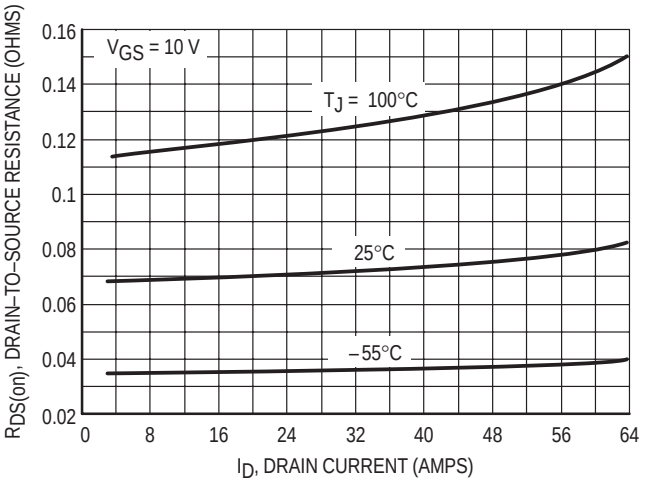


Figure 3. On–Resistance versus Drain Current and Temperature

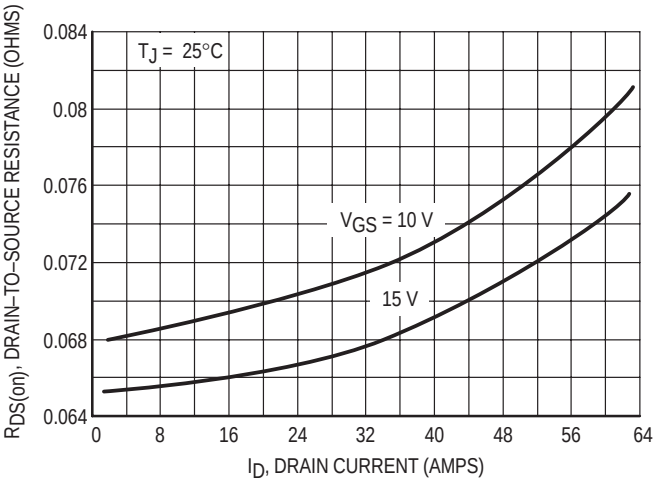


Figure 4. On–Resistance versus Drain Current and Gate Voltage

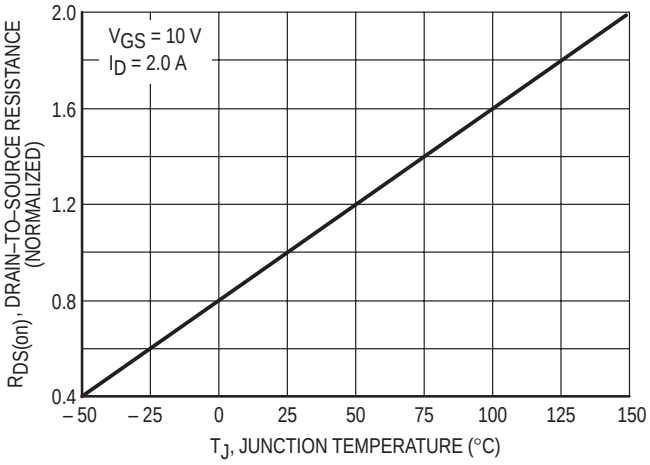


Figure 5. On–Resistance Variation with Temperature

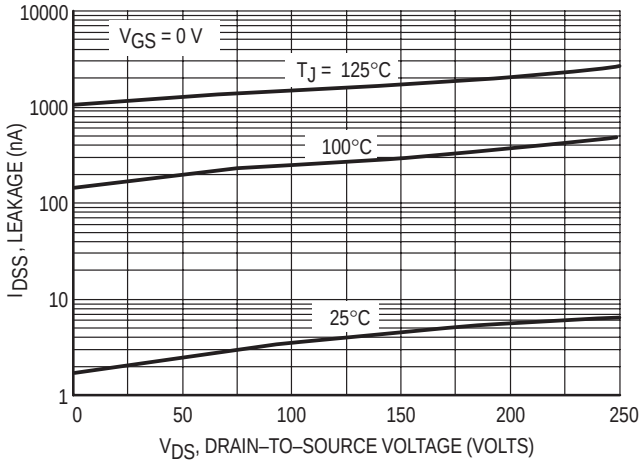


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

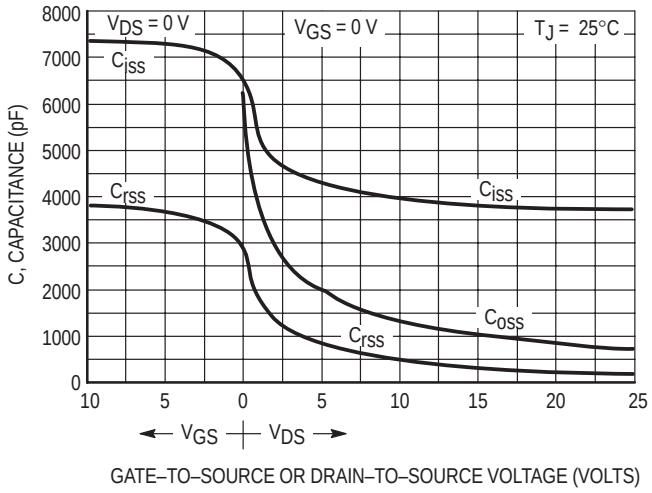


Figure 7. Capacitance Variation

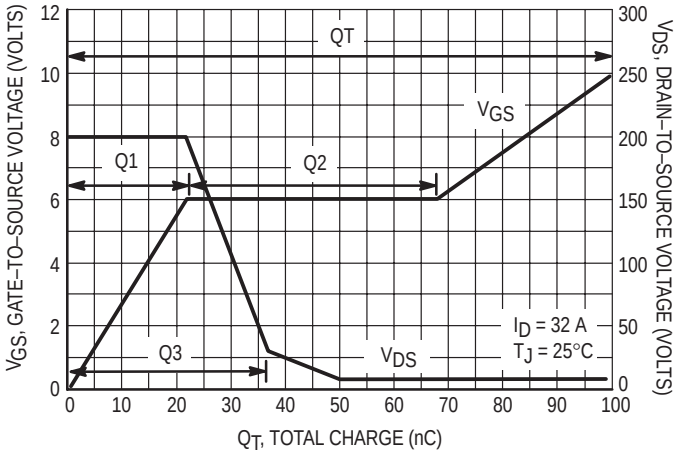


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

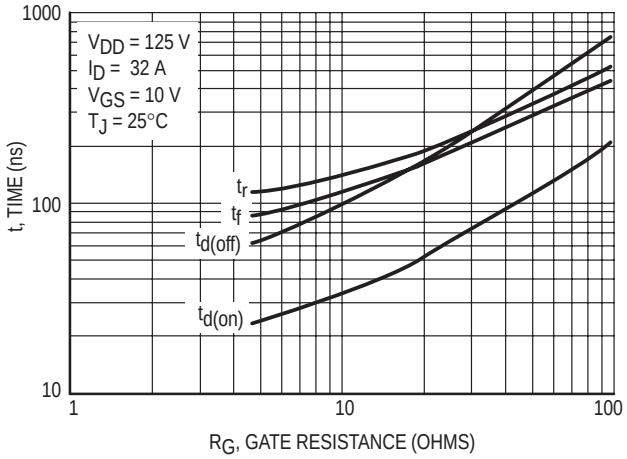


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

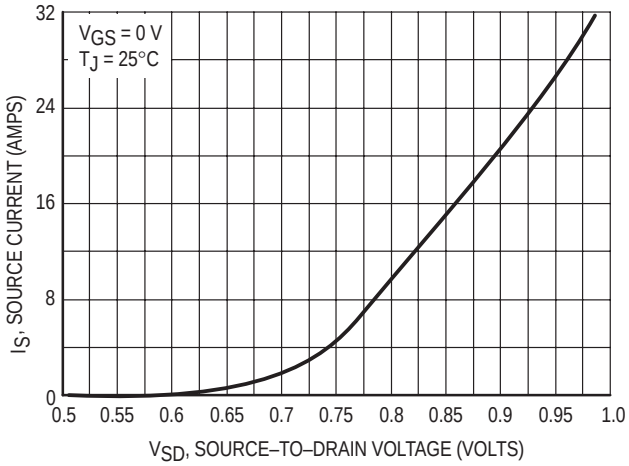


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

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Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

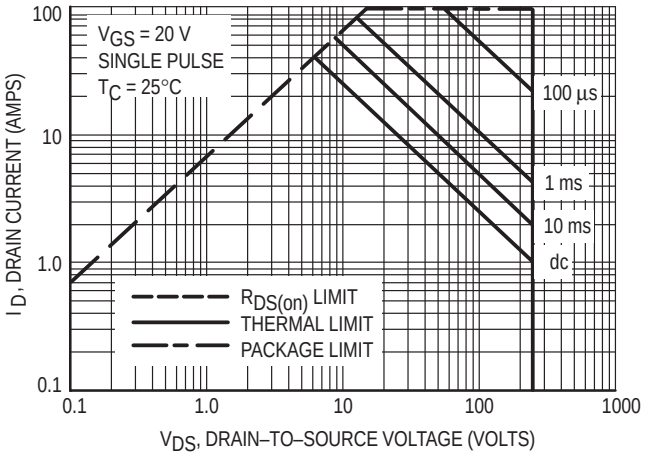
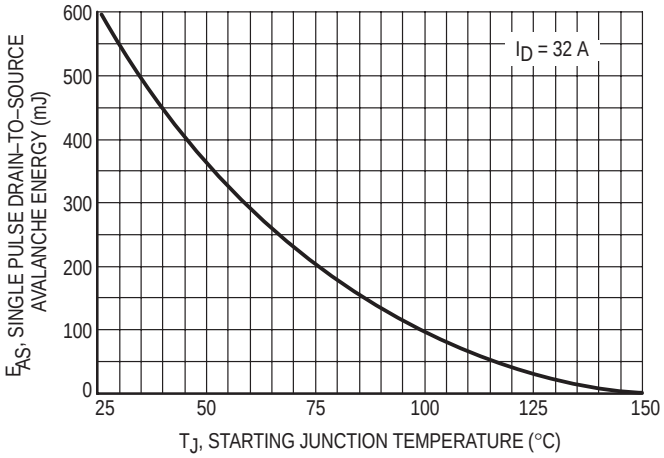


Figure 11. Maximum Rated Forward Biased Safe Operating Area



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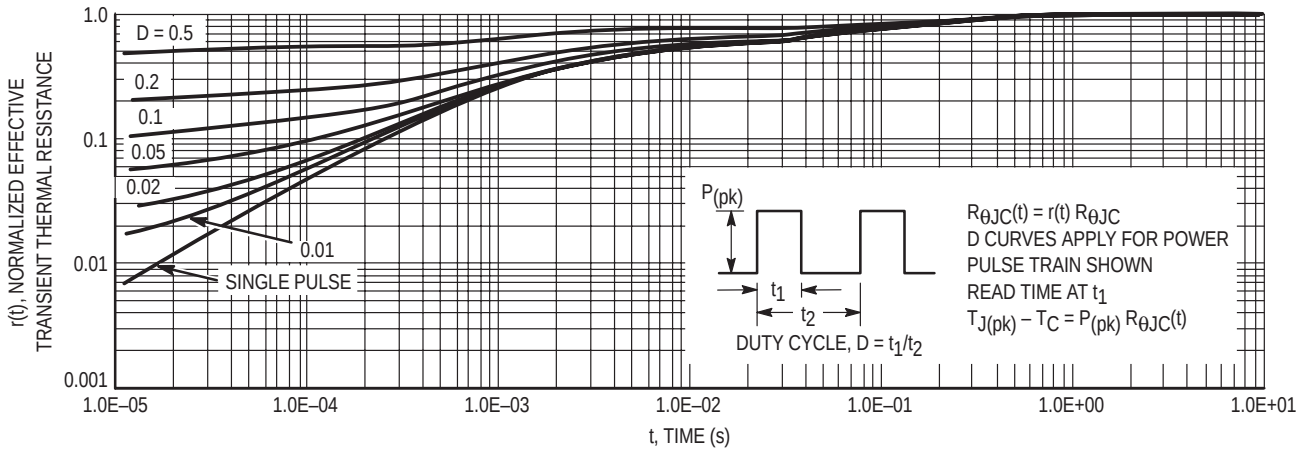

Figure 13. Thermal Response

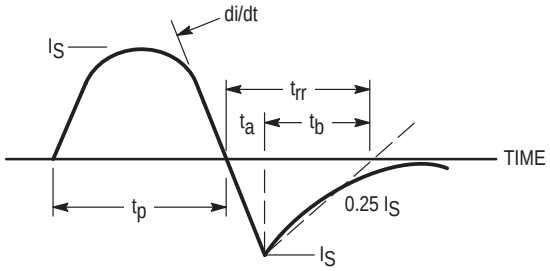

Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

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Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

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Motorola Preferred Device

TMOS POWER FET
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150 VOLTS
$R_{DS(on)}$ = 0.05 OHM

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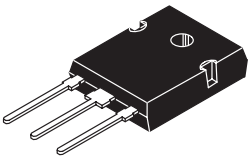
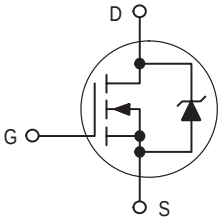
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	150	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	150	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	35 26.9 105	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	180 1.45	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, I_L = 20 Apk, L = 3.0 mH, R_G = 25 Ω)	E_{AS}	600	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.70 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	150	—	—	Vdc
Temperature Coefficient (Positive)			—	210	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 150 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 150 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	—	4.0	Vdc
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 17.5 Adc)		$R_{DS(on)}$	—	—	0.05	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 35 Adc)		$V_{DS(on)}$	—	1.45	1.8	Vdc
(I_D = 17.5 Adc, T_J = 125°C)			—	—	1.7	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 17.5 Adc)		g_{FS}	11	18	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3600	5040	pF
Output Capacitance		C_{oss}	—	855	1170	
Reverse Transfer Capacitance		C_{rss}	—	165	330	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 75 Vdc, I_D = 35 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	28	56	ns
Rise Time		t_r	—	170	346	
Turn–Off Delay Time		$t_{d(off)}$	—	90	180	
Fall Time		t_f	—	103	210	
Gate Charge (See Figure 8)	(V_{DS} = 120 Vdc, I_D = 35 Adc, V_{GS} = 10 Vdc)	Q_T	—	98	137	nC
		Q_1	—	19	—	
		Q_2	—	49	—	
		Q_3	—	40	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 35 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.95	1.5	Vdc
	(I_S = 35 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.9	—	
Reverse Recovery Time (See Figure 14)	(I_S = 35 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	200	—	ns
		t_a	—	167	—	
		t_b	—	32	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.63	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

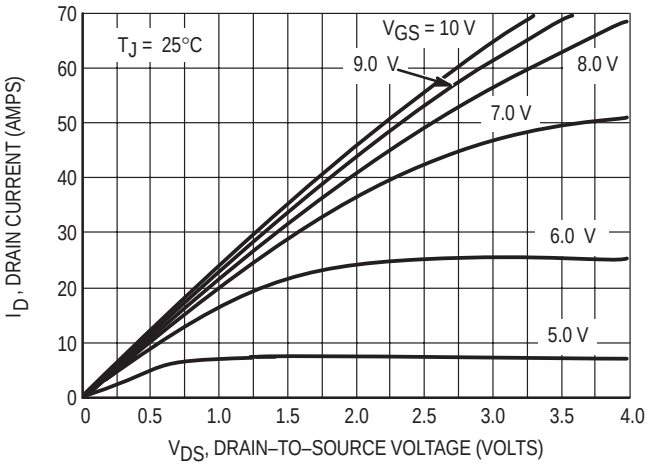


Figure 1. On–Region Characteristics

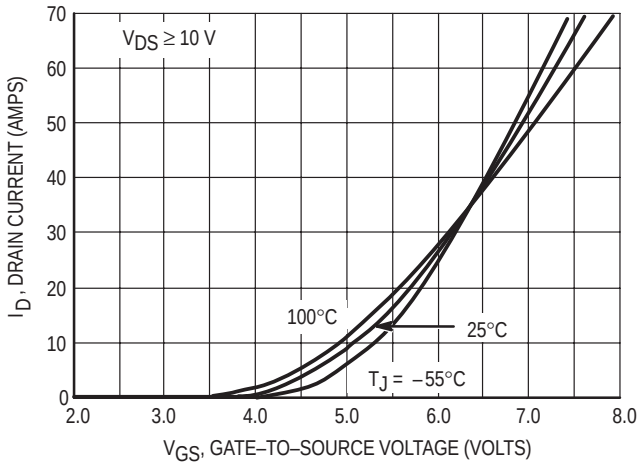


Figure 2. Transfer Characteristics

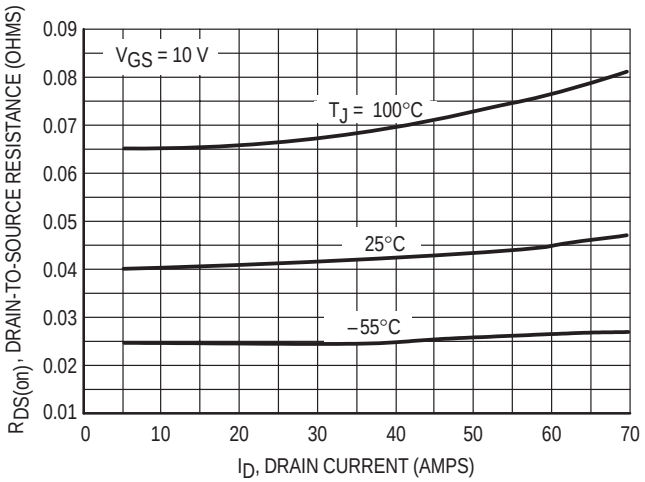


Figure 3. On–Resistance versus Drain Current and Temperature

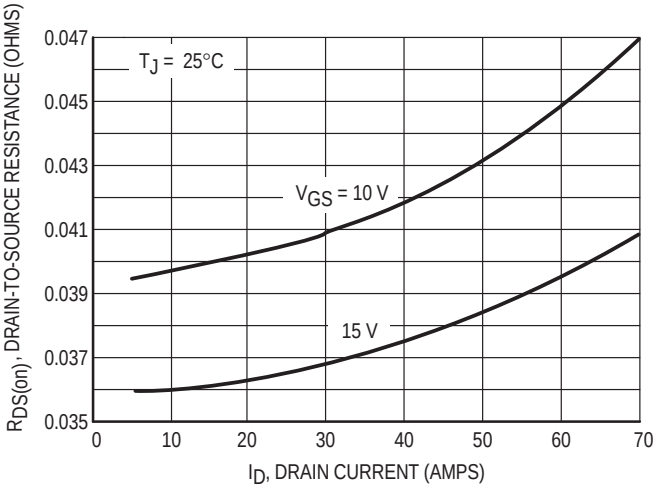


Figure 4. On–Resistance versus Drain Current and Gate Voltage

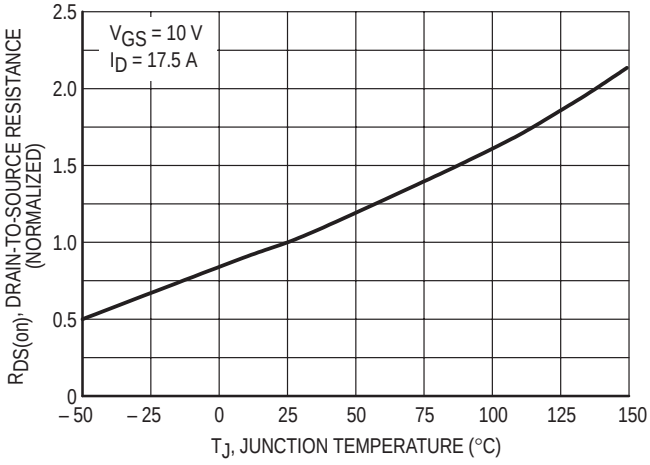


Figure 5. On–Resistance Variation with Temperature

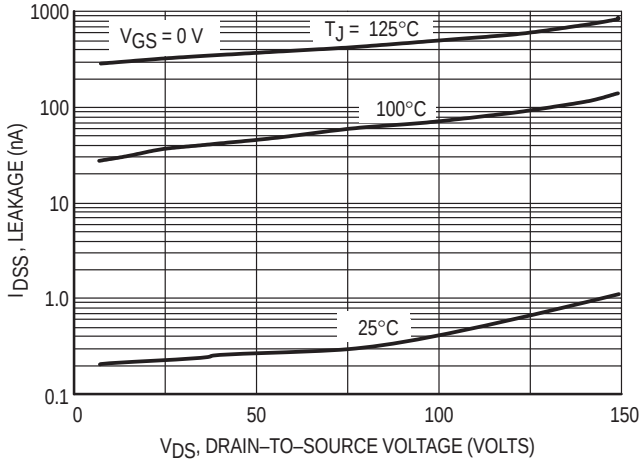


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

space

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

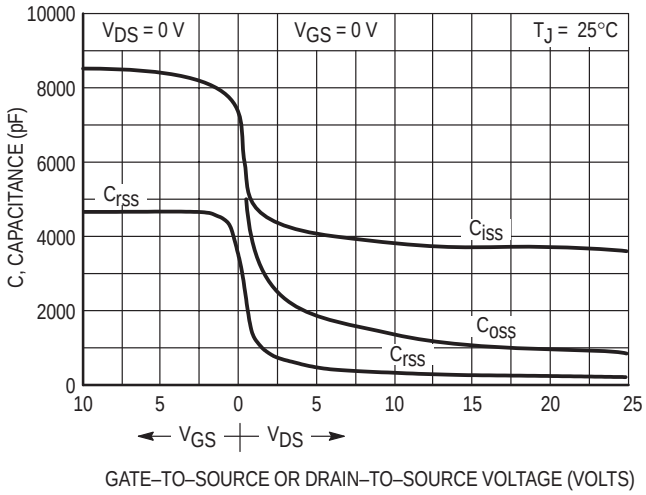


Figure 7. Capacitance Variation

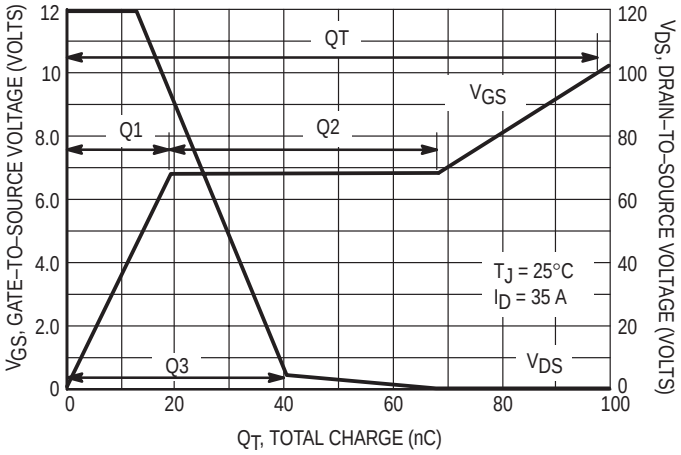


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

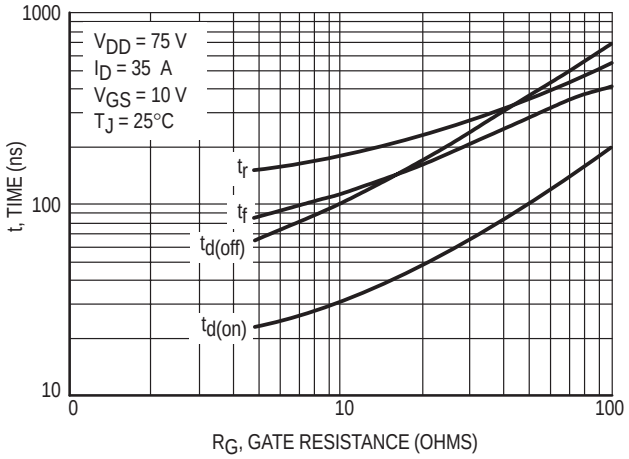


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

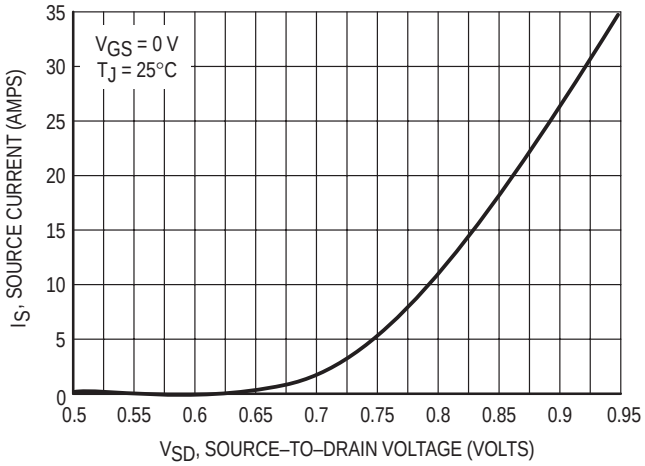


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

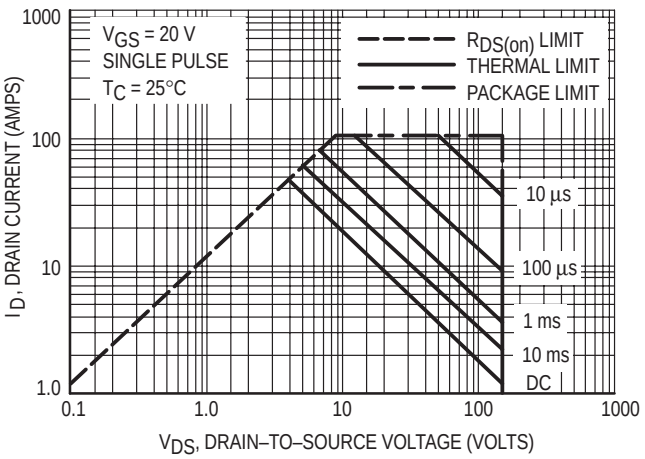


Figure 11. Maximum Rated Forward Biased Safe Operating Area

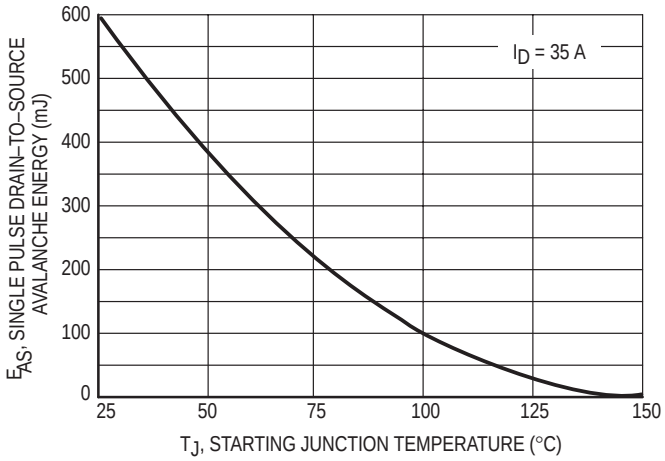


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

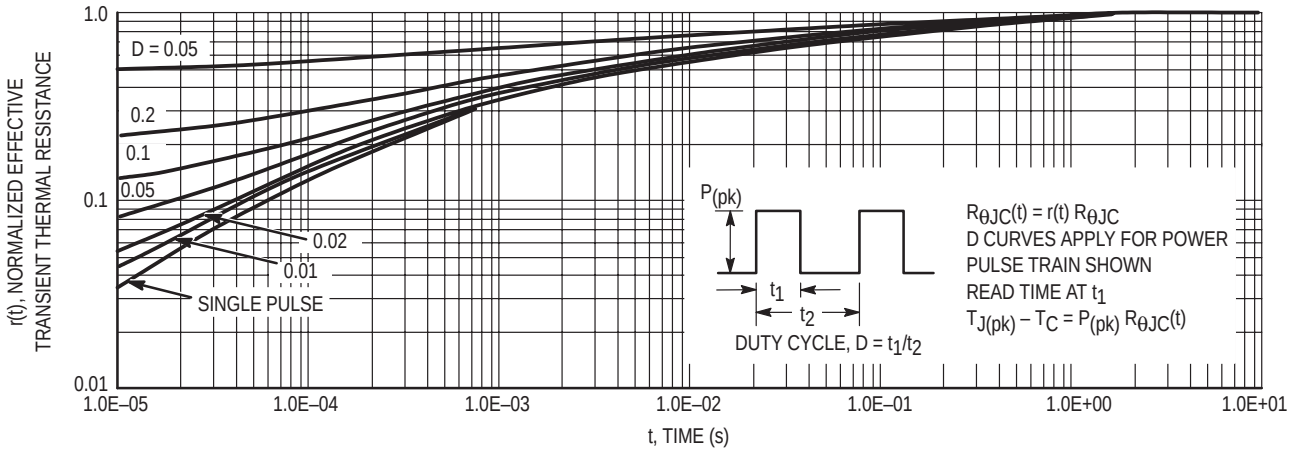


Figure 13. Thermal Response

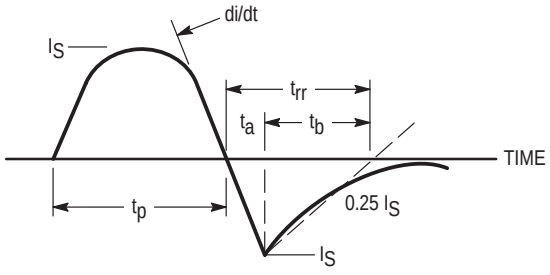


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
TO-247 with Isolated Mounting Hole

N–Channel Enhancement–Mode Silicon Gate

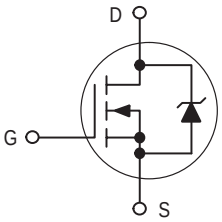
MTW45N10E

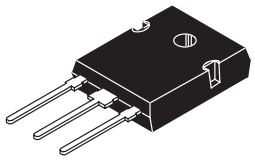
Motorola Preferred Device

TMOS POWER FET
45 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.035 OHM

This advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware





CASE 340F–03, Style 1
TO–247AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	100	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	45 34.6 135	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	180 1.44	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 10 Vdc, I_L = 45 Apk, L = 0.8 mH, R_G = 25 Ω)	E_{AS}	810	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.70 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 1

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	100	—	—	Vdc
Temperature Coefficient (Positive)			—	116	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	—	4.0	Vdc
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 22.5 Adc)		$R_{DS(on)}$	—	0.027	0.035	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 45 Adc)		$V_{DS(on)}$	—	1.13	2.16	Vdc
(I_D = 22.5 Adc, T_J = 125°C)			—	—	1.53	
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 22.5 Adc)		g_{FS}	12	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3480	5000	pF
Output Capacitance		C_{oss}	—	1240	2000	
Reverse Transfer Capacitance		C_{rss}	—	315	650	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD}= 50 Vdc, I_D = 45 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	25	50	ns
Rise Time		t_r	—	234	470	
Turn–Off Delay Time		$t_{d(off)}$	—	83	170	
Fall Time		t_f	—	116	240	
Gate Charge (See Figure 8)	(V_{DS} = 80 Vdc, I_D = 45 Adc, V_{GS} = 10 Vdc)	Q_T	—	106	220	nC
		Q_1	—	26	—	
		Q_2	—	54	—	
		Q_3	—	44	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 45 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.09	1.635	Vdc
	(I_S = 45 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.04	—	
Reverse Recovery Time (See Figure 14)	(I_S = 45 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	166	—	ns
		t_a	—	118	—	
		t_b	—	48	—	
Reverse Recovery Stored Charge		Q_{RR}	—	1.1	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

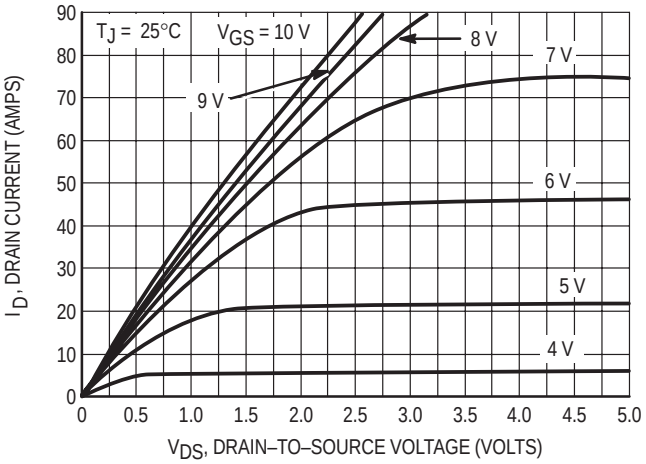
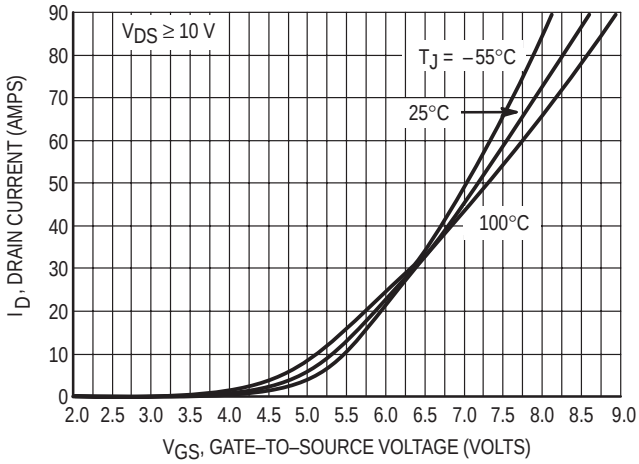


Figure 1. On–Region Characteristics



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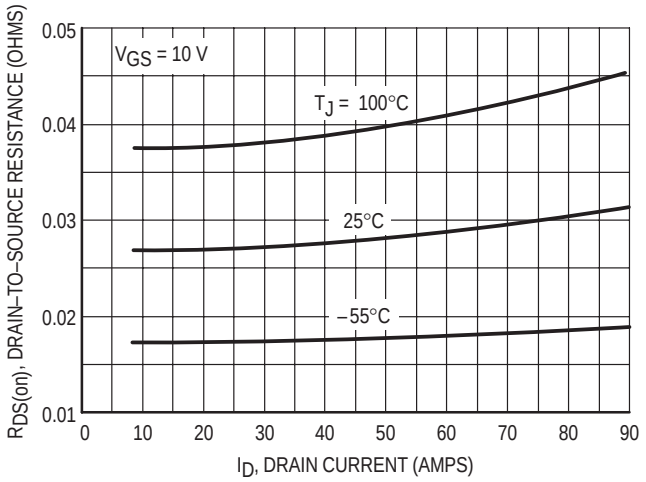

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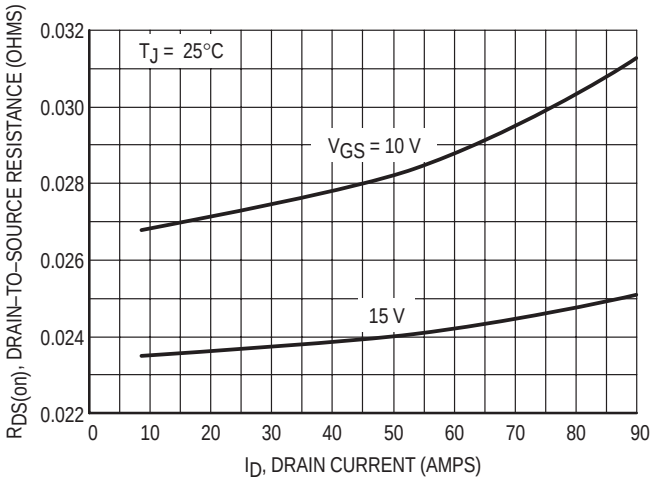


Figure 4. On–Resistance versus Drain Current and Gate Voltage

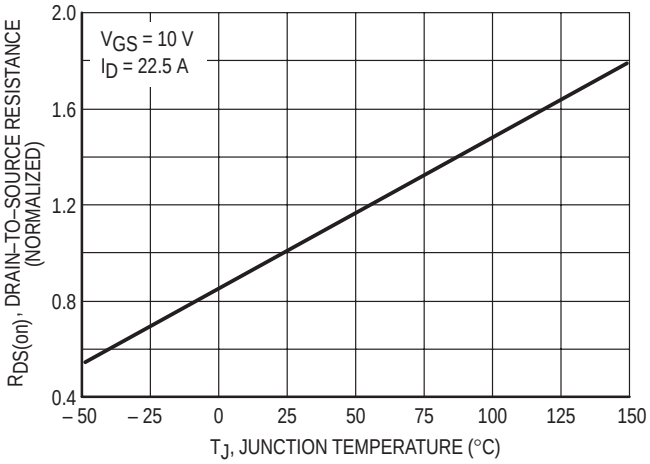
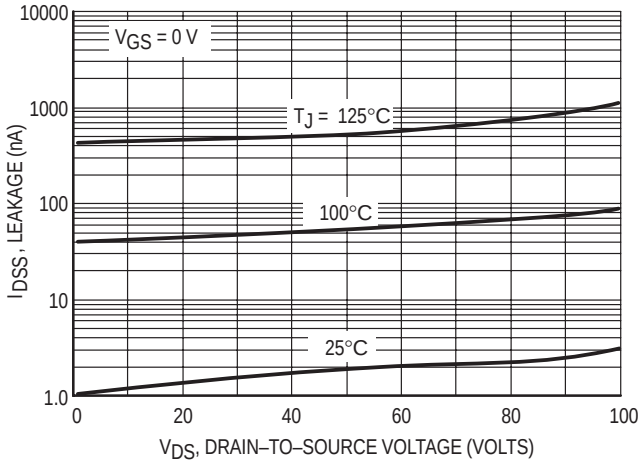


Figure 5. On–Resistance Variation with Temperature



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During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

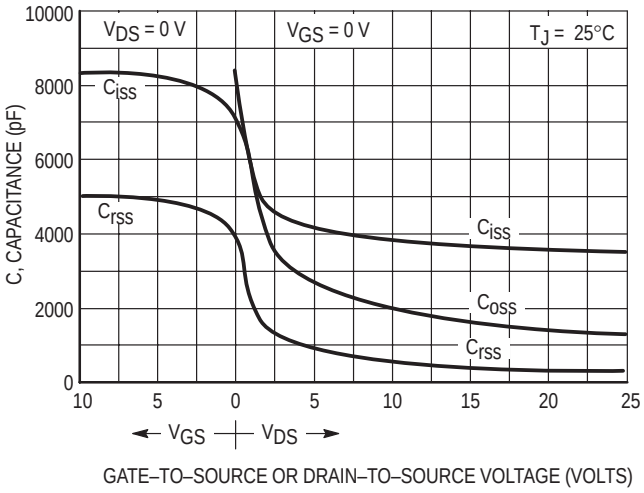


Figure 7. Capacitance Variation

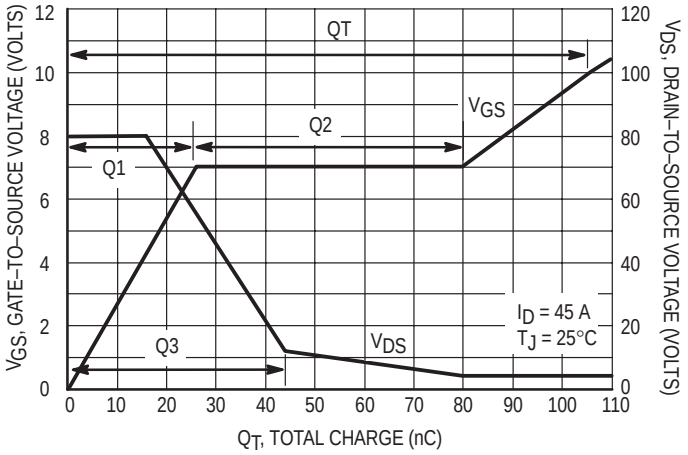


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

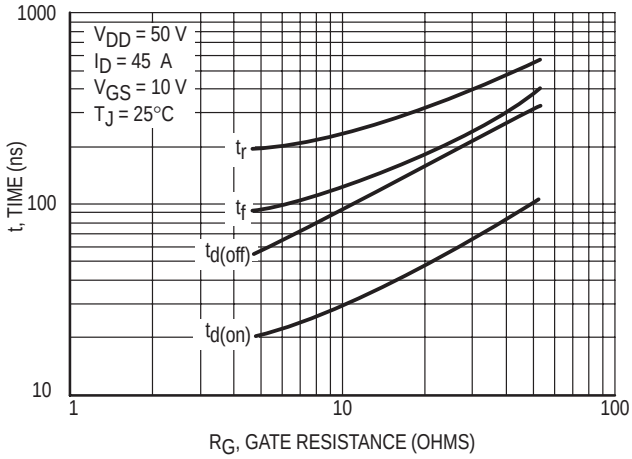


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

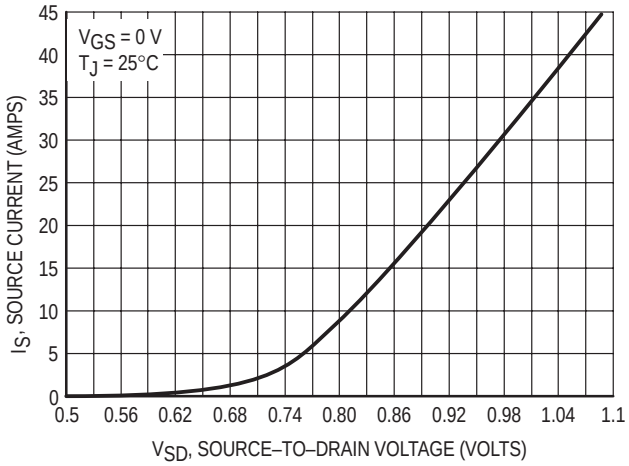


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

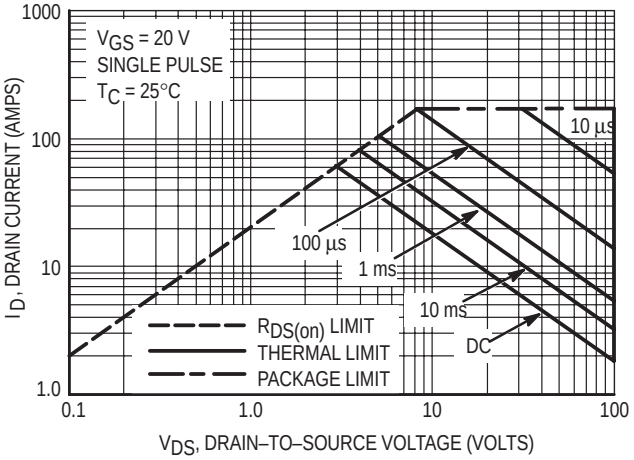


Figure 11. Maximum Rated Forward Biased Safe Operating Area

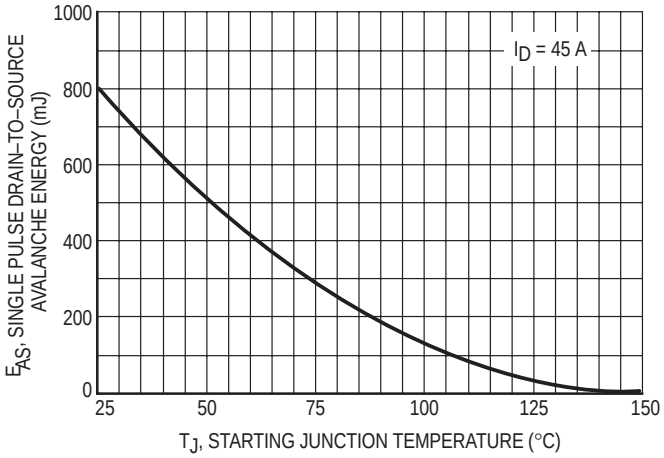


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

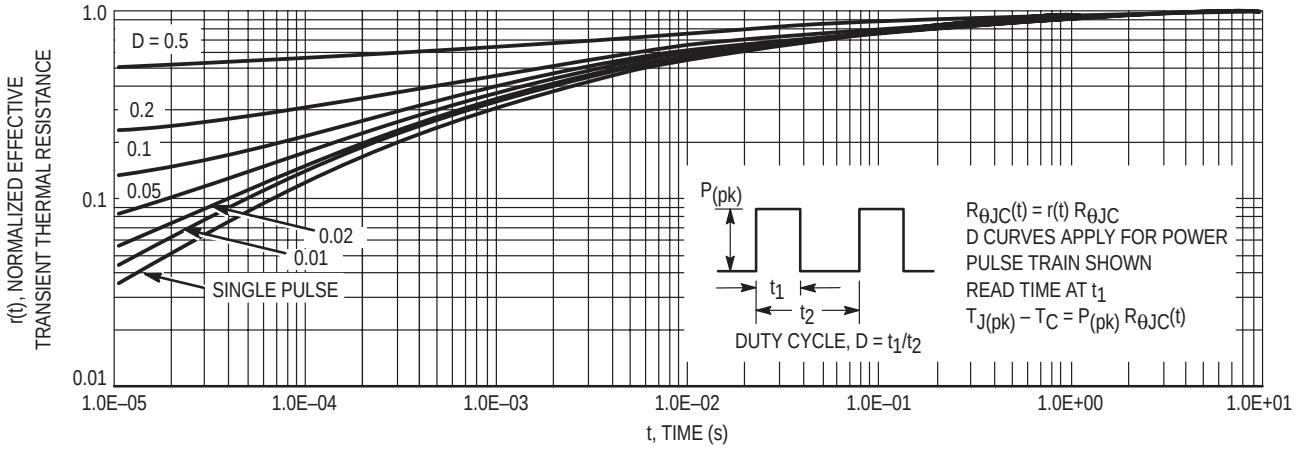


Figure 13. Thermal Response

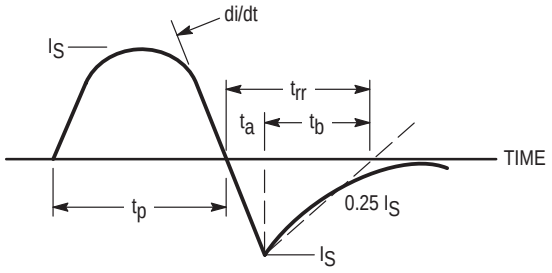


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

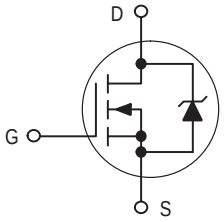
TMOS E-FET ™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

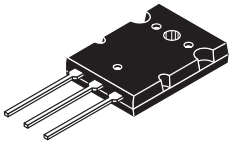
MTY14N100E
Motorola Preferred Device

TMOS POWER FET
14 AMPERES
1000 VOLTS
$R_{DS(on)}$ = 0.80 OHM

This advanced TMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters, PWM motor controls, and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 340G–02, STYLE 1
TO–264

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	1000	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	1000	Vdc
Gate–to–Source Voltage — Continuous — Single Pulse ($t_p \le 50$ μs)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ T_C = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	14 8.7 49	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	300 2.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 14 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	980	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.42 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0, I_D = 0.250 mAdc)		$V_{(BR)DSS}$	1000	—	—	Vdc
Temperature Coefficient (Positive)			—	1.0	—	V/°C
Zero Gate Voltage Drain Current (V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 1000 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.250 mAdc)		$V_{GS(th)}$	2.0	3.3	4.0	Vdc
Threshold Temperature Coefficient (Negative)			—	9.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 7.0 Adc)		$R_{DS(on)}$	—	0.67	0.8	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 14 Adc)		$V_{DS(on)}$	—	12.3	13.4	Vdc
(V_{GS} = 10 Vdc, I_D = 7.0 Adc, T_J = 125°C)			—	—	11.8	
Forward Transconductance (V_{DS} ≥ 15 Vdc, I_D = 7.0 Adc)		g_{FS}	10	12	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	7230		pF
Output Capacitance		C_{oss}	—	462		
Reverse Transfer Capacitance		C_{rss}	—	61		
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 500 Vdc, I_D = 14 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	49		ns
Rise Time		t_r	—	98		
Turn–Off Delay Time		$t_{d(off)}$	—	132		
Fall Time		t_f	—	83		
Gate Charge (See Figure 8)	(V_{DS} = 500 Vdc, I_D = 14 Adc, V_{GS} = 10 Vdc)	Q_T	—	142		nC
		Q_1	—	34	—	
		Q_2	—	46	—	
		Q_3	—	56	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 14 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	1.36	1.5	Vdc
	(I_S = 14 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	1.26	—	
Reverse Recovery Time (See Figure 14)	(I_S = 14 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	831	—	ns
		t_a	—	364	—	
		t_b	—	467	—	
Reverse Recovery Stored Charge		Q_{RR}	—	15.3	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

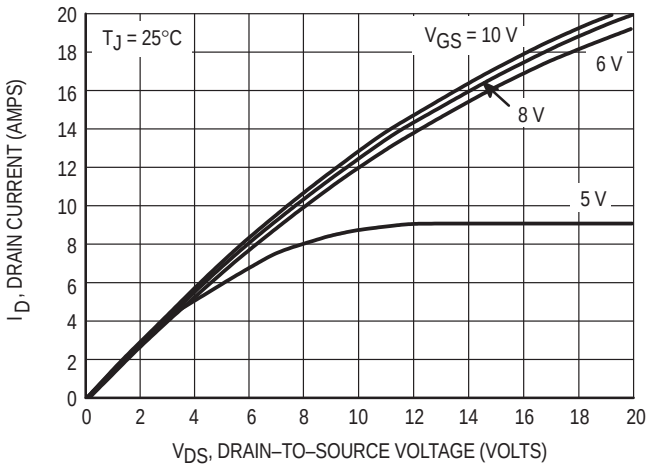


Figure 1. On–Region Characteristics

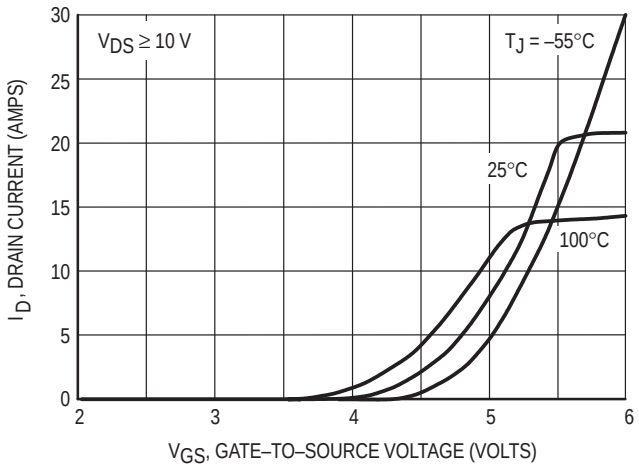


Figure 2. Transfer Characteristics

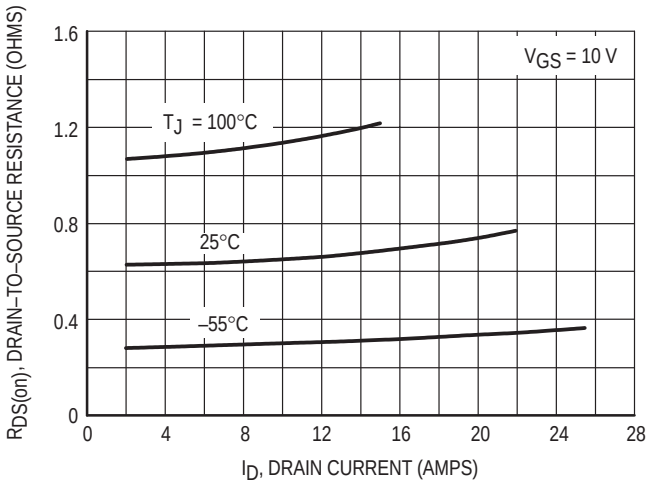


Figure 3. On–Resistance versus Drain Current and Temperature

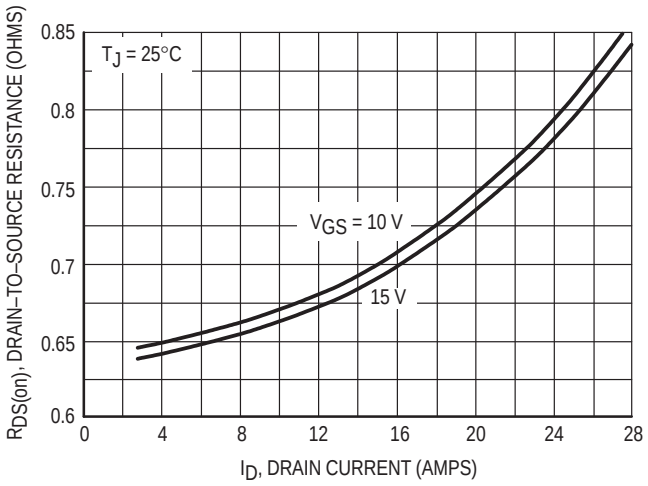


Figure 4. On–Resistance versus Drain Current and Gate Voltage

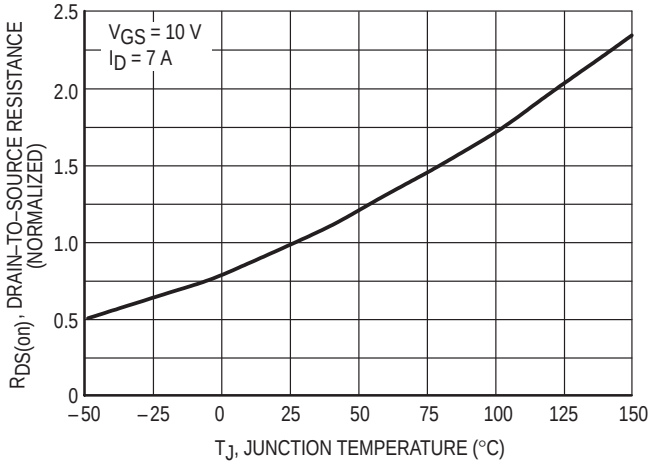


Figure 5. On–Resistance Variation with Temperature

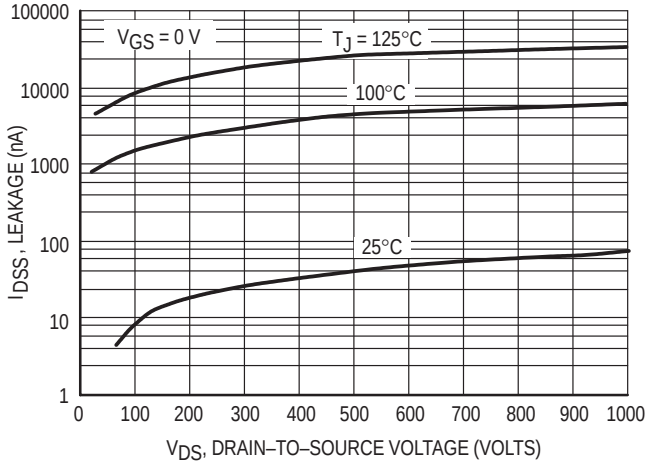


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

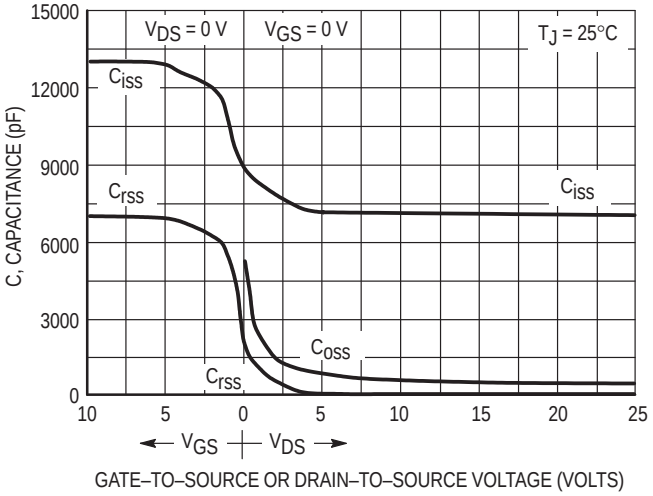


Figure 7a. Capacitance Variation

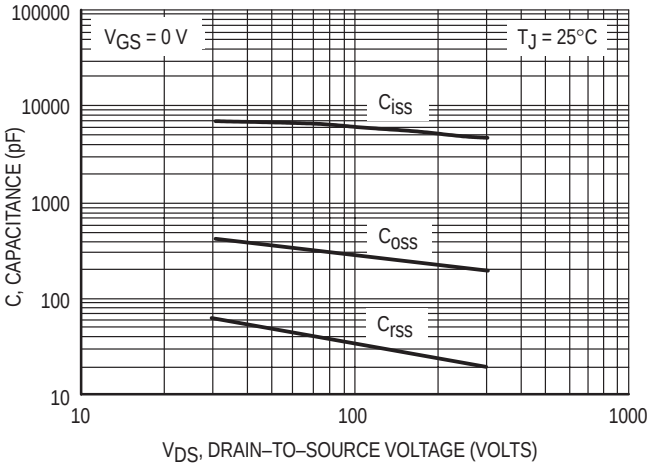


Figure 7b. High Voltage Capacitance Variation

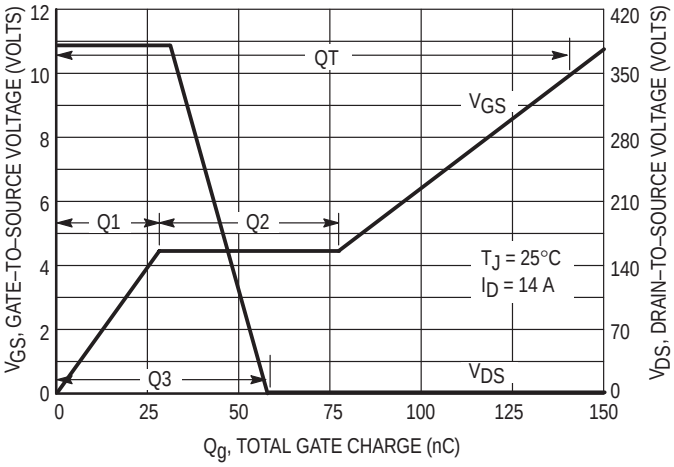


Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

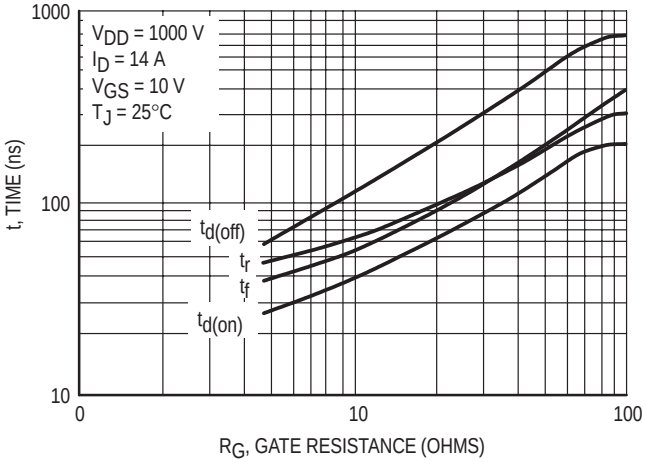
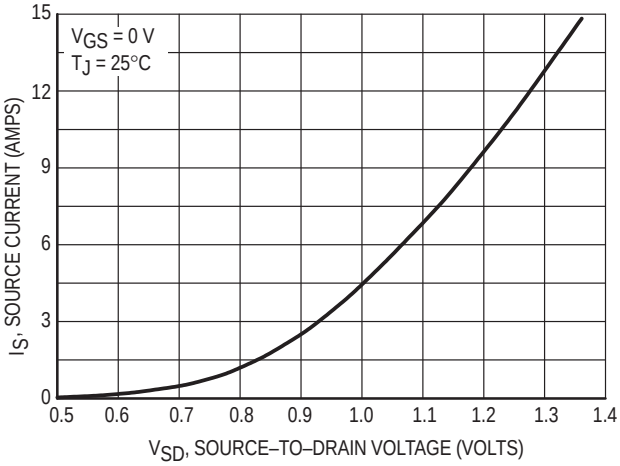


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS



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Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

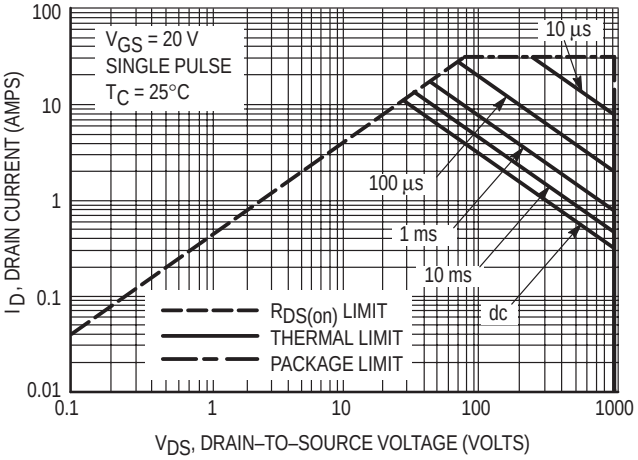


Figure 11. Maximum Rated Forward Biased Safe Operating Area

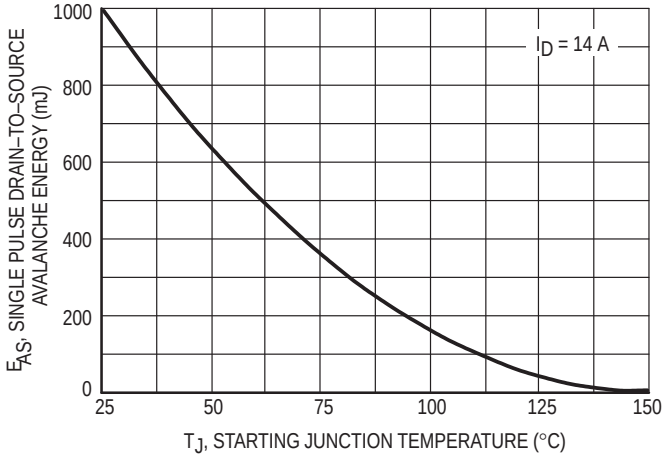


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

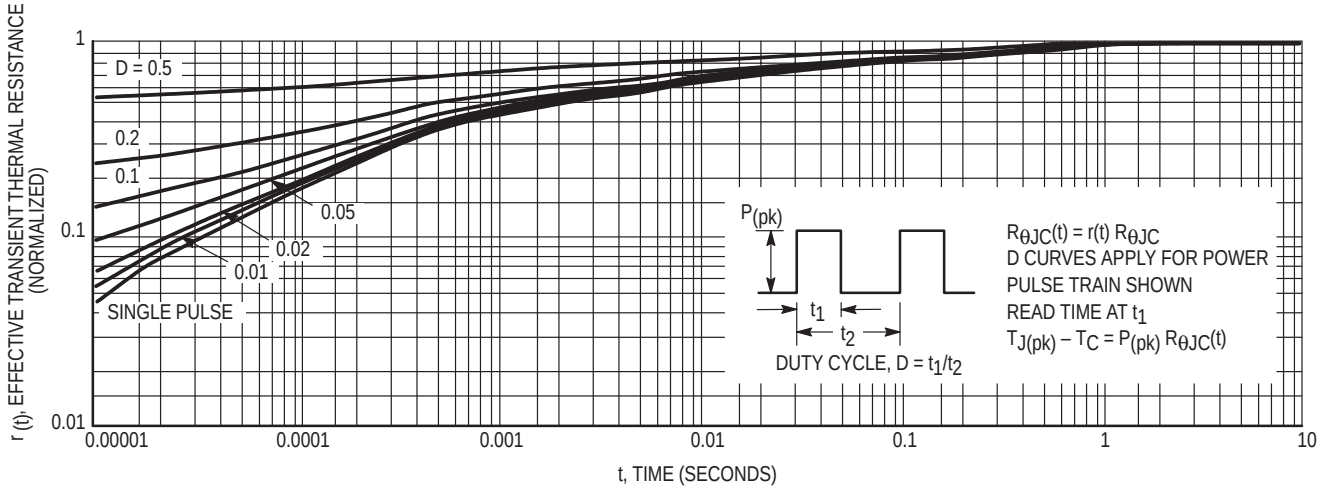


Figure 13. Thermal Response

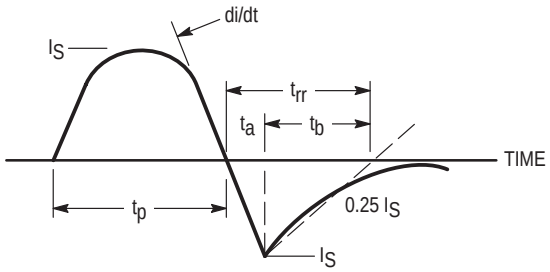


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

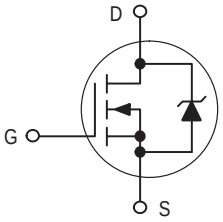
TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

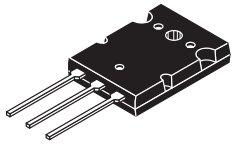
MTY16N80E
Motorola Preferred Device

TMOS POWER FET
16 AMPERES
800 VOLTS
$R_{DS(on)}$ = 0.50 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 340G–02, STYLE 1
TO–264

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	800	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	800	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ T_C = 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	16 11 55	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	300 2.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 16 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	 1280	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.42 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)		$V_{(BR)DSS}$	800	—	—	Vdc
Temperature Coefficient (Positive)			—	570	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 800 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 800 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	9.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 8.0 Adc)		$R_{DS(on)}$	—	0.42	0.5	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 16 Adc)		$V_{DS(on)}$	—	7.3	9.4	Vdc
(V_{GS} = 10 Vdc, I_D = 8.0 Adc, T_J = 125°C)			—	—	8.4	
Forward Transconductance (V_{DS} ≥ 15 Vdc, I_D = 8.0 Adc)		g_{FS}	10	15	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	7220	10110	pF
Output Capacitance		C_{oss}	—	508	710	
Reverse Transfer Capacitance		C_{rss}	—	65	130	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 400 Vdc, I_D = 16 Adc, V_{GS} = 10 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	52	100	ns
Rise Time		t_r	—	112	200	
Turn–Off Delay Time		$t_{d(off)}$	—	122	240	
Fall Time		t_f	—	100	200	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 16 Adc, V_{GS} = 10 Vdc)	Q_T	—	146	200	nC
		Q_1	—	39	—	
		Q_2	—	48	—	
		Q_3	—	53	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 16 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.9	1.2	Vdc
	(I_S = 16 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.79	—	
Reverse Recovery Time (See Figure 14)	(I_S = 16 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	995	—	ns
		t_a	—	428	—	
		t_b	—	567	—	
Reverse Recovery Stored Charge		Q_{RR}	—	20	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

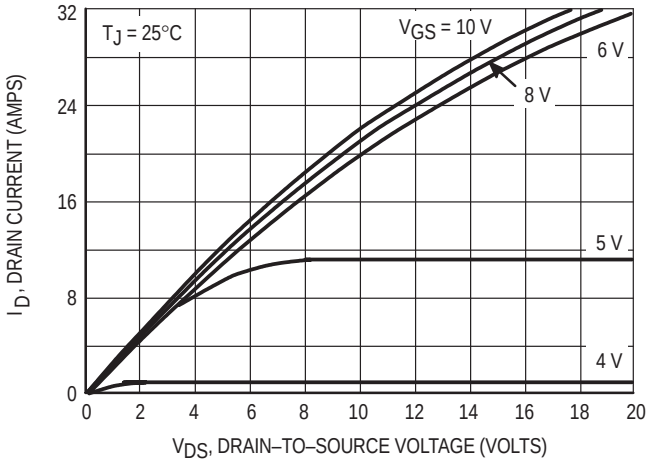


Figure 1. On–Region Characteristics

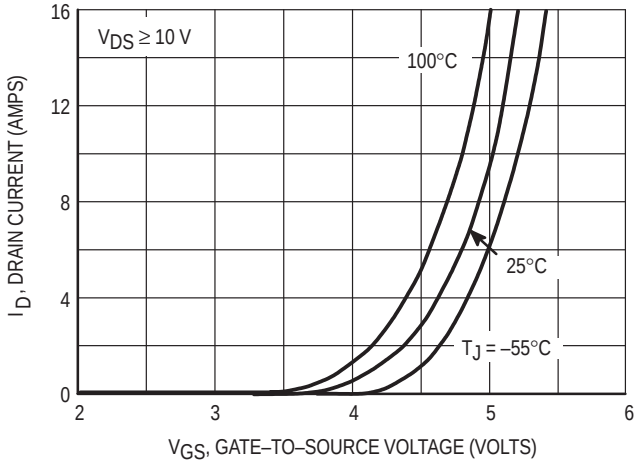


Figure 2. Transfer Characteristics

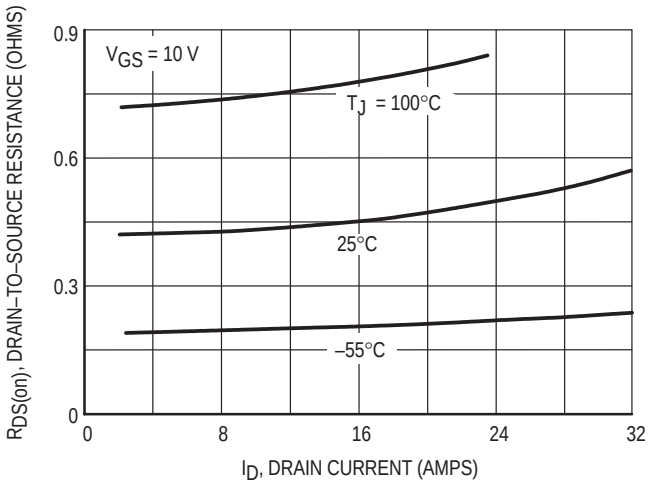


Figure 3. On–Resistance versus Drain Current and Temperature

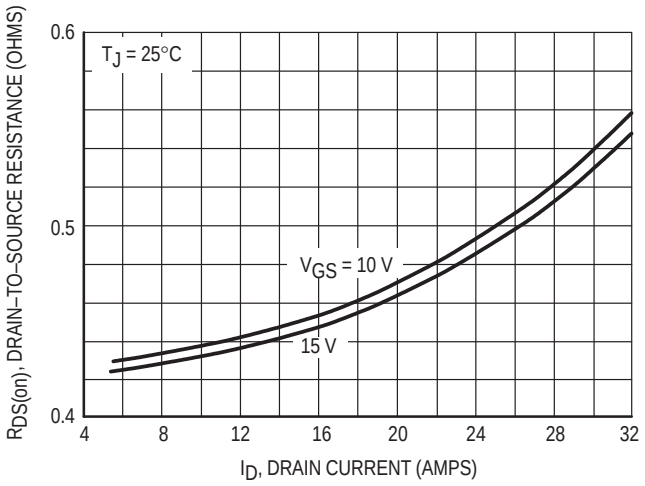


Figure 4. On–Resistance versus Drain Current and Gate Voltage

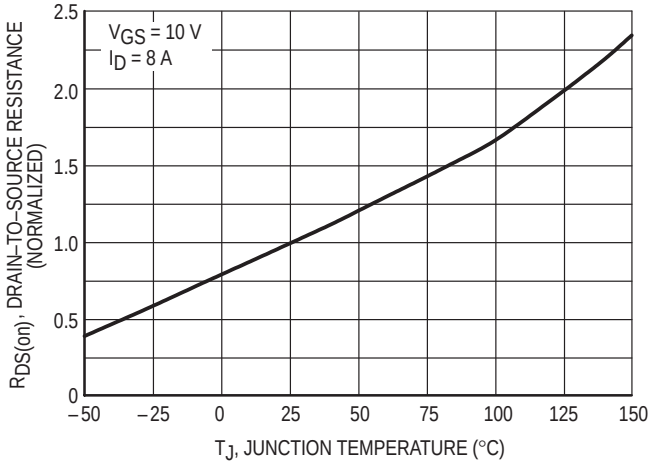


Figure 5. On–Resistance Variation with Temperature

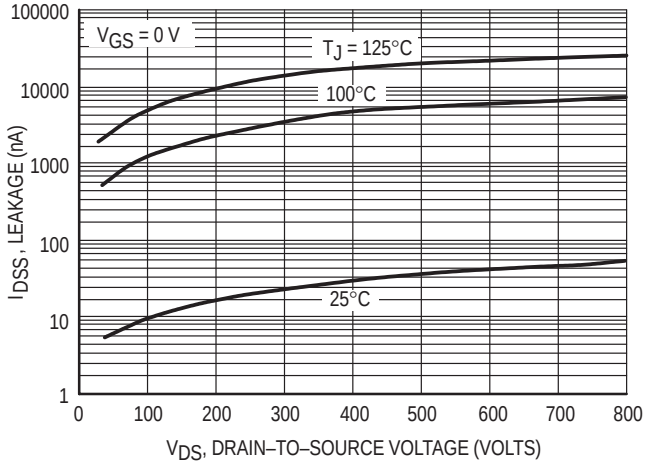


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

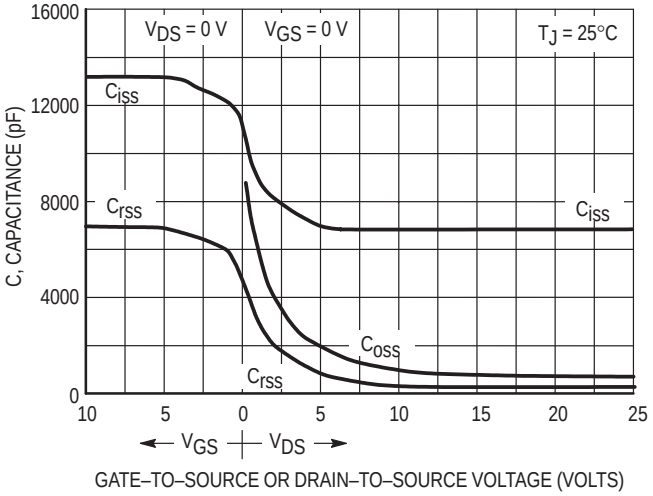


Figure 7a. Capacitance Variation

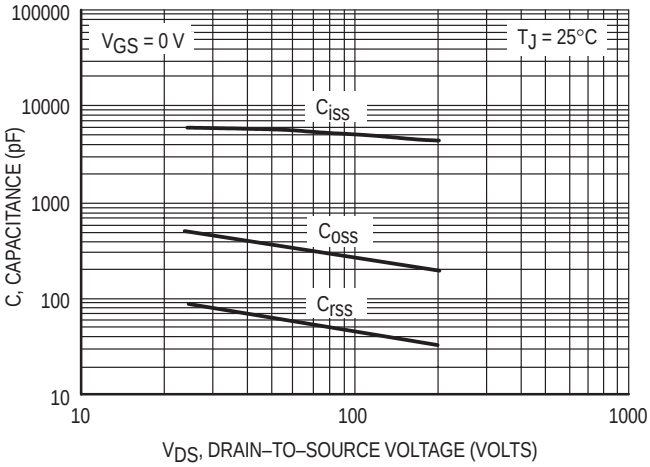


Figure 7b. High Voltage Capacitance Variation

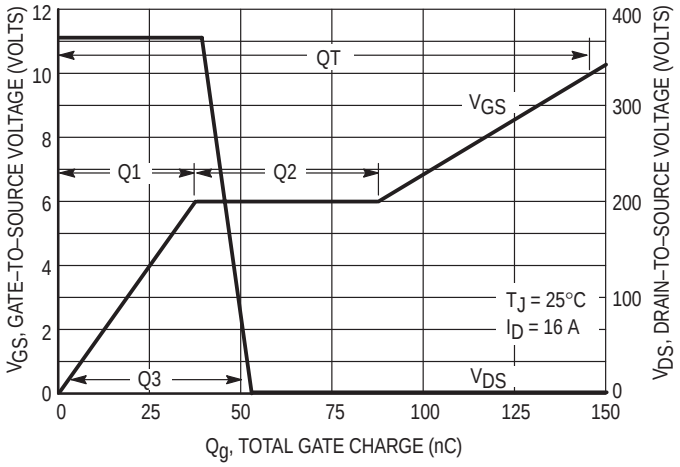


Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

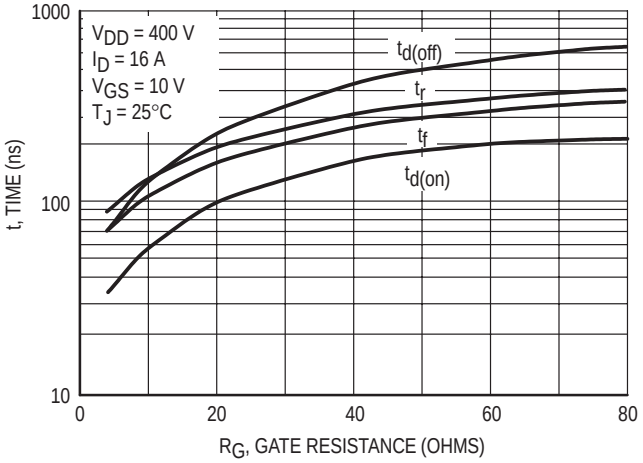


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

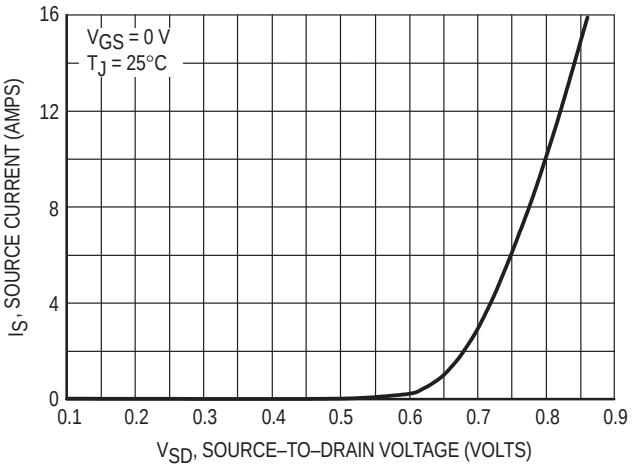


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

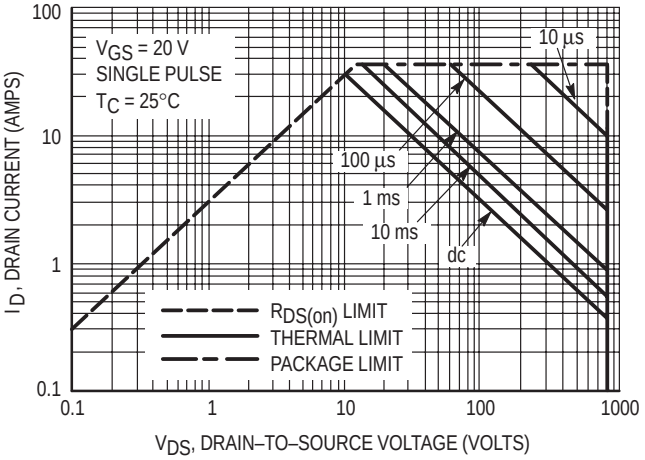


Figure 11. Maximum Rated Forward Biased Safe Operating Area

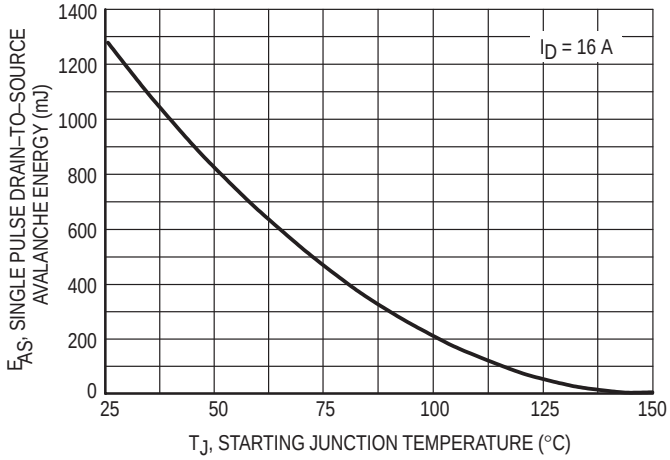


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

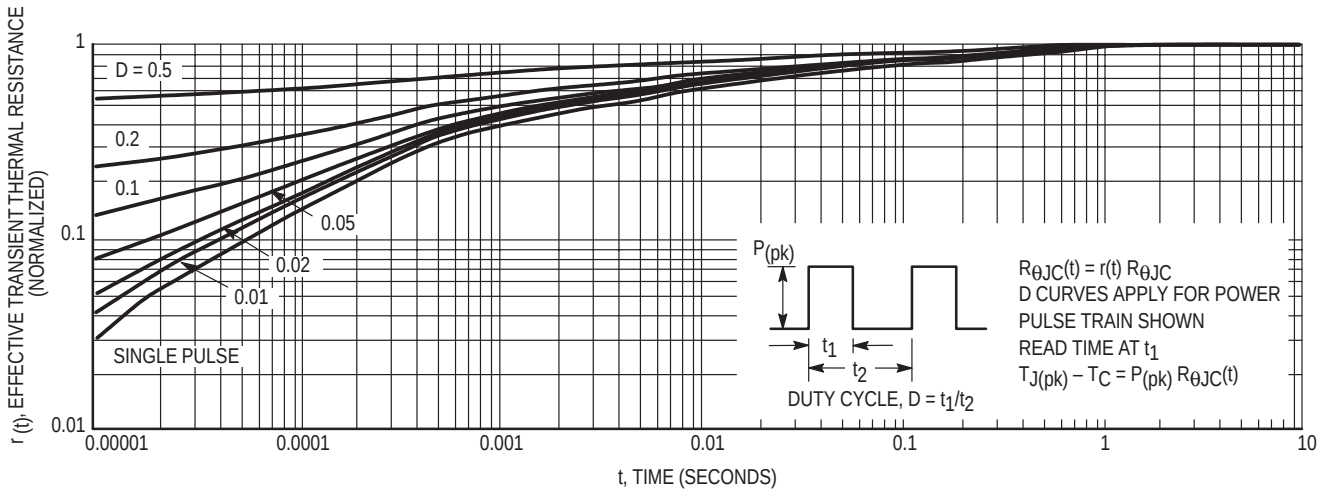


Figure 13. Thermal Response

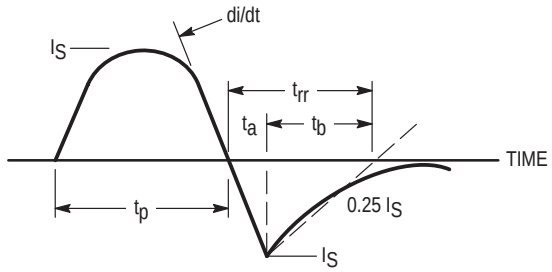


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet
TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

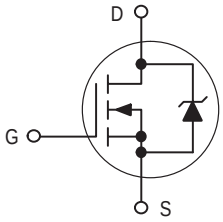
MTY20N50E

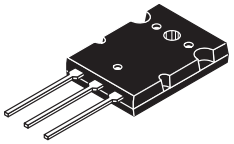
Motorola Preferred Device

TMOS POWER FET
20 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.26 OHM

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 340G–02, Style 1
TO–264

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	500	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	± 20 ± 40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ μs)	I_D I_D I_{DM}	20 13.9 60	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	250 2.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 20 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	2000	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.50 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)		$V_{(BR)DSS}$	500	—	—	Vdc
Temperature Coefficient (Positive)			—	583	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc)		I_{DSS}	—	—	10	μAdc
(V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)			—	—	100	
Gate–Body Leakage Current (V_{GS} = ± 20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)		$V_{GS(th)}$	2.0	3.0	4.0	Vdc
Temperature Coefficient (Negative)			—	7.0	—	mV/°C
Static Drain–to–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$R_{DS(on)}$	—	0.22	0.26	Ohm
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 20 Adc)		$V_{DS(on)}$	—	4.75	6.2	Vdc
(V_{GS} = 10 Vdc, I_D = 10 Adc, T_J = 125°C)			—	—	6.5	
Forward Transconductance (V_{DS} = 13 Vdc, I_D = 10 Adc)		g_{FS}	11	16.2	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	3880	6980	pF
Output Capacitance		C_{oss}	—	452	920	
Reverse Transfer Capacitance		C_{rss}	—	96	140	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	29	60	ns
Rise Time		t_r	—	90	170	
Turn–Off Delay Time		$t_{d(off)}$	—	97	190	
Fall Time		t_f	—	84	170	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 20 Adc, V_{GS} = 10 Vdc)	Q_T	—	100	140	nC
		Q_1	—	20	—	
		Q_2	—	44	—	
		Q_3	—	36	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage (1)	(I_S = 20 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.92	1.1	Vdc
	(I_S = 20 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.81	—	
Reverse Recovery Time (See Figure 14)	(I_S = 20 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	431	—	ns
		t_a	—	272	—	
		t_b	—	159	—	
Reverse Recovery Stored Charge		Q_{RR}	—	6.67	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from contact screw on tab to center of die)		L_D	—	3.5	—	nH
(Measured from the drain lead 0.25″ from package to center of die)			—	4.5	—	
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

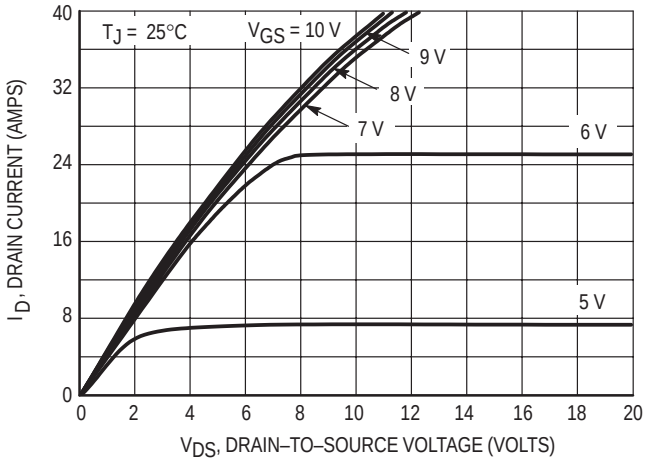


Figure 1. On–Region Characteristics

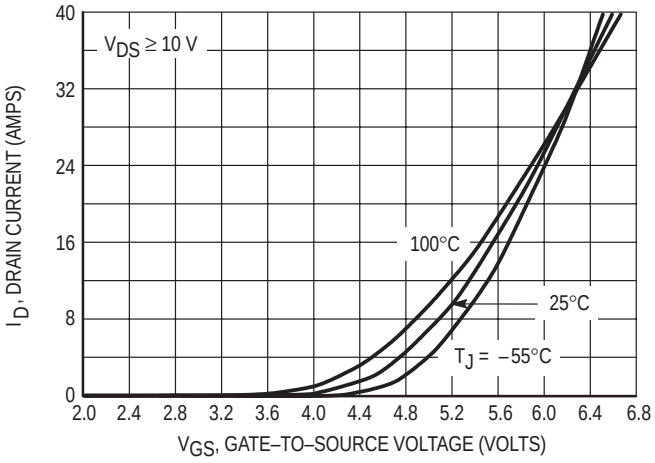


Figure 2. Transfer Characteristics

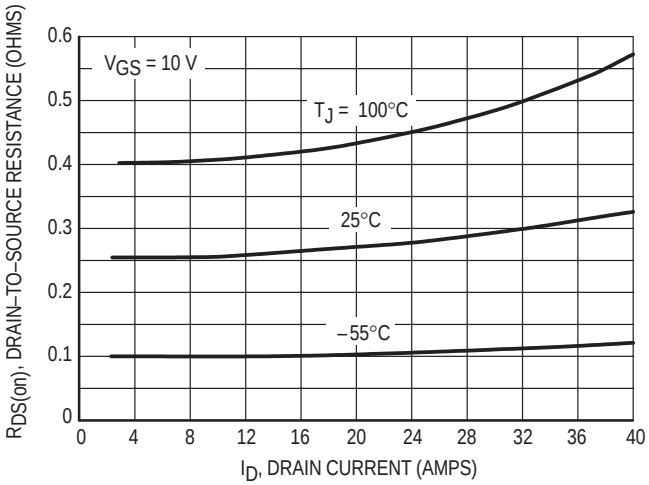


Figure 3. On–Resistance versus Drain Current and Temperature

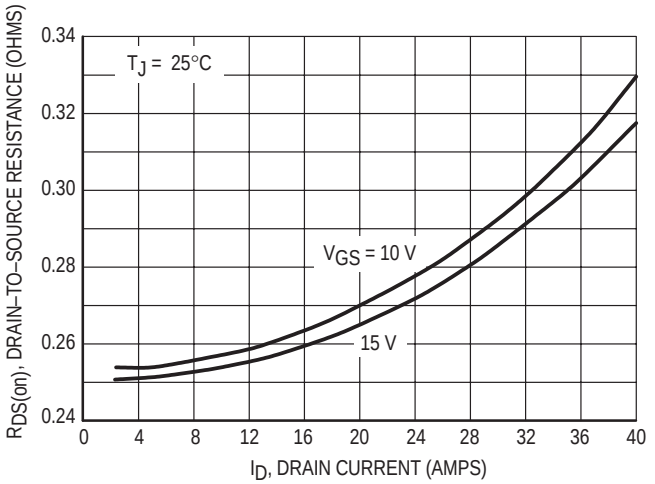


Figure 4. On–Resistance versus Drain Current and Gate Voltage

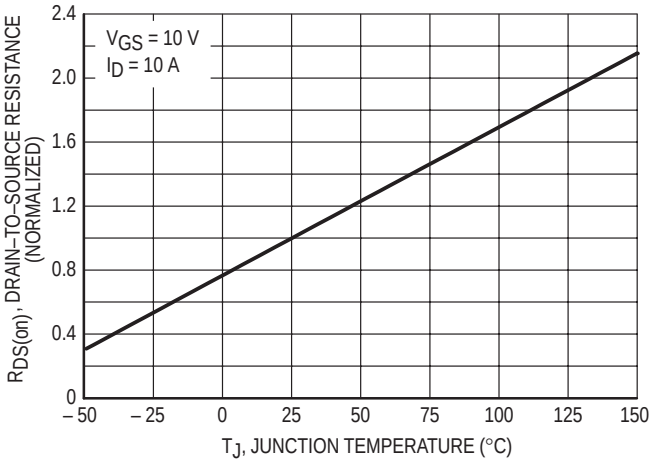


Figure 5. On–Resistance Variation with Temperature

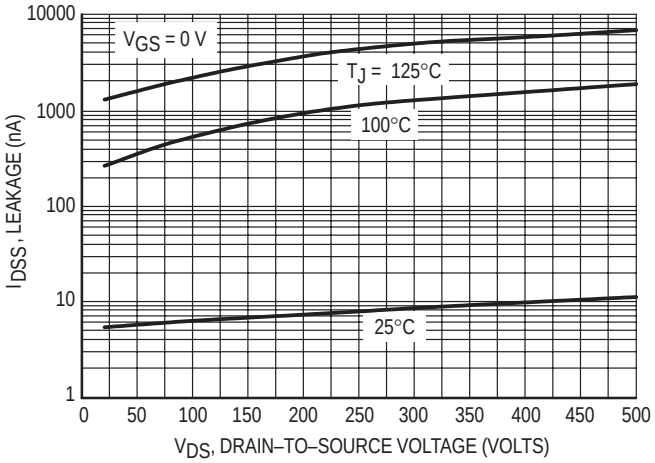


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

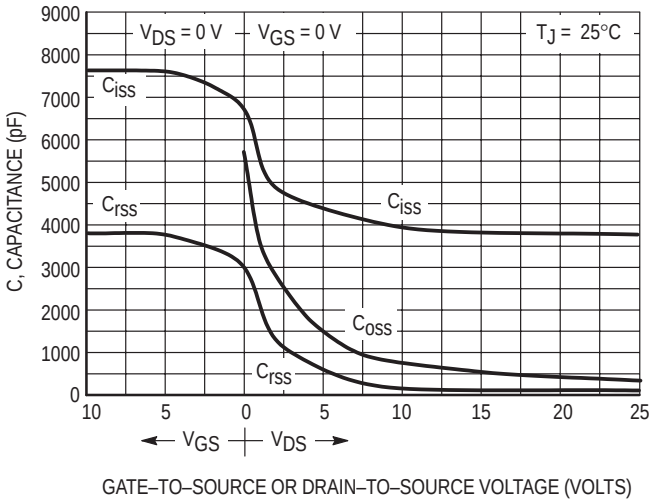


Figure 7a. Capacitance Variation

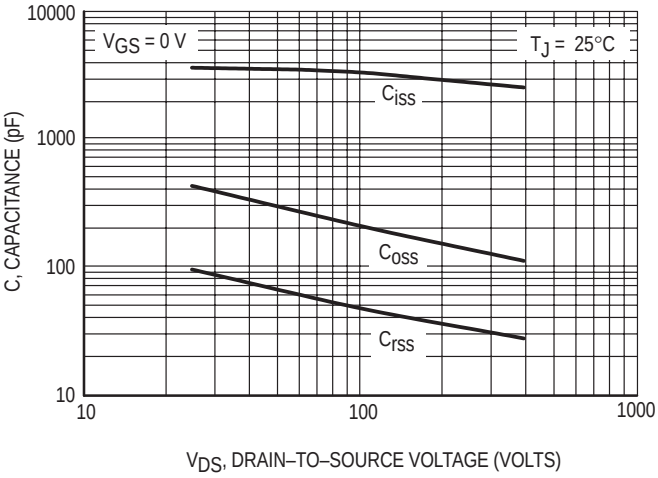


Figure 7b. High Voltage Capacitance-Variation

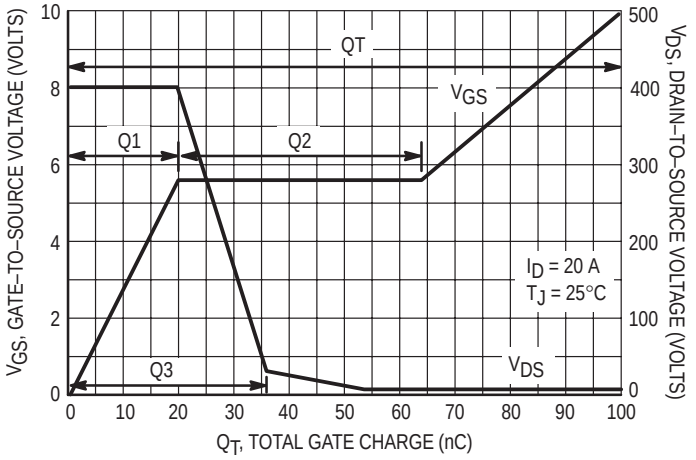


Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Gate Charge

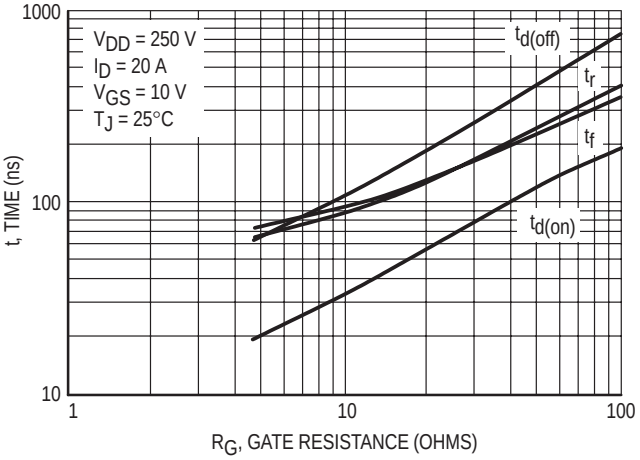


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

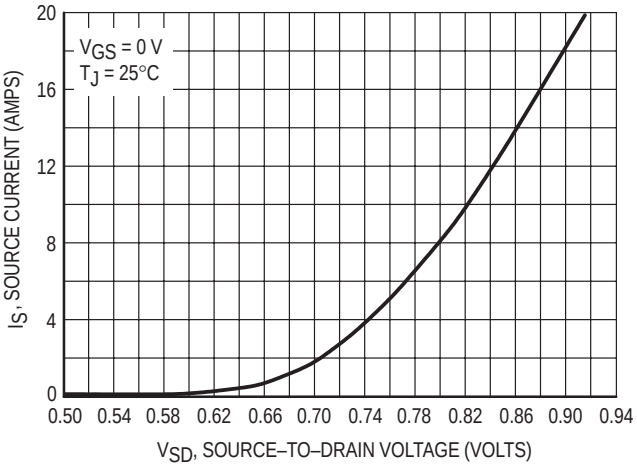


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

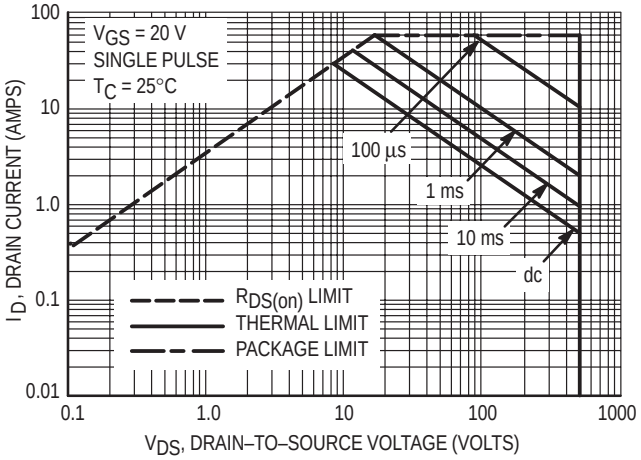


Figure 11. Maximum Rated Forward Biased Safe Operating Area

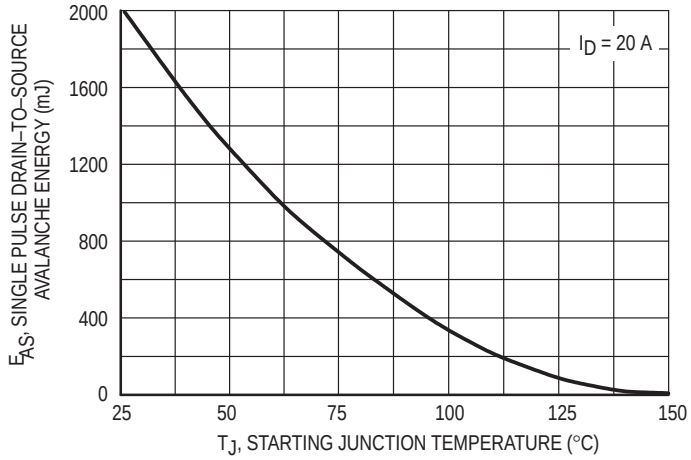


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

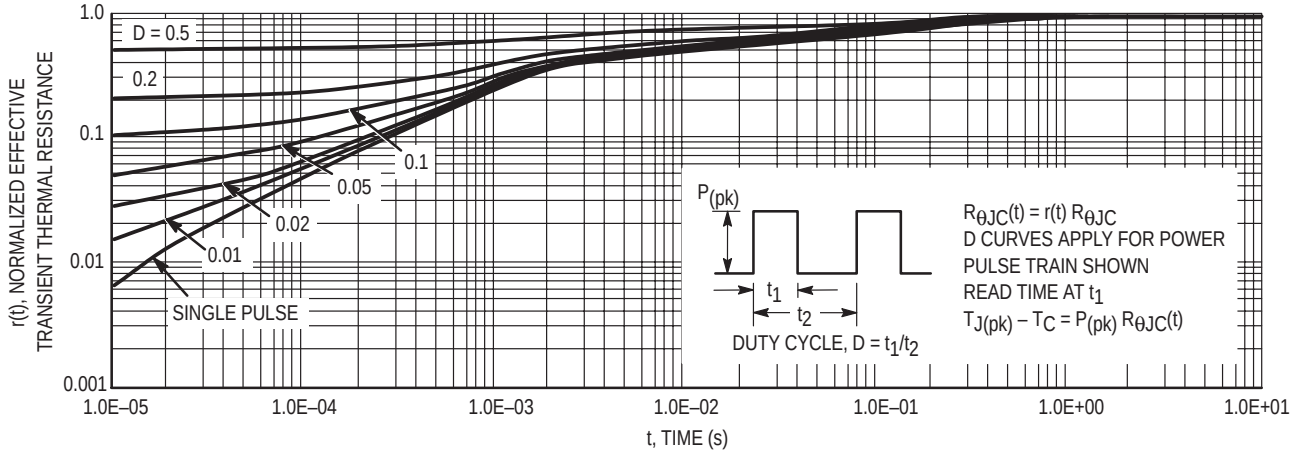


Figure 13. Thermal Response

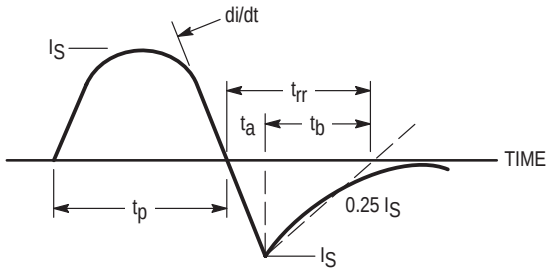


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

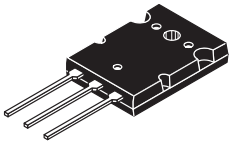
TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

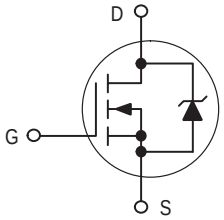
MTY25N60E
Motorola Preferred Device

TMOS POWER FET
25 AMPERES
600 VOLTS
$R_{DS(on)}$ = 0.21 OHM

This advanced TMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters, PWM motor controls, and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 340G–02, STYLE 1
TO–264

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	600	Vdc
Drain–Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous @ T_C = 25°C — Single Pulse ($t_p \le 10$ μs)	I_D I_{DM}	25 65	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	300 2.38	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 25 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	3000	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.42 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

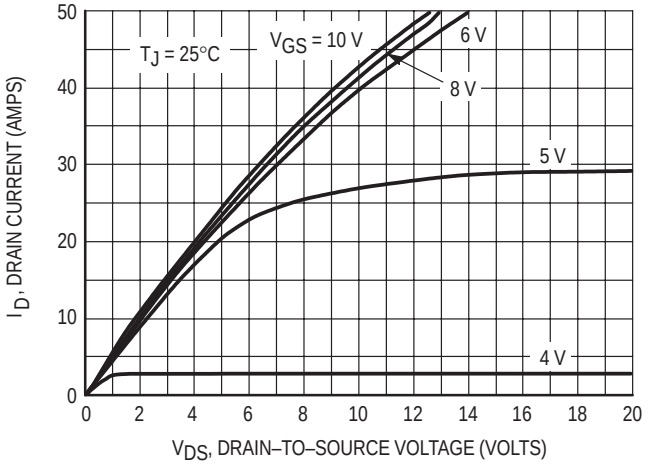
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	600 —	— 714	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 600 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 200	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	2 —	— 7	4 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 12.5 Adc)		$R_{DS(on)}$	—	—	0.21	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 25 Adc) (I_D = 12.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	5.2 —	6 7	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 12.5 Adc)		g_{FS}	18	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	7300	10220	pF
Output Capacitance		C_{oss}	—	700	1100	
Reverse Transfer Capacitance		C_{rss}	—	110	250	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 300 Vdc, I_D = 25 Adc, V_{GS} = 10 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	32	60	ns
Rise Time		t_r	—	90	175	
Turn–Off Delay Time		$t_{d(off)}$	—	170	300	
Fall Time		t_f	—	110	200	
Gate Charge (See Figure 8)	(V_{DS} = 480 Vdc, I_D = 25 Adc, V_{GS} = 10 Vdc)	Q_T	—	240	350	nC
		Q_1	—	30	—	
		Q_2	—	110	—	
		Q_3	—	65	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 25 Adc, V_{GS} = 0 Vdc) (I_S = 25 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.9 0.8	1.2 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 25 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	620	—	ns
		t_a	—	310	—	
		t_b	—	310	—	
Reverse Recovery Stored Charge		Q_{RR}	—	10.42	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	7.5	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS



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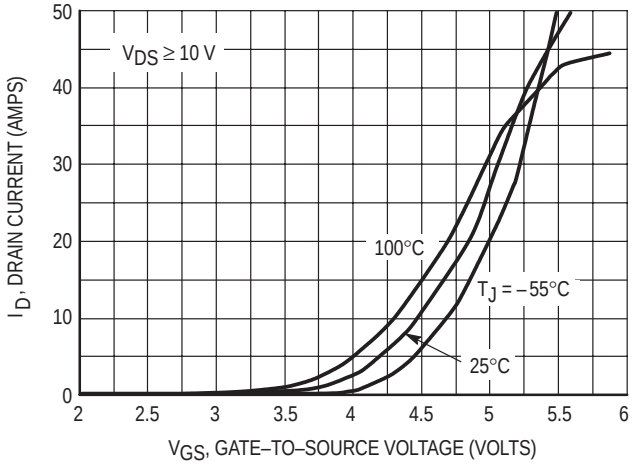

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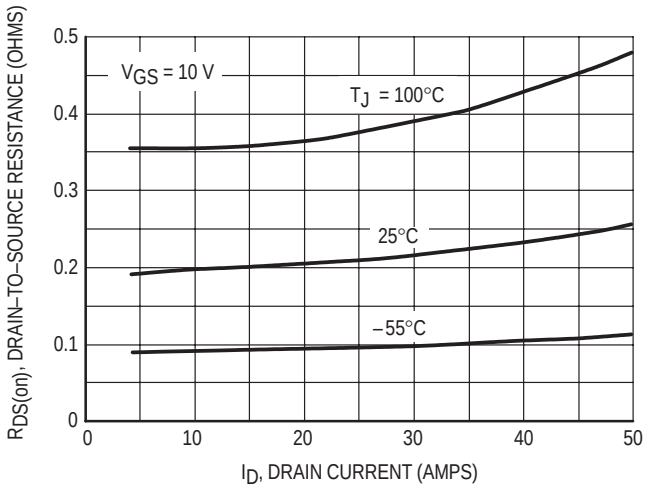

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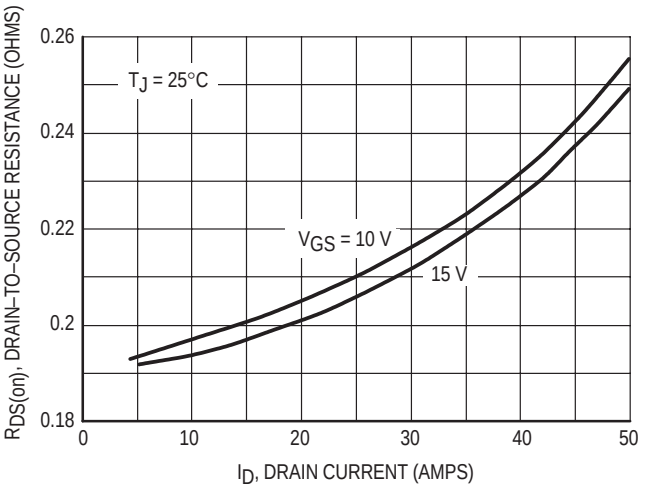

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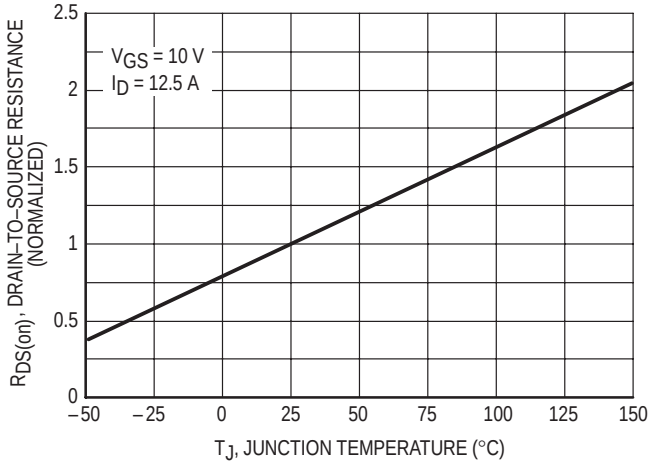
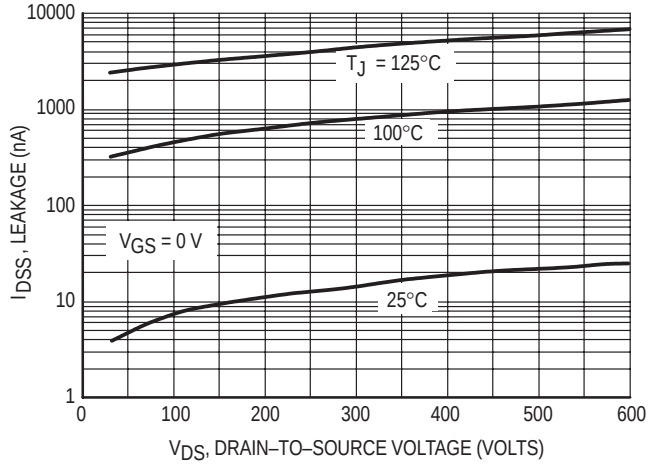


Figure 5. On–Resistance Variation with Temperature



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During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

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$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

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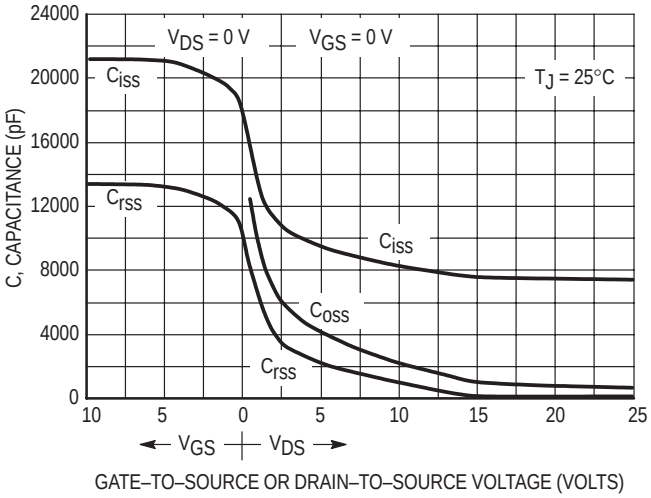


Figure 7a. Capacitance Variation

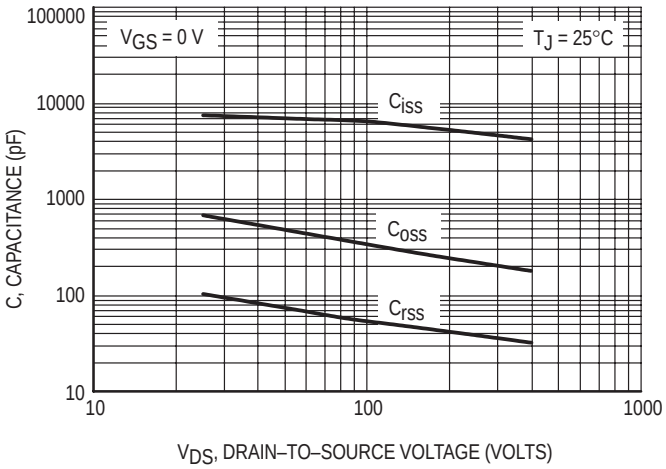


Figure 7b. High Voltage Capacitance Variation

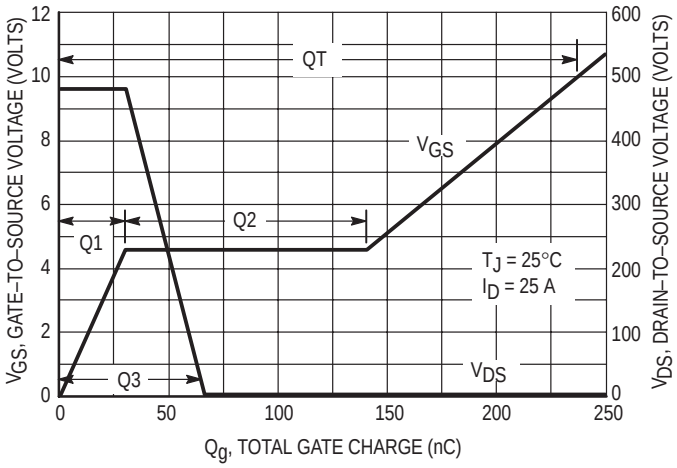


Figure 8. Gate Charge versus Gate–to–Source Voltage

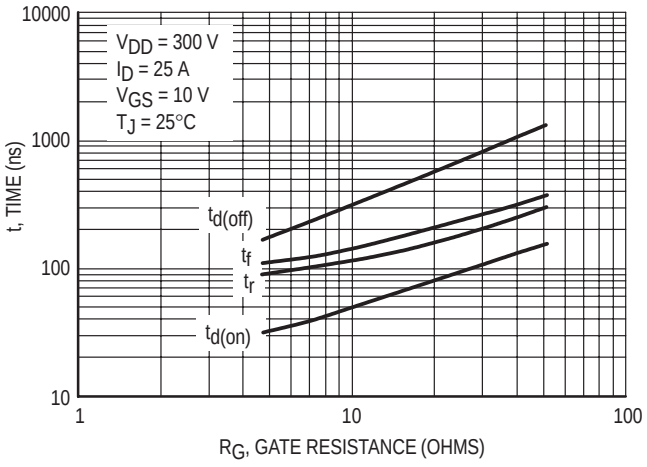


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

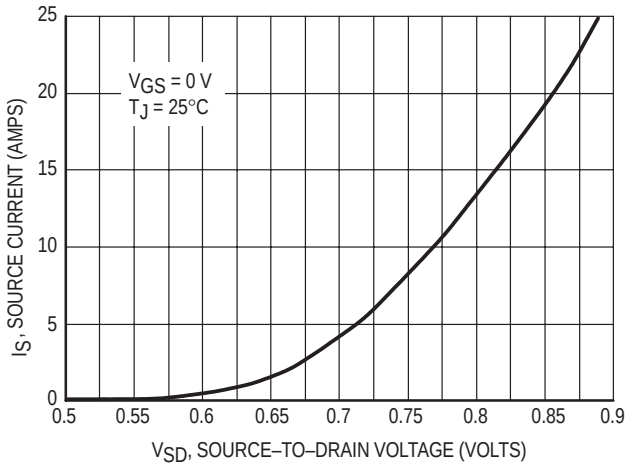


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

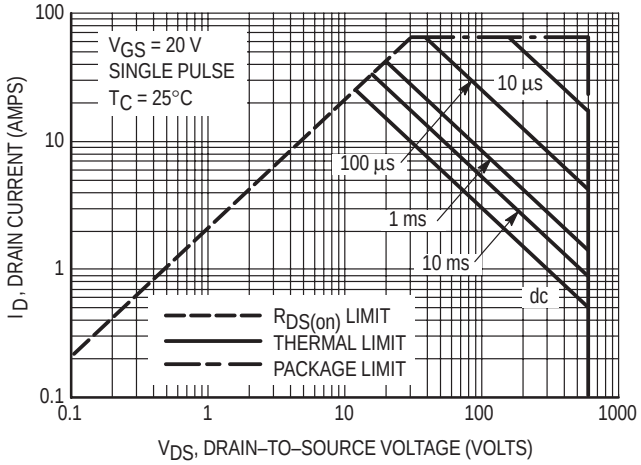


Figure 11. Maximum Rated Forward Biased Safe Operating Area

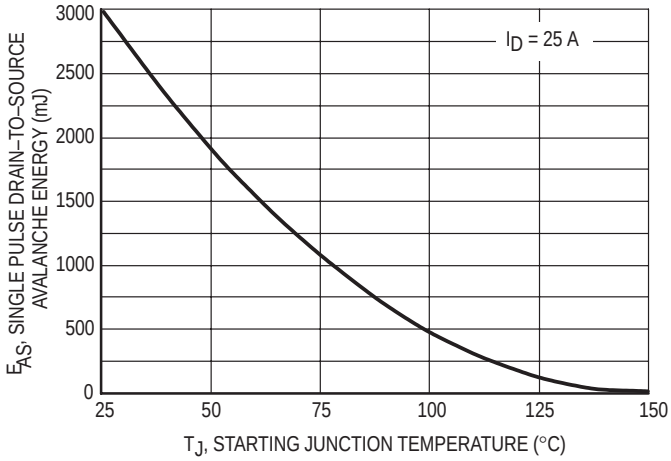


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

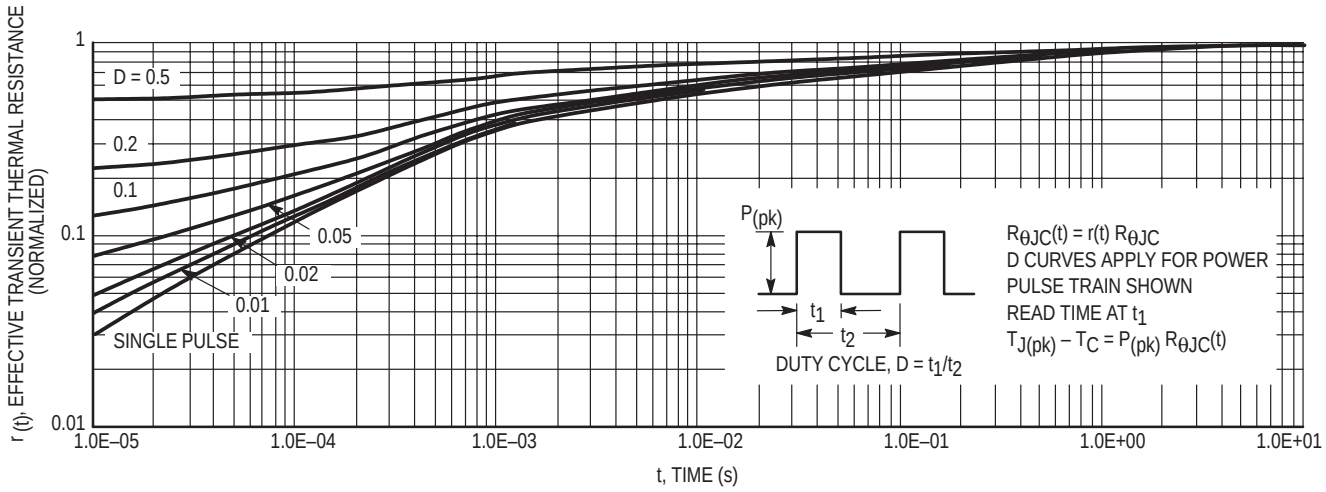


Figure 13. Thermal Response

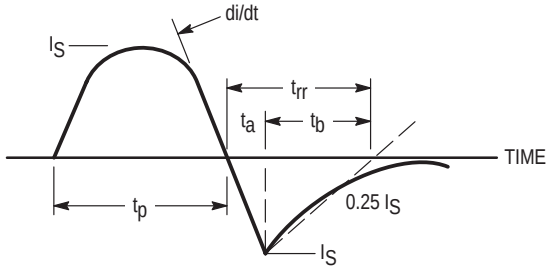


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

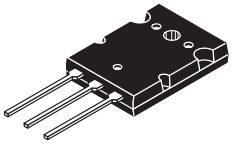
TMOS E-FET ™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

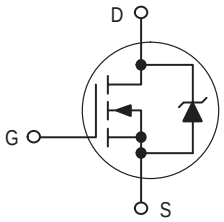
MTY30N50E
Motorola Preferred Device

TMOS POWER FET
30 AMPERES
500 VOLTS
$R_{DS(on)}$ = 0.15 OHM

This advanced TMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters, PWM motor controls, and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 340G–02, STYLE 1
TO–264

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	500	Vdc
Drain–Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	500	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous @ T_C = 25°C — Single Pulse ($t_p \le 10$ μs)	I_D I_{DM}	30 80	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	300 2.38	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, Peak I_L = 30 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	3000	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.42 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	500 —	— 566	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 500 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 200	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	2 —	— 7	4 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 15 Adc)		$R_{DS(on)}$	—	—	0.15	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 30 Adc) (I_D = 15 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	4.1 —	5 7	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 15 Adc)		g_{FS}	17	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1 MHz)	C_{iss}	—	7200	10080	pF
Output Capacitance		C_{oss}	—	775	1200	
Reverse Transfer Capacitance		C_{rss}	—	120	250	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 250 Vdc, I_D = 30 Adc, V_{GS} = 10 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	32	60	ns
Rise Time		t_r	—	105	175	
Turn–Off Delay Time		$t_{d(off)}$	—	160	275	
Fall Time		t_f	—	115	200	
Gate Charge (See Figure 8)	(V_{DS} = 400 Vdc, I_D = 30 Adc, V_{GS} = 10 Vdc)	Q_T	—	235	350	nC
		Q_1	—	35	—	
		Q_2	—	110	—	
		Q_3	—	65	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 30 Adc, V_{GS} = 0 Vdc) (I_S = 30 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.95 0.88	1.2 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 30 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	485	—	ns
		t_a	—	312	—	
		t_b	—	173	—	
Reverse Recovery Stored Charge		Q_{RR}	—	8.2	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

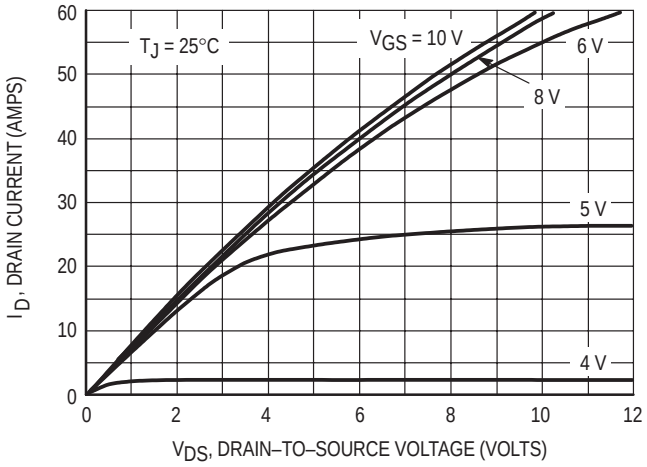


Figure 1. On–Region Characteristics

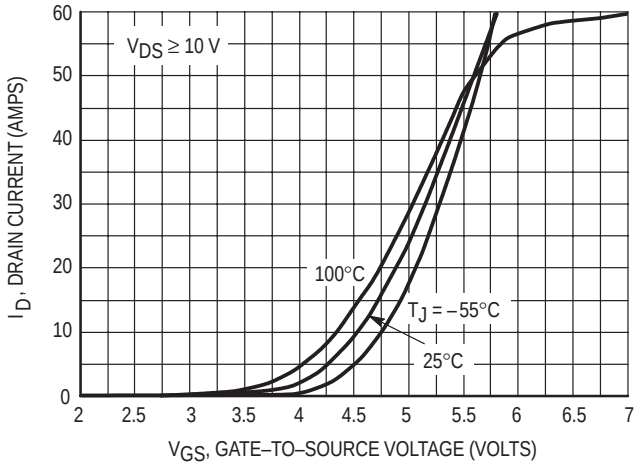


Figure 2. Transfer Characteristics

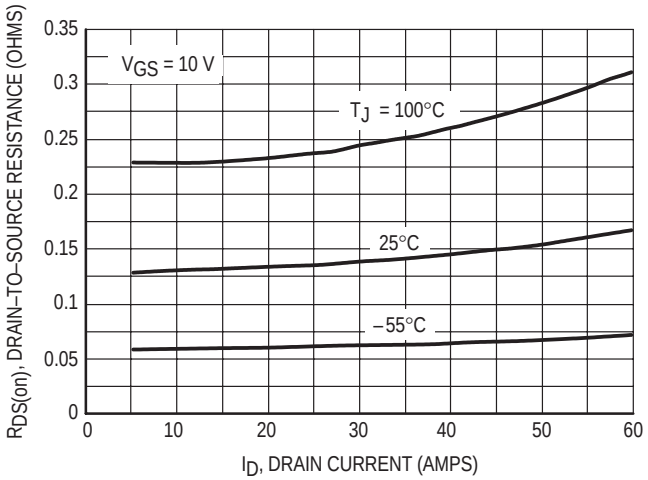


Figure 3. On–Resistance versus Drain Current and Temperature

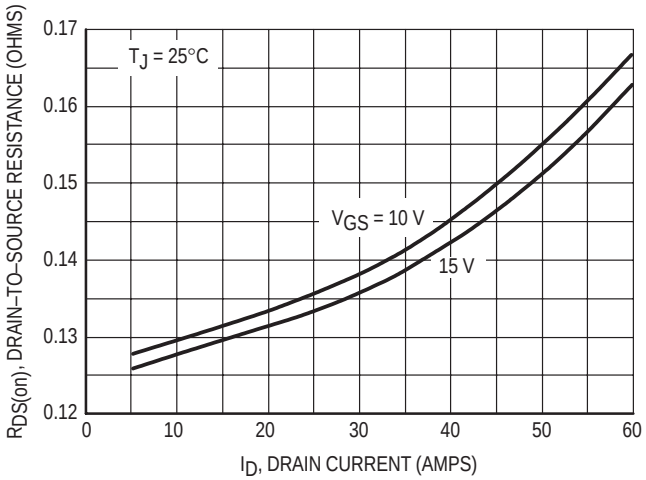


Figure 4. On–Resistance versus Drain Current and Gate Voltage

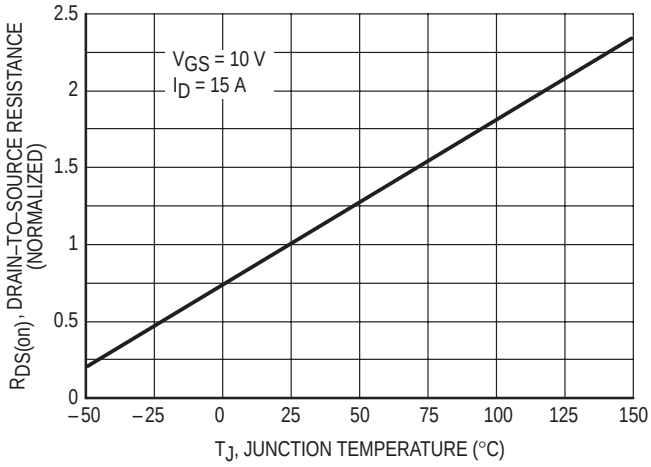


Figure 5. On–Resistance Variation with Temperature

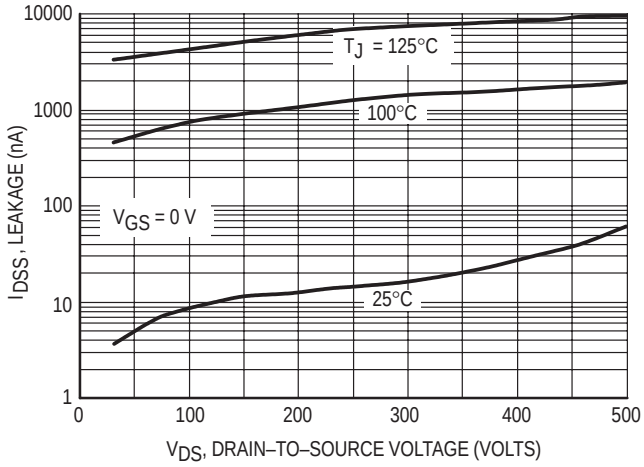


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

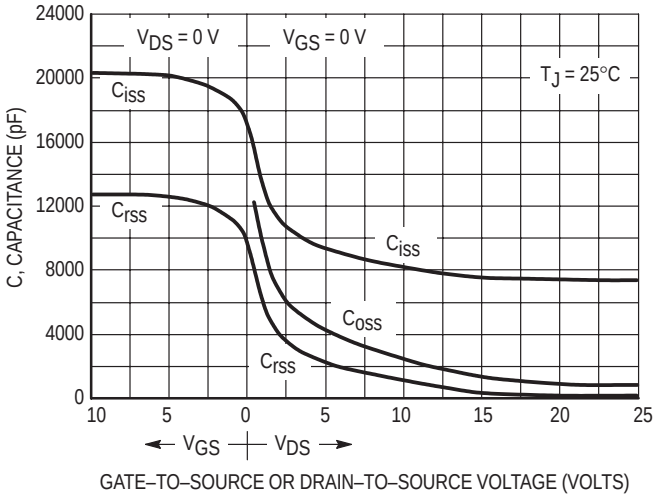


Figure 7a. Capacitance Variation

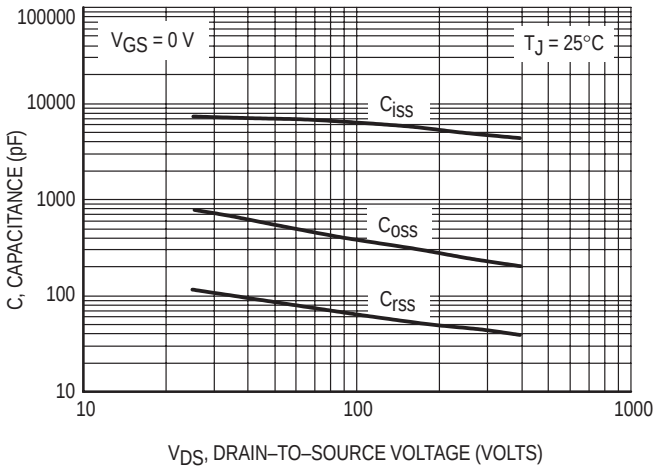


Figure 7b. High Voltage Capacitance Variation

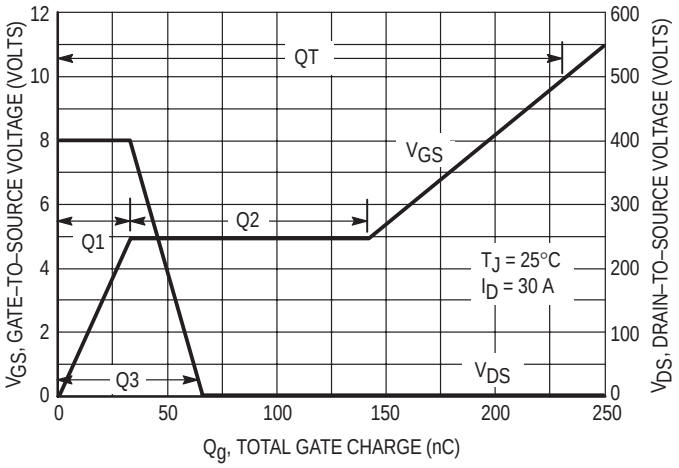


Figure 8. Gate Charge versus Gate–to–Source Voltage

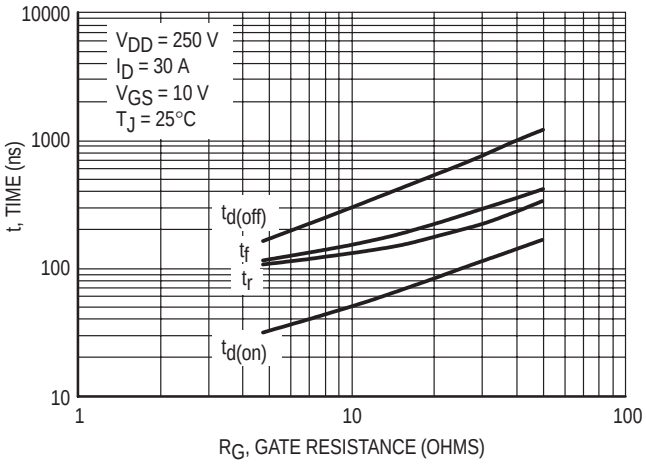


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

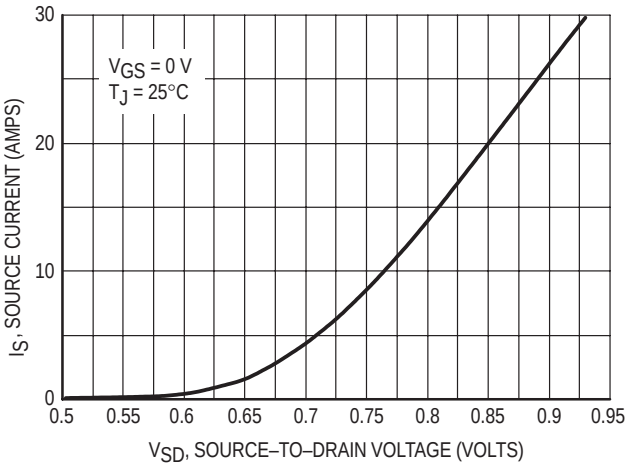


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

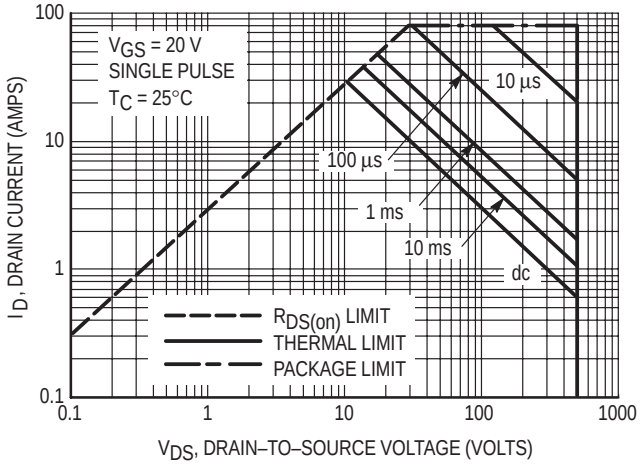


Figure 11. Maximum Rated Forward Biased Safe Operating Area

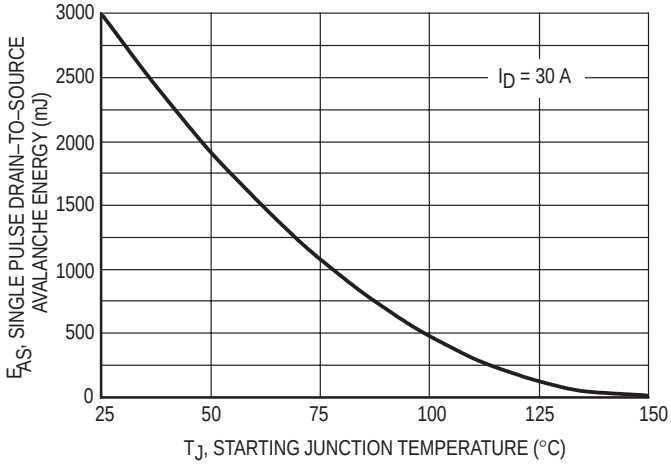


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

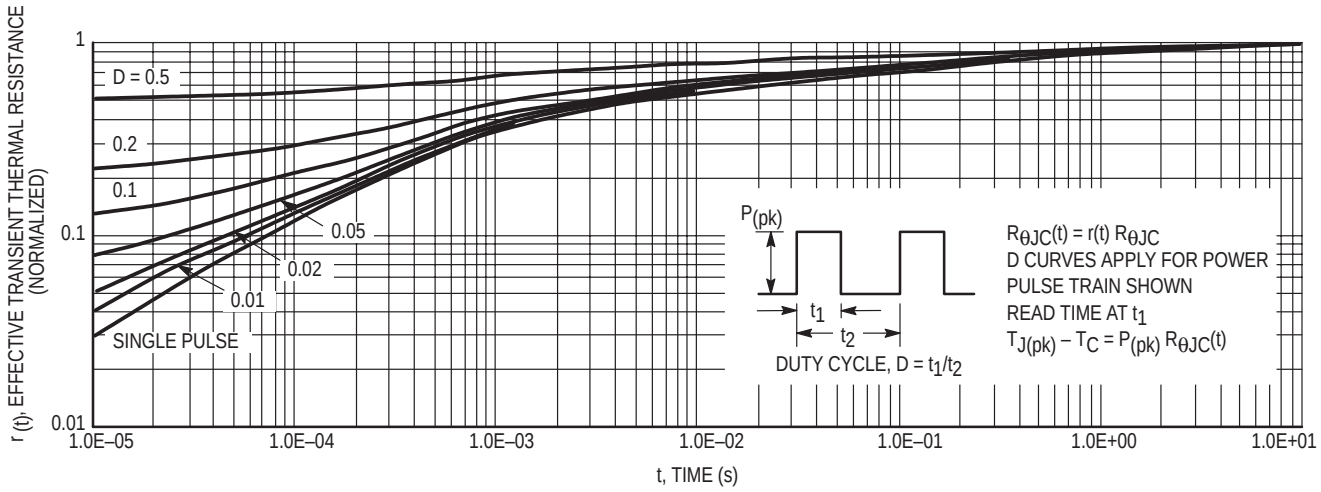


Figure 13. Thermal Response

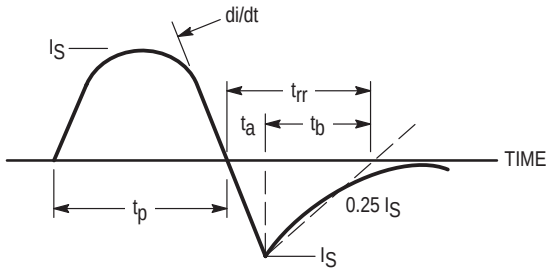


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

TMOS E-FET ™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

MTY55N20E
Motorola Preferred Device

TMOS POWER FET
55 AMPERES
200 VOLTS
$R_{DS(on)}$ = 0.028 OHM

This advanced TMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters, PWM motor controls, and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

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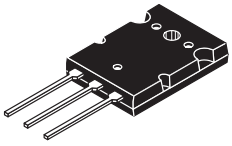
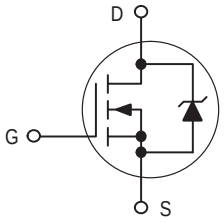
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 340G–02, STYLE 1
TO–264

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	200	Vdc
Drain–Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	200	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous @ T_C = 25°C — Single Pulse ($t_p \le 10$ µs)	I_D I_{DM}	55 165	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	300 2.38	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, Peak I_L = 110 Apk, L = 0.3 mH, R_G = 25 Ω)	E_{AS}	3000	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.42 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	200 —	— 250	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 200 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 200	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	2 —	— 7	4 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 27.5 Adc)		$R_{DS(on)}$	—	—	0.028	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 55 Adc) (I_D = 27.5 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	1.3 —	1.6 1.8	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 27.5 Adc)		g_{FS}	30	37	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1 MHz)	C_{iss}	—	7200	10080	pF
Output Capacitance		C_{oss}	—	1800	2520	
Reverse Transfer Capacitance		C_{rss}	—	460	920	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 100 Vdc, I_D = 55 Adc, V_{GS} = 10 Vdc, R_G = 4.7 Ω)	$t_{d(on)}$	—	33	66	ns
Rise Time		t_r	—	200	400	
Turn–Off Delay Time		$t_{d(off)}$	—	150	300	
Fall Time		t_f	—	170	340	
Gate Charge (See Figure 8)	(V_{DS} = 160 Vdc, I_D = 55 Adc, V_{GS} = 10 Vdc)	Q_T	—	245	343	nC
		Q_1	—	33	—	
		Q_2	—	128	—	
		Q_3	—	79	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 55 Adc, V_{GS} = 0 Vdc) (I_S = 55 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	0.75 1.1	1.2 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 55 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	310	—	ns
		t_a	—	220	—	
		t_b	—	90	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4.6	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

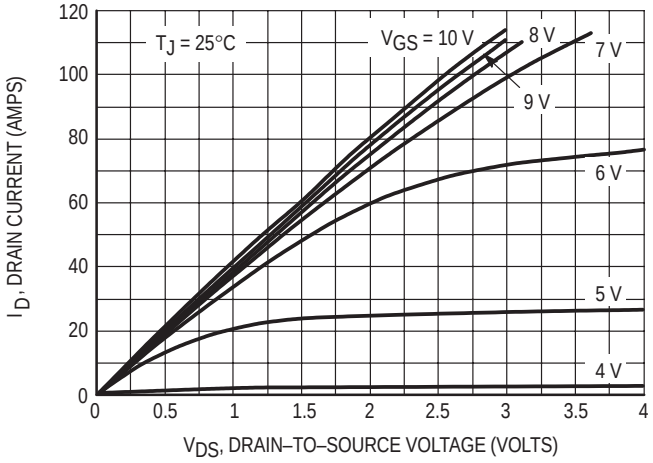


Figure 1. On–Region Characteristics

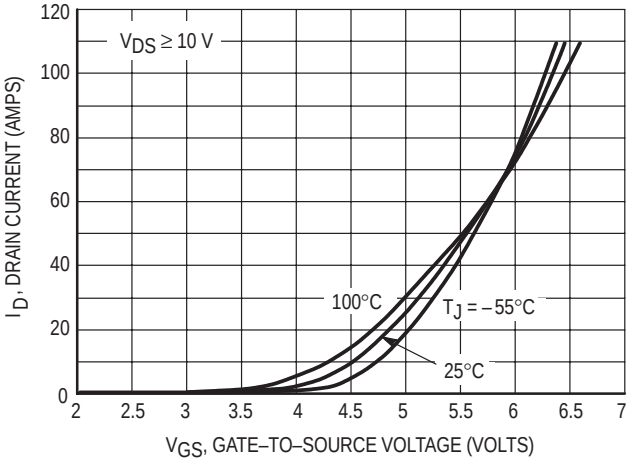


Figure 2. Transfer Characteristics

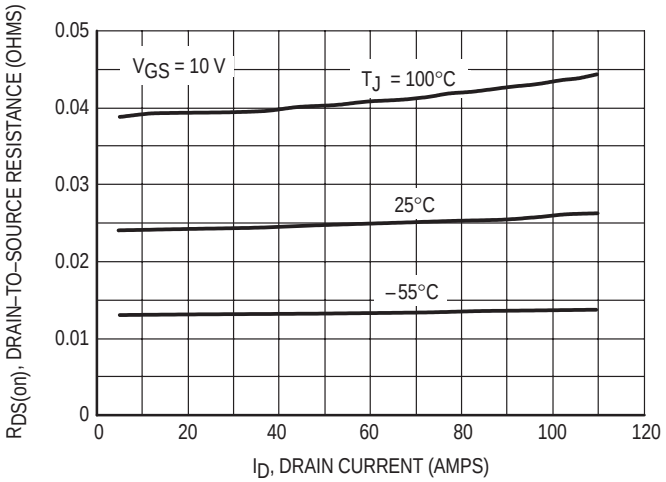


Figure 3. On–Resistance versus Drain Current and Temperature

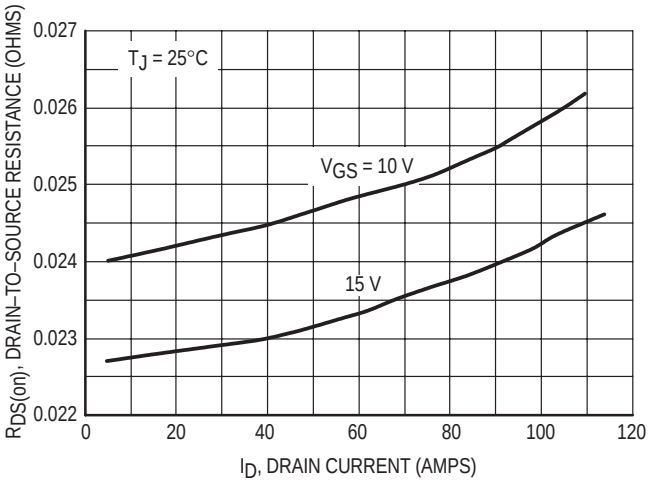


Figure 4. On–Resistance versus Drain Current and Gate Voltage

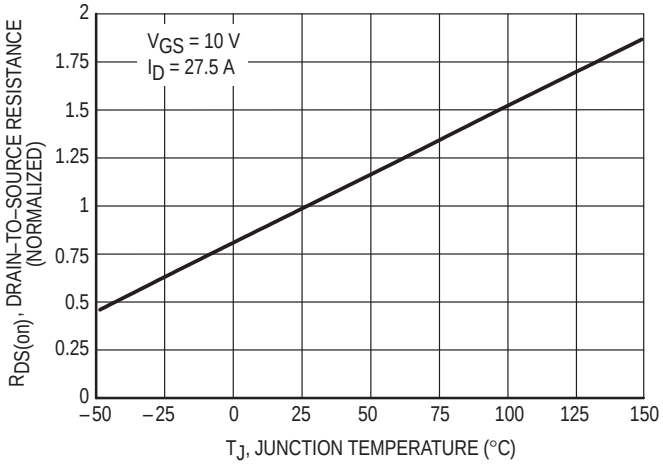


Figure 5. On–Resistance Variation with Temperature

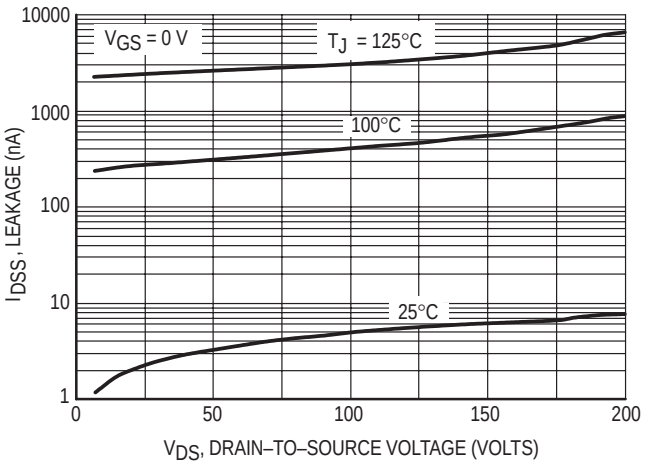


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

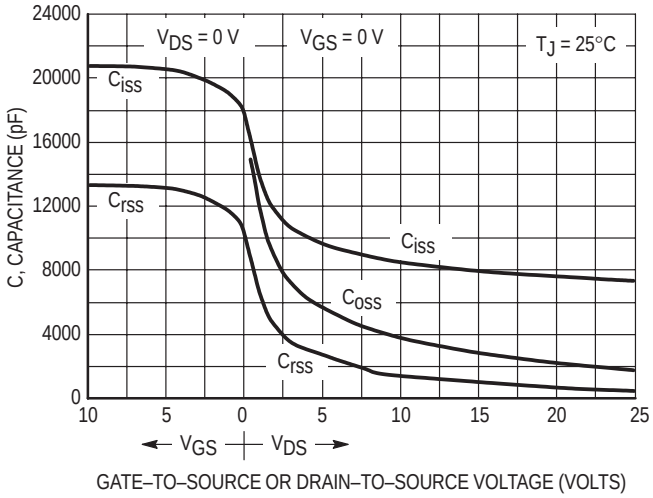


Figure 7. Capacitance Variation

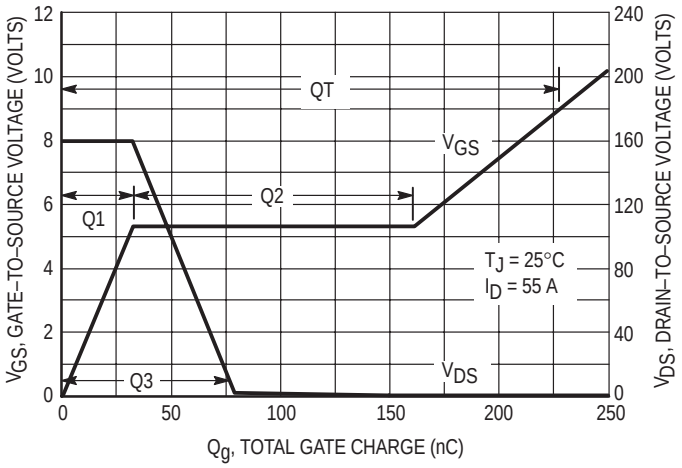


Figure 8. Gate Charge versus Gate–to–Source Voltage

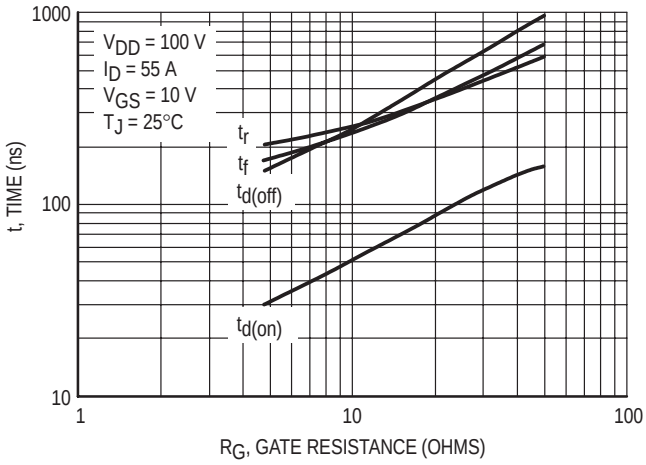


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

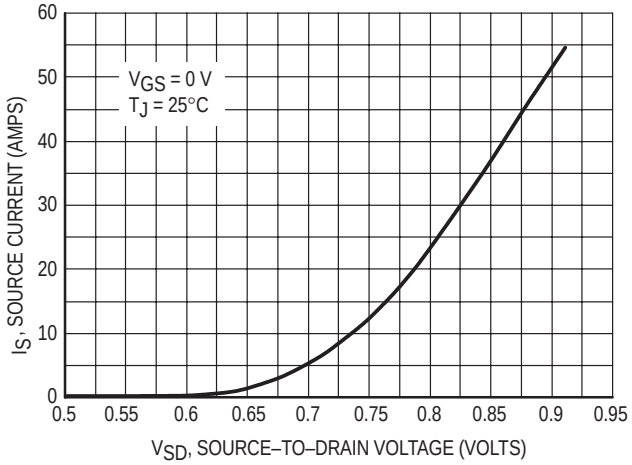


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

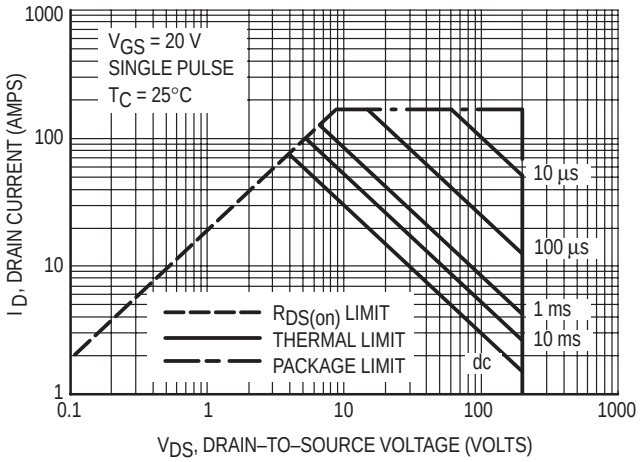


Figure 11. Maximum Rated Forward Biased Safe Operating Area

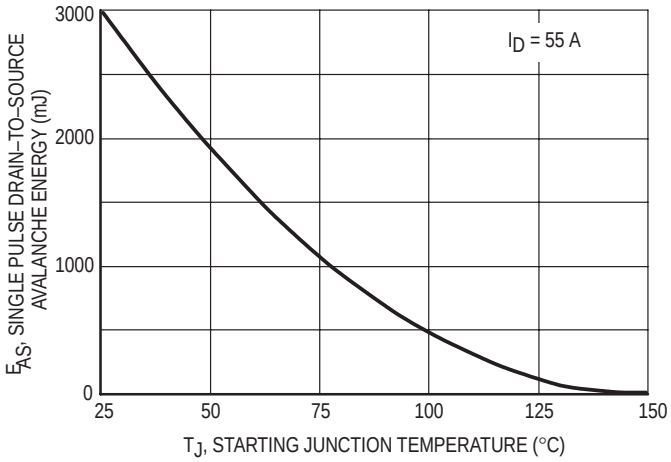


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

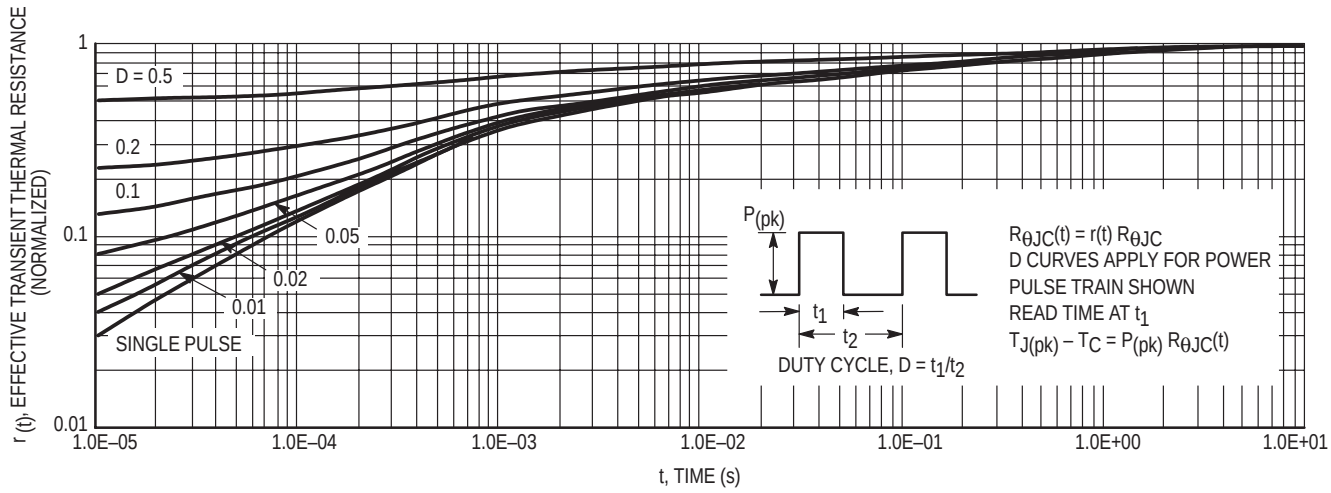


Figure 13. Thermal Response

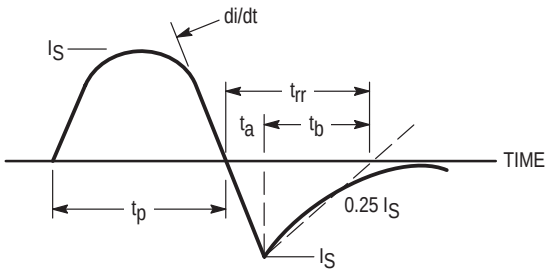


Figure 14. Diode Reverse Recovery Waveform

Designer's™ Data Sheet

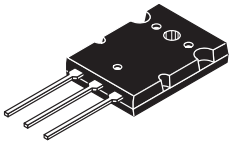
TMOS E-FET™
Power Field Effect Transistor
N–Channel Enhancement–Mode Silicon Gate

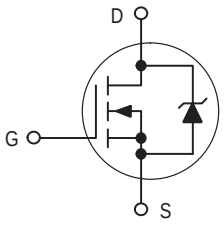
MTY100N10E
Motorola Preferred Device

TMOS POWER FET
100 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.011 OHM

This advanced TMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters, PWM motor controls, and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 340G–02, STYLE 1
TO–264

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	100	Vdc
Drain–Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	Vdc
Gate–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous @ T_C = 25°C — Single Pulse ($t_p \le 10$ μs)	I_D I_{DM}	100 300	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	300 2.38	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 80 Vdc, V_{GS} = 10 Vdc, Peak I_L = 100 Apk, L = 0.1 mH, R_G = 25 Ω)	E_{AS}	250	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.42 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–Source Breakdown Voltage (V_{GS} = 0, I_D = 250 μA) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	100 —	— 115	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		I_{DSS}	— —	— —	10 200	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	— 7	4 —	Vdc mV/°C
Static Drain–Source On–Resistance (V_{GS} = 10 Vdc, I_D = 50 Adc)		$R_{DS(on)}$	—	—	0.011	Ohm
Drain–Source On–Voltage (V_{GS} = 10 Vdc) (I_D = 100 Adc) (I_D = 50 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	1.0 —	1.2 1.0	Vdc
Forward Transconductance (V_{DS} = 6 Vdc, I_D = 50 Adc)		g_{FS}	30	49	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1 MHz)	C_{iss}	—	7600	10640	pF
Output Capacitance		C_{oss}	—	3300	4620	
Reverse Transfer Capacitance		C_{rss}	—	1200	2400	
SWITCHING CHARACTERISTICS (2)						
Turn–On Delay Time	(V_{DD} = 50 Vdc, I_D = 100 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω)	$t_{d(on)}$	—	48	96	ns
Rise Time		t_r	—	490	980	
Turn–Off Delay Time		$t_{d(off)}$	—	186	372	
Fall Time		t_f	—	384	768	
Gate Charge (See Figure 8)	(V_{DS} = 80 Vdc, I_D = 100 Adc, V_{GS} = 10 Vdc)	Q_T	—	270	378	nC
		Q_1	—	50	—	
		Q_2	—	150	—	
		Q_3	—	118	—	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 100 Adc, V_{GS} = 0 Vdc) (I_S = 100 Adc, V_{GS} = 0 Vdc, T_J = 125°C)	V_{SD}	— —	1 0.9	1.2 —	Vdc
Reverse Recovery Time (See Figure 14)	(I_S = 100 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs)	t_{rr}	—	145	—	ns
		t_a	—	90	—	
		t_b	—	55	—	
Reverse Recovery Stored Charge		Q_{RR}	—	2.34	—	μC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)		L_D	—	4.5	—	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

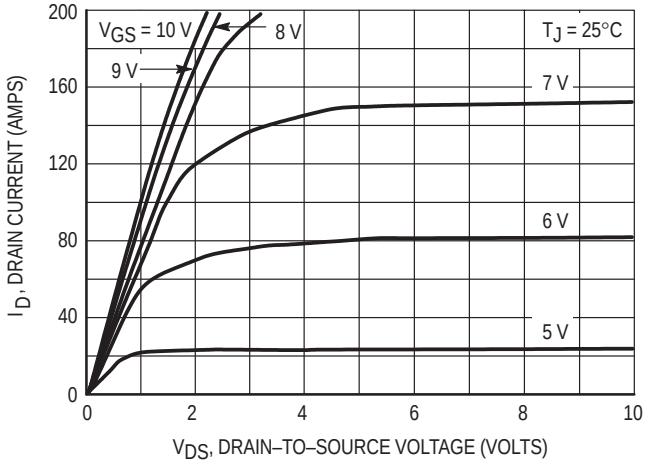


Figure 1. On–Region Characteristics

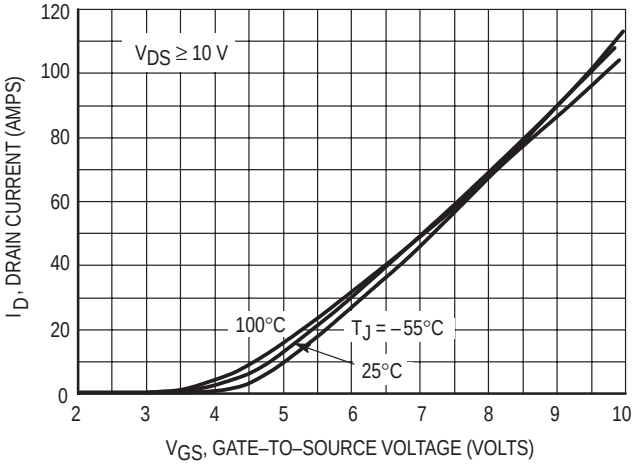


Figure 2. Transfer Characteristics

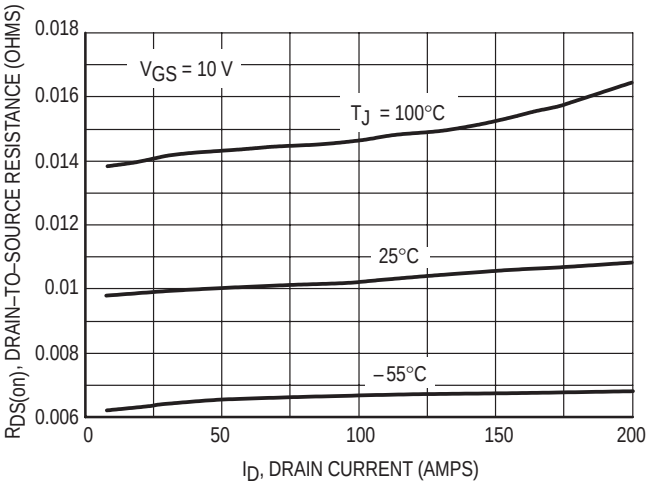


Figure 3. On–Resistance versus Drain Current and Temperature

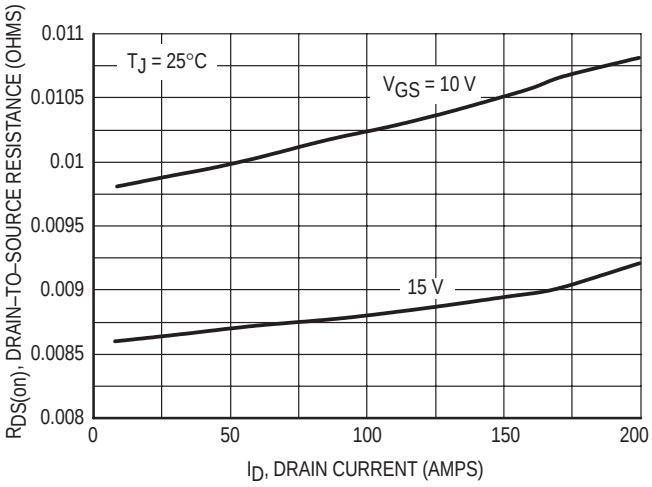


Figure 4. On–Resistance versus Drain Current and Gate Voltage

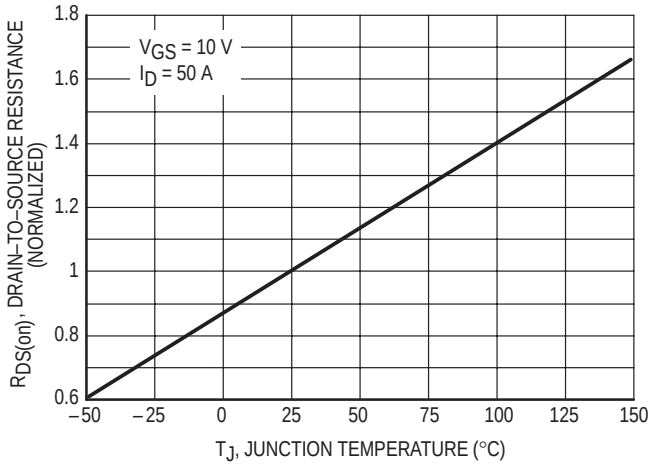


Figure 5. On–Resistance Variation with Temperature

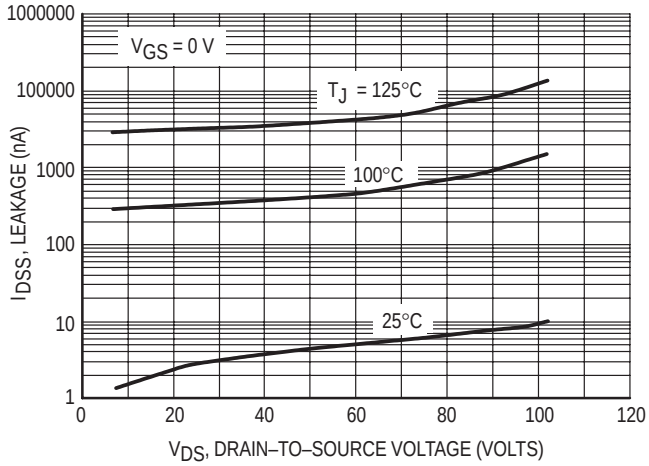


Figure 6. Drain–To–Source Leakage Current versus Voltage

POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, V_{GS} remains virtually constant at a level known as the plateau voltage, V_{SGP}. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

V_{GG} = the gate drive voltage, which varies from zero to V_{GG}

R_G = the gate drive resistance

and Q_2 and V_{GSP} are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance (C_{iss}) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

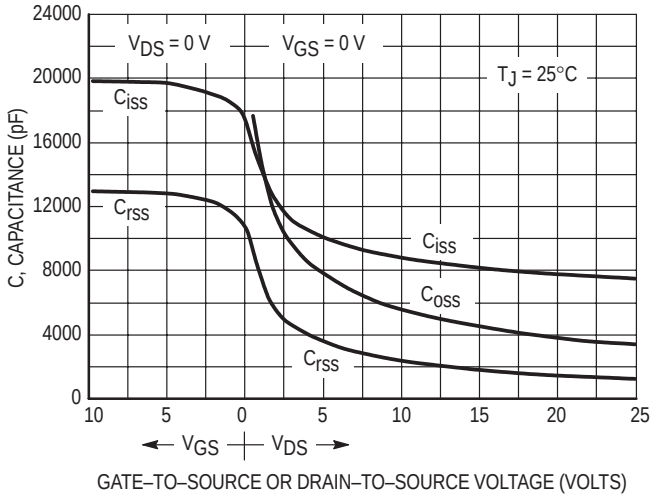


Figure 7. Capacitance Variation

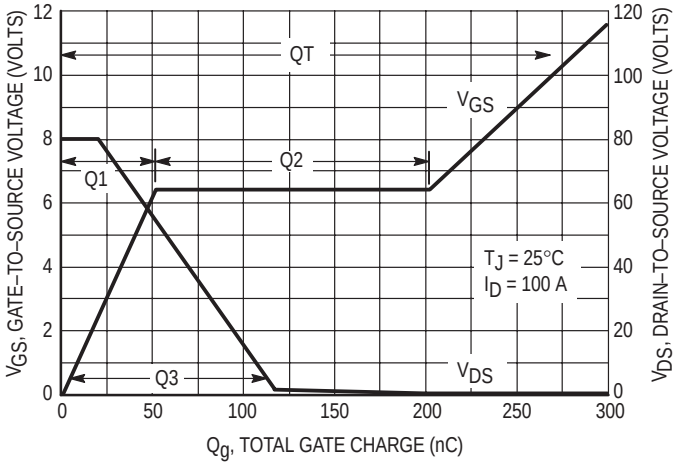


Figure 8. Gate Charge versus Gate–to–Source Voltage

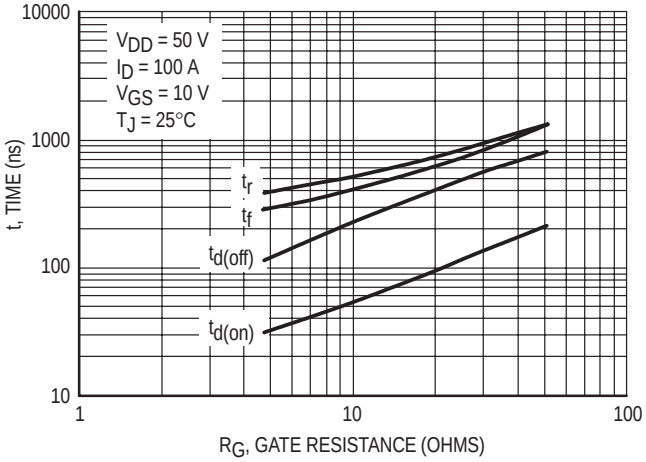


Figure 9. Resistive Switching Time Variation versus Gate Resistance

DRAIN–TO–SOURCE DIODE CHARACTERISTICS

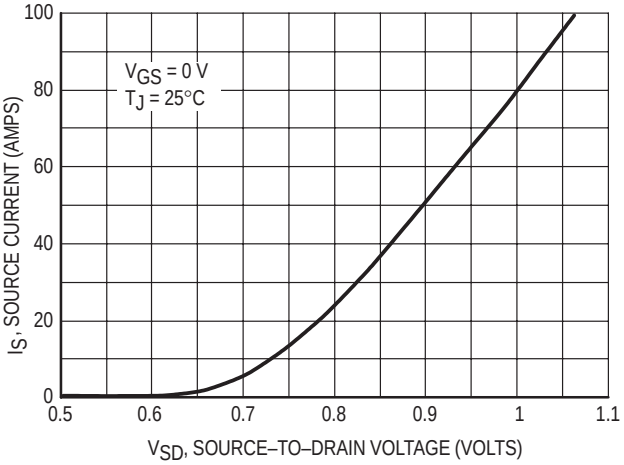


Figure 10. Diode Forward Voltage versus Current

SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature (T_C) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current (I_{DM}) nor rated voltage (V_{DSS}) is exceeded and the transition time (t_r,t_f) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current (I_{DM}), the energy rating is specified at rated continuous current (I_D), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous I_D can safely be assumed to equal the values indicated.

SAFE OPERATING AREA

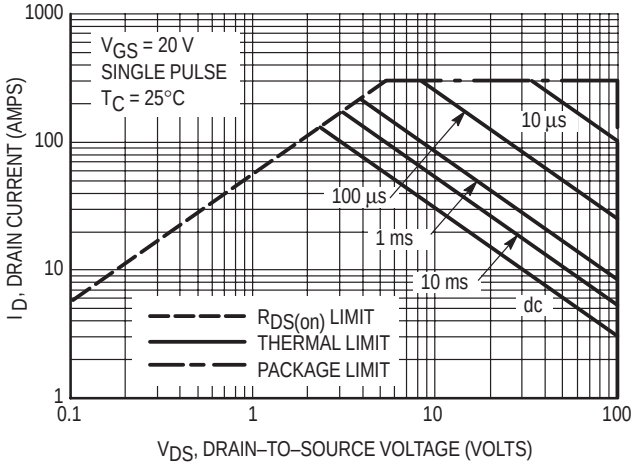


Figure 11. Maximum Rated Forward Biased Safe Operating Area

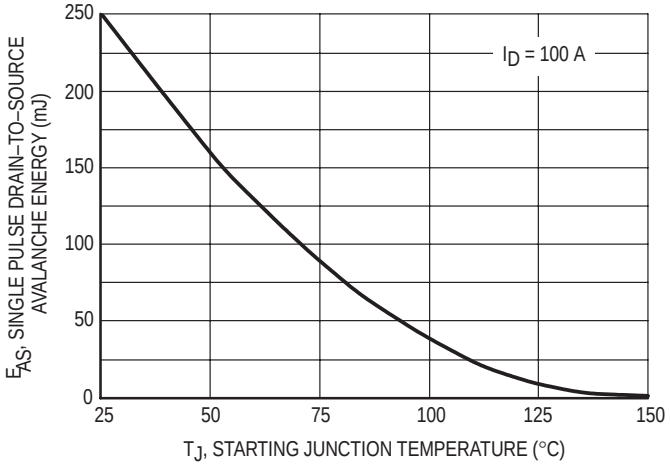


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

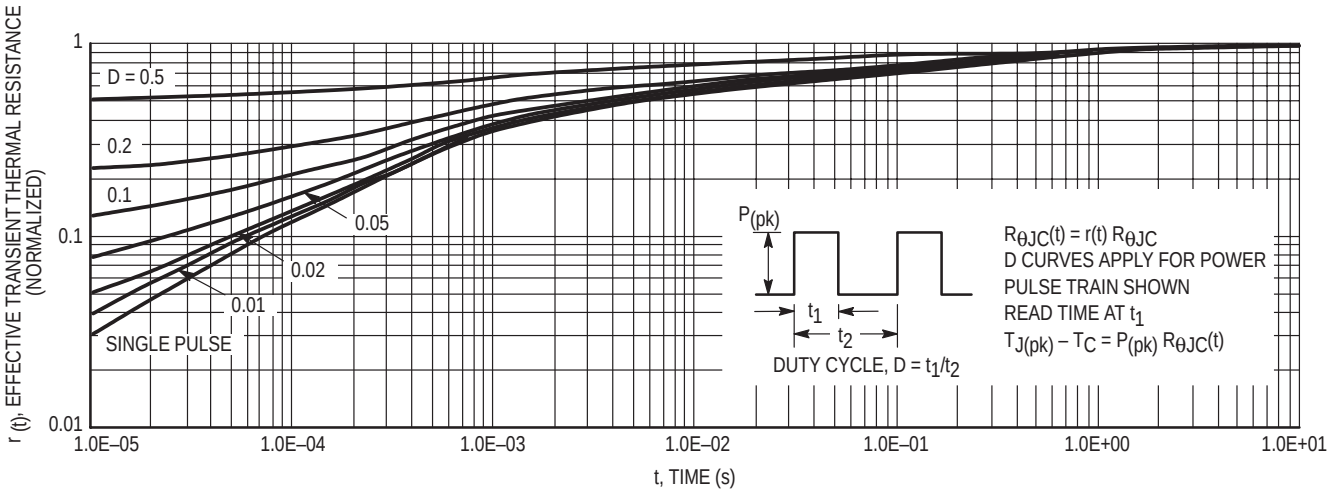


Figure 13. Thermal Response

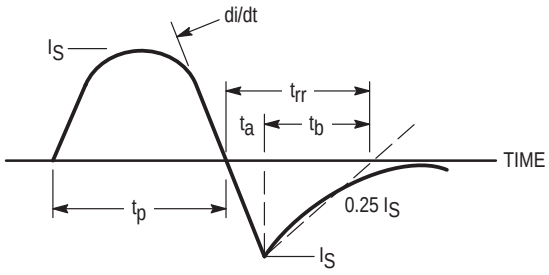


Figure 14. Diode Reverse Recovery Waveform

Section Five

Surface Mount Package Information Tape and Reel Specifications

Table of Contents

INFORMATION FOR USING SURFACE MOUNT PACKAGES

RECOMMENDED FOOTPRINTS FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain/collector pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device. For example, for a SOT–223 device, P_D is calculated as follows.

$$P_D = \frac{150°C - 25°C}{156°C/W} = 800 \text{ milliwatts}$$

The 156°C/W for the SOT–223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 800 milliwatts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain/collector pad. By increasing the area of the drain/collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figures 1, 2 and 3.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

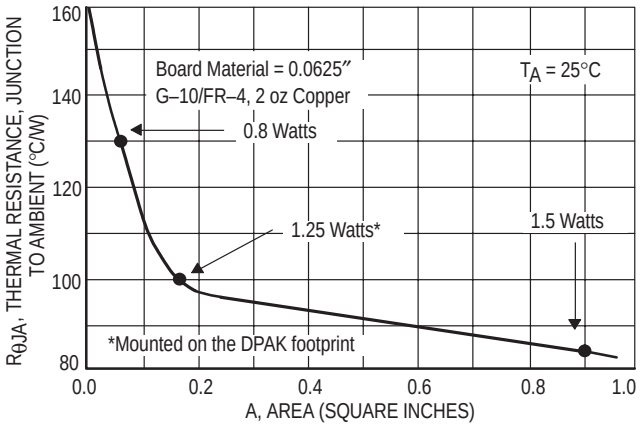


Figure 1. Thermal Resistance versus Drain Pad Area for the SOT–223 Package (Typical)

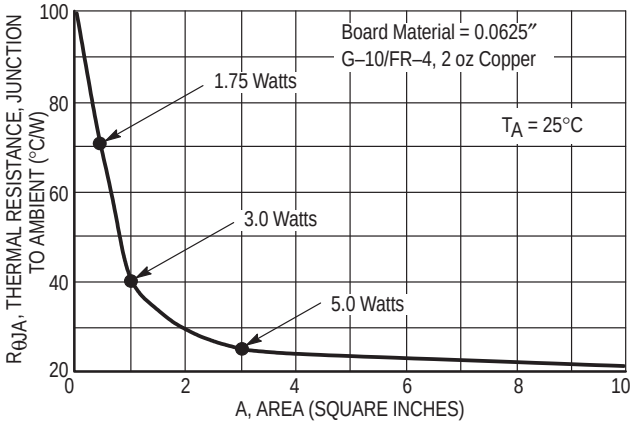


Figure 2. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)

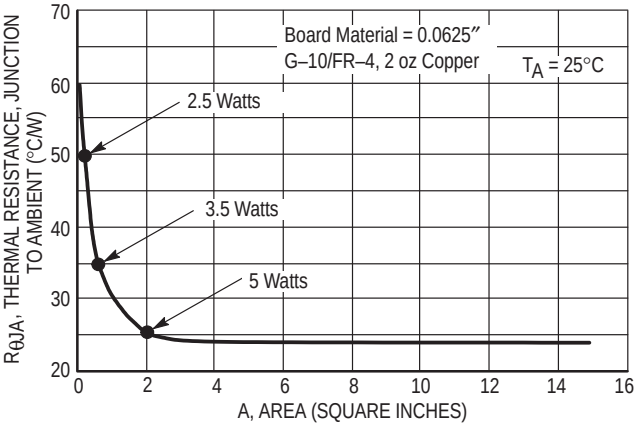


Figure 3. Thermal Resistance versus Drain Pad Area for the D²PAK Package (Typical)

SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SOT–223, SO–8 and Micro8, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK, D^2PAK and D^3PAK packages. If a 1:1 opening is used to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 4 shows a typical stencil for the DPAK, D^2PAK and D^3PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

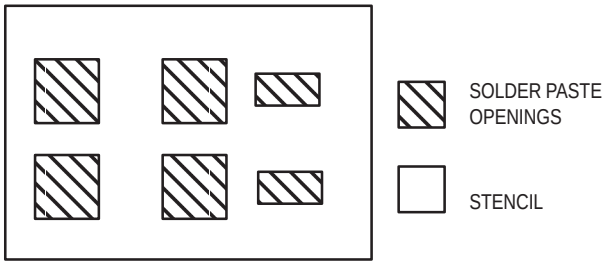


Figure 4. Typical Stencil for DPAK, D^2PAK and D^3PAK Packages

SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used since the use of forced cooling will increase the temperature gradient and will result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D^2PAK and D^3PAK are not recommended for wave soldering.

TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 5 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

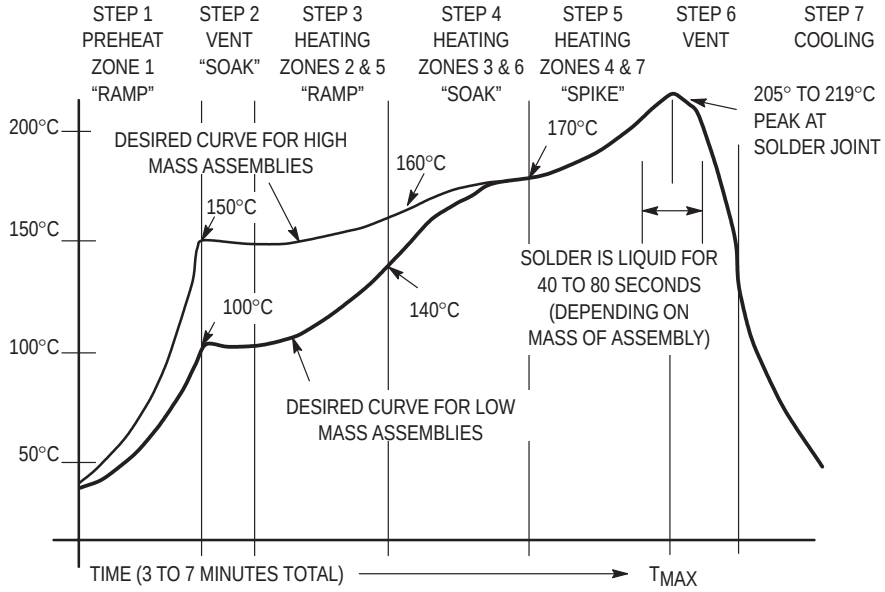
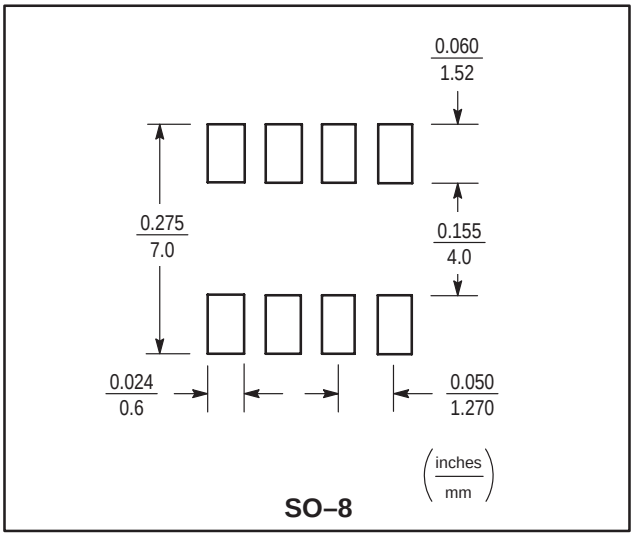
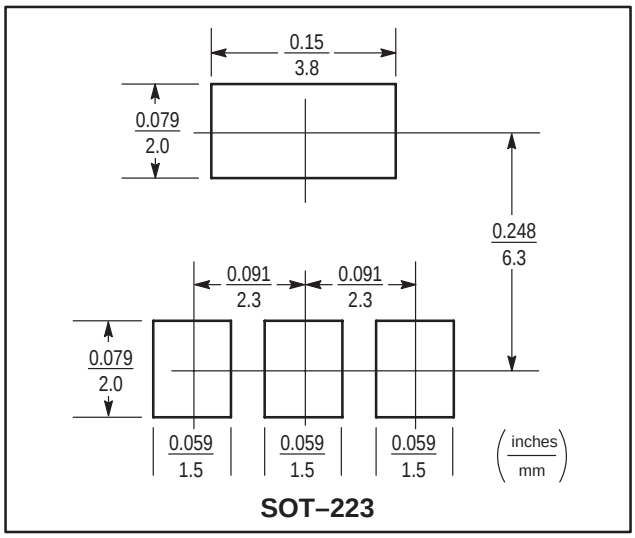


Figure 5. Typical Solder Heating Profile

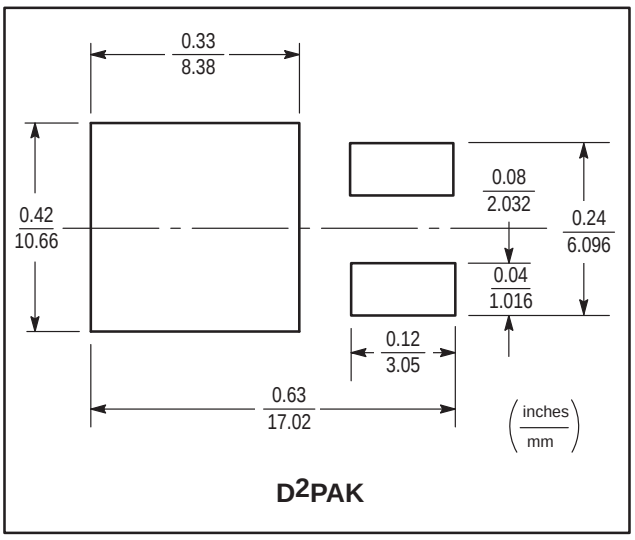
Footprints for Soldering



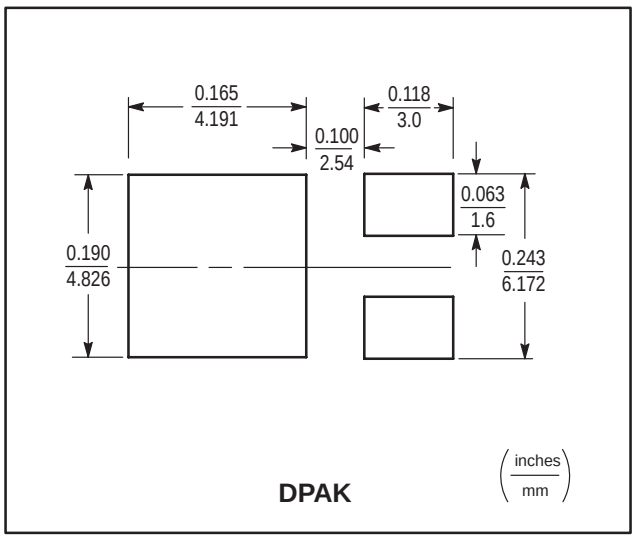
SO–8



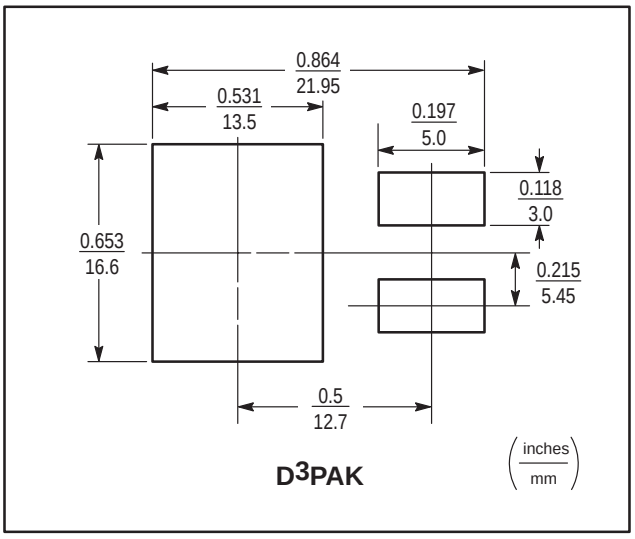
SOT–223



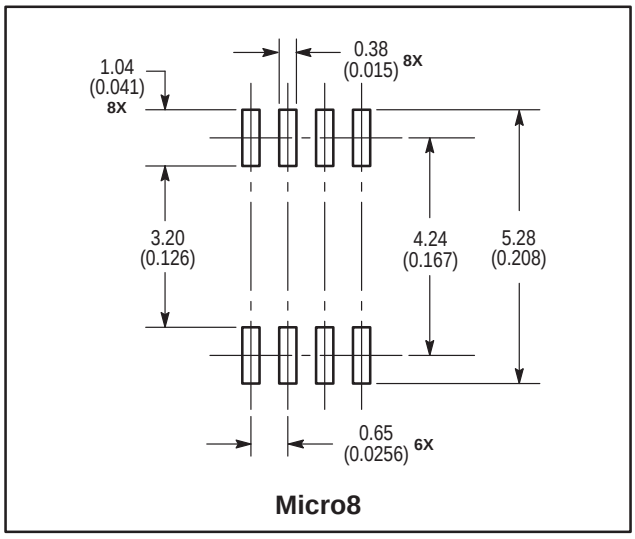
D^{2}PAK



DPAK



D^{3}PAK



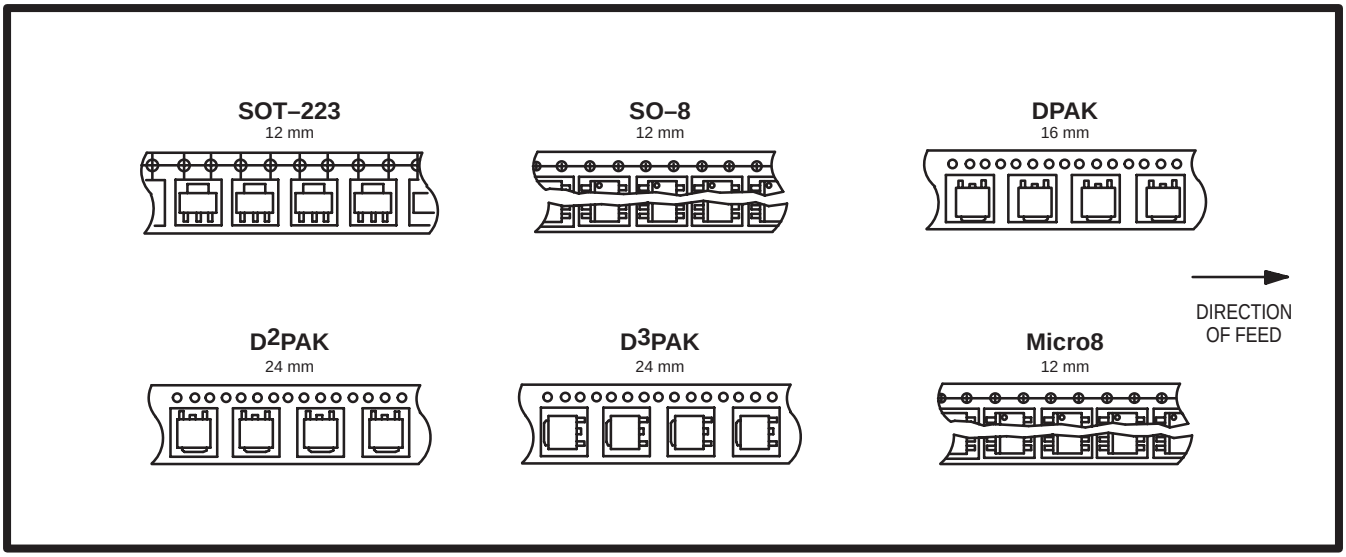
Micro8

Tape and Reel Specifications

Embossed Tape and Reel is used to facilitate automatic pick and place equipment feed requirements. The tape is used as the shipping container for various products and requires a minimum of handling. The antistatic/conductive tape provides a secure cavity for the product when sealed with the “peel–back” cover tape.

- Two Reel Sizes Available (7″ and 13″)
- Used for Automatic Pick and Place Feed Systems
- Minimizes Product Handling
- EIA 481, –1, –2
- Micro8, SO–8 and SOT–223 in 12 mm Tape
- DPAK in 16 mm Tape
- D^2PAK in 24 mm Tape
- D^3PAK in 24 mm Tape

Use the standard device title and add the required suffix as listed in the option table on the following page. Note that the individual reels have a finite number of devices depending on the type of product contained in the tape. Also note the minimum lot size is one full reel for each line item, and orders are required to be in increments of the single reel quantity.

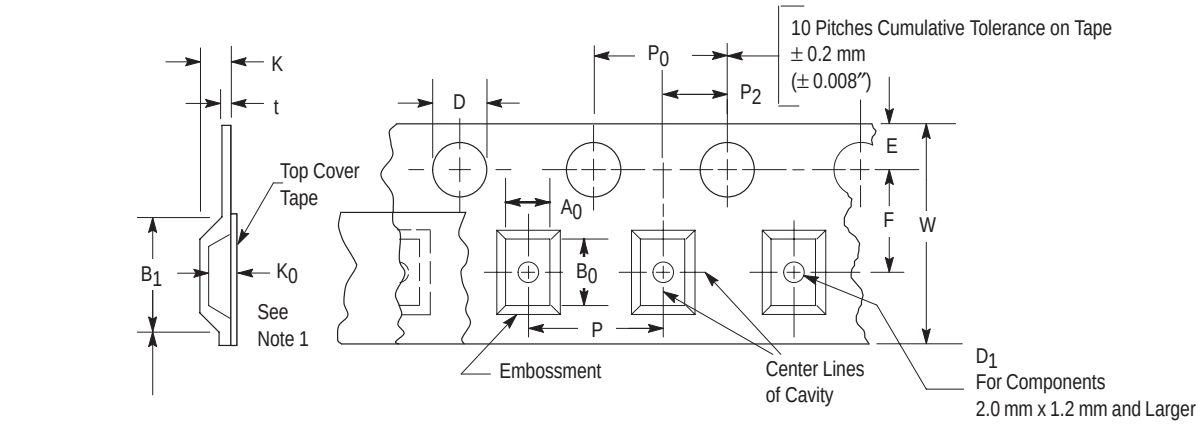


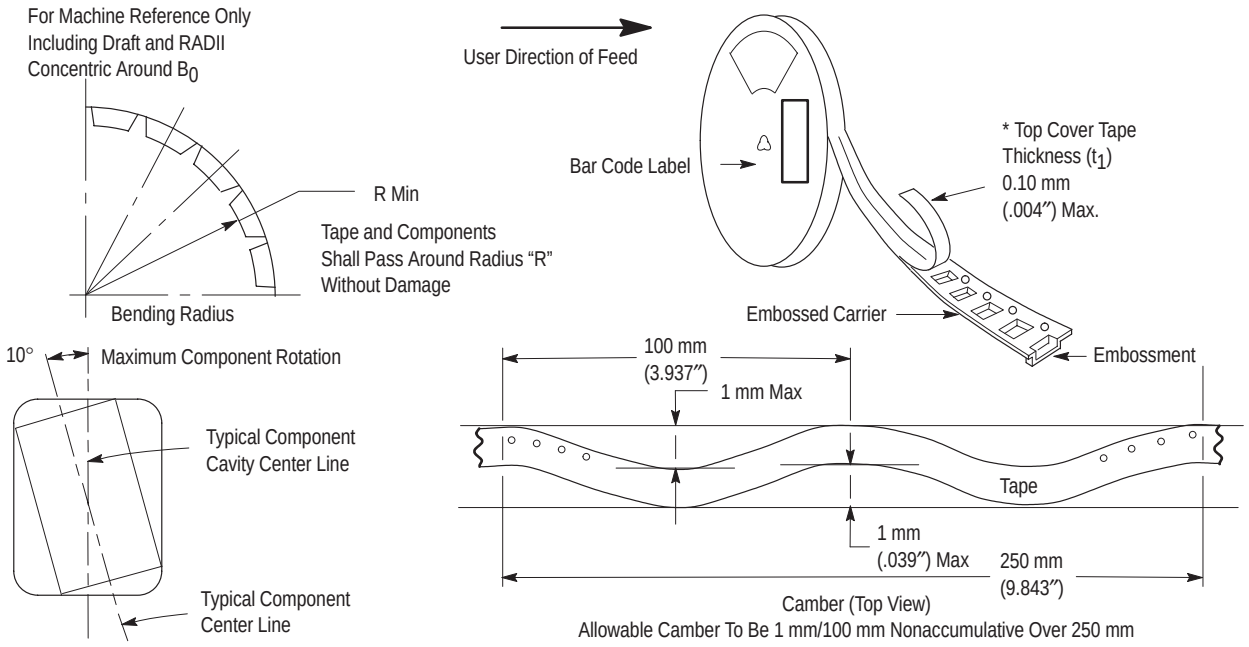
EMBOSSED TAPE AND REEL ORDERING INFORMATION

Package	Tape Width (mm)	Pitch mm (inch)	Reel Size mm (inch)	Devices Per Reel and Minimum Order Quantity	Device Suffix
DPAK	16	8.0 ± 0.1 (.315 ± .004)	330 (13)	2,500	T4
D^2PAK	24	16.0 ± 0.1 (.630 ± .004)	330 (13)	800	T4
D^3PAK	24	24.0 ± 0.1 (.944 ± .004)	330 (13)	500	RL
SO–8	12 12	8.0 ± 0.1 (.315 ± .004)	178 (7) 330 (13)	500 2,500	R1 R2
SOT–223	12 12	8.0 ± 0.1 (.315 ± .004)	178 (7) 330 (13)	1,000 4,000	T1 T3
Micro8	12	8.0 ± 0.1 (.315 ± .004)	330 (13)	4000	R2

EMBOSSED TAPE AND REEL DATA FOR DISCRETES

CARRIER TAPE SPECIFICATIONS





DIMENSIONS

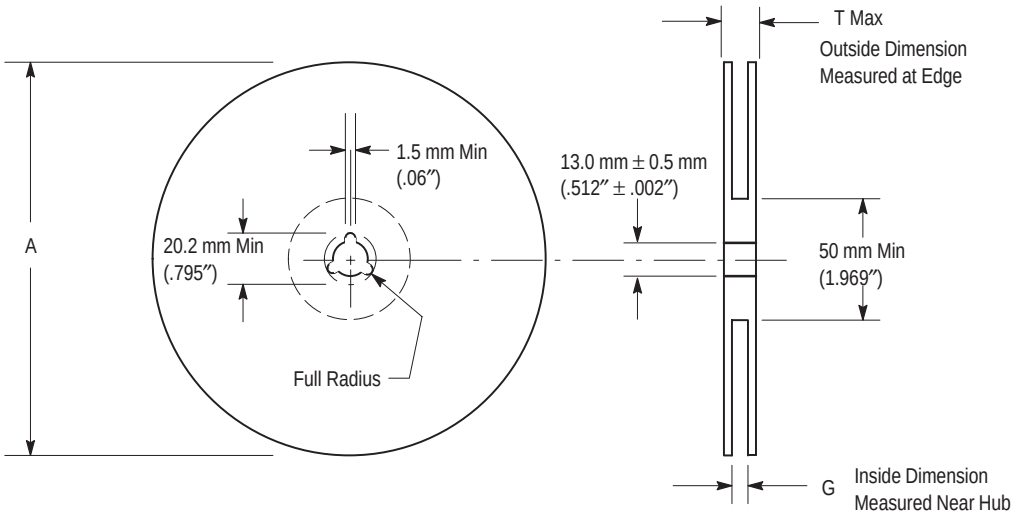
Tape Size	B_1 Max	D	D_1	E	F	K	P_0	P_2	R Min	T Max	W Max
12 mm	8.2 mm (.323″)	1.5 + 0.1 mm − 0.0 (.059 + .004″ − 0.0)	1.5 mm Min (.060″)	1.75 ± 0.1 mm (.069 ± .004″)	5.5 ± 0.05 mm (.217 ± .002″)	6.4 mm Max (.252″)	4.0 ± 0.1 mm (.157 ± .004″)	2.0 ± 0.1 mm (.079 ± .002″)	30 mm (1.18″)	0.6 mm (.024″)	12 ± .30 mm (.470 ± .012″)
16 mm	12.1 mm (.476″)				7.5 ± 0.10 mm (.295 ± .004″)	7.9 mm Max (.311″)					16.3 mm (.642″)
24 mm	20.1 mm (.791″)				11.5 ± 0.1 mm (.453 ± .004″)	11.9 mm Max (.468″)					24.3 mm (.957″)

Metric dimensions govern — English are in parentheses for reference only.

NOTE 1: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within .05 mm min. to .50 mm max., the component cannot rotate more than 10° within the determined cavity.

NOTE 2: Pitch information is contained in the Embossed Tape and Reel Ordering Information on pg. 5–6.

EMBOSSED TAPE AND REEL DATA FOR DISCRETES



Size	A Max	G	T Max
12 mm	330 mm (12.992″)	12.4 mm + 2.0 mm, –0.0 (.49″ + .079″, –0.00)	18.4 mm (.72″)
16 mm	360 mm (14.173″)	16.4 mm + 2.0 mm, –0.0 (.646″ + .078″, –0.00)	22.4 mm (.882″)
24 mm	360 mm (14.173″)	24.4 mm + 2.0 mm, –0.0 (.961″ + .070″, –0.00)	30.4 mm (1.197″)

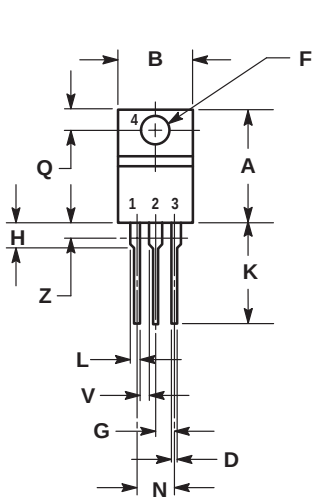
Reel Dimensions

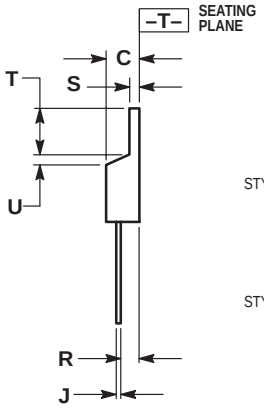
Metric Dimensions Govern — English are in parentheses for reference only

Section Six

Package Outline Dimensions and Footprints

Package Outline Dimensions and Footprints





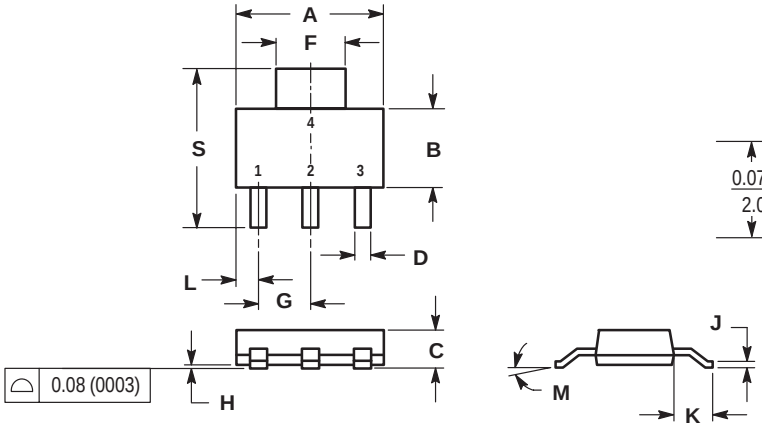
STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 221A–06
(TO–220AB)
ISSUE Y

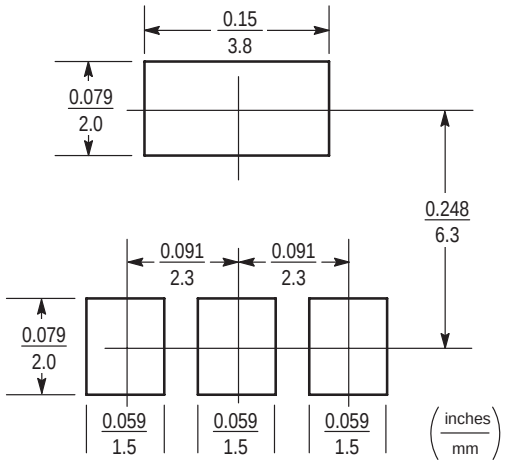
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04



STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

CASE 318E–04
(SOT–223)
ISSUE H

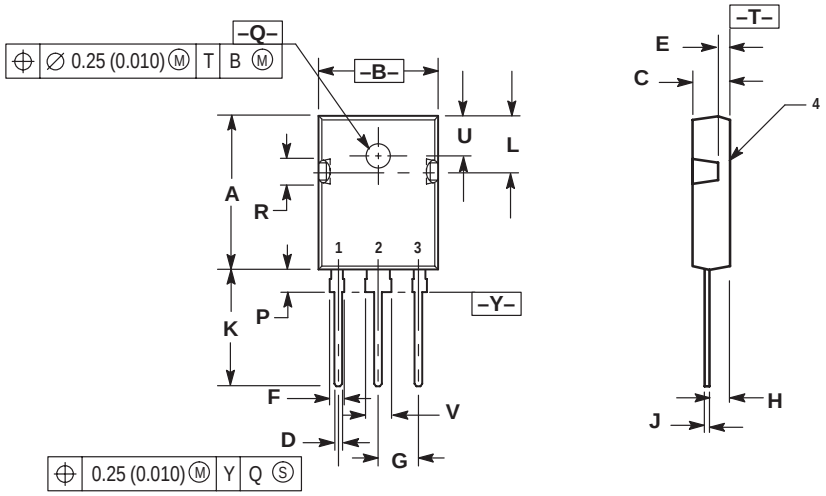


SOT–223 FOOTPRINT

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.249	0.263	6.30	6.70
B	0.130	0.145	3.30	3.70
C	0.060	0.068	1.50	1.75
D	0.024	0.035	0.60	0.89
F	0.115	0.126	2.90	3.20
G	0.087	0.094	2.20	2.40
H	0.0008	0.0040	0.020	0.100
J	0.009	0.014	0.24	0.35
K	0.060	0.078	1.50	2.00
L	0.033	0.041	0.85	1.05
M	0 °	10 °	0 °	10 °
S	0.264	0.287	6.70	7.30

PACKAGE OUTLINE DIMENSIONS AND FOOTPRINTS (continued)



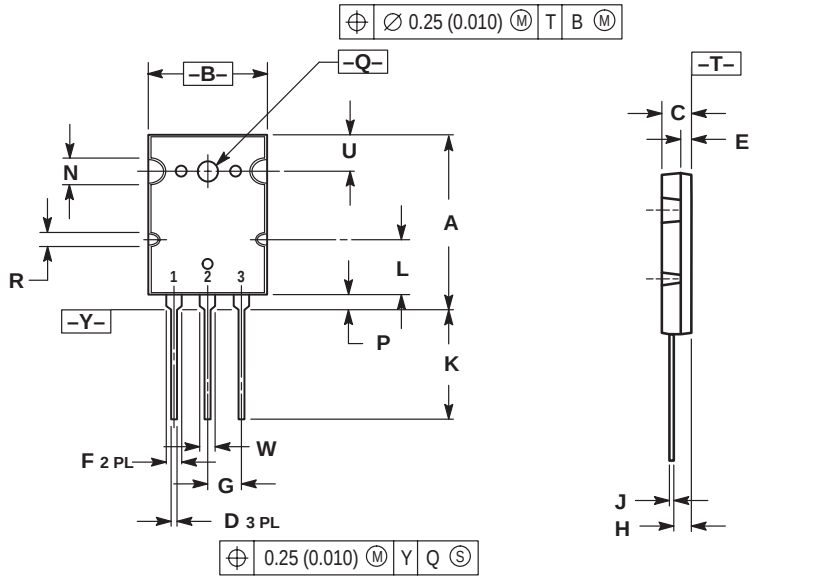
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.40	20.90	0.803	0.823
B	15.44	15.95	0.608	0.628
C	4.70	5.21	0.185	0.205
D	1.09	1.30	0.043	0.051
E	1.50	1.63	0.059	0.064
F	1.80	2.18	0.071	0.086
G	5.45 BSC		0.215 BSC	
H	2.56	2.87	0.101	0.113
J	0.48	0.68	0.019	0.027
K	15.57	16.08	0.613	0.633
L	7.26	7.50	0.286	0.295
P	3.10	3.38	0.122	0.133
Q	3.50	3.70	0.138	0.145
R	3.30	3.80	0.130	0.150
U	5.30 BSC		0.209 BSC	
V	3.05	3.40	0.120	0.134

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

CASE 340F–03
(TO–247)
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

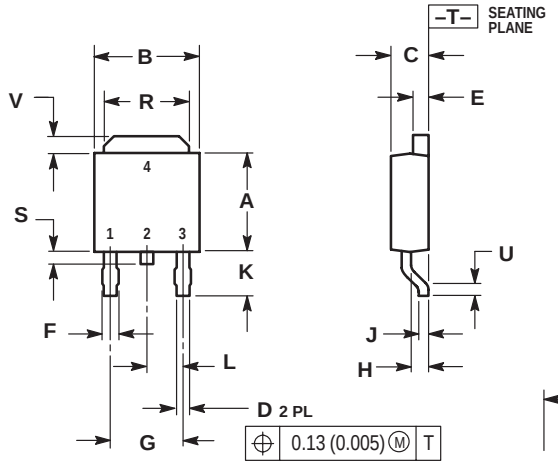
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.8	2.9	1.102	1.142
B	19.3	20.3	0.760	0.800
C	4.7	5.3	0.185	0.209
D	0.93	1.48	0.037	0.058
E	1.9	2.1	0.075	0.083
F	2.2	2.4	0.087	0.102
G	5.45 BSC		0.215 BSC	
H	2.6	3.0	0.102	0.118
J	0.43	0.78	0.017	0.031
K	17.6	18.8	0.693	0.740
L	11.0	11.4	0.433	0.449
N	3.95	4.75	0.156	0.187
P	2.2	2.6	0.087	0.102
Q	3.1	3.5	0.122	0.137
R	2.15	2.35	0.085	0.093
U	6.1	6.5	0.240	0.256
W	2.8	3.2	0.110	0.125

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 5:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

CASE 340G–02
(TO–264)
ISSUE E

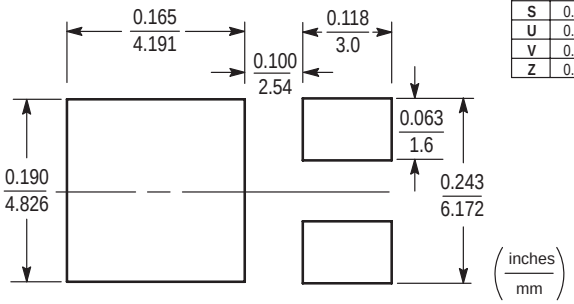
PACKAGE OUTLINE DIMENSIONS AND FOOTPRINTS (continued)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

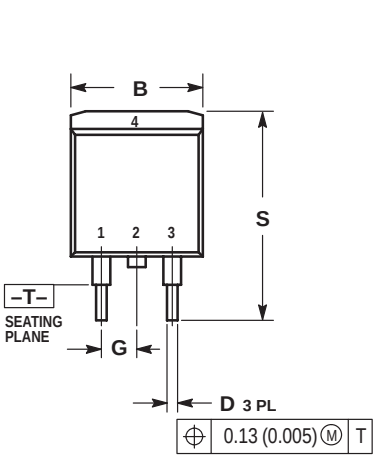
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	—	0.51	—
V	0.030	0.050	0.77	1.27
Z	0.138	—	3.51	—

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



DPAK FOOTPRINT

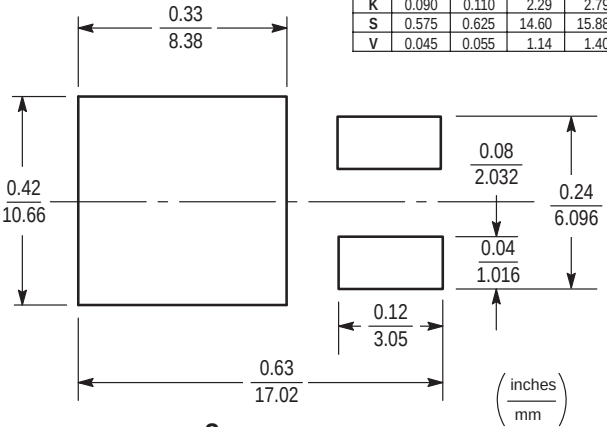
CASE 369A–13
(DPAK)
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

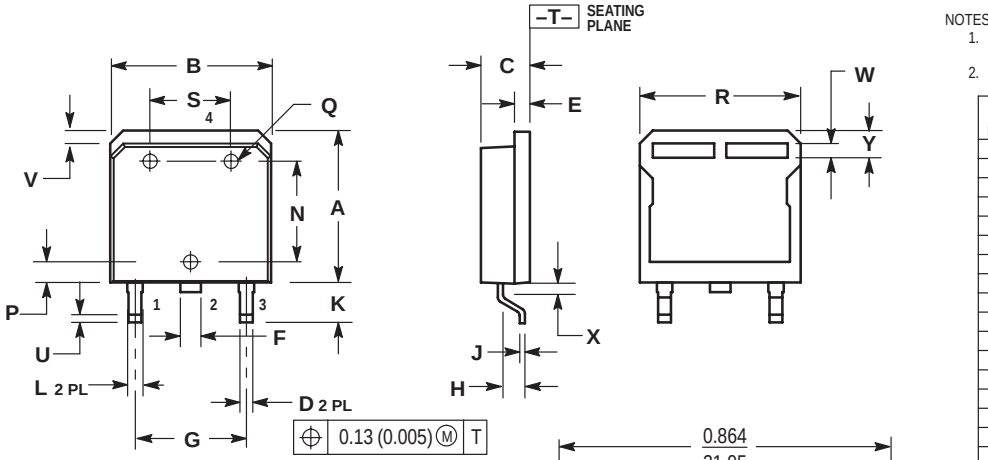
STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



CASE 418B–02
(D²PAK)
ISSUE B

D²PAK FOOTPRINT

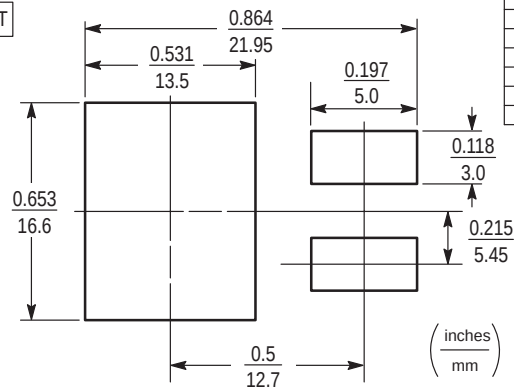
PACKAGE OUTLINE DIMENSIONS AND FOOTPRINTS (continued)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

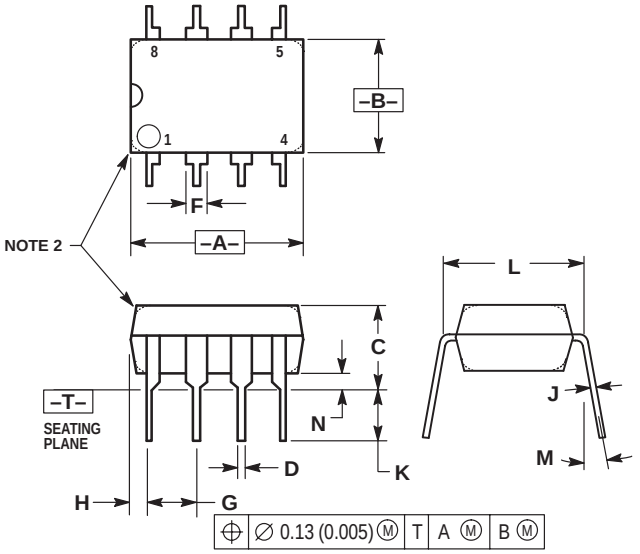
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.588	0.592	14.94	15.04
B	0.623	0.627	15.82	15.93
C	0.196	0.200	4.98	5.08
D	0.048	0.052	1.22	1.32
E	0.058	0.062	1.47	1.57
F	0.078	0.082	1.98	2.08
G	0.430 BSC		1.092 BSC	
H	0.105	0.110	2.67	2.79
J	0.018	0.022	0.46	0.56
K	0.150	0.160	3.81	4.06
L	0.058	0.062	1.47	1.57
N	0.353	0.357	8.97	9.07
P	0.078	0.082	1.98	2.08
Q	0.053	0.057	1.35	1.45
R	0.623	0.627	15.82	15.93
S	0.313	0.317	7.95	8.05
U	0.028	0.032	0.71	0.81
V	0.050	—	1.27	—
W	0.054	0.058	1.37	1.47
X	0.050	0.060	1.27	1.52
Y	0.104	0.108	2.64	2.74

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



D^{3}PAK FOOTPRINT

CASE 433–01
ISSUE B



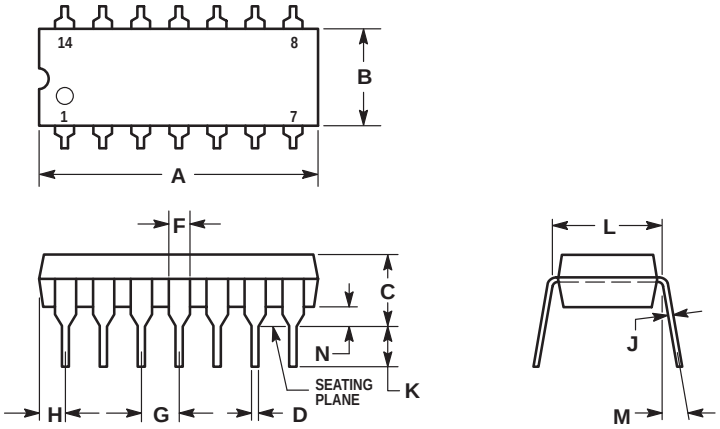
NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC – IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

CASE 626–05
ISSUE K

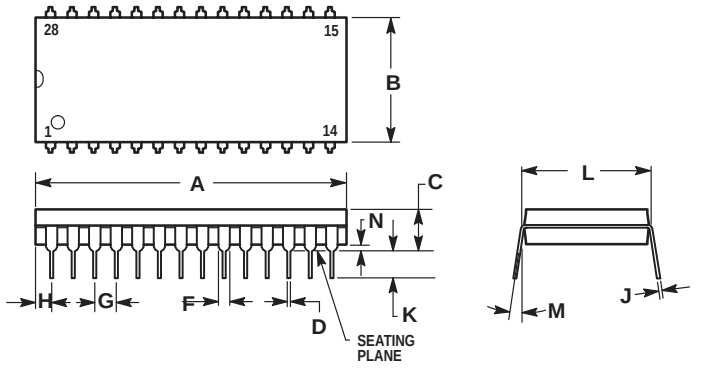
PACKAGE OUTLINE DIMENSIONS AND FOOTPRINTS (continued)



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

CASE 646–06
ISSUE L

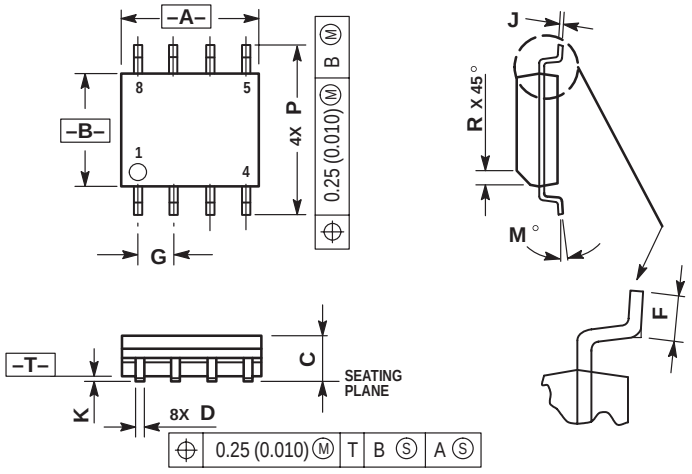


NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

CASE 710–02
ISSUE B

PACKAGE OUTLINE DIMENSIONS AND FOOTPRINTS (continued)



NOTES:
1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

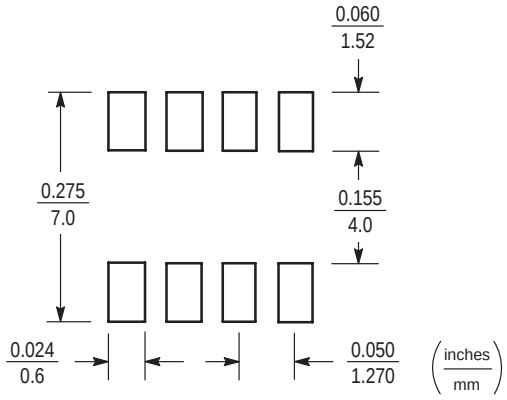
	MILLIMETERS	
DIM	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0 °	7 °
P	5.80	6.20
R	0.25	0.50

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

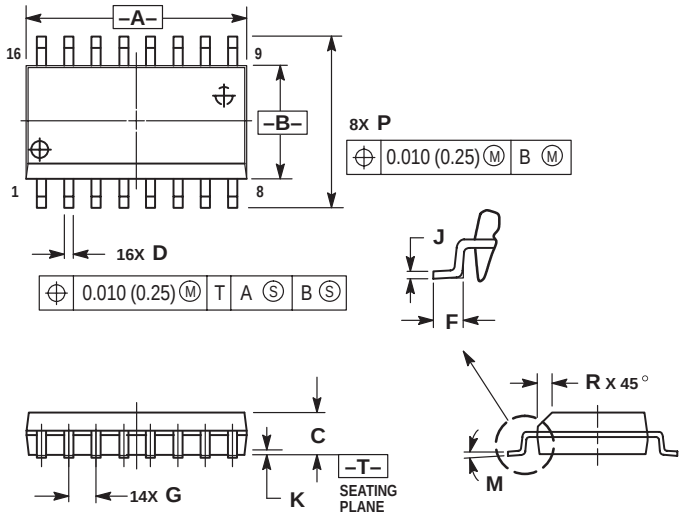
STYLE 14:
PIN 1. N–SOURCE
2. N–GATE
3. P–SOURCE
4. P–GATE
5. P–DRAIN
6. P–DRAIN
7. N–DRAIN
8. N–DRAIN



SO–8 FOOTPRINT

CASE 751–05
(SO–8)
ISSUE P

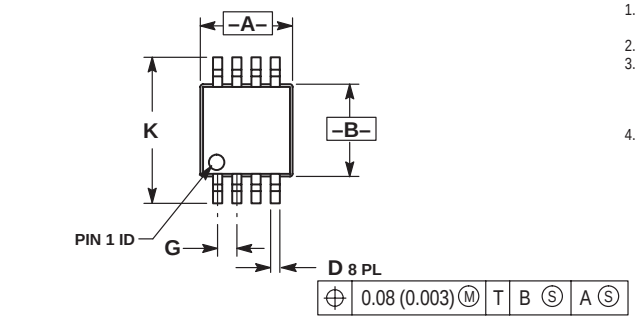
PACKAGE OUTLINE DIMENSIONS AND FOOTPRINTS (continued)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

CASE 751G–02
ISSUE A



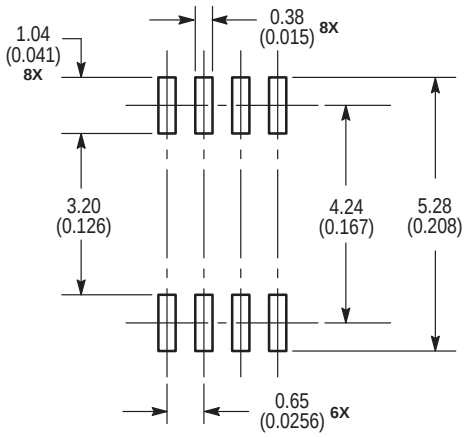
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION D DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	—	1.10	—	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

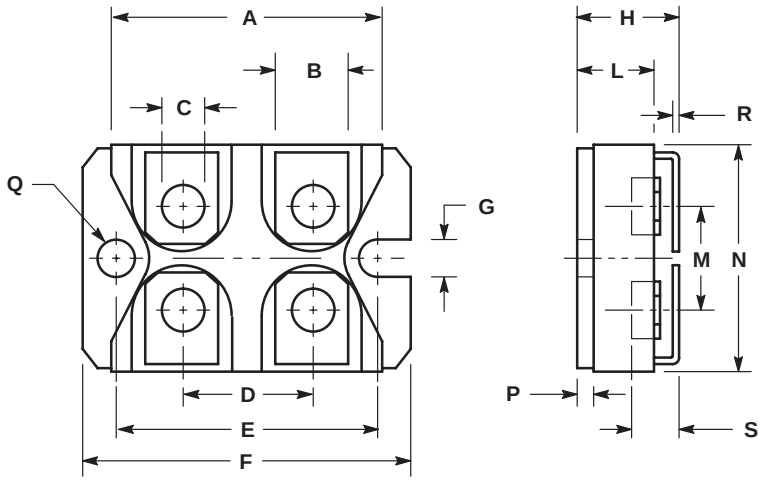
STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

CASE 846A–02
ISSUE B



MICRO8 FOOTPRINT



Recommended screw torque: 1.3 ± 0.2 Nm
Maximum screw torque: 1.5 Nm

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	31.50	31.70	1.240	1.248
B	7.80	8.20	0.307	0.322
C	4.10	4.30	0.161	0.169
D	14.90	15.10	0.586	0.590
E	30.10	30.30	1.185	1.193
F	38.00	38.20	1.496	1.503
G	4.00	—	0.157	—
H	11.80	12.20	0.464	0.480
L	8.90	9.10	0.350	0.358
M	12.60	12.80	0.496	0.503
N	25.20	25.40	0.992	1.000
P	1.95	2.05	0.076	0.080
Q	4.10	—	0.157	—
R	0.75	0.85	0.030	0.033
S	5.50	—	0.217	—

STYLE 1:
PIN 1. SOURCE
2. GATE
3. DRAIN
4. SOURCE 2

SOT–227B

Section Seven

Distributors and Sales Offices

MOTOROLA AUTHORIZED DISTRIBUTOR & WORLDWIDE SALES OFFICES

NORTH AMERICAN DISTRIBUTORS

UNITED STATES

ALABAMA

Huntsville
- Arrow/Schweber Electronics . . . (205)837–6955
- FAI . . . (205)837–9209
- Future Electronics . . . (205)830–2322
- Hamilton/Hallmark . . . (205)837–8700
- Newark . . . (205)837–9091
- Time Electronics . . . 1–800–789–TIME
- Wyle Electronics . . . (205)830–1119

ARIZONA

Phoenix
- FAI . . . (602)731–4661
- Future Electronics . . . (602)968–7140
- Hamilton/Hallmark . . . (602)414–3000
- Wyle Electronics . . . (602)804–7000

Tempe
- Arrow/Schweber Electronics . . . (602)431–0030
- Newark . . . (602)966–6340
- PENSTOCK . . . (602)967–1620
- Time Electronics . . . 1–800–789–TIME

CALIFORNIA

Agoura Hills
- Future Electronics . . . (818)865–0040
- Time Electronics Corporate . . 1–800–789–TIME

Belmont
- Richardson Electronics . . . (415)592–9225

Calabassas
- Arrow/Schweber Electronics . . . (818)880–9686
- Wyle Electronics . . . (818)880–9000

Chatsworth
- Time Electronics . . . 1–800–789–TIME

Costa Mesa
- Hamilton/Hallmark . . . (714)789–4100

Culver City
- Hamilton/Hallmark . . . (310)558–2000

Garden Grove
- Newark . . . (714–893–4909

Irvine
- Arrow/Schweber Electronics . . (714)587–0404
- FAI . . . (714)753–4778
- Future Electronics . . . (714)453–1515
- Wyle Laboratories Corporate . . . (714)753–9953
- Wyle Electronics . . . (714)863–9953

Los Angeles
- FAI . . . (818)879–1234
- Wyle Electronics . . . (818)880–9000

Manhattan Beach
- PENSTOCK . . . (310)546–8953

Mountain View
- Richardson Electronics . . . (415)960–6900

Newberry Park
- PENSTOCK . . . (805)375–6680

Palo Alto
- Newark . . . (415)812–6300

Riverside
- Newark . . . (909)784–1101

Rocklin
- Hamilton/Hallmark . . . (916)632–4500

Sacramento
- FAI . . . (916)782–7882
- Newark . . . (916)565–1760
- Wyle Electronics . . . (916)638–5282

San Diego
- Arrow/Schweber Electronics . . (619)565–4800
- FAI . . . (619)623–2888
- Future Electronics . . . (619)625–2800
- Hamilton/Hallmark . . . (619)571–7540
- Newark . . . (619)453–8211
- PENSTOCK . . . (619)623–9100
- Wyle Electronics . . . (619)565–9171

San Jose
- Arrow/Schweber Electronics . . . (408)441–9700
- Arrow/Schweber Electronics . . . (408)428–6400
- FAI . . . (408)434–0369
- Future Electronics . . . (408)434–1122

Santa Clara
- Wyle Electronics . . . (408)727–2500

Sierra Madre
- PENSTOCK . . . (818)355–6775

Sunnyvale
- Hamilton/Hallmark . . . (408)435–3500
- PENSTOCK . . . (408)730–0300
- Time Electronics . . . 1–800–789–TIME

Thousand Oaks
- Newark . . . (805)449–1480

Torrance
- Time Electronics . . . 1–800–789–TIME

Tustin
- Time Electronics . . . 1–800–789–TIME

Woodland Hills
- Hamilton/Hallmark . . . (818)594–0404
- Richardson Electronics . . . (615)594–5600

COLORADO

Lakewood
- FAI . . . (303)237–1400
- Future Electronics . . . (303)232–2008

Denver
- Newark . . . (303)373–4540

Englewood
- Arrow/Schweber Electronics . . . (303)799–0258
- Hamilton/Hallmark . . . (303)790–1662
- PENSTOCK . . . (303)799–7845
- Time Electronics . . . 1–800–789–TIME

Thornton
- Wyle Electronics . . . (303)457–9953

CONNECTICUT

Bloomfield
- Newark . . . (203)243–1731

Cheshire
- FAI . . . (203)250–1319
- Future Electronics . . . (203)250–0083
- Hamilton/Hallmark . . . (203)271–2844

Southbury
- Time Electronics . . . 1–800–789–TIME

Wallingfort
- Arrow/Schweber Electronics . . . (203)265–7741

FLORIDA

Altamonte Springs
- Future Electronics . . . (407)865–7900

Clearwater
- FAI . . . (813)530–1665
- Future Electronics . . . (813)530–1222

Deerfield Beach
- Arrow/Schweber Electronics . . . (305)429–8200
- Wyle Electronics . . . (305)420–0500

Ft. Lauderdale
- FAI . . . (305)428–9494
- Future Electronics . . . (305)436–4043
- Hamilton/Hallmark . . . (305)484–5482
- Newark . . . (305)486–1151
- Time Electronics . . . 1–800–789–TIME

Lake Mary
- Arrow/Schweber Electronics . . . (407)333–9300

Largo/Tampa/St. Petersburg
- Hamilton/Hallmark . . . (813)547–5000
- Newark . . . (813)287–1578
- Wyle Electronics . . . (813)576–3004
- Time Electronics . . . 1–800–789–TIME

Orlando
- FAI . . . (407)865–9555

Tallahassee
- FAI . . . (904)668–7772

Tampa
- PENSTOCK . . . (813)247–7556

Winter Park
- Hamilton/Hallmark . . . (407)657–3300
- PENSTOCK . . . (407)672–1114
- Richardson Electronics . . . (407)644–1453

GEORGIA

Atlanta
- FAI . . . (404)447–4767
- Time Electronics . . . 1–800–789–TIME
- Wyle Electronics . . . (404)441–9045

Duluth
- Arrow/Schweber Electronics . . . (404)497–1300
- Hamilton/Hallmark . . . (404)623–4400

Norcross
- Future Electronics . . . (770)441–7676
- Newark . . . (770)448–1300
- PENSTOCK . . . (770)734–9990
- Wyle Electronics . . . (770)441–9045

IDAHO

Boise
- FAI . . . (208)376–8080

ILLINOIS

Addison
- Wyle Laboratories . . . (708)620–0969

Bensenville
- Hamilton/Hallmark . . . (708)797–7322

Chicago
- FAI . . . (708)843–0034
- Newark Electronics Corp. . . . . (312)784–5100

Hoffman Estates
- Future Electronics . . . (708)882–1255

Itasca
- Arrow/Schweber Electronics . . (708)250–0500

LaFox
- Richardson Electronics . . . (708)208–2401

Palatine
- PENSTOCK . . . (708)934–3700

Schaumburg
- Newark . . . (708)310–8980
- Time Electronics . . . 1–800–789–TIME

INDIANA

Indianapolis
- Arrow/Schweber Electronics . . . (317)299–2071
- Hamilton/Hallmark . . . (317)575–3500
- FAI . . . (317)469–0441
- Future Electronics . . . (317)469–0447
- Newark . . . (317)259–0085
- Time Electronics . . . 1–800–789–TIME

Ft. Wayne
- Newark . . . (219)484–0766
- PENSTOCK . . . (219)432–1277

IOWA

Cedar Rapids
- Newark . . . (319)393–3800
- Time Electronics . . . 1–800–789–TIME

KANSAS

Kansas City
- FAI . . . (913)381–6800

Lenexa
- Arrow/Schweber Electronics . . . (913)541–9542
- Hamilton/Hallmark . . . (913)663–7900

Olathe
- PENSTOCK . . . (913)829–9330

Overland Park
- Future Electronics . . . (913)649–1531
- Newark . . . (913)677–0727
- Time Electronics . . . 1–800–789–TIME

MARYLAND

Baltimore
- FAI . . . (410)312–0833

Columbia
- Arrow/Schweber Electronics . . . (301)596–7800
- Future Electronics . . . (410)290–0600
- Hamilton/Hallmark . . . (410)720–3400
- Time Electronics . . . 1–800–789–TIME
- PENSTOCK . . . (410)290–3746
- Wyle Electronics . . . (410)312–4844

Hanover
- Newark . . . (410)712–6922

AUTHORIZED DISTRIBUTORS – continued

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Boston
Arrow/Schweber Electronics . . . (508)658–0900
FAI . . . . . (508)779–3111
Bolton
Future Corporate . . . . . (508)779–3000
Burlington
PENSTOCK . . . . . (617)229–9100
Wyle Electronics . . . . . (617)271–9953
Norwell
Richardson Electronics . . . . . (617)871–5162
Peabody
Time Electronics 1–800–789–TIME
Hamilton/Hallmark . . . . . (508)532–9893
Woburn
Newark . . . . . (617)935–8350

MICHIGAN
Detroit
FAI . . . . . (313)513–0015
Future Electronics . . . . . (616)698–6800
Grand Rapids
Newark . . . . . (616)954–6700
Livonia
Arrow/Schweber Electronics . . . (810)455–0850
Future Electronics . . . . . (313)261–5270
Hamilton/Hallmark . . . . . (313)416–5800
Time Electronics 1–800–789–TIME
Troy
Newark . . . . . (810)583–2899

MINNESOTA
Bloomington
Wyle Electronics . . . . . (612)853–2280
Burnsville
PENSTOCK . . . . . (612)882–7630
Eden Prairie
Arrow/Schweber Electronics . . . (612)941–5280
FAI . . . . . (612)947–0909
Future Electronics . . . . . (612)944–2200
Hamilton/Hallmark . . . . . (612)881–2600
Time Electronics 1–800–789–TIME
Minneapolis
Newark . . . . . (612)331–6350
Earth City
Hamilton/Hallmark . . . . . (314)291–5350

MISSOURI
St. Louis
Arrow/Schweber Electronics . . . (314)567–6888
Future Electronics . . . . . (314)469–6805
FAI . . . . . (314)542–9922
Newark . . . . . (314)453–9400
Time Electronics 1–800–789–TIME

NEW JERSEY
Bridgewater
PENSTOCK . . . . . (908)575–9490
Cherry Hill
Hamilton/Hallmark . . . . . (609)424–0110
East Brunswick
Newark . . . . . (908)937–6600
Fairfield
FAI . . . . . (201)331–1133
Long Island
FAI . . . . . (516)348–3700
Marlton
Arrow/Schweber Electronics . . . (609)596–8000
FAI . . . . . (609)988–1500
Future Electronics . . . . . (609)596–4080
Pinebrook
Arrow/Schweber Electronics . . . (201)227–7880
Wyle Electronics . . . . . (201)882–8358
Parsippany
Future Electronics . . . . . (201)299–0400
Hamilton/Hallmark . . . . . (201)515–1641
Wayne
Time Electronics 1–800–789–TIME

NEW MEXICO
Albuquerque
Alliance Electronics . . . . . (505)292–3360
Hamilton/Hallmark . . . . . (505)828–1058
Newark . . . . . (505)828–1878

NEW YORK
Bohemia
Newark . . . . . (516)567–4200
Hauppauge
Arrow/Schweber Electronics . . . (516)231–1000
Future Electronics . . . . . (516)234–4000
Hamilton/Hallmark . . . . . (516)434–7400
PENSTOCK . . . . . (516)724–9580
Konkoma
Hamilton/Hallmark . . . . . (516)737–0600
Melville
Wyle Laboratories . . . . . (516)293–8446
Pittsford
Newark . . . . . (716)381–4244
Rochester
Arrow/Schweber Electronics . . . (716)427–0300
Future Electronics . . . . . (716)387–9550
FAI . . . . . (716)387–9600
Hamilton/Hallmark . . . . . (716)272–2740
Richardson Electronics . . . . . (716)264–1100
Time Electronics 1–800–789–TIME
Rockville Centre
Richardson Electronics . . . . . (516)872–4400
Syracuse
FAI . . . . . (315)451–4405
Future Electronics . . . . . (315)451–2371
Newark . . . . . (315)457–4873
Time Electronics 1–800–789–TIME

NORTH CAROLINA
Charlotte
FAI . . . . . (704)548–9503
Future Electronics . . . . . (704)547–1107
Richardson Electronics . . . . . (704)548–9042
Raleigh
Arrow/Schweber Electronics . . . (919)876–3132
FAI . . . . . (919)876–0088
Future Electronics . . . . . (919)790–7111
Hamilton/Hallmark . . . . . (919)872–0712
Newark . . . . . (919)781–7677
Time Electronics 1–800–789–TIME

OHIO
Centerville
Arrow/Schweber Electronics . . . (513)435–5563
Cleveland
FAI . . . . . (216)446–0061
Newark . . . . . (216)391–9330
Time Electronics 1–800–789–TIME
Columbus
Newark . . . . . (614)326–0352
Time Electronics 1–800–789–TIME
Dayton
FAI . . . . . (513)427–6090
Future Electronics . . . . . (513)426–0090
Hamilton/Hallmark . . . . . (513)439–6735
Newark . . . . . (513)294–8980
Time Electronics 1–800–789–TIME
Mayfield Heights
Future Electronics . . . . . (216)449–6996
Solon
Arrow/Schweber Electronics . . . (216)248–3990
Hamilton/Hallmark . . . . . (216)498–1100
Worthington
Hamilton/Hallmark . . . . . (614)888–3313

OKLAHOMA
Tulsa
FAI . . . . . (918)492–1500
Hamilton/Hallmark . . . . . (918)459–6000
Newark . . . . . (918)252–5070

OREGON
Beaverton
Arrow/Almac Electronics Corp. . (503)629–8090
Future Electronics . . . . . (503)645–9454
Hamilton/Hallmark . . . . . (503)526–6200
Wyle Electronics . . . . . (503)643–7900
Portland
FAI . . . . . (503)297–5020
Newark . . . . . (503)297–1984
PENSTOCK . . . . . (503)646–1670
Time Electronics 1–800–789–TIME

PENNSYLVANIA
Coatesville
PENSTOCK . . . . . (610)383–9536
Ft. Washington
Newark . . . . . (215)654–1434
Mt. Laurel
Wyle Electronics . . . . . (609)439–9110
Montgomeryville
Richardson Electronics . . . . . (215)628–0805
Philadelphia
Time Electronics 1–800–789–TIME
Wyle Electronics . . . . . (609)439–9110
Pittsburgh
Arrow/Schweber Electronics . . . (412)963–6807
Newark . . . . . (412)788–4790
Time Electronics 1–800–789–TIME

TENNESSEE
Franklin
Richardson Electronics . . . . . (615)791–4900
Knoxville
Newark . . . . . (615)588–6493

TEXAS
Austin
Arrow/Schweber Electronics . . . (512)835–4180
Future Electronics . . . . . (512)502–0991
FAI . . . . . (512)346–6426
Hamilton/Hallmark . . . . . (512)219–3700
Newark . . . . . (512)338–0287
PENSTOCK . . . . . (512)346–9762
Time Electronics 1–800–789–TIME
Wyle Electronics . . . . . (512)833–9953
Benbrook
PENSTOCK . . . . . (817)249–0442
Carollton
Arrow/Schweber Electronics . . . (214)380–6464
Dallas
FAI . . . . . (214)231–7195
Future Electronics . . . . . (214)437–2437
Hamilton/Hallmark . . . . . (214)553–4300
Newark . . . . . (214)458–2528
Richardson Electronics . . . . . (214)239–3680
Time Electronics 1–800–789–TIME
Wyle Electronics . . . . . (214)235–9953
El Paso
FAI . . . . . (915)577–9531
Ft. Worth
Allied Electronics . . . . . (817)336–5401
Houston
Arrow/Schweber Electronics . . . (713)647–6868
FAI . . . . . (713)952–7088
Future Electronics . . . . . (713)785–1155
Hamilton/Hallmark . . . . . (713)781–6100
Newark . . . . . (713)894–9334
Time Electronics 1–800–789–TIME
Wyle Electronics . . . . . (713)879–9953
Richardson
PENSTOCK . . . . . (214)479–9215
San Antonio
FAI . . . . . (210)738–3330

UTAH
Salt Lake City
Arrow/Schweber Electronics . . . (801)973–6913
FAI . . . . . (801)467–9696
Future Electronics . . . . . (801)467–4448
Hamilton/Hallmark . . . . . (801)266–2022
Newark . . . . . (801)261–5660
Wyle Electronics . . . . . (801)974–9953
West Valley City
Time Electronics 1–800–789–TIME
Wyle Electronics . . . . . (801)974–9953

AUTHORIZED DISTRIBUTORS – continued

UNITED STATES – continued

WASHINGTON

Bellevue
- Almac Electronics Corp. ..... (206)643–9992
- Newark ..... (206)641–9800
- PENSTOCK ..... (206)454–2371
- Richardson Electronics ..... (206)646–7224

Bothell
- Future Electronics ..... (206)489–3400

Redmond
- Hamilton/Hallmark ..... (206)882–7000
- Time Electronics 1–800–789–TIME
- Wyle Electronics ..... (206)881–1150

Seattle
- FAI ..... (206)485–6616
- Wyle Electronics ..... (206)881–1150

WISCONSIN

Brookfield
- Arrow/Schweber Electronics ... (414)792–0150
- Future Electronics ..... (414)879–0244
- Wyle Electronics ..... (414)521–9333

Milwaukee
- FAI ..... (414)792–9778
- Time Electronics 1–800–789–TIME

New Berlin
- Hamilton/Hallmark ..... (414)780–7200

Wauwatosa
- Newark ..... (414)453–9100

CANADA

ALBERTA

Calgary
- Electro Sonic Inc. ..... (403)255–9550
- FAI ..... (403)291–5333

BRITISH COLUMBIA
- Future Electronics ..... (403)250–5550
- Hamilton/Hallmark ..... (800)663–5500

Edmonton
- FAI ..... (403)438–5888
- Future Electronics ..... (403)438–2858
- Hamilton/Hallmark ..... (800)663–5500

Saskatchewan
- Hamilton/Hallmark ..... (800)663–5500

Vancouver
- Arrow Electronics ..... (604)421–2333
- Electro Sonic Inc. ..... (604)273–2911
- FAI ..... (604)654–1050
- Future Electronics ..... (604)294–1166
- Hamilton/Hallmark ..... (604)420–4101

MANITOBA

Winnipeg
- Electro Sonic Inc. ..... (204)783–3105
- FAI ..... (204)786–3075
- Future Electronics ..... (204)944–1446
- Hamilton/Hallmark ..... (800)663–5500

ONTARIO

Kanata
- PENSTOCK ..... (613)592–6088

Mississauga
- PENSTOCK ..... (905)403–0724

Ottawa
- Arrow Electronics ..... (613)226–6903
- Electro Sonic Inc. ..... (613)728–8333
- FAI ..... (613)820–8244
- Future Electronics ..... (613)820–8313
- Hamilton/Hallmark ..... (613)226–1700

Toronto
- Arrow Electronics ..... (905)670–7769
- Electro Sonic Inc. ..... (416)494–1666
- FAI ..... (905)612–9888
- Future Electronics ..... (905)612–9200
- Hamilton/Hallmark ..... (905)564–6060
- Newark ..... (905)670–2888
- Richardson Electronics ..... (905)795–6300

QUEBEC

Montreal
- Arrow Electronics ..... (514)421–7411
- FAI ..... (514)694–8157
- Future Electronics ..... (514)694–7710
- Hamilton/Hallmark ..... (514)335–1000
- Richardson Electronics ..... (514)748–1770

Quebec City
- Arrow Electronics ..... (418)687–4231
- FAI ..... (418)682–5775
- Future Electronics ..... (418)877–6666

INTERNATIONAL DISTRIBUTORS

AUSTRALIA
- AVNET VSI Electronics (Australia) ..... (61)2 878–1299
- Veltek Australia Pty Ltd ..... (61)3 9574–9300

AUSTRIA
- EBV Austria ..... (43) 1 8941774
- Elbatex GmbH ..... (43) 1 866420
- Spoerle Austria ..... (43) 1 31872700

BELGIUM
- Diode Spoerle ..... (32) 2 725 4660
- EBV Belgium ..... (32) 2 716 0010

CHINA
- Advanced Electronics Ltd. ... (852)2 305–3633
- AVNET WKK Components Ltd. (852)2 357–8888
- China El. App. Corp. Xiamen Co ..... (86)592 513–2489
- Nanco Electronics Supply Ltd. ..... (852) 2 333–5121
- Qing Cheng Enterprises Ltd. (852) 2 493–4202

DENMARK
- Arrow Exatec ..... (45) 44 927000
- Avnet Nortec A/S ..... (45) 44 880800
- EBV Denmark ..... (45) 39690511

ESTONIA
- Arrow Field Eesti ..... (372) 6503288
- Avnet Baltronic ..... (372) 6397000

FINLAND
- Arrow Field OY ..... (35) 807 775 71
- Avnet Nortec OY ..... (35) 806 13181

FRANCE
- Arrow Electronique ..... (33) 1 49 78 49 78
- Avnet Components ..... (33) 1 49 65 25 00
- EBV France ..... (33) 1 64 68 86 00
- Future Electronics ..... (33)1 69821111
- Newark ..... (33)1–30954060
- SEI/Scaib ..... (33) 1 69 19 89 00

GERMANY
- Avnet E2000 ..... (49) 89 4511001
- EBV Elektronik GmbH ..... (49) 89 99114–0
- Future Electronics GmbH ... (49) 89–957 270
- Jermyn GmbH ..... (49) 6431–5080
- Newark ..... (49)2154–70011
- Sasco Semiconductor ..... (49) 89–46110
- Spoerle Electronic ..... (49) 6103–304–0

HOLLAND
- EBV Holland ..... (31) 3465 623 53
- Diode Spoerle BV ..... (31) 4054 5430

HONG KONG
- AVNET WKK Components Ltd. (852)2 357–8888
- Nanshing Clr. & Chem. Co. Ltd (852)2 333–5121

INDIA
- Canyon Products Ltd ..... (91) 80 558–7758

INDONESIA
- P.T. Ometraco ..... (62) 21 619–6166

ITALY
- Avnet Adelsy SpA ..... (39) 2 381901
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