# Fractional-*N* Frequency Synthesis: Overview and Practical Aspects with FIR-Embedded Design

**Woogeun Rhee*, Ni Xu*, Bo Zhou**, and Zhihua Wang***

***Abstract*—This paper gives an overview of fractional-*N* phase-locked loops (PLLs) with practical design perspectives focusing on a ΔΣ modulation technique and a finite-impulse response (FIR) filtering method. Spur generation and nonlinearity issues in the ΔΣ fractional-*N* PLLs are discussed with simulation and hardware results. High-order ΔΣ modulation with FIR-embedded filtering is considered for low noise frequency generation. Also, various architectures of finite-modulo fractional-*N* PLLs are reviewed for alternative low cost design, and the FIR filtering technique is shown to be useful for spur reduction in the finite-modulo fractional-*N* PLL design.**

***Index Terms*—CMOS integrated circuits, PLL, frequency synthesizer, fractional-*N*, delta-sigma modulator**

## I. INTRODUCTION

The phase-locked loop (PLL) based frequency synthesizers play a critical role in multi-standard transceiver systems. The integer-*N* PLL has difficulty in meeting design trade-offs when the frequency division ratio needs to be very high. Fig. 1 shows the block diagram which generates 2 GHz output from a fixed crystal frequency of 19.68 MHz. If 200 kHz is set for a channel raster like WCDMA systems, the phase detector frequency needs to be set to 40 kHz and the frequency division ratio is as high as 50,000 to meet the frequency resolution of 200 kHz. In that case, the in-band noise contributions of the phase detector and the reference source are amplified by 114 dB at the VCO output. Moreover, with the phase detector frequency of 40 kHz, the PLL bandwidth can be only a few kHz for stability, resulting in poor voltage-controlled oscillator (VCO) noise suppression and slow settling time.

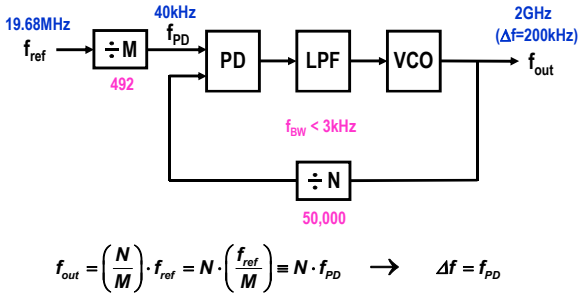


**Fig. 1.** Frequency synthesis example with integer-*N* PLL.

Having the phase detector frequency higher than the resolution frequency, the fractional-*N* PLL offers several advantages over the integer-*N* PLL. The unique problem of the fractional-*N* PLL is unwanted spur generation which is caused by the periodic operation of the dual-modulus divider. The fractional-*N* frequency synthesis is not useful in practical applications unless the fractional spurs are suppressed. Hence, additional circuitry must be added to suppress those fractional spurs.

In this paper, practical design aspects for high-performance fractional-*N* PLLs are discussed. The paper is organized as follows. In Section II, the overview of the fractional-*N* frequency synthesis technique is given. Section III gives the detailed design aspects of the ΔΣ

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fractional-*N* PLL and quantization noise reduction methods are presented in Section IV. Section V addresses the advantages of the finite-modulo fractional-*N* PLLs for alternative low cost design, followed by conclusion in Section VI.

## II. OVERVIEW OF FRACTIONAL-*N* PLL

The fractional-*N* PLL achieves finer resolution frequency than the phase detector frequency. The fractional-*N* method originally comes from the *Digiphase* technique in which the phase is digitally controlled to interpolate the frequency [1, 2]. Fig. 2 shows a block diagram of the traditional fractional-*N* PLL in which the fractional division ratio of 1/4 is shown as an example in Fig. 2(b). Fractional division ratio is obtained by periodically modulating the control input of the dual-modulus divider. With such a periodic modulation, an unwanted spur is generated. Therefore, various spur reduction methods are proposed in the literature.

### 1. DAC Cancellation Method

The phase cancellation method using a digital-to-analog converter (DAC) is a traditional spur reduction method. Fig. 3 shows the basic architecture and its operation [1, 2]. Since the phase error is compensated in the voltage domain, this method suffers from analog imperfections. The mismatch results mainly from the limited DAC resolution and the limited accuracy of the DAC. This approach is more effective when a sample-and-hold (S/H) phase detector is used instead of the phase/frequency detector (P/FD) since the DAC needs to match only the dc voltage during one reference clock period.

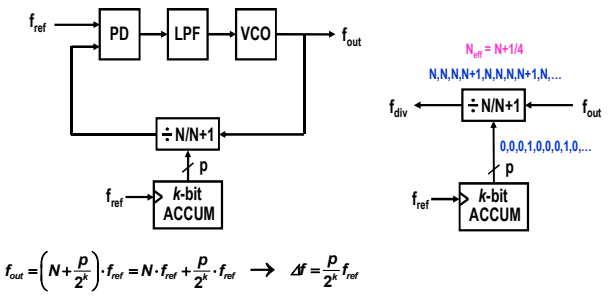



**Fig. 2.** Traditional fractional-*N* PLL: (a) basic block diagram, (b) fractional division ratio example for *N* + 1/4.

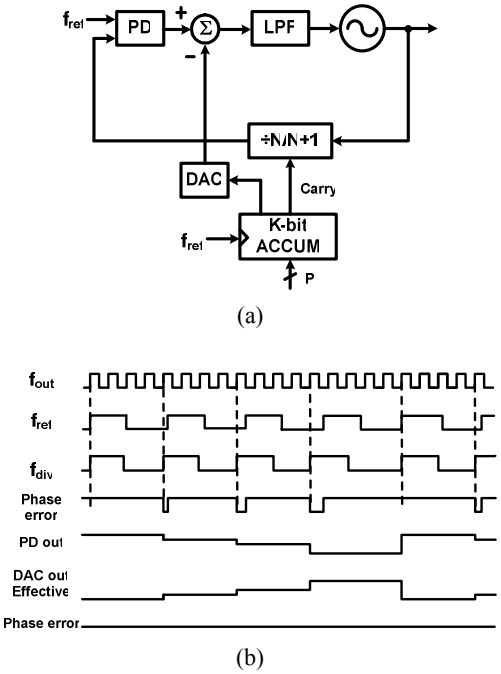



**Fig. 3**. DAC cancellation method [1, 2] (a) basic block diagram, (b) fractional division ratio example for *N* + 1/4.

### 2. Phase Interpolation Method

The fact that an *N*-stage ring oscillator generates *N* different phases is applied to implement a fractional divider as depicted in Fig. 4 [3]. Since the number of inverters in the ring oscillator is limited, a phase interpolator is used to generate finer phases out of the available phases from the multi-phase ring VCO. By choosing the correct phase among the interpolated phases, a fractional division is achieved. Since the phase edges used for the fractional division ratio are selected periodically, any inaccuracy in the timing interval of the interpolated phase edges generates fixed tones.

### 3. Random Jittering Method

The conventional fractional-*N* synthesizers suffer from poor fractional spur performance when the analog matching is not well controlled. In addition, design complexity depends on the VCO output frequency. The instantaneous phase error which needs to be cancelled at the phase detector output is the fraction of the VCO output period, which can be as low as $10^{-3}$ rad. A random jittering approach solves the spur problem in the digital domain by digitally randomizing the digital sequence of

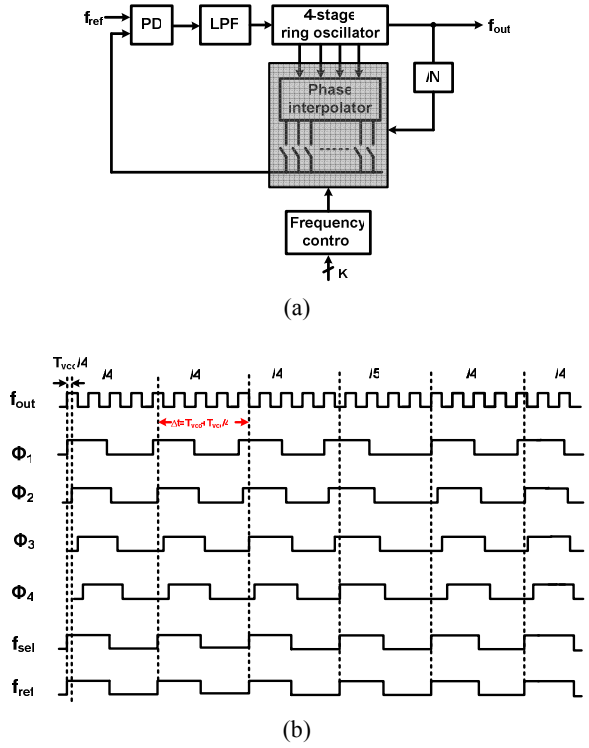



**Fig. 4.** Phase interpolation method [3] (a) block diagram, (b) timing diagram.

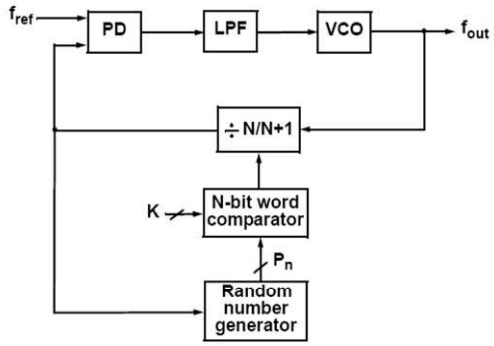



**Fig. 5.** Random jittering method [4].

the dual-modulus divider control bits. Fig. 5 shows a block diagram of a fractional-*N* divider with random jittering [4]. At each output of the divider, the random or pseudorandom number generator produces a new random word $P_n$ which is compared with the frequency word $K$. The frequency word $K$ controls the dual-modulus divider so that the average value can track the desired fractional division ratio. This method suffers from frequency jitter because the white noise injected in the frequency domain results in $1/f^2$ noise in the phase domain.

## III. Frequency Synthesis with ΔΣ Modulation

### 1. Basic Operation

A ΔΣ fractional-*N* frequency synthesizer enables direct digital frequency modulation for low cost transmitter design, thus becoming a key building block in modern transceiver systems [5-7]. Basic operation is to use an oversampling ΔΣ modulator to interpolate fractional frequency with a coarse integer divider as shown in Fig. 6 [8, 9]. While the traditional finite-modulo fractional-*N* PLLs see more difficulties in spur reduction with higher VCO frequency, the resolution of the ΔΣ fractional-*N* PLLs does not depend on the VCO frequency. By simply increasing the number of modulation bits, a very fine frequency resolution, e.g. 1 Hz, can be obtained. This method is similar to the random jittering method, but it does not generate a frequency jitter because of the noise-shaping property of the ΔΣ modulator. Frequency-domain comparison of the random jittering and ΔΣ modulation methods is given in Fig. 7. Since the second-

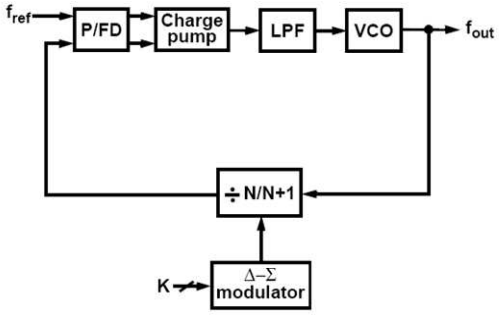



**Fig. 6.** ΔΣ fractional-*N* PLL [8, 9].

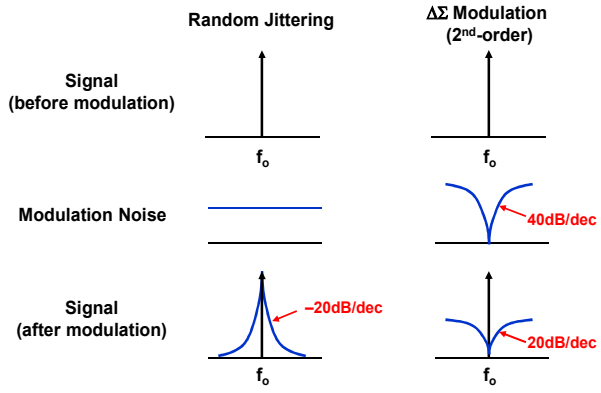



**Fig. 7.** Noise shaping comparison: random jittering vs. ΔΣ modulation.

or higher-order ΔΣ modulators, in theory, do not generate fixed tones for dc inputs, they effectively shape the phase noise without causing any spur. The operation of the ΔΣ fractional-*N* PLL is based on following key properties:

- Frequency interpolation by oversampling;
- Randomization with high-order modulation;
- Noise shaping with low frequency noise suppression;
- Digital input modulation with very fine resolution.

By interpreting well-known theoretical results of the oversampling ADC, we can derive the upper bound of the loop bandwidth $f_c$ in terms of the in-band phase noise $A_n$, the integrated phase error $\theta_{rms}$, the phase detector frequency $f_{PD}$, and the order of the ΔΣ modulator $L$, which is given by [10-12]

$$f_c < \left[ A_n \cdot \frac{L+0.5}{(2\pi)^{2L}} \right]^{\frac{1}{2L-2}} \cdot f_{PD}^{\frac{2L-1}{2L-2}},$$

$$\text{or} \quad f_c < \left[ \left( \frac{\theta_{rms}}{\sqrt{2}} \right)^2 \cdot \frac{L+0.5}{(2\pi)^{2L}} \right]^{\frac{1}{2L-1}} \cdot f_{PD}$$

The conceptual diagram showing the dynamic range in the ΔΣ fractional-*N* PLL is shown in Fig. 8. For example, when the phase detector frequency is 8 MHz, the upper bound of the bandwidth with the third-order ΔΣ modulator to meet less than $1^{o}_{rms}$ phase error is 195 kHz. In practice, the required loop bandwidth is narrower than that by the above equation since the quantization noise of the third-order modulator is tapered off after the fourth pole of the PLL.

For fractional-*N* frequency synthesis, two types of ΔΣ modulators have been used. One is a single-loop delta-sigma modulator (SLDSM), and the other is a cascaded modulator called the MASH modulator. The SLDSM has

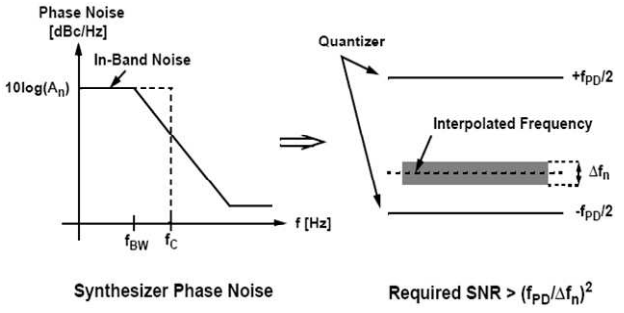



**Fig. 8.** Dynamic range consideration in ΔΣ fractional division.

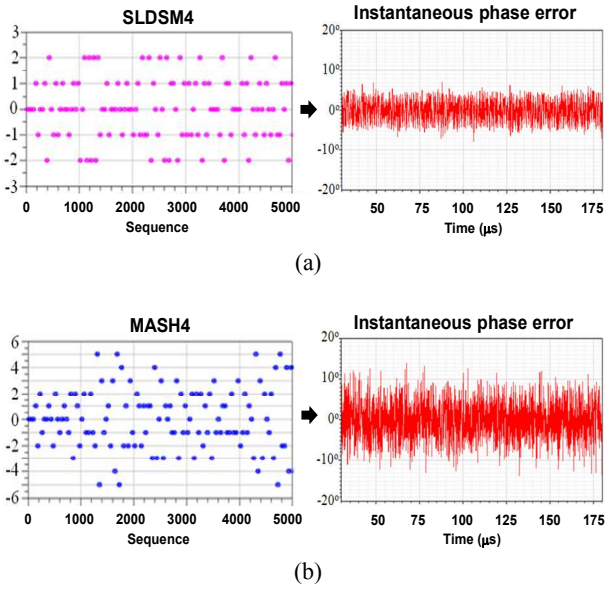



**Fig. 9.** Modulator output and corresponding phase error (a) SLDSM, (b) MASH.

a choice of a single-bit or a multi-bit output depending on the quantizer while the MASH architecture outputs only multi bits. The high-order SLDSM with a single-bit quantizer is less sensitive to nonlinearity. The drawback of this architecture is the limited dynamic input range due to the nonlinear stability problem. By having a multi-level quantizer, the dynamic input range problem can be solved [10]. Compared to the MASH modulator, the multi-bit SLDSM has less high-frequency noise at the phase detector output. Fig. 9(a) and Fig. 9(b) show the output spread patterns and the corresponding phase errors of the fourth-order SLDSM and the fourth-order MASH respectively.

However, the SLDSM suffers from the internal quantization error caused by bit shifting operation, which cannot be avoided to realize feed-forward coefficients in a simple way [10]. As a result, the MASH modulator generates better uncorrelated output with less idle tone than the SLDSM. Especially, the SLDSM exhibits poor randomization performance when the fractional division value is set to large rational numbers, namely, 1/2 and 1/4. For those fractional division values, the dithering needs to be automatically disabled from the PLL design. Since the fractional spur due to the fractional division value of 1/2 or 1/4 is higher than the PLL bandwidth, those spurs can be easily suppressed by the loop filter. Having better idle tone performance and a simpler architecture with

guaranteed stability, the MASH modulator is dominantly used for most RF applications. Unless the PLL bandwidth is extremely wide, the in-band noise contribution of the ΔΣ modulator is negligible even with the order of two. However, low-order modulators having less uncorrelated output bits may exhibit phase noise fluctuation over time, which will degrade the worst-case phase noise performance. In practice, it is good to have the modulator with the order of at least three in fractional-*N* PLL design.

## 2. Nonlinearity

The all-digital multi-bit modulator has no linearity problem, but when it is combined with the PLL, the nonlinearity of the phase detector (charge pump) can be a concern. Fig. 10 shows similarity between the multi-bit oversampling ADC and the frequency synthesizer having the multi-bit modulator. It is well known that the multi-bit DAC performance limits the in-band noise performance as well as the spur performance. A similar behavior can be deduced for the multi-modulus divider with the modulator. The phase detector converts the digital quantity into an analog quantity by generating the multi-phase errors, and the phase detector nonlinearity is considered a main contributor for nonideal effects of the ΔΣ fractional-*N* PLL. Circuit-level nonideal effects on the performance of the ΔΣ fractional-*N* PLL are well described in the literature [13-15].

When the PLL bandwidth is set wide, a discrete time *z*-domain model describes loop behavior more accurately than a continuous-time model [16]. One of linearizing assumptions in the *z*-domain analysis is that phase samples occur at constant intervals. The ΔΣ fractional-*N* PLL has wide variation of the sampling time in nature, and the amount of relative variation to the reference

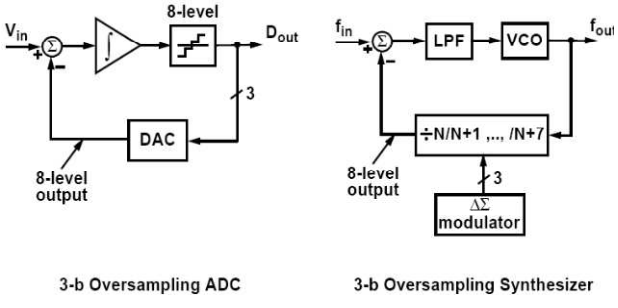



**Fig. 10.** Multi-bit oversampling: ADC vs. fractional-*N* PLL.

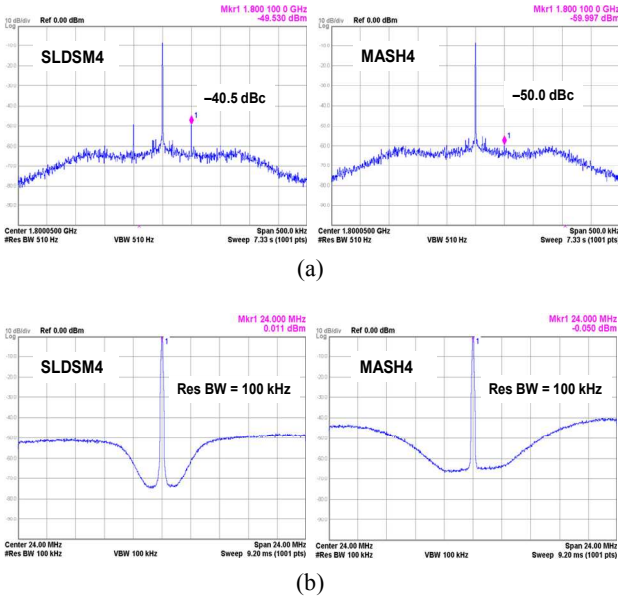



**Fig. 11.** Measured output spectra: SLDSM vs. MASH (a) VCO output at 1.8 GHz, (b) divider output at 24 MHz.

clock period increases as the division ratio decreases. Therefore, compared to MASH modulator, less spread output bit pattern of the SLDSM alleviates the nonlinearity problem by reducing the non-uniform sampling effect, which is especially effective for high-order modulation.

Fig. 11(a) shows that the fourth-order MASH modulator exhibits better fractional spur performance since it does not have internal coefficients realized by bit shifting like the SLDSM. As a rule of thumb, the fractional spur performance of the $L^{\text{th}}$-order SLDSM is similar to that of the $(L-1)^{\text{th}}$-order MASH modulator. Clear noise shaping performances can be seen at the divider output in which the VCO phase noise is negligible. Fig. 11(b) shows that the fourth-order SLDSM can offer better in-band noise performance than the fourth-order MASH modulator when less spread output bit pattern reduces the phase detector nonlinearity.

## 3. Integer-Boundary Spur

In theory, the ΔΣ fractional-*N* PLL with high-order digital modulation can achieve spur-free output spectrum. In practice, sidebands are observed in hardware especially when the VCO frequency is near the integer multiple of the reference clock frequency, which is often referred to as an integer-boundary spur or a fractional

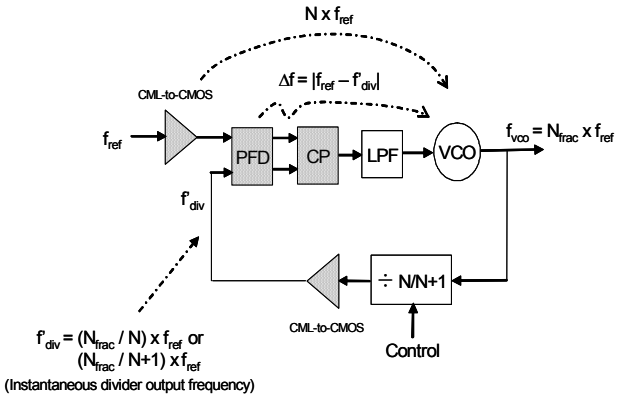



**Fig. 12.** Fractional spur generation by coupling in fractional-*N* PLL.

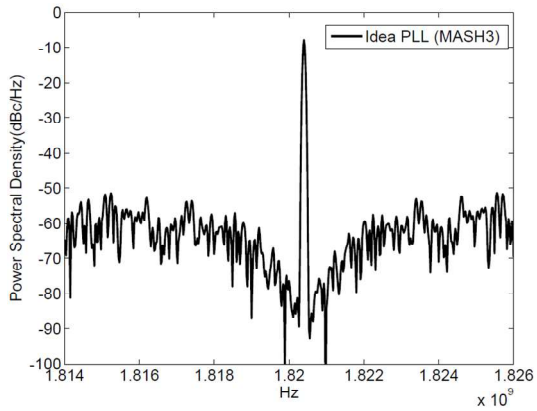



**Fig. 13.** Behavioral simulation of ΔΣ fractional-*N* PLL with third-order MASH modulator ($F_{out}$=1820.4 MHz, $F_{ref}$=52 MHz).

spur. It is shown that the intermodulation between the reference clock path and the feedback clock path generates a beat tone that modulates the VCO and causes the fractional spur as illustrated in Fig. 12 [17]. Accordingly, it is important to modulate the multi-modulus divider with uncorrelated control sequence, which can be better achieved with high-order ΔΣ modulation. Also, designing a good CML-to-CMOS converter design [18] and providing good supply voltage isolation between the charge pump (CP) and the VCO are important to minimize the intermodulation effect due to noise coupling. As the quantized phases formed by the multi-modulus divider are to be linearly interpolated by the phase detector, the spurious tone generation by the time-to-digital converter (TDC) in the all-digital PLL (ADPLL) has a somewhat similar mechanism as that of the ΔΣ fractional-*N* PLL [19].

To verify the fractional spur generation, closed-loop fractional-*N* PLL simulations are done. In the simulation, the reference clock frequency of 52 MHz is used and the output frequency of the PLL is 1820.4 MHz with the effective division ratio of about 35.0077. Therefore, the integer-boundary spur at 400 kHz offset frequency from the carrier frequency is expected. To reduce the simulation time and boost the spur level, a wide loop bandwidth of about 1 MHz is designed. In the simulation, both the third-order and the fourth-order ΔΣ modulators are tried for comparison.

Fig. 13 shows the simulated output spectra of the closed-loop ΔΣ fractional-*N* PLLs. The closed-loop simulation is done with an ideal ΔΣ fractional-*N* PLL and an ideal third-order ΔΣ modulator which are based on the Verilog-A model. The carrier frequency is clearly locked at 1820.4 MHz and no fractional spur at 400 kHz offset frequency is observed.

To see the nonlinearity effect of the PLL, the ideal CP and the ideal VCO are replaced with the transistor-level single-ended CP and VCO circuits and the bond-wire inductance of 1 nH is included for each supply voltage. As shown in Fig. 14(a), the fractional spur level of –35 dBc and –47 dBc are observed at 400 kHz offset frequency with the third- and fourth-order modulators respectively. It shows that the fractional spur generation is caused not by the idle tone of the ΔΣ modulator but by the PLL nonlinearity. It also implies that the use of the high order modulator is good to reduce the spur level.

Finally, to add the coupling effect between the supply voltages of the CP and the VCO, the supply voltages are shared with the bond-wire inductance of 1 nH, which also aggravates the CP nonlinearity. As shown in Fig. 14(b), the spur level is increased significantly. Interestingly, the spur performance degradation of the fourth-order modulator is more serious, resulting in only a few dB improvement. The result indicates that the high-order modulator having the wide spread output bit pattern can suffer more from the coupling and the nonlinearity.

## IV. QUANTIZATION NOISE REDUCTION

### 1. Quantization Noise

In frequency synthesizer design, it is important to

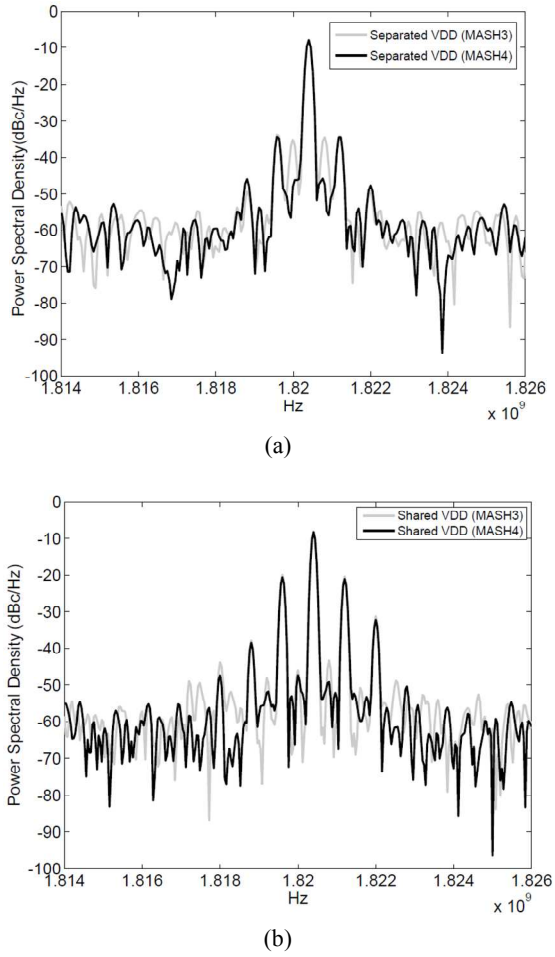



**Fig. 14.** Mixed-mode simulations (a) with transistor-level CP and VCO having separate supply voltages, (b) with shared supply voltages of CP and VCO.

identify phase noise contribution from each source. The noise contributions from various sources for a type-II, fourth order PLL with a third-order modulator are plotted in Fig. 15. Depending on open-loop gain design, the ΔΣ modulator can affect in-band noise or out-of-band noise. The in-band noise may be limited by PLL nonlinearity. The out-of-band noise can be possibly determined by the residual quantization noise of the modulator rather than the VCO noise. Note that the quantization noise contribution does not depend on division ratio, because it is generated by frequency modulation having the resolution of one VCO clock period. As shown in Fig. 15, the open loop gain needs to be carefully designed to have the overall noise performance meet the system specification. High-order poles are important not only for spur suppression but also for noise performance, which is different from integer-*N* synthesizer design.

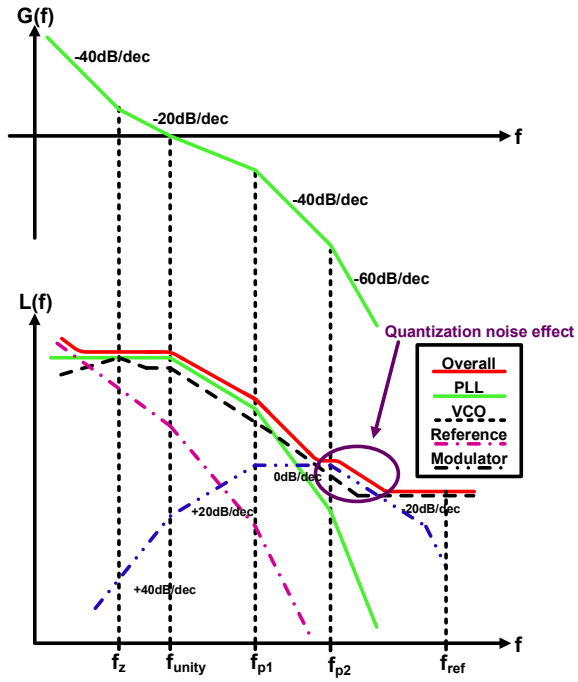



**Fig. 15.** Phase noise contribution example of type-II fourth-order fractional-*N* PLL with third-order ΔΣ modulator.

There are several techniques proposed for quantization noise reduction. The phase error cancellation method by using a DAC [6, 20, 21] achieves significant reduction of phase noise and spurs but the performance depends on the high resolution DAC and analog matching, resulting in high design complexity.

## 2. FIR-Embedded ΔΣ Modulation

The semi-digital approach based on a finite-impulse response (FIR) filtering method offers moderate quantization noise reduction without using the DAC [22-27]. With wide bandwidth, out-of-band noise could be more problematic than in-band noise to meet the phase noise mask required by wireless standards. The hybrid FIR filtering method effectively reduces the out-of-band noise without affecting the PLL loop dynamics.

Fig. 16 shows a conceptual diagram of how the FIR filter can be utilized in the fractional-*N* PLL. For simplicity, a fractional-*N* PLL with 9-modulo fractional division is assumed. The 9-modulo fractional-*N* PLL with the reference frequency $f_{ref}$ exhibits a periodic phase error with the frequency of $f_{ref}/9$. When a 3-tap FIR filter is applied, the fixed tone with the frequency of $f_{ref}/9$ is increased to higher frequency of $f_{ref}/3$ as depicted in Fig.

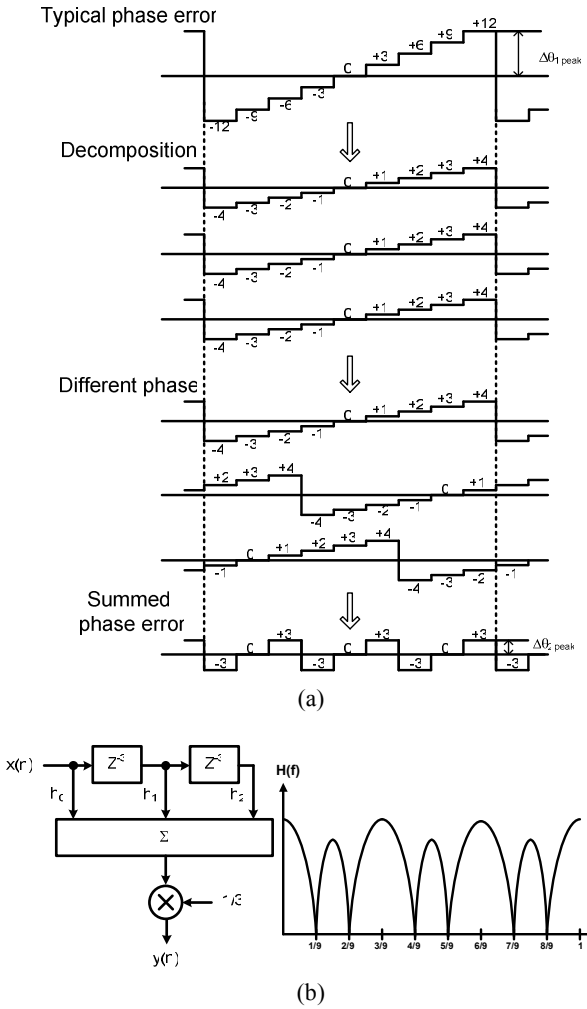



**Fig. 16.** (a) Shaping periodic tone with phase decomposition and shifting, (b) equivalent *z*-domain model and transfer function.

16. As the fundamental frequency of the fixed tone increases, further spur reduction can be achieved by the PLL loop filter. If a 9-tap FIR filter is used, the fixed tone can be completely removed.

The FIR filtering method can be now extended to the quantization noise reduction of the ΔΣ fractional-*N* PLL. A straightforward implementation is shown in Fig. 17. As the FIR filter creates notches in the noise transfer function of the ΔΣ modulator, it suppresses the quantization noise in high frequencies. The transfer function of the FIR filter can be designed regardless of the PLL loop dynamics, thus making a customized quantization noise shaping possible. Fig. 18 shows measured PLL output spectra with different FIR modes [22]. The notches in each output spectrum correspond to the zeros of the FIR transfer function in each mode,

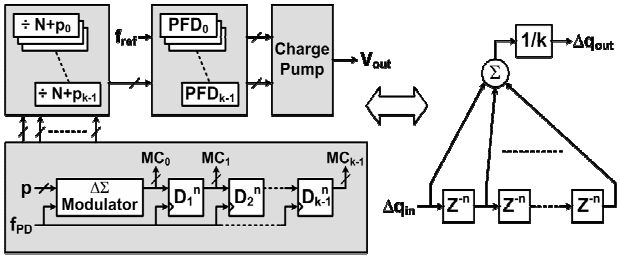



**Fig. 17.** ΔΣ modulation with embedded FIR filtering [22, 23].

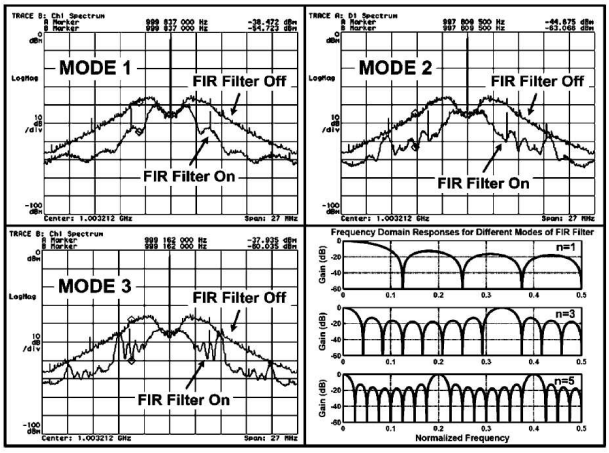



**Fig. 18.** Measured PLL output spectra with different FIR modes [23].

showing that the embedded FIR filter suppresses the quantization noise as predicted by the transfer function. The results also imply that a customized noise shaping can be achieved with the propose method [23].

Even though the DAC cancellation method achieves better performance with good analog matching and linearity assumed, the hybrid FIR filtering method provides a straightforward way of noise reduction by simply implementing multiple dividers and phase detectors. Since noise reduction is done by the semi-digital filtering method, the quantization noise suppression is more predictable with less dependency on PVT variations. In addition, the power and area of the FIR filtering circuitry can be scaled with the advanced CMOS technology when the phase-interpolated multi-modulus divider is employed [23, 26, 27], while difficult for the DAC cancellation method.

The FIR filtering method is especially useful when high order ΔΣ modulators are used. Fig. 19 shows the quantization noise comparison of the SLDSMs and the MASH modulators in the fourth-order PLL design. In the simulation, the PLL bandwidth of 200 kHz is assumed

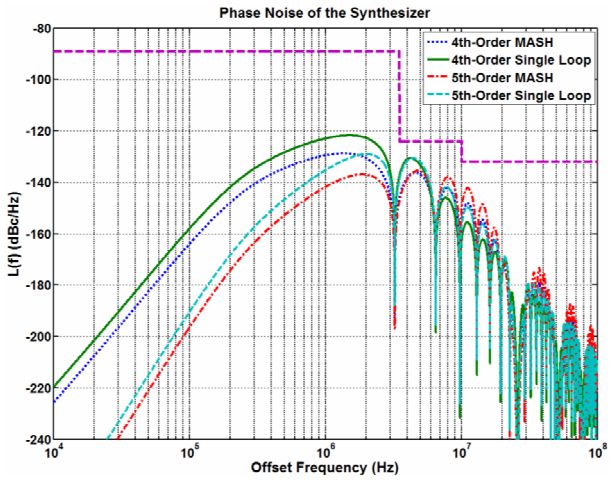



**Fig. 19.** Quantization noise of fourth- and fifth-order modulators in type-II fourth-order ΔΣ PLL with hybrid FIR filtering.

with the 3rd pole and 4th pole at 560 kHz and 1.77 MHz, respectively. Note that the fourth-order or fifth-order modulators can be used in the conventional fourth-order PLL with the hybrid FIR filtering method [23, 24]. Fig. 20 shows the measured in-band fractional spur of <–65 dBc. With widened bandwidth, the in-band noise contribution as low as –100 dBc/Hz is achieved [24], showing that the FIR filtering method enhances the linearity of the multi-input charge pump.

## V. FINITE-MODULO FRACTIONAL-*N* PLL

Even though the ΔΣ fractional-*N* PLL offers superior performance to the integer-*N* PLL, it is more exposed to nonlinearity and coupling issues than other PLLs. Having moderate performance between the integer-*N* PLL and the ΔΣ fractional-*N* PLL, the traditional finite-modulo fractional-*N* PLL provides an alternative way of reducing the division ratio with negligible digital power and coupling.

### 1. Phase Interpolated Finite-Modulo

Fig. 21 shows a fractional-*N* PLL in which the phase interpolation is done after the dual-modulus divider with on-chip delay calibration [28]. Compared to Fig. 4, the phase compensation is done before the P/FD and the multi-phase VCO is not needed. The on-chip tuning circuit corrects the different amount of phase

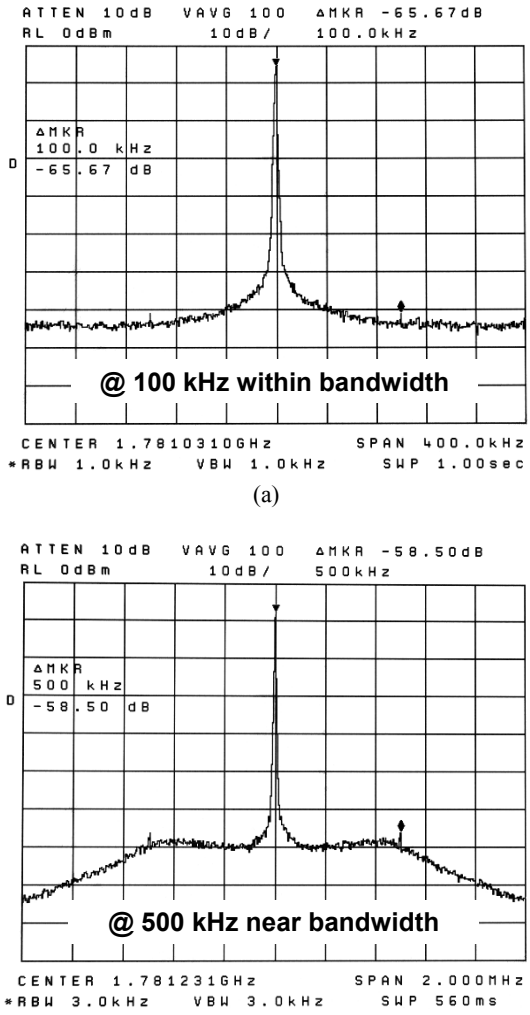



**Fig. 20.** Measured spur performances with fifth-order SLDSM and 13-tap FIR [24] (a) in-band spur, (b) near-bandwidth spur.

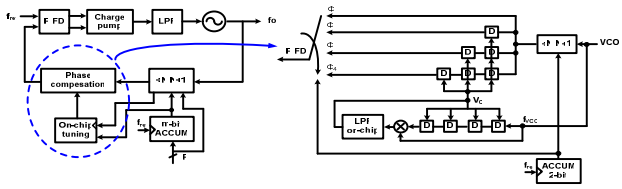



**Fig. 21.** Phase interpolation with on-chip tuning [28].

interpolation as the output frequency varies, which is performed by the delay-locked loop (DLL). With deliberate calibration or dithering method, spur reduction performance can be further enhanced for the phase interpolation based fractional-*N* PLLs [29, 30].

In Fig. 22, a finite-modulo fractional-*N* PLL utilizing a low-bit high-order ΔΣ modulator is presented [31]. Only 4-bit MASH modulator is used to achieve 16-modulo fractional-*N* division. The 4-bit fourth-order ΔΣ modulator

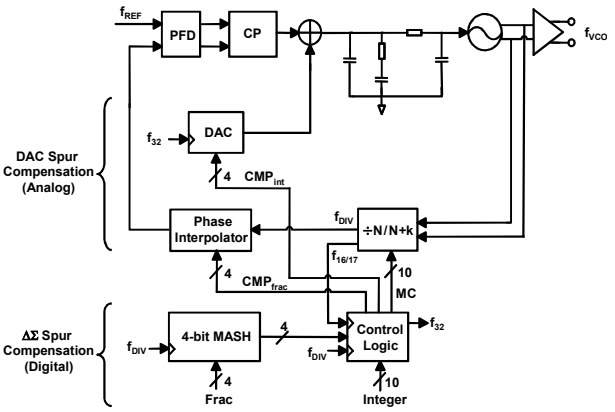



**Fig. 22.** Hybrid spur compensation with 4-bit 4[th]-order MASH [31].

not only performs non-dithered 16-modulo fractional operation but also offers less spur generation with negligible quantization noise. Further spur reduction is achieved by charge compensation in the voltage domain and phase interpolation in the time domain, which significantly relaxes the dynamic range requirement of the charge pump compensation current. In [31], the fourth-order MASH modulator itself provides about 15 dB spur reduction, and the use of the current DAC after the charge pump provides total reduction of 27 dB.

## 2. FIR-Embedded Finite Modulo

As illustrated in Fig. 16, the FIR filtering method can be also employed for the finite-modulo fractional-*N* PLL [25, 32, 33]. Fig. 23 shows an example of an 8-modulo fractional-*N* PLL [32]. A sample-and-hold (S/H) phase detector is used since it performs complete phase error cancellation when there is no analog mismatch. The detailed timing diagram is shown in Fig. 23. With the S/H phase detector, multi-input operation can be implemented in a simpler way and the ideal S/H phase detector does not create any high-frequency voltage ripple. Since eight dual-modulus dividers are used with eight unit delay elements, it creates the zero frequency at 1/8 of the phase detector frequency.

In practice, the P/FD based PLL is dominant. Compared to the PLL with the S/H phase detector, the PLL with the P/FD cannot perform perfect phase cancellation at the P/FD output. To compensate for the limited FIR filtering performance, the phase interpolation method to reduce the maximum phase error at the P/FD

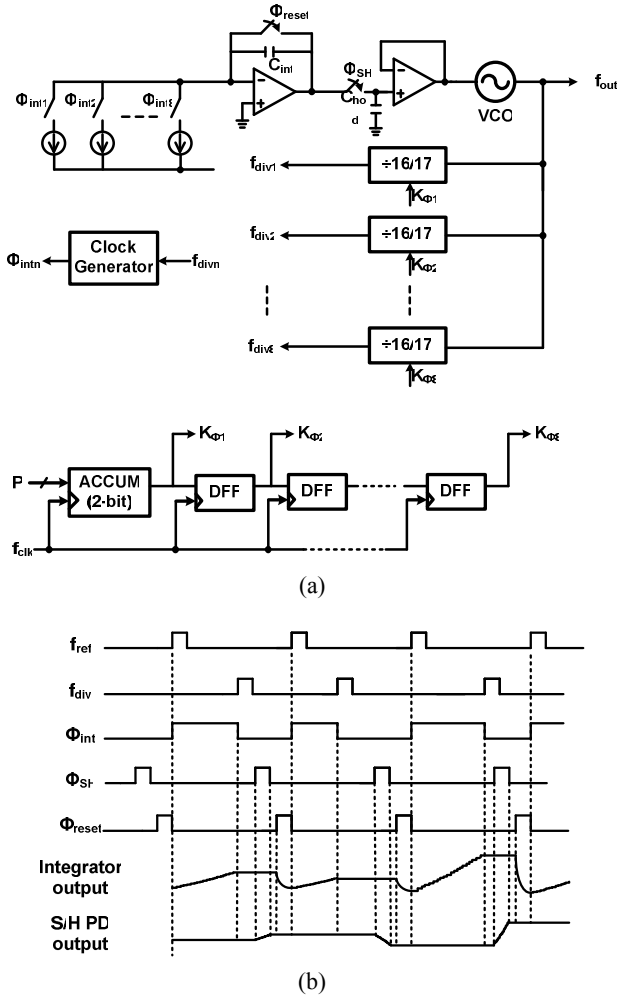



**Fig. 23.** 8-modulo FIR-embedded fractional-N PLL with S/H phase detector [32] (a) block diagram, (b) timing diagram.

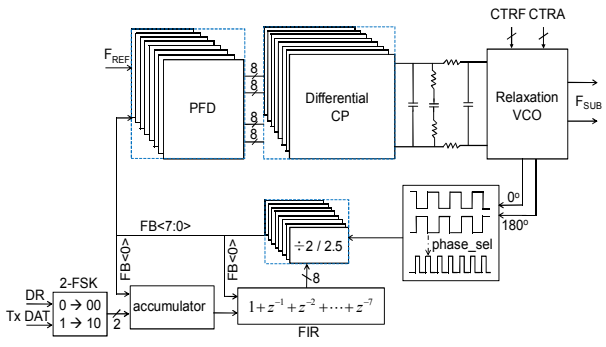
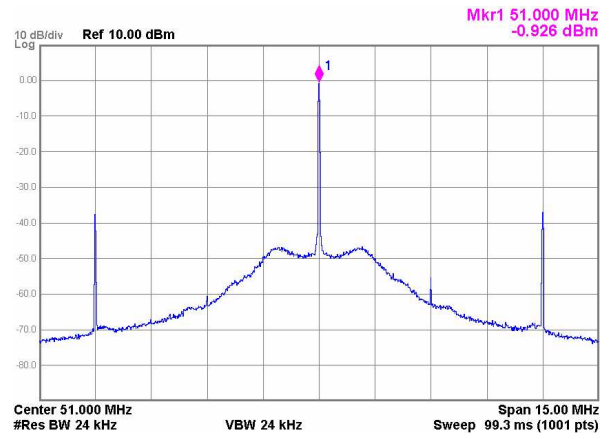


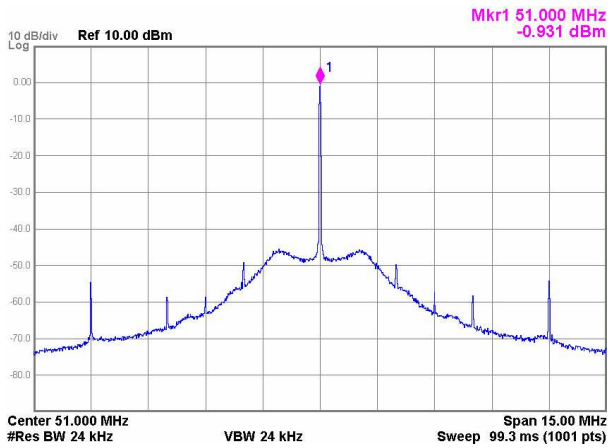

**Fig. 24.** 8-modulo fractional-*N* PLL with 8-tap FIR filtering [33].

output can be combined. The 8-modulo fractional-*N* PLL shown in Fig. 24 combines the phase interpolation method with the 8-tap FIR filtering method [33]. By utilizing differential outputs from the VCO, a 2/2.5 dual-

modulus divider is designed. With the sub-integer dual-modulus divider and a 2-bit accumulator, the 8-modulo fractional operation is obtained. To suppress the fractional spur at 3 MHz, an 8-tap FIR filtering method is employed. Since the 8-tap FIR filter has a notch transfer function at the one eighth of the reference clock frequency, the notch frequency is located at 3 MHz with the reference clock frequency of 24 MHz. Fig. 25 shows the measured output spectra of the 51 MHz fractional-*N* PLL [33]. The 8-modulo fractional-*N* PLL with the reference clock frequency of 24 MHz exhibits a fractional spur at 6 MHz offset frequency and not at 3 MHz offset frequency, showing that the fractional spur is caused by the 4-modulo periodic operation of the 2/2.5 dual-modulus divider and that the mismatch in the sub-integer 2/2.5 dual-modulus divider is not significant. When the hybrid FIR filter is enabled, the fractional spur is reduced to –55 dBc from –38 dBc as shown in Fig. 25.




(a)




(b)

**Fig. 25.** Measured output spectra of 8-modulo fractional-*N* PLL (a) without hybrid FIR, (b) with hybrid FIR [33].

## VI. CONCLUSIONS

An overview of the fractional-*N* PLL is presented with emphasis on the ΔΣ modulation method. The FIR-embedded ΔΣ modulation effectively reduces the out-of-band quantization noise and enhances the charge pump linearity. In this paper, high-order ΔΣ modulation with FIR-embedded filtering is considered for low noise frequency generation, and simulation and hardware results are presented. In addition, finite-modulo fractional-*N* PLLs are reviewed for alternative low cost design. It is shown that the FIR filtering method can be also useful for spur reduction in the finite-modulo fractional-*N* PLL design.

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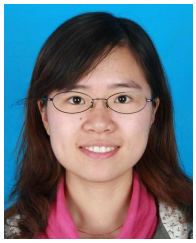

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